TEXAS INSTRUMENTS

ISO7710-Q1

SLLSEU2 – MARCH 2017

ISO7710-Q1 High Speed, Robust EMC Reinforced Single-Channel Digital Isolator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- Signaling Rate: Up to 100 Mbps
- Wide Supply Range: 2.25 V to 5.5 V
- 2.25 V to 5.5 V Level Translation
- Default Output *High* and *Low* Options
- Low Power Consumption, Typical 1.7 mA at 1 Mbps
- Low Propagation Delay: 11 ns Typical (5-V Supplies)
- High CMTI: ±100 kV/μs Typical
- Robust Electromagnetic Compatibility (EMC)
  - System-Level ESD, EFT, and Surge Immunity
  - Low Emissions
- Isolation Barrier Life: > 40 Years
- Wide-SOIC (DW-16) and Narrow-SOIC (D-8) Package Options
- Safety and Regulatory Approvals:
  - VDE Reinforced Insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - UL 1577 Component Recognition Program
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
  - TUV Certification according to EN 60950-1 and EN 61010-1
  - VDE, UL, CSA, and TUV Certifications for DW-16 Package Complete; All Other Certifications Planned

2 Applications

- Hybrid Electric Vehicles
- Motor Control
- Power Supplies
- Solar Inverters

3 Description

The ISO7710-Q1 device is a high-performance, single-channel digital isolator with 5000 V_{RMS} (DW package) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. This device is also certified by VDE, TUV, CSA, and CQC.

The ISO7710-Q1 device provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. The isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. In the event of input power or signal loss, default output is *high* for a device without suffix F and *low* for a device with suffix F. See the *Device Functional Modes* section for further details.

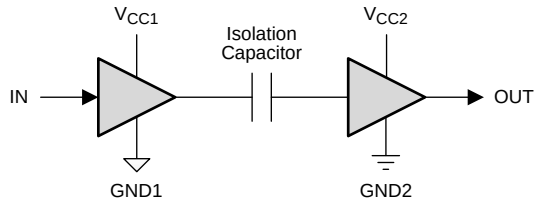
Used in conjunction with isolated power supplies, the device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO7710-Q1 device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO7710-Q1 device is available in 16-pin SOIC wide-body (DW) and 8-pin SOIC narrow-body (D) packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7710-Q1	SOIC (D)	4.90 mm × 3.91 mm
	SOIC (DW)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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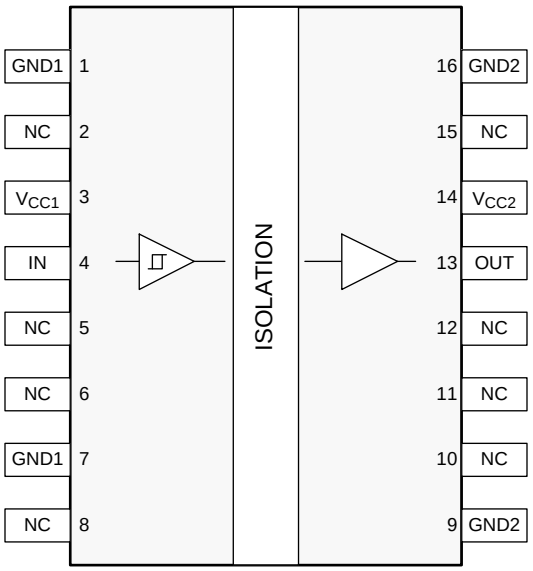
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

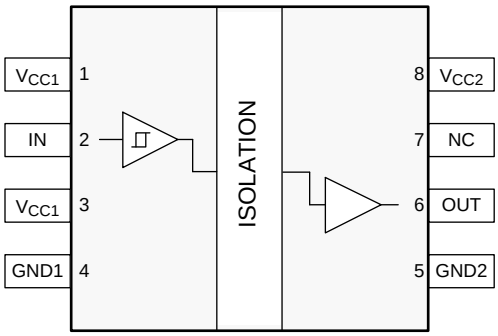
DATE	REVISION	NOTES
March 2017	*	Initial release.

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



D Package
8-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DW	D		
V_{CC1}	3	1, 3	—	Power supply, V_{CC1}
V_{CC2}	14	8	—	Power supply, V_{CC2}
GND1	1, 7	4	—	Ground connection for V_{CC1}
GND2	9, 16	5	—	Ground connection for V_{CC2}
IN	4	2	I	Input channel
OUT	13	6	O	Output channel
NC	2, 5, 6, 8, 10 ,11, 12, 15	7	—	Not connect pin; it has no internal connection

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)	–0.5	6	V
V	Voltage at IN, OUT	–0.5	V_{CC} + 0.5(3)	V
I_O	Output Current	–15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±6000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High-level output current	V_{CC2} = 5 V	–4			mA
		V_{CC2} = 3.3 V	–2			
		V_{CC2} = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CC2} = 5 V			4	mA
		V_{CC2} = 3.3 V			2	
		V_{CC2} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CC1}		V_{CC1}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CC1}	V
DR	Signaling rate		0		100	Mbps
T_A	Ambient temperature		–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ISO7710-Q1		UNIT
		DW (SOIC) (16-Pin)	D (SOIC) (8-Pin)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.4	146.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	57.3	63.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.1	80.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.0	9.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.8	79.0	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			50	mW
P_{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			12.5	mW
P_{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave			37.5	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	D-8	
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–IV	I–III	
		Rated mains voltage ≤ 600 V_{RMS}	I–IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	n/a	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 (2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	637	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) test	1000	450	V_{RMS}
		DC voltage	1414	637	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification) t= 1 s (100% production)	8000	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	5000	V_{PK}
q_{pd}	Apparent charge (4)	Method a, After Input/Output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.4	~0.4	pF
R_{IO}	Isolation resistance (5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE, CSA, UL and TUV certifications for DW-16 package are complete; All other certifications are planned.

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Maximum transient isolation voltage, 8000 V_{PK} (DW-16, Reinforced) and 4242 V_{PK} (D-8); Maximum repetitive peak isolation voltage, 1414 V_{PK} (DW-16, Reinforced) and 637 V_{PK} (D-8); Maximum surge isolation voltage, 8000 V_{PK} (DW-16, Reinforced) and 5000 V_{PK} (D-8)	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} (DW-16) and 400 V_{RMS} (D-8) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (DW-16) max working voltage	**DW-16:** Single protection, 5000 V_{RMS} ; **D-8:** Single protection, 3000 V_{RMS}	**DW-16:** Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage; **D-8:** Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5000 V_{RMS} (DW-16) and 3000 V_{RMS} (D-8) Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW-16) and 300 V_{RMS} (D-8) 5000 V_{RMS} (DW-16) and 3000 V_{RMS} (D-8) Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V_{RMS} (DW-16) and 400 V_{RMS} (D-8)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certification Planned	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 94.4 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			241	mA
		$R_{\theta JA}$ = 94.4 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 1			368	
		$R_{\theta JA}$ = 94.4 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 1			482	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 94.4 °C/W, T_J = 150°C, T_A = 25°C, see Figure 2			1324	mW
T_S	Maximum safety temperature				150	°C
D-8 Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 146.1 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 3			156	mA
		$R_{\theta JA}$ = 146.1 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 3			238	
		$R_{\theta JA}$ = 146.1 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 3			311	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 146.1 °C/W, T_J = 150°C, T_A = 25°C, see Figure 4			856	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K test board for leaded surface mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 11	V_{CC2} – 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 11		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CC1}	0.7 x V_{CC1}	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CC1}	0.4 x V_{CC1}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CC1}	0.2 × V_{CC1}		V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at IN			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at IN	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1200 V; see Figure 13	85	100		kV/µs
C_I	Input Capacitance(1)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = V_{CC1} (ISO7710-Q1), V_I = 0 V (ISO7710-Q1 with F suffix)		I_{CC1}		0.5	0.8	mA
			I_{CC2}		0.6	1	
	V_I = 0 V (ISO7710-Q1), V_I = V_{CC1} (ISO7710-Q1 with F suffix)		I_{CC1}		1.6	2.5	
			I_{CC2}		0.6	1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.1	1.5	
			I_{CC2}		0.6	1.1	
		10 Mbps	I_{CC1}		1.1	1.6	
			I_{CC2}		1.1	1.6	
		100 Mbps	I_{CC1}		1.4	2	
			I_{CC2}		5.9	7	

6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 11	V_{CC2} – 0.3	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 11		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 x V_{CC1}	0.7 x V_{CC1}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 x V_{CC1}	0.4 x V_{CC1}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CC1}	0.2 × V_{CC1}		V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at IN			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at IN	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1200 V; see Figure 13	85	100		kV/µs

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = V_{CC1} (ISO7710-Q1), V_I = 0 V (ISO7710-Q1 with F suffix)		I_{CC1}		0.5	0.8	mA
			I_{CC2}		0.6	1	
	V_I = 0 V (ISO7710-Q1), V_I = V_{CC1} (ISO7710-Q1 with F suffix)		I_{CC1}		1.6	2.5	
			I_{CC2}		0.6	1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.1	1.5	
			I_{CC2}		0.6	1	
		10 Mbps	I_{CC1}		1	1.6	
			I_{CC2}		1.1	1.4	
		100 Mbps	I_{CC1}		1.3	1.8	
			I_{CC2}		4.3	5.3	

6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 11	V_{CC2} – 0.2	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 11		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 x V_{CC1}	0.7 x V_{CC1}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 x V_{CC1}	0.4 x V_{CC1}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CC1}	0.2 × V_{CC1}		V
I_{IH}	High-level input current	V_{IH} = V_{CC1} at IN			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at IN	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} = 1200 V; see Figure 13	85	100		kV/µs

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - DC signal	V_I = V_{CC1} (ISO7710-Q1), V_I = 0 V (ISO7710-Q1 with F suffix)		I_{CC1}		0.5	0.8	mA
			I_{CC2}		0.6	1	
	V_I = 0 V (ISO7710-Q1), V_I = V_{CC1} (ISO7710-Q1 with F suffix)		I_{CC1}		1.6	2.5	
			I_{CC2}		0.6	1	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		1.1	1.5	
			I_{CC2}		0.6	1	
		10 Mbps	I_{CC1}		1.1	1.5	
			I_{CC2}		0.9	1.4	
		100 Mbps	I_{CC1}		1.2	1.6	
			I_{CC2}		3.4	4.4	

6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 11	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.9	ns
$t_{sk(pp)}$	Part-to-part skew time(2)				4.5	ns
t_r	Output signal rise time	See Figure 11		1.8	3.9	ns
t_f	Output signal fall time			1.9	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7 V. See Figure 12		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 11	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.1	5	ns
$t_{sk(pp)}$	Part-to-part skew time(2)				4.5	ns
t_r	Output signal rise time	See Figure 11		0.7	3	ns
t_f	Output signal fall time			0.7	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7 V. See Figure 12		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 11	7.5	12	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	5.1	ns
$t_{sk(pp)}$	Part-to-part skew time(2)				4.6	ns
t_r	Output signal rise time	See Figure 11		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC1} goes below 1.7 V. See Figure 12		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

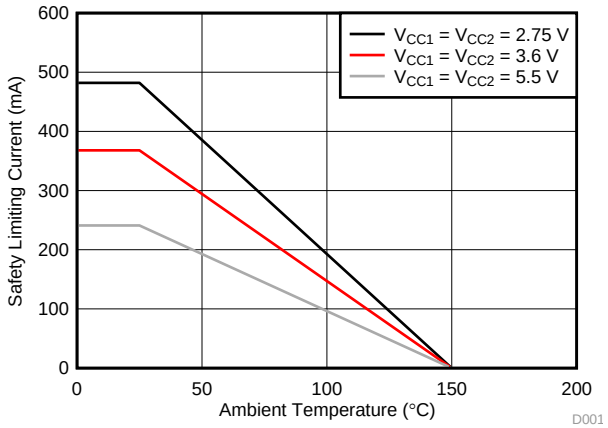


Figure 1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

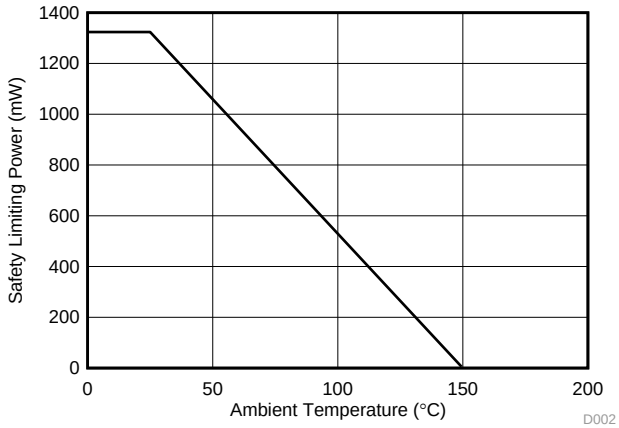


Figure 2. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

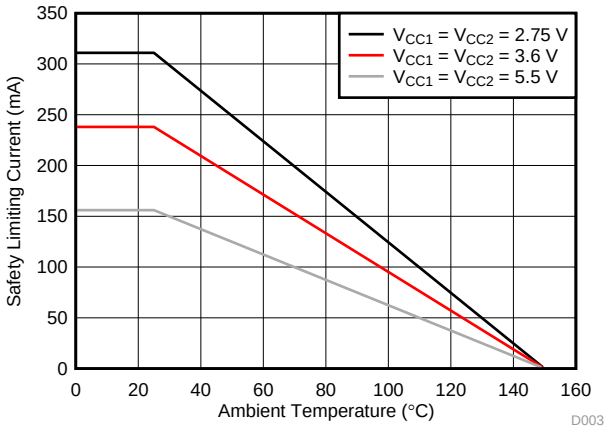


Figure 3. Thermal Derating Curve for Limiting Current per VDE for D-8 Package

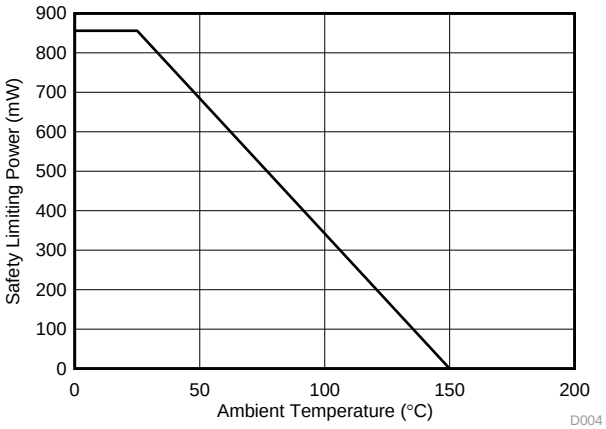


Figure 4. Thermal Derating Curve for Limiting Power per VDE for D-8 Package

6.19 Typical Characteristics

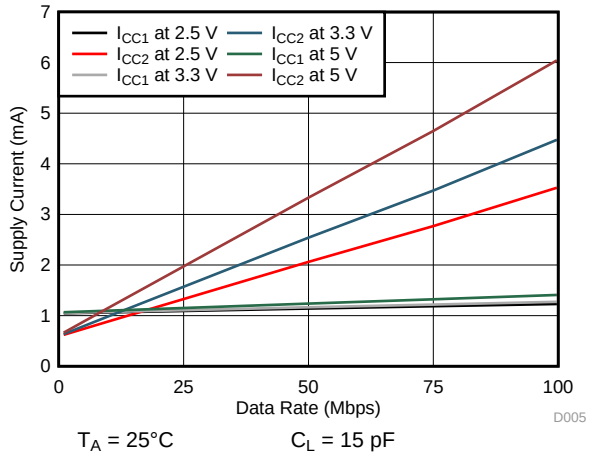


Figure 5. ISO7710-Q1 Supply Current vs Data Rate (With 15 pF Load)

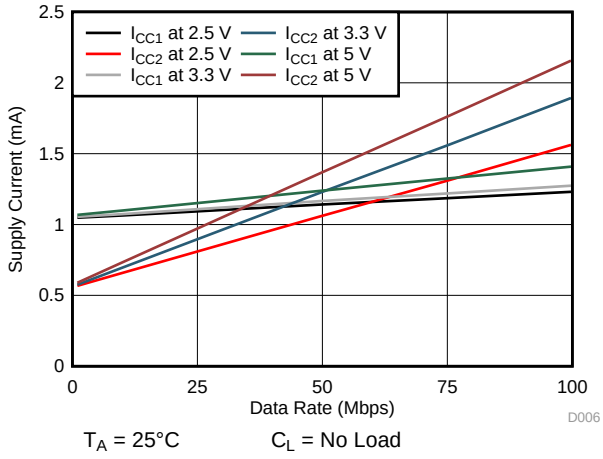


Figure 6. ISO7710-Q1 Supply Current vs Data Rate (With No Load)

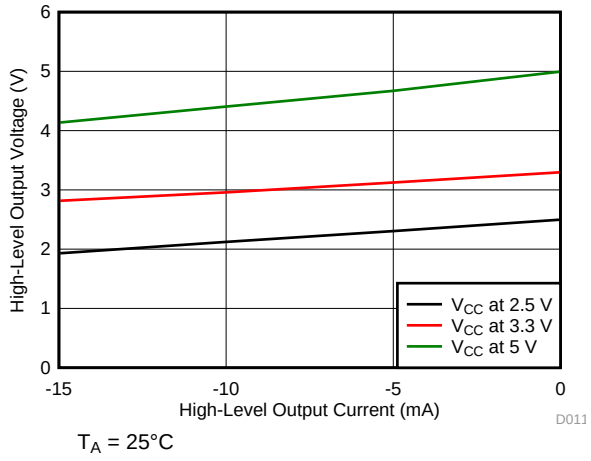


Figure 7. High-Level Output Voltage vs High-level Output Current

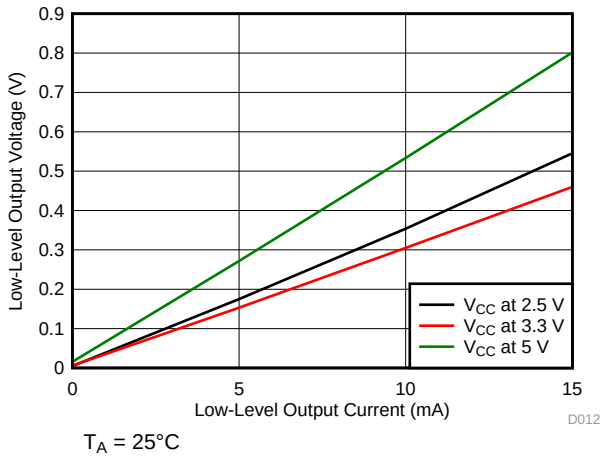


Figure 8. Low-Level Output Voltage vs Low-Level Output Current

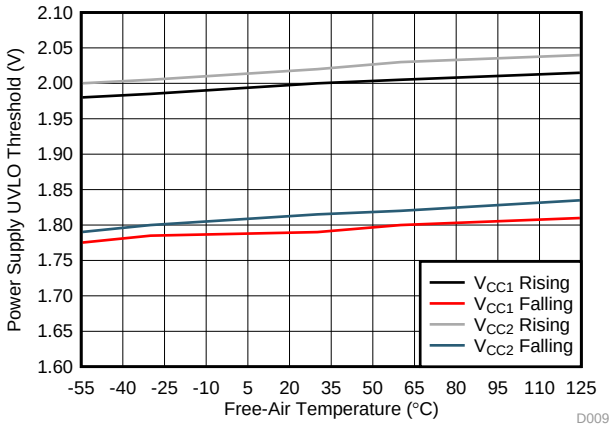


Figure 9. Power Supply Undervoltage Threshold vs Free-Air Temperature

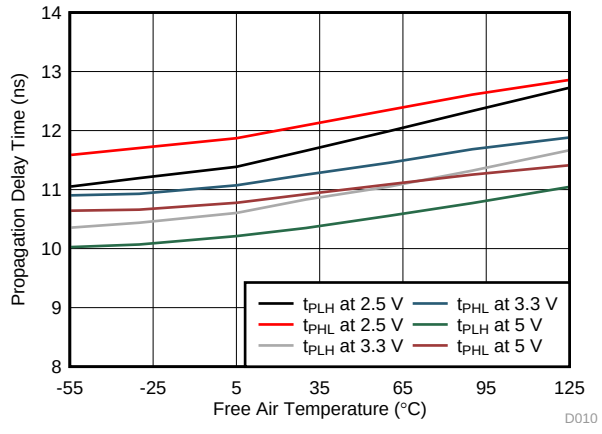
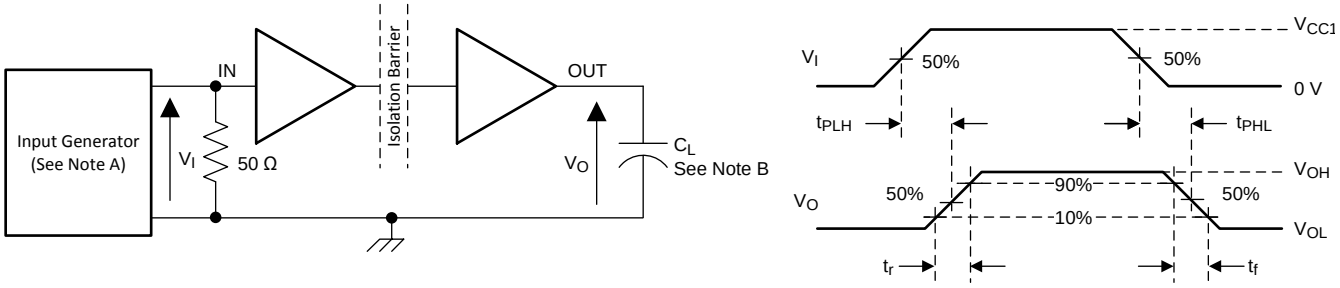


Figure 10. Propagation Delay Time vs Free-Air Temperature

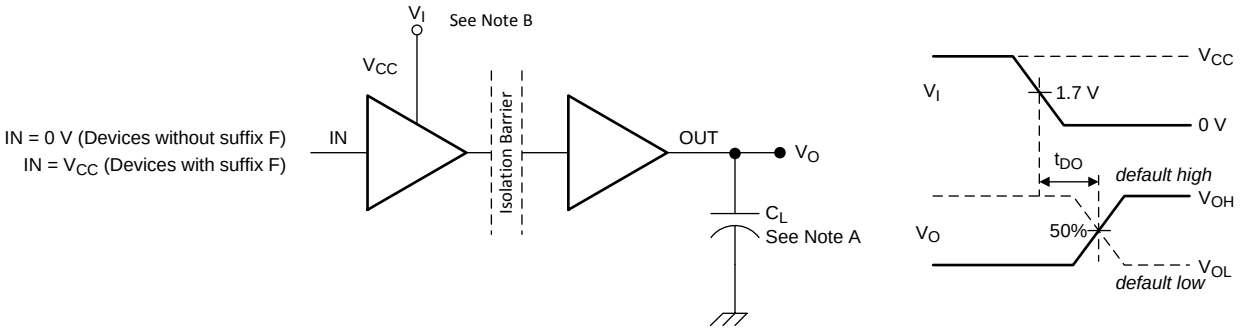
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

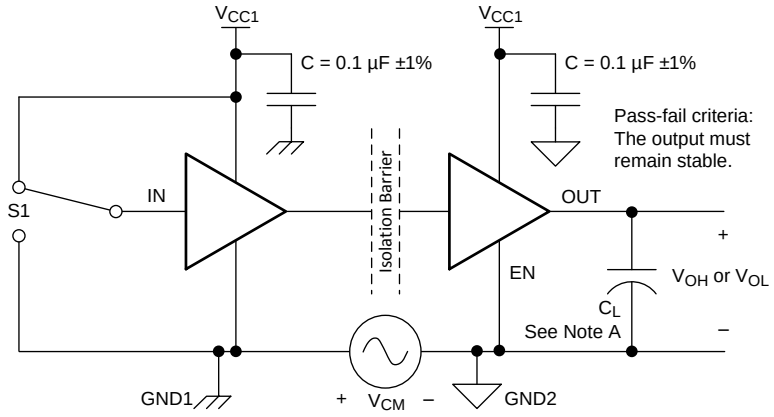
Figure 11. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

Figure 12. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO7710-Q1 device has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 14, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

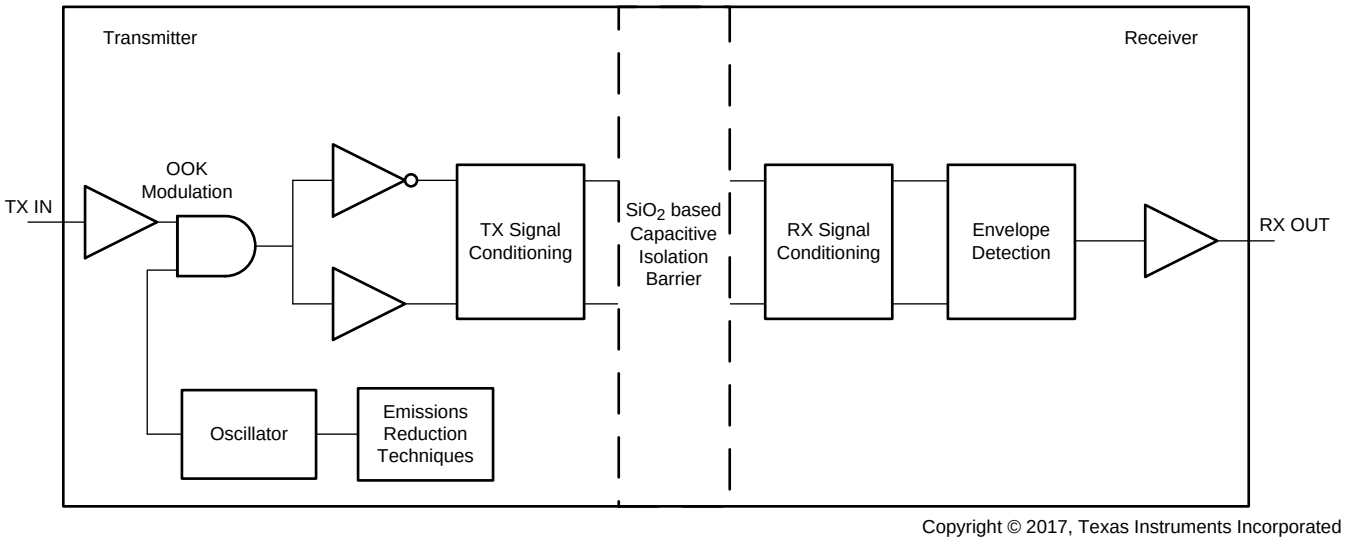


Figure 14. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 15 shows a conceptual detail of how the OOK scheme works.

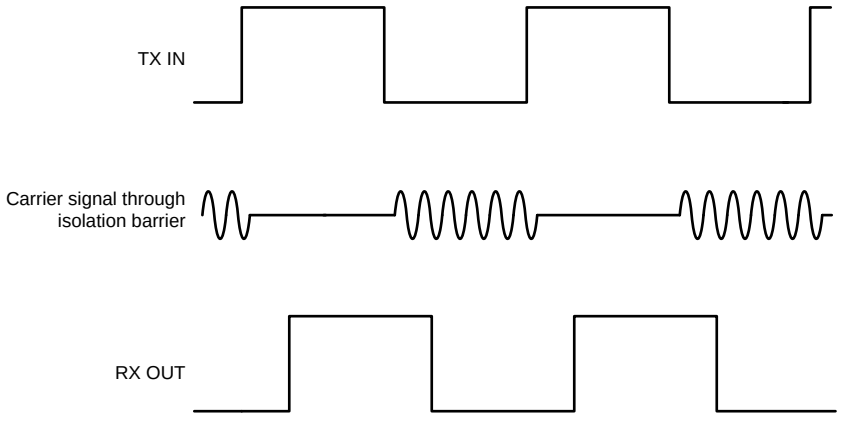


Figure 15. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISO7710-Q1 device is available in two default output state options to enable a variety of application uses. Table 1 lists the device features.

Table 1. Device Features

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION(1)
ISO7710-Q1	100 Mbps	1 Forward, 0 Reverse	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7710-Q1 with F suffix	100 Mbps	1 Forward, 0 Reverse	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}

(1) See the *Safety-Related Certifications* section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7710-Q1 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

Table 2 lists the functional modes of ISO7710-Q1 device.

Table 2. Function Table(1)

V_{CC1}	V_{CC2}	INPUT (IN)(2)	OUTPUT (OUT)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of its input.
		L	L	
		Open	Default	Default mode: When IN is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO7710-Q1 and *Low* for ISO7710-Q1 with F suffix.
PD	PU	X	Default	Default mode: When V_{CC1} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO7710-Q1 and *Low* for ISO7710-Q1 with F suffix. When V_{CC1} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CC1} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CC2} is unpowered, a channel output is undetermined (3). When V_{CC2} transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level
(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CC1}, V_{CC2} < 2.25 V.

8.4.1 Device I/O Schematics

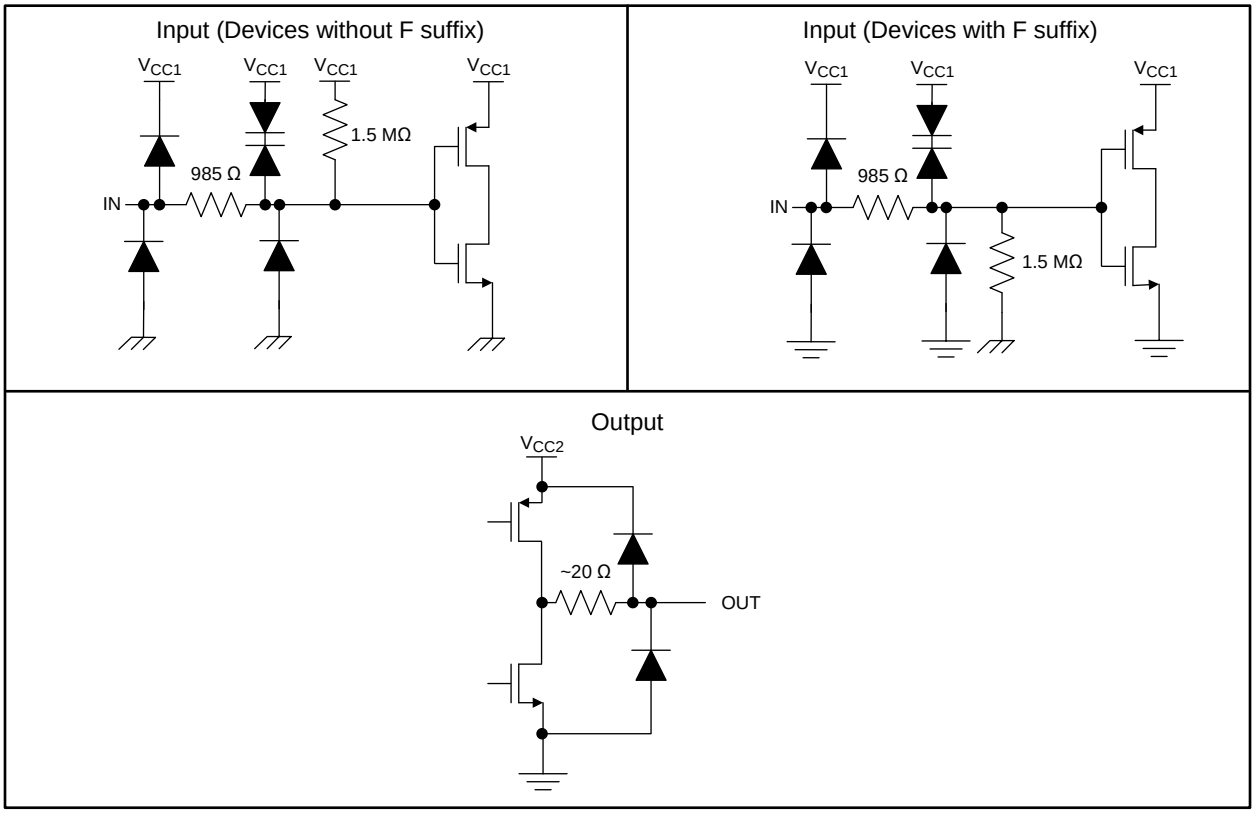


Figure 16. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7710-Q1 device is a high-performance, single-channel digital isolator. The device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7710-Q1 device can be used with Texas Instruments' mixed signal microcontroller, CAN transceiver, transformer driver, and low-dropout voltage regulator to create an Isolated CAN Interface as shown below.

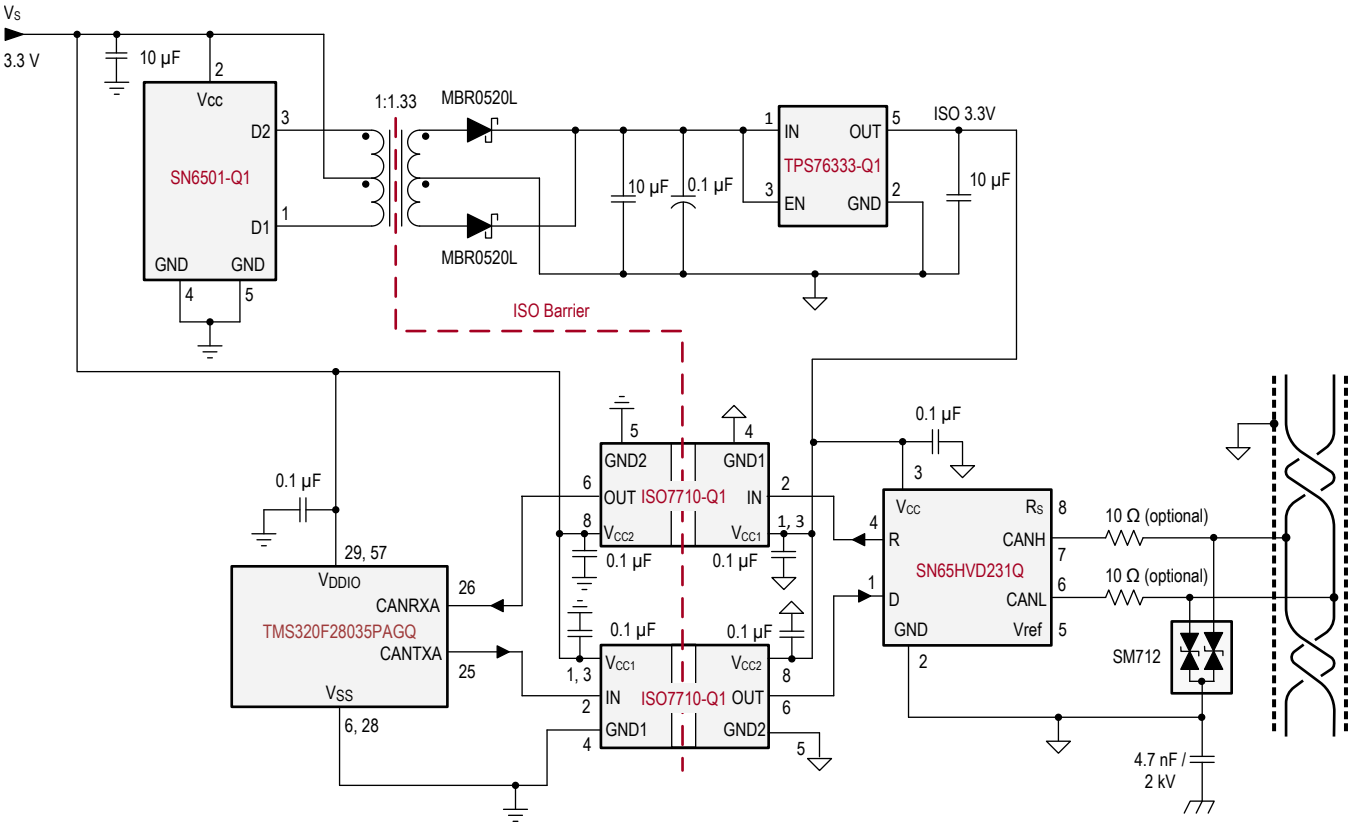


Figure 17. Isolated CAN Interface

Typical Application (continued)

9.2.1 Design Requirements

To design with this device, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require components to improve performance, provide bias, or limit current, the ISO7710-Q1 device only requires two external bypass capacitors to operate.

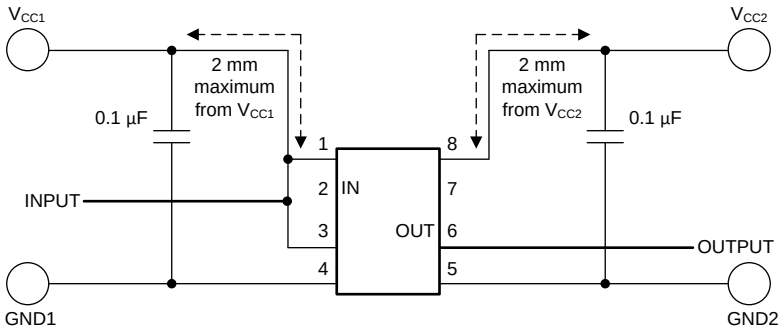


Figure 18. Typical ISO7710-Q1 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagram of the ISO7710-Q1 device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

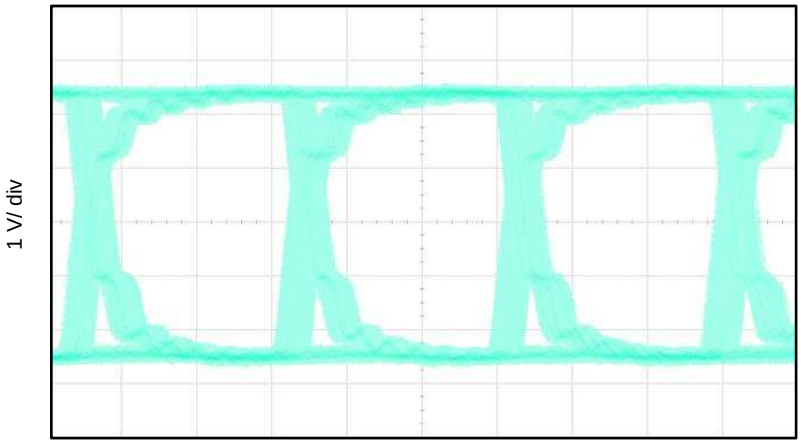


Figure 19. ISO7710-Q1 Eye Diagram at 100 Mbps PRBS, 5-V Supplies and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies*.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 20). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

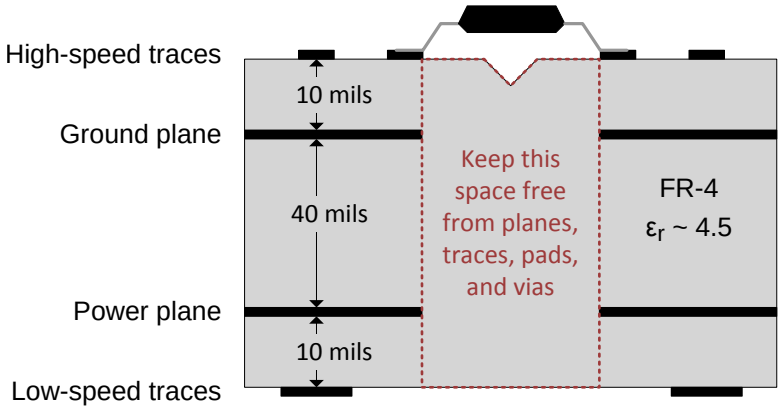


Figure 20. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Digital Isolator Design Guide*
- *Isolation Glossary*
- *SN6501-Q1 Transformer Driver for Isolated Power Supplies*
- SN65HVD231Q *Automotive 3.3-V CAN Transceiver*
- TPS76333-Q1*Low-Power 150-mA Low-Dropout Linear Regulators*
- TMS320F28035PAGQ *Piccolo™ Microcontrollers*

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

Piccolo, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

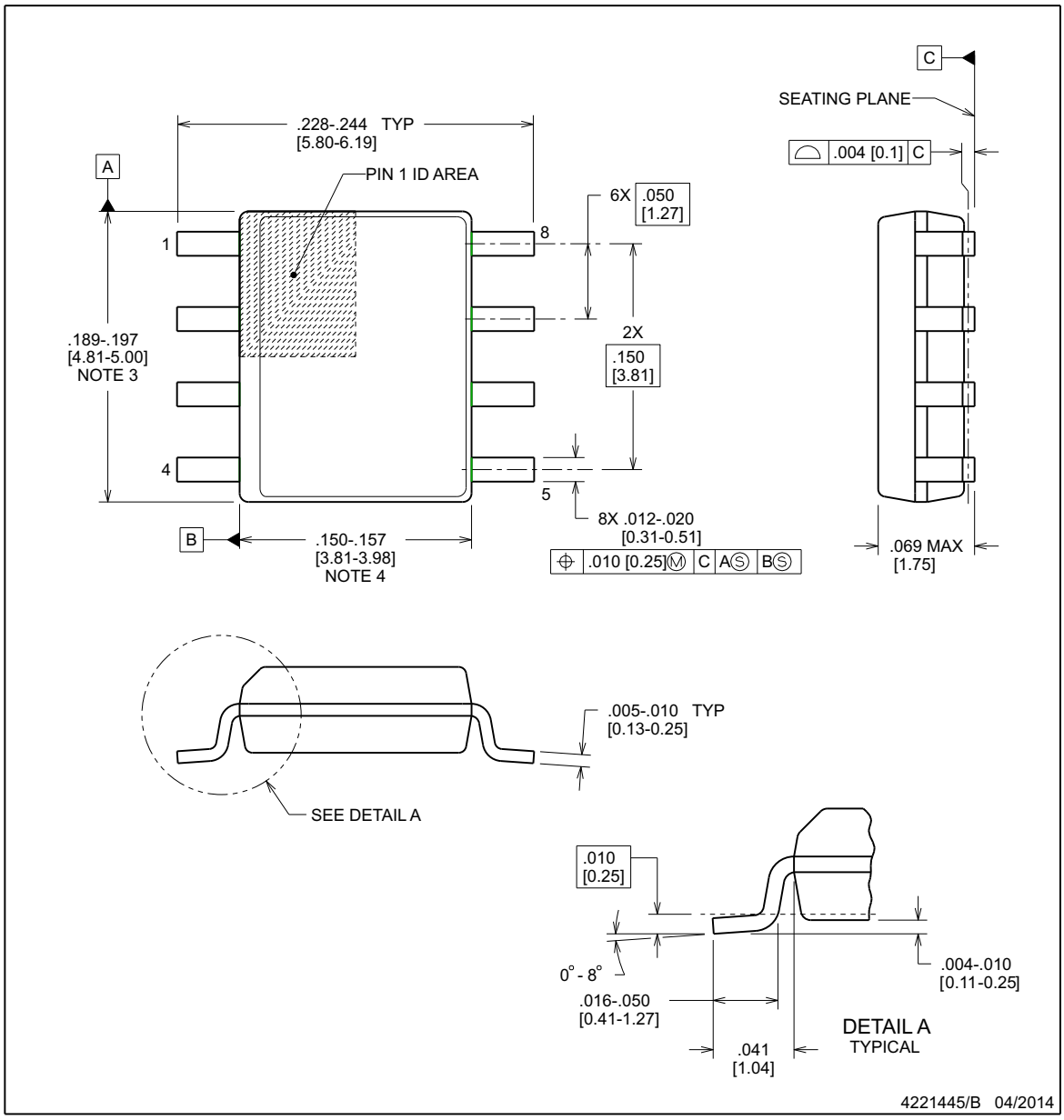
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES:

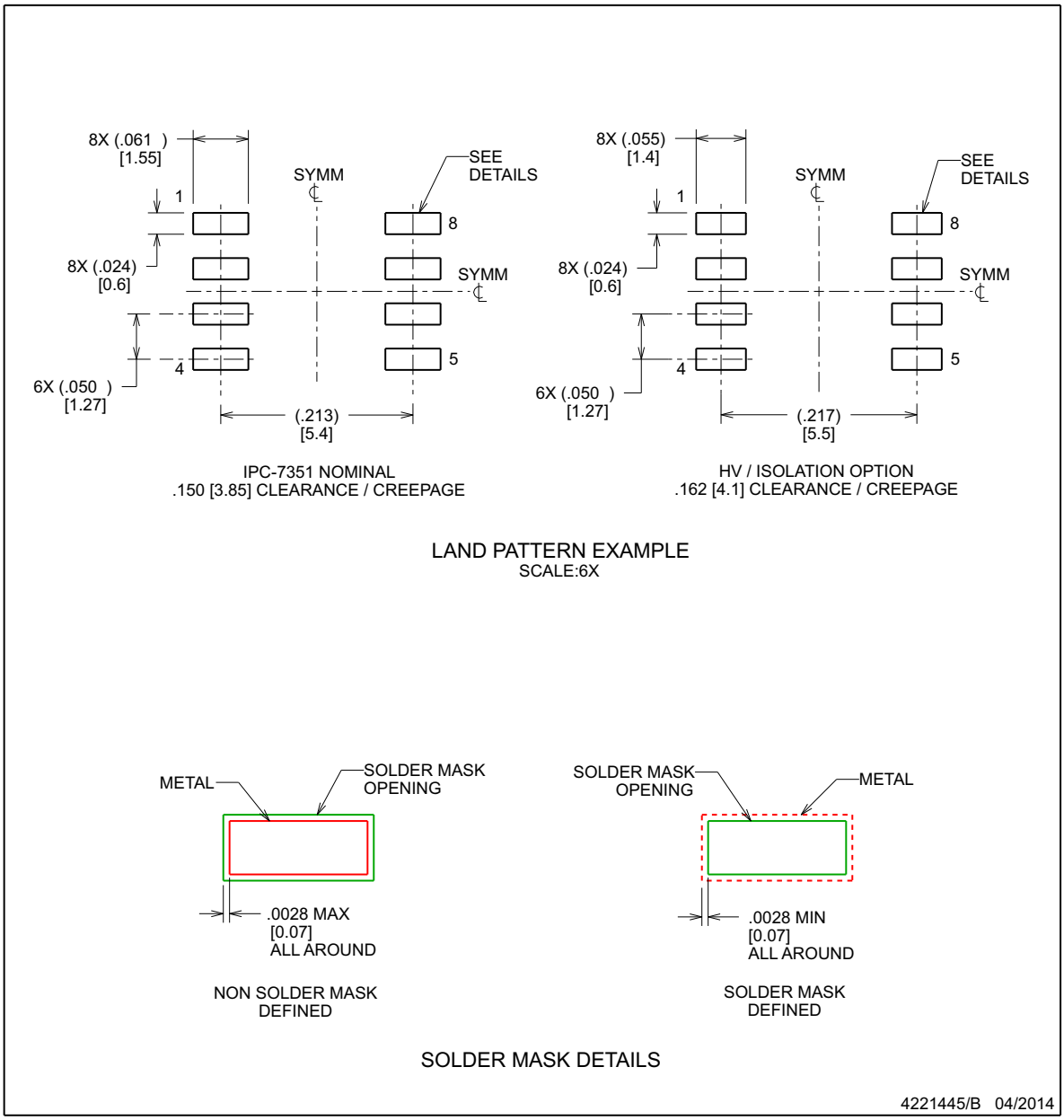
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SOIC



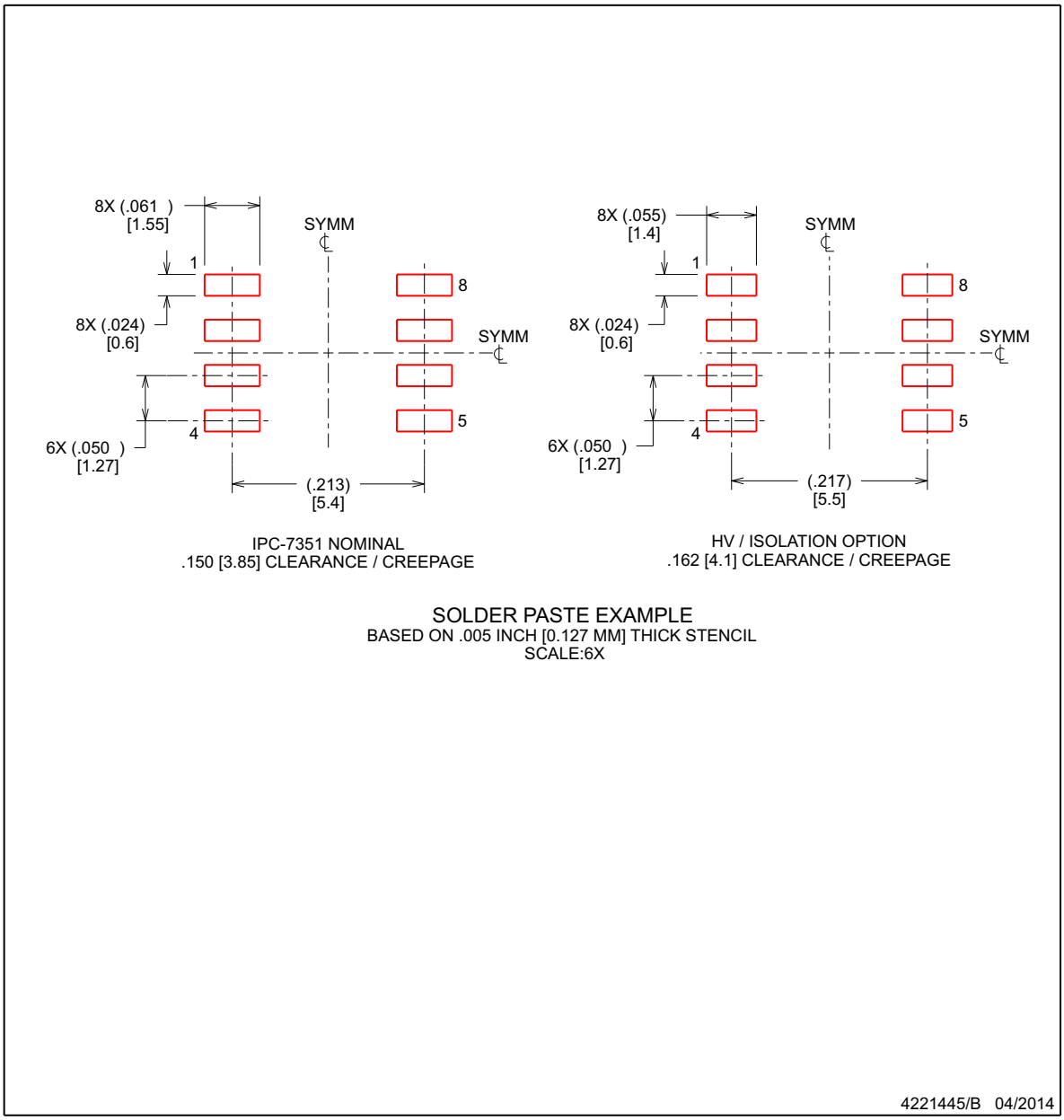
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SOIC



NOTES: (continued)

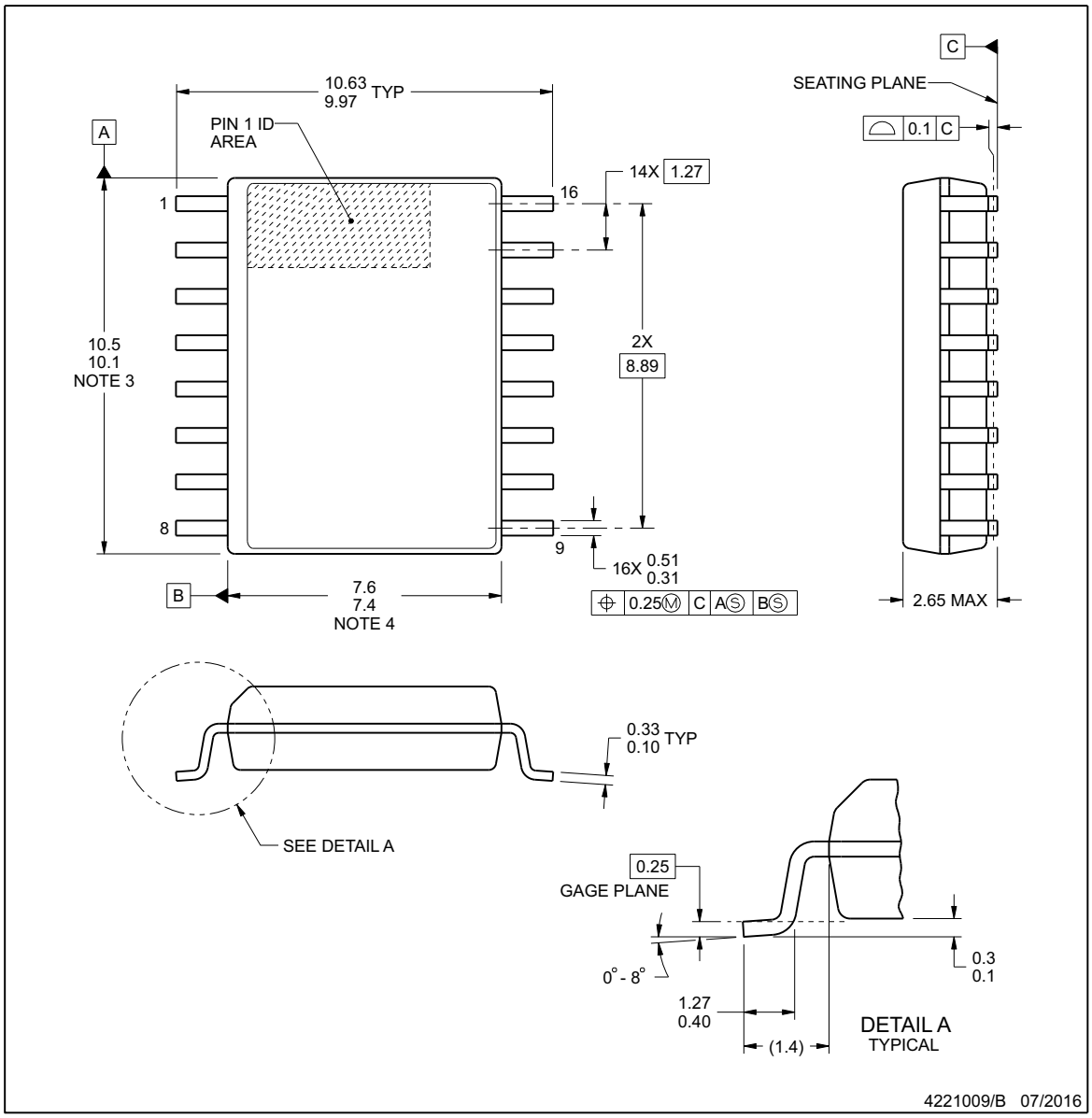
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

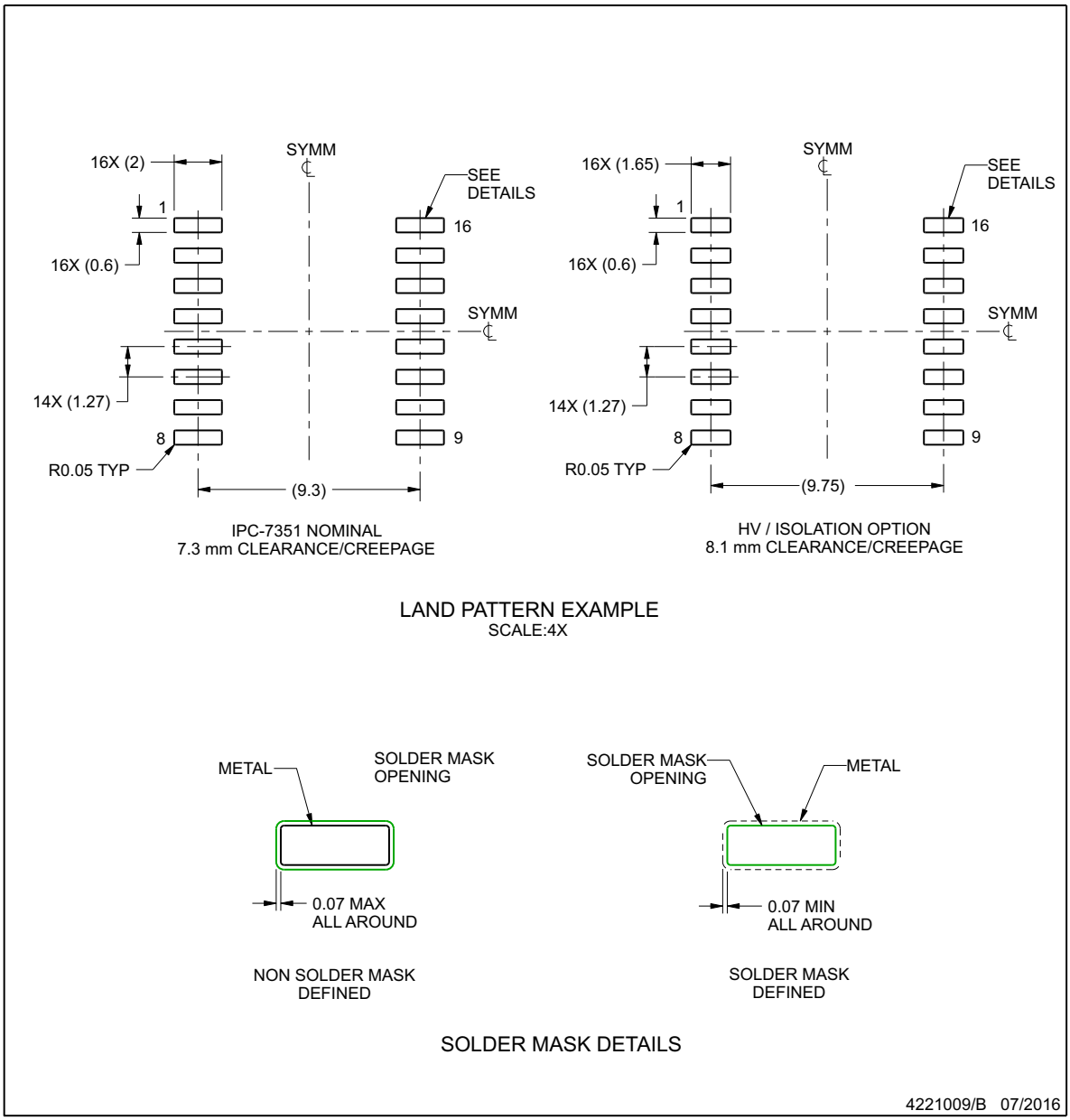
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

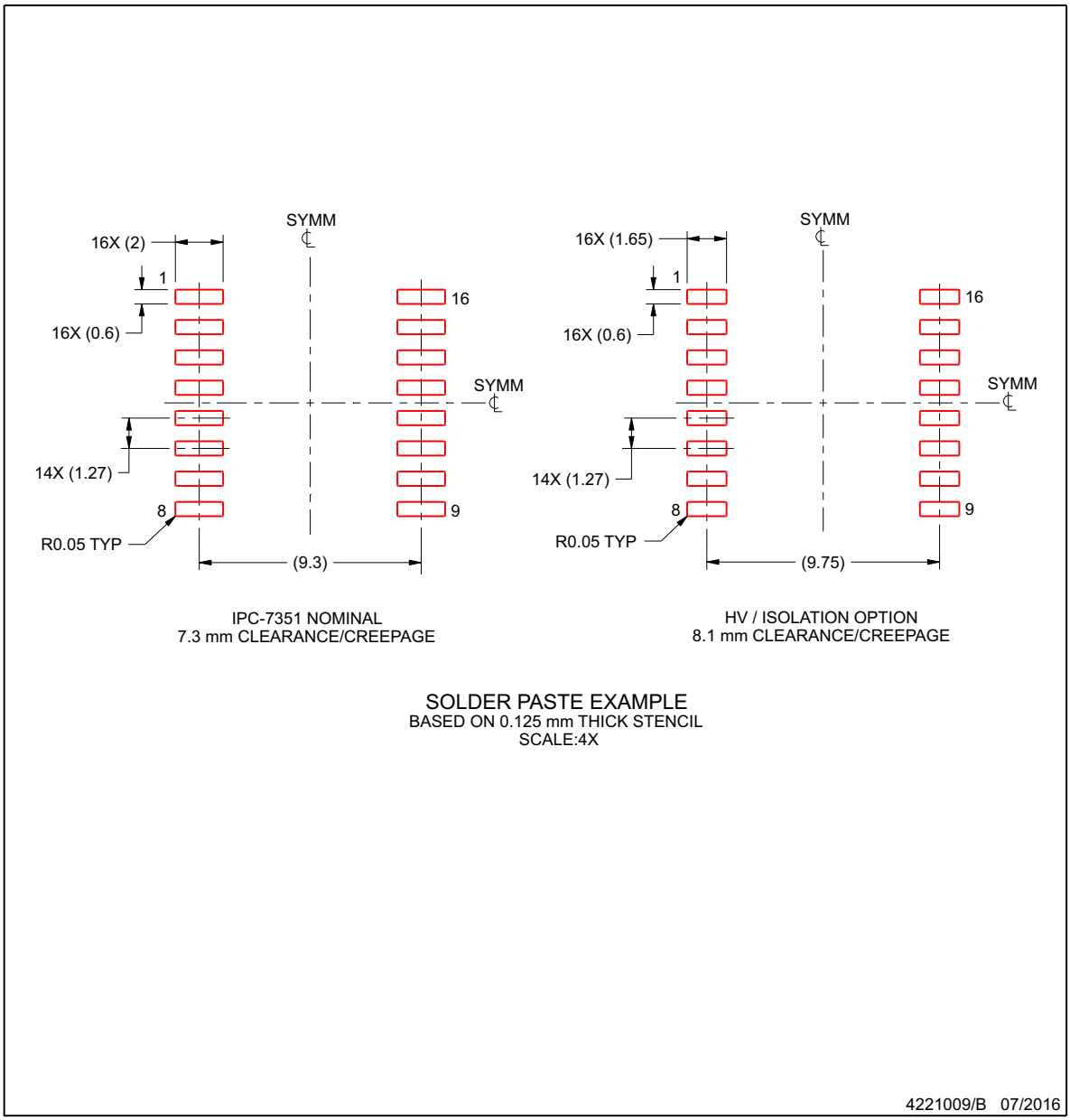
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7710FQDQ1	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7710FQ	
ISO7710FQDRQ1	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7710FQ	
ISO7710FQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7710FQ	Samples
ISO7710FQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7710FQ	Samples
ISO7710QDQ1	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7710Q	
ISO7710QDRQ1	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7710Q	
ISO7710QDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7710Q	Samples
ISO7710QDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7710Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7710-Q1 :

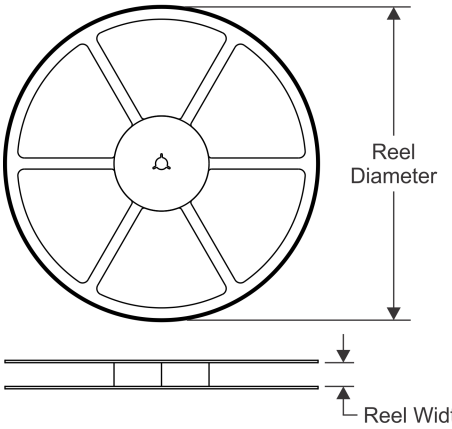
- Catalog: ISO7710

NOTE: Qualified Version Definitions:

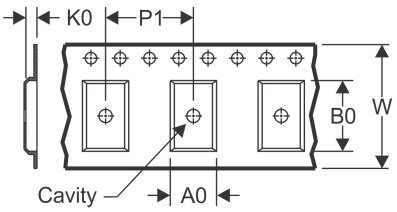
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

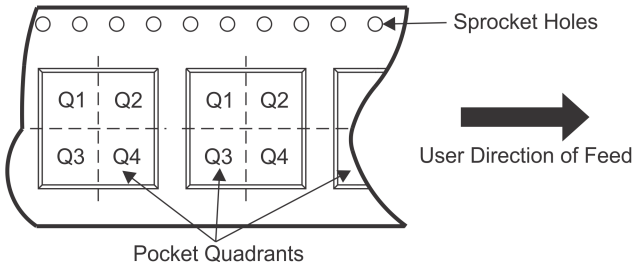


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

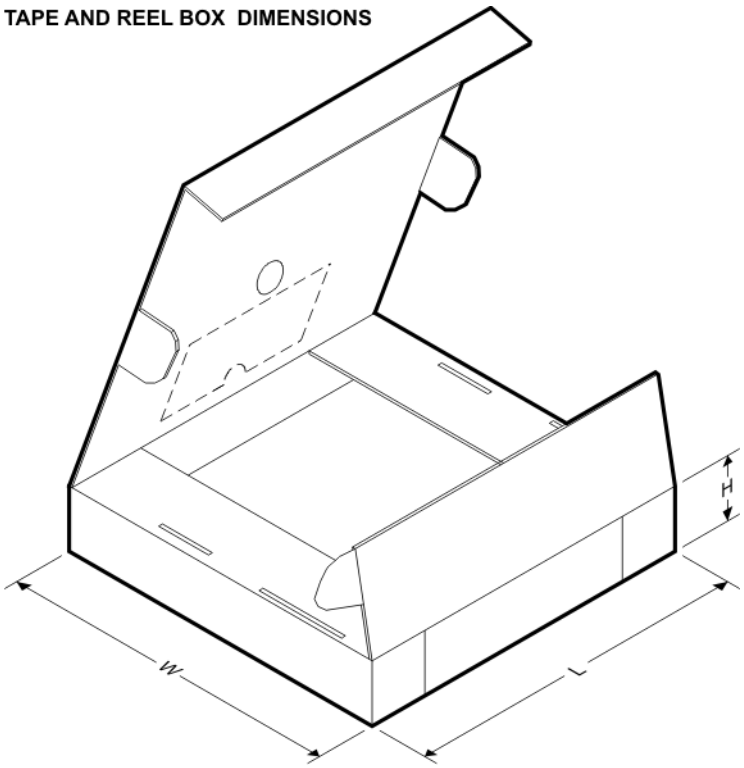
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7710FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7710QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

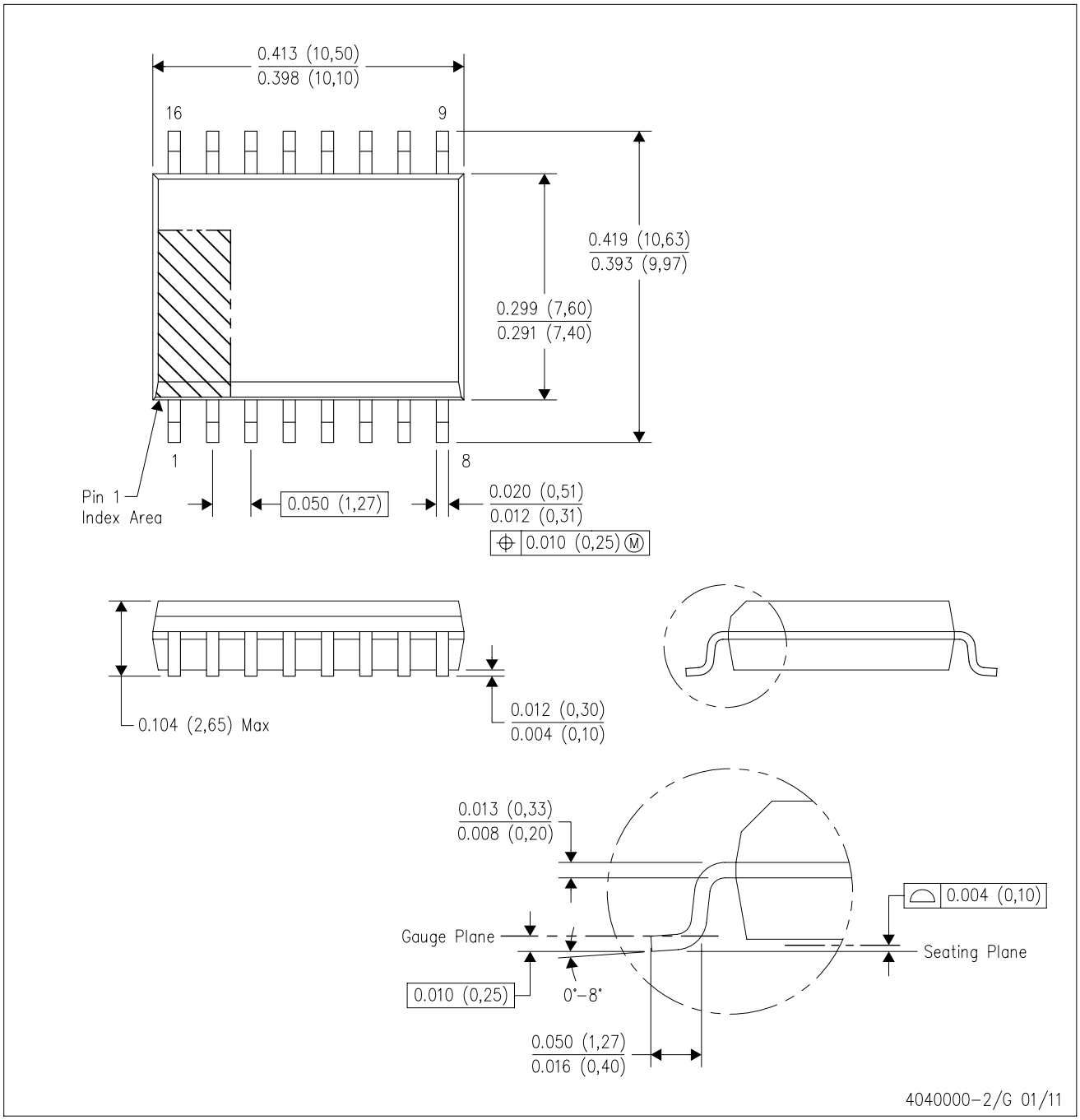
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

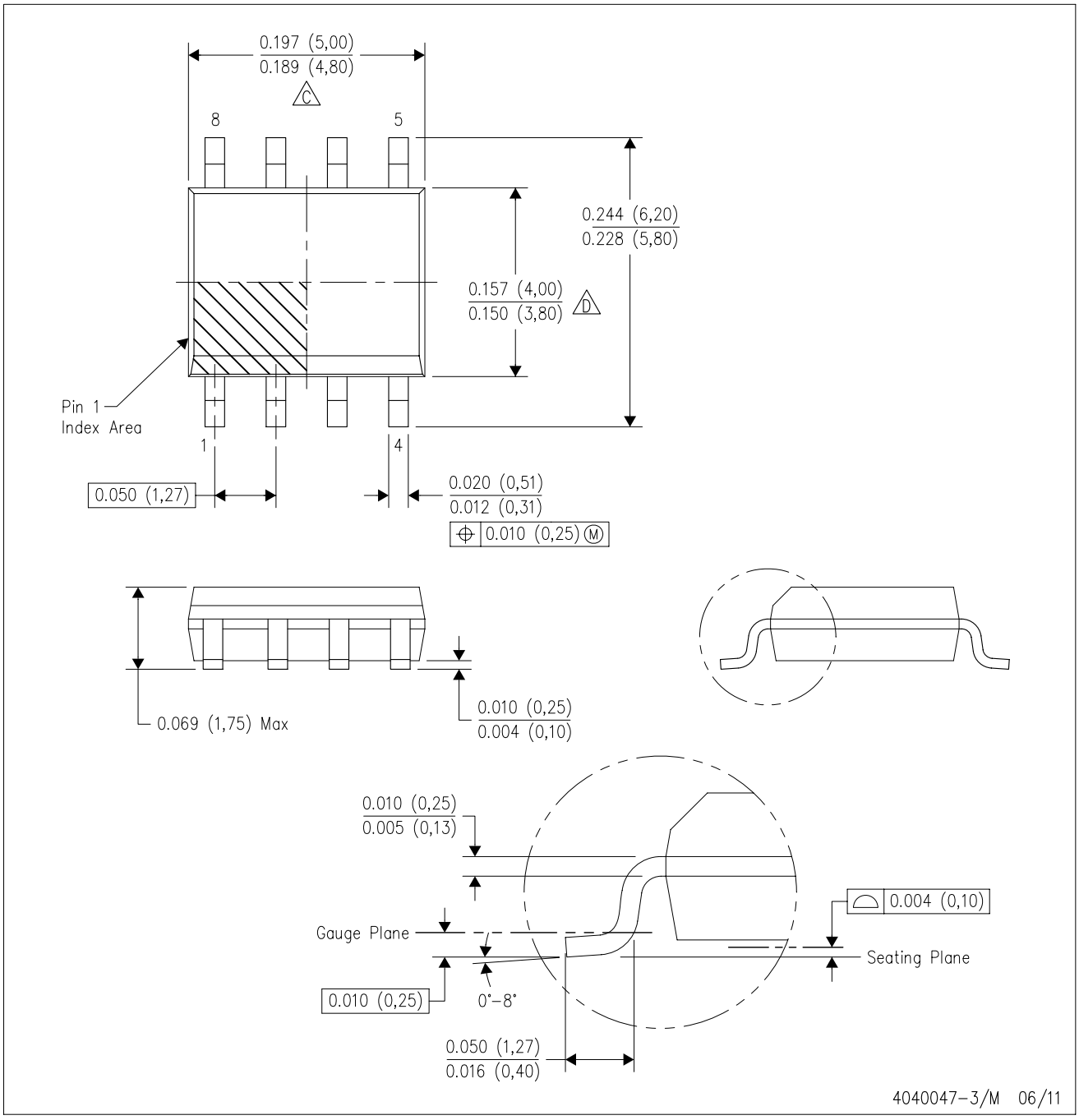
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7710FQDWRQ1	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7710QDWRQ1	SOIC	DW	16	2000	367.0	367.0	38.0

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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