TEXAS INSTRUMENTS

ISO7631FM, ISO7631FC, ISO7641FC

SLLSEC3E – SEPTEMBER 2012 – REVISED AUGUST 2015

# ISO76x1 Low-Power Triple and Quad-Channels Digital Isolators

## 1 Features

- Signaling Rate: 150 Mbps (M-Grade), 25 Mbps (C-Grade)
- Robust Design with Integrated Noise Filter (C-Grade)
- Low Power Consumption, Typical $I_{CC}$ per Channel (3.3-V Supplies):
  - ISO7631FM: 2 mA at 10 Mbps
  - ISO7631FC: 1.5 mA at 10 Mbps
  - ISO7641FC: 1.3 mA at 10 Mbps
- Extremely-Low $I_{CC\_disable}$ (C-Grade)
- Low Propagation Delay: 7 ns Typical (M-Grade)
- Output Defaults to Low-State in Fail-Safe Mode
- Wide Temperature Range: –40°C to 125°C
- 50 KV/µs Transient Immunity, Typical
- Long Life With $SiO_2$ Isolation Barrier
- Operates From 2.7-V (M-Grade), 3.3-V and 5-V Supply and Logic Levels
- 2.7-V (M-Grade), 3.3-V and 5-V Level Translation
- Wide Body SOIC-16 Package
- Safety and Regulatory Approvals
  - 2500 $V_{RMS}$ Isolation for 1 Minute per UL 1577
  - 4242 $V_{PK}$ Basic Insulation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
  - TUV 3000 $V_{RMS}$ Reinforced Insulation according to EN/UL/CSA 60950-1 and EN/UL/CSA 61010-1

## 2 Applications

- Optocoupler Replacement in:
  - Industrial Fieldbus
    - Profibus
    - Modbus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

## 3 Description

The ISO7631F and ISO7641F devices provide galvanic isolation up to 4242 $V_{PK}$ per VDE. The ISO7631F device has three channels, two of which operate in the forward direction and one which operates in the reverse direction. The ISO7641F device has 4 channels, three of which operate in the forward direction and one of which operates in the reverse direction. Suffix F indicates that output defaults to low-state in fail-safe conditions (see ). M-Grade devices are high-speed isolators capable of up to150-Mbps data rates with fast propagation delays, whereas C-Grade devices are capable of up to 25-Mbps data rates with low power consumption and integrated filters for noise-prone applications. C-Grade devices are recommended for lower-speed applications where input noise pulses of less than 6 ns duration must be suppressed, or when low-power consumption is critical.

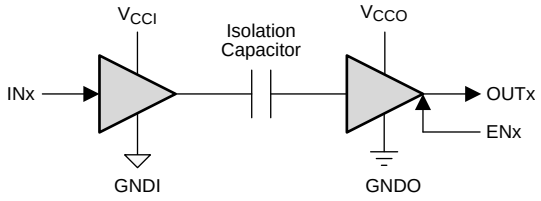
Each isolation channel has a logic input and output buffer separated by a silicon dioxide ($SiO_2$) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 2.7-V (M-Grade), 3.3-V and 5-V supplies. All inputs are 5-V tolerant when supplied from 3.3-V or 2.7-V supplies.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ISO7631FM | SOIC (16) | 10.30 mm × 7.50 mm |
| ISO7631FC | | |
| ISO7641FC | | |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematic**




(1) $V_{CCI}$ and GNDI are supply and ground connections respectively for the input channels.

(2) $V_{CCO}$ and GNDO are supply and ground connections respectively for the output channels.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision D (September 2013) to Revision E** **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added 2.7-V (M-Grade), 3.3-V and 5-V Level Translation to *Features* section ... 1
- Deleted *marked as* column from *Available Options* table ... 4
- Added Footnote 3 to *Absolute Maximum Ratings* table. ... 5
- Changed thermal metric values in the *Thermal Information* table. ... 6
- Changed $V_{CCX}$ to $V_{CCO}$ in *Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5 V ± 10%* table. ... 6
- Added cross-reference to VI = $V_{CCI}$ in the *Electrical Characteristics: VCC1 and VCC2 at 5 V ± 10%* table. ... 6
- Changed Footnote 1 of the *Electrical Characteristics: VCC1 and VCC2 at 5 V ± 10%* table for clarification. ... 6
- Added cross-reference to VI = $V_{CCI}$ in the *Electrical Characteristics: VCC1 at 5 V ± 10% and VCC2 at 3.3 V ± 10%* table. ... 6
- Added footnote to the *Electrical Characteristics: VCC1 at 3.3 V ± 10% and VCC2 at 5 V ± 10%* table. ... 7
- Changed $V_{CCX}$ to $V_{CCO}$ in the *Electrical Characteristics: VCC1 and VCC2 at 3.3 V ± 10%* table. ... 7

## Revision History (continued)

- Changed footnote 1 in the *Electrical Characteristics: VCC1 and VCC2 at 3.3 V ± 10%* table for clarification. ..... 7
- Changed $V_{CCX}$ to $V_{CCO}$ in the *Electrical Characteristics: VCC1 and VCC2 at 2.7 V* table. ..... 7
- Deleted *IEC* and *for DW-16 Package* from *IEC Package Insulation and Safety-Related Specifications for DW-16 Package* section. ..... 20
- Changed L(I01) MIN from 8.3 mm to 8 mm, L(IO2) MIN from 8.1 mm to 8 mm, and DIN IEC 60112 / VDE 0303 Part 1 to DIN EN 60112 (VDE 0303-11); IEC 60112 in the *Package Insulation and Safety-Related Specifications* table. ..... 20
- Deleted footnote 2 from *Package Insulation and Safety-Related Specifications IEC and for DW-16 Package from IEC Package Insulation and Safety-Related Specifications for DW-16 Package* section.. ..... 20
- Changed VDE Standard to DIN V VDE V 0884-10 (VDE V 0084-10): 2006-12. ..... 21
- Changed the value for $\theta_{JA}$ from 72 °C/W to 77.5 °C/W for the Test Conditions and the values for Safety input, output, or supply current max from 316, 482, and 643 to 293, 448 and 597 in the *Safety Limiting Values* table. ..... 22
- Changed *safety temperature* to *case temperature* in *Safety Limiting Values*. ..... 22
- Changed name of *DW-16 θJC Thermal Derating Curve per IEC 64747-5-2* to *Thermal Derating Curve for Safety Limiting Current per VDE*..... 22
- Changed graph in *Safety Limiting Values* section. ..... 22
- Changed I/O schematics figure in *Feature Description* section. ..... 23

**Changes from Revision C (August 2013) to Revision D** **Page**

- Deleted 2500 $V_{RMS}$ from Rated Isolation Data ..... 4
- Changed the REGULATORY INFORMATION table, TUV column From: Certificate Number: U8V 13 07 77311 009 To: Certificate Number: U8V 13 09 77311 010 ..... 21

**Changes from Revision B (April 2013) to Revision C** **Page**

- Deleted the device image from the top of the page ..... 1
- Deleted device number ISO7640FC..... 1
- Changed the Description ..... 1
- Deleted ISO7640FC from the Available Options table ..... 4
- Changed The ISO7631FC Rated Isolation values in the Available Options table ..... 4
- Deleted Graph ISO7640FC Supply Current Per Channel vs Data Rate ..... 14
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- Added the TUV column to the REGULATORY INFORMATION table ..... 21
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- Deleted the ISO7640 circuit from the APPLICATION INFORMATION section..... 27

**Changes from Revision A (September 2012) to Revision B** **Page**

- Changed the $V_{IOTM}$ SPECIFICATION From: 4000 $V_{PEAK}$ to 4242 $V_{PEAK}$..... 21
- Changed the REGULATORY INFORMATION table: 4242 $V_{PK}$ To: 4000 $V_{PK}$ ..... 21

**Changes from Original (September 2012) to Revision A** **Page**

- Changed Description text From: "applications where input noise pulses of less than 10 ns duration..." To:"applications where input noise pulses of less than 6 ns duration..."..... 1
- Added note *Product Preview* to ISO7640FC in the Available Options table..... 4
- Changed Input PU in the Function table From: Z To: 'Undetermined ..... 22

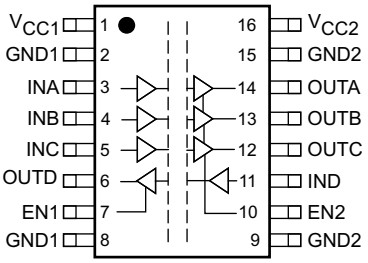
# 5 Available Options

| PRODUCT | RATED ISOLATION(1) | PACKAGE | INPUT THRESHOLD | DATA RATE | INTEGRATED NOISE FILTER | CHANNEL DIRECTION |
|---|---|---|---|---|---|---|
| ISO631FM | 4242 $V_{PK}$ | DW-16 | ~1.5 V TTL | 150 Mbps | No | 2 Forward, 1 Reverse |
| ISO7631FC | 4242 $V_{PK}$ | DW-16 | ~1.5 V TTL | 25 Mbps | Yes | 2 Forward, 1 Reverse |
| ISO7641FC | 4242 $V_{PK}$ | DW-16 | ~1.5 V TTL | 25 Mbps | Yes | 3 Forward, 1 Reverse |

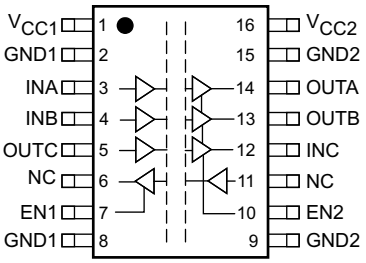
(1) See the Regulatory Information table for detailed isolation ratings.

# 6 Pin Configuration and Functions

**ISO7641 DW Package**
**16-Pin SOIC**
**Top View**




**ISO07631 DW Package**
**16-Pin SOIC**
**Top View**




**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | ISO7641 | ISO7631 | | |
| EN1 | 7 | 7 | I | Enables (when input is High or Open) or Disables (when input is Low) OUTD of ISO7641 and OUTC of ISO7631 |
| EN2 | 10 | 10 | I | Enables (when input is High or Open) or Disables (when input is Low) OUTA, OUTB, and OUTC of ISO7641<br>Enables (when input is High or Open) or Disables (when input is Low) OUTA and OUTB of ISO7631 |
| GND1 | 2, 8 | 2, 8 | – | Ground connection for $V_{CC1}$ |
| GND2 | 9, 15 | 9, 15 | – | Ground connection for $V_{CC2}$ |
| INA | 3 | 3 | I | Input, channel A |
| INB | 4 | 4 | I | Input, channel B |
| INC | 5 | 12 | I | Input, channel C |
| IND | 11 | – | I | Input, channel D |
| NC | – | 6,11 | – | No Connect pins are floating with no internal connection |
| OUTA | 14 | 14 | O | Output, channel A |
| OUTB | 13 | 13 | O | Output, channel B |
| OUTC | 12 | 5 | O | Output, channel C |
| OUTD | 6 | – | O | Output, channel D |
| $V_{CC1}$ | 1 | 1 | – | Power supply, $V_{CC1}$ |
| $V_{CC2}$ | 16 | 16 | – | Power supply, $V_{CC2}$ |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

See (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC1}$ $V_{CC2}$ (2) | Supply voltage | | –0.5 | 6 | V |
| | Voltage | INx, OUTx, ENx | –0.5 | 6 (3) | V |
| $I_O$ | Output current | | | ±15 | mA |
| $T_J$ | Maximum junction temperature | | | 150 | °C |
| $T_{STG}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±1500 | |
| | | Machine model (MM), JEDEC JESD22-A115-A | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply voltage | M-Grade | 2.7 | | 5.5 | V |
| | | C-Grade | 3 | | 5.5 | |
| $I_{OH}$ | High-level output current | | –4 | | | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | mA |
| $V_{IH}$ | High-level input voltage | | 2 | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | | 0 | | 0.8 | V |
| $t_{ui}$ | Input pulse duration | M-Grade: ≥3-V Operation | 6.67 | | | ns |
| | | M-Grade: <3-V Operation | 10 | | | |
| | | C-Grade: ≥3-V Operation | 40 | | | |
| 1 / $t_{ui}$ | Signaling rate | M-Grade: ≥3-V Operation | 0 | | 150 | Mbps |
| | | M-Grade: <3-V Operation | 0 | | 100 | |
| | | C-Grade: ≥3-V Operation | 0 | | 25 | |
| $T_J$ | Junction temperature | | –40 | | 136 | °C |
| $T_A$ | Ambient temperature | | –40 | 25 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC[1] | | ISO76x1Fx DW (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 77.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 40.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 42.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 15 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 41.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5 V ± 10%

$V_{CC1}$ and $V_{CC2}$ at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA; see Figure 16 | $V_{CCO}$[1] – 0.8 | 4.8 | | $V_{CCO}$ – 0.8 | 4.7 | | V |
| | | $I_{OH}$ = –20 µA; see Figure 16 | $V_{CCO}$ – 0.1 | 5 | | $V_{CCO}$ – 0.1 | 5 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; see Figure 16 | | 0.2 | 0.4 | | 0.3 | 0.5 | V |
| | | $I_{OL}$ = 20 µA; see Figure 16 | | 0 | 0.1 | | 0 | 0.1 | |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | | 450 | | | 450 | | mV |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CC}$ at INx or ENx | | | 10 | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx or ENx | –10 | | | -10 | | | µA |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CCI}$ [1] or 0 V; see Figure 19 | 25 | 75 | | 25 | 75 | | kV/µs |

(1) $V_{CCI}$ = Input-side supply voltage; $V_{CCO}$ = Output-side supply voltage

## 7.6 Electrical Characteristics: $V_{CC1}$ at 5 V ± 10% and $V_{CC2}$ at 3.3 V ± 10%

$V_{CC1}$ at 5 V ± 10% and $V_{CC2}$ at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA; see Figure 16 | OUTx on $V_{CC1}$ (5 V) side | $V_{CC1}$ – 0.8 | 4.8 | | $V_{CC1}$ – 0.8 | 4.7 | | V |
| | | | OUTx on $V_{CC2}$ (3.3 V) side | $V_{CC2}$ - 0.4 | 3 | | $V_{CC2}$ - 0.6 | 2.9 | | |
| | | $I_{OH}$ = –20 µA; see Figure 16 | OUTx on $V_{CC1}$ (5 V) side | $V_{CC1}$ – 0.1 | 5 | | $V_{CC1}$ – 0.1 | 5 | | |
| | | | OUTx on $V_{CC2}$ (3.3 V) side | $V_{CC2}$ – 0.1 | 3.3 | | $V_{CC2}$ – 0.1 | 3.3 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; see Figure 16 | | | 0.2 | 0.4 | | 0.3 | 0.5 | V |
| | | $I_{OL}$ = 20 µA; see Figure 16 | | | 0 | 0.1 | | 0 | 0.1 | |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | | | 430 | | | 430 | | mV |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CC}$ at INx or ENx | | | | 10 | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx or ENx | | -10 | | | -10 | | | µA |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CCI}$ [1] or 0 V; see Figure 19 | | 25 | 50 | | 25 | 50 | | kV/µs |

(1) $V_{CCI}$ = Input-side supply voltage

## 7.7 Electrical Characteristics: $V_{CC1}$ at 3.3 V ± 10% and $V_{CC2}$ at 5 V ± 10%

$V_{CC1}$ at 3.3 V ± 10% and $V_{CC2}$ at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA; see Figure 16 | OUTx on $V_{CC1}$ (3.3 V) side | $V_{CC1}$–0.4 | 3 | | $V_{CC1}$-0.6 | 2.9 | | V |
| | | | OUTx on $V_{CC2}$ (5 V) side | $V_{CC2}$–0.8 | 4.8 | | $V_{CC2}$–0.8 | 4.7 | | |
| | | $I_{OH}$ = –20 μA; see Figure 16 | OUTx on $V_{CC1}$ (3.3 V) side | $V_{CC1}$–0.1 | 3.3 | | $V_{CC1}$–0.1 | 3.3 | | |
| | | | OUTx on $V_{CC2}$ (5 V) side | $V_{CC2}$–0.1 | 5 | | $V_{CC2}$–0.1 | 5 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; see Figure 16 | | | 0.2 | 0.4 | | 0.3 | 0.5 | V |
| | | $I_{OL}$ = 20 μA; see Figure 16 | | | 0 | 0.1 | | 0 | 0.1 | |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | | | 430 | | | 430 | | mV |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CC}$ at INx or ENx | | | | 10 | | | 10 | μA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx or ENx | | -10 | | | -10 | | | μA |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CCI}$ (1) or 0 V; see Figure 19 | | 25 | 50 | | 25 | 50 | | kV/μs |

(1) $V_{CCI}$ = Input-side supply voltage

## 7.8 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V ± 10%

$V_{CC1}$ and $V_{CC2}$ at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA; see Figure 16 | $V_{CCO}$ (1) – 0.4 | 3 | | $V_{CCO}$ – 0.6 | 2.9 | | V |
| | | $I_{OH}$ = –20 μA; see Figure 16 | $V_{CCO}$ – 0.1 | 3.3 | | $V_{CCO}$ – 0.1 | 3.3 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; see Figure 16 | | 0.2 | 0.4 | | 0.3 | 0.5 | V |
| | | $I_{OL}$ = 20 μA; see Figure 16 | | 0 | 0.1 | | 0 | 0.1 | |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | | 425 | | | 425 | | mV |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CC}$ at INx or ENx | | | 10 | | | 10 | μA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx or ENx | -10 | | | -10 | | | μA |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CCI}$ (1) or 0 V; see Figure 19 | 25 | 50 | | 25 | 50 | | kV/μs |

(1) $V_{CCI}$ = Input-side supply voltage; $V_{CCO}$ = Output-side supply voltage

## 7.9 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 2.7 V (ISO7631FM Only)

$V_{CC1}$ and $V_{CC2}$ at 2.7 V(1) (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA; see Figure 16 | $V_{CCO}$ (2) – 0.5 | 2.4 | | V |
| | | $I_{OH}$ = –20 μA; see Figure 16 | $V_{CCO}$ – 0.1 | 2.7 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; see Figure 16 | | 0.2 | 0.4 | V |
| | | $I_{OL}$ = 20 μA; see Figure 16 | | 0 | 0.1 | |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | | 350 | | mV |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CC}$ at INx or ENx | | | 10 | μA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx or ENx | -10 | | | μA |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CCI}$ (2) or 0 V; see Figure 19 | 25 | 50 | | kV/μs |

(1) Only M-Grade devices are recommended for operation down to 2.7 V supplies. For 2.7 V-operation, max data rate is 100 Mbps.
(2) $V_{CCI}$ = Input-side supply voltage; $V_{CCO}$ = Output-side supply voltage

## 7.10 Power Dissipation Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Maximum Device Power Dissipation | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, CL = 15 pF<br>Input a 75 MHz 50% duty cycle square wave | | | 399 | mW |

## 7.11 Supply Current Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5 V ± 10%

$V_{CC1}$ and $V_{CC2}$ at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISO7631F** | | | | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | 2.5 | 4 | | 1.1 | 1.9 | mA |
| $I_{CC2}$ | | | | 3.7 | 5.4 | | 1.5 | 2.6 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I$ = $V_{CC}$ or 0 V<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | 2.6 | 4.1 | | 1.8 | 2.7 | mA |
| $I_{CC2}$ | | | | 3.8 | 5.5 | | 2.6 | 3.9 | mA |
| $I_{CC1}$ | 10 Mbps | | | 3.3 | 4.5 | | 2.7 | 3.7 | mA |
| $I_{CC2}$ | | | | 4.9 | 6.6 | | 3.9 | 5.3 | mA |
| $I_{CC1}$ | 25 Mbps | | | 4.5 | 6 | | 4.1 | 5.4 | mA |
| $I_{CC2}$ | | | | 6.8 | 9 | | 5.9 | 7.8 | mA |
| $I_{CC1}$ | 150 Mbps | | | 15 | 19.5 | Not Applicable | | | mA |
| $I_{CC2}$ | | | | 22 | 30 | Not Applicable | | | mA |
| **ISO7641F** | | | | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | | | | 1.2 | 2.1 | mA |
| $I_{CC2}$ | | | | | | | 1.6 | 2.6 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I$ = $V_{CC}$ or 0 V,<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | | | | 1.8 | 2.8 | mA |
| $I_{CC2}$ | | | | | | | 3.1 | 4.2 | mA |
| $I_{CC1}$ | 10 Mbps | | | | | | 3 | 4 | mA |
| $I_{CC2}$ | | | | | | | 4.9 | 6.1 | mA |
| $I_{CC1}$ | 25 Mbps | | | | | | 4.8 | 6 | mA |
| $I_{CC2}$ | | | | | | | 7.7 | 9.5 | mA |

## 7.12 Supply Current Characteristics: $V_{CC1}$ at 5 V ± 10% and $V_{CC2}$ at 3.3 V ± 10%

$V_{CC1}$ at 5 V ± 10% and $V_{CC2}$ at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISO7631F** | | | | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | 2.5 | 4 | | 1.1 | 1.9 | mA |
| $I_{CC2}$ | | | | 2.7 | 3.7 | | 0.7 | 1.3 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I$ = $V_{CC}$ or 0 V<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | 2.6 | 4.1 | | 1.8 | 2.7 | mA |
| $I_{CC2}$ | | | | 2.8 | 3.8 | | 1.8 | 2.6 | mA |
| $I_{CC1}$ | 10 Mbps | | | 3.3 | 4.5 | | 2.7 | 3.7 | mA |
| $I_{CC2}$ | | | | 3.5 | 4.6 | | 2.6 | 3.5 | mA |
| $I_{CC1}$ | 25 Mbps | | | 4.5 | 6 | | 4.1 | 5.4 | mA |
| $I_{CC2}$ | | | | 4.7 | 5.9 | | 3.8 | 5 | mA |
| $I_{CC1}$ | 150 Mbps | | | 15 | 19.5 | Not Applicable | | | mA |
| $I_{CC2}$ | | | | 14.6 | 19 | Not Applicable | | | mA |
| **ISO7641F** | | | | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | | | | 1.2 | 2.1 | mA |
| $I_{CC2}$ | | | | | | | 0.8 | 1.3 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I$ = $V_{CC}$ or 0 V,<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | | | | 1.8 | 2.8 | mA |
| $I_{CC2}$ | | | | | | | 2 | 2.9 | mA |
| $I_{CC1}$ | 10 Mbps | | | | | | 3 | 4 | mA |
| $I_{CC2}$ | | | | | | | 3.2 | 4.1 | mA |
| $I_{CC1}$ | 25 Mbps | | | | | | 4.8 | 6 | mA |
| $I_{CC2}$ | | | | | | | 5.1 | 7 | mA |

## 7.13 Supply Current Characteristics: $V_{CC1}$ at 3.3 V ± 10% and $V_{CC2}$ at 5 V ± 10%

$V_{CC1}$ at 3.3 V ± 10% and $V_{CC2}$ at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISO7631F** | | | | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | 1.8 | 2.8 | | 0.6 | 1.1 | mA |
| $I_{CC2}$ | | | | 3.7 | 5.4 | | 1.5 | 2.6 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I$ = $V_{CC}$ or 0 V<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | 1.9 | 2.9 | | 1.2 | 1.8 | mA |
| $I_{CC2}$ | | | | 3.8 | 5.5 | | 2.6 | 3.9 | mA |
| $I_{CC1}$ | 10 Mbps | | | 2.4 | 3.4 | | 1.8 | 2.6 | mA |
| $I_{CC2}$ | | | | 4.9 | 6.6 | | 3.9 | 5.3 | mA |
| $I_{CC1}$ | 25 Mbps | | | 3.2 | 4.2 | | 2.7 | 3.6 | mA |
| $I_{CC2}$ | | | | 6.8 | 9 | | 5.9 | 7.8 | mA |
| $I_{CC1}$ | 150 Mbps | | | 9.3 | 12.5 | Not Applicable | | | mA |
| $I_{CC2}$ | | | | 22 | 30 | Not Applicable | | | mA |
| **ISO7641F** | | | | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | | | | 0.7 | 1.1 | mA |
| $I_{CC2}$ | | | | | | | 1.6 | 2.6 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I$ = $V_{CC}$ or 0 V,<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | | | | 1.2 | 1.9 | mA |
| $I_{CC2}$ | | | | | | | 3.1 | 4.2 | mA |
| $I_{CC1}$ | 10 Mbps | | | | | | 2 | 2.8 | mA |
| $I_{CC2}$ | | | | | | | 4.9 | 6.1 | mA |
| $I_{CC1}$ | 25 Mbps | | | | | | 3.1 | 4 | mA |
| $I_{CC2}$ | | | | | | | 7.7 | 9.5 | mA |

## 7.14 Supply Current Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V ± 10%

$V_{CC1}$ and $V_{CC2}$ at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISO7631F** | | | | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | 1.8 | 2.8 | | 0.6 | 1.1 | mA |
| $I_{CC2}$ | | | | 2.7 | 3.7 | | 0.7 | 1.3 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I = V_{CC}$ or 0 V<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | 1.9 | 2.9 | | 1.2 | 1.8 | mA |
| $I_{CC2}$ | | | | 2.8 | 3.8 | | 1.8 | 2.6 | mA |
| $I_{CC1}$ | 10 Mbps | | | 2.4 | 3.4 | | 1.8 | 2.6 | mA |
| $I_{CC2}$ | | | | 3.5 | 4.6 | | 2.6 | 3.5 | mA |
| $I_{CC1}$ | 25 Mbps | | | 3.2 | 4.2 | | 2.7 | 3.6 | mA |
| $I_{CC2}$ | | | | 4.7 | 5.9 | | 3.8 | 5 | mA |
| $I_{CC1}$ | 150 Mbps | | | 9.3 | 12.5 | Not Applicable | | | mA |
| $I_{CC2}$ | | | | 14.6 | 19 | Not Applicable | | | mA |
| **ISO7641F** | | | | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | | | | 0.7 | 1.1 | mA |
| $I_{CC2}$ | | | | | | | 0.8 | 1.3 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I = V_{CC}$ or 0 V,<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | | | | 1.2 | 1.9 | mA |
| $I_{CC2}$ | | | | | | | 2 | 2.9 | mA |
| $I_{CC1}$ | 10 Mbps | | | | | | 2 | 2.8 | mA |
| $I_{CC2}$ | | | | | | | 3.2 | 4.1 | mA |
| $I_{CC1}$ | 25 Mbps | | | | | | 3.1 | 4 | mA |
| $I_{CC2}$ | | | | | | | 5.1 | 7 | mA |

## 7.15 Supply Current Characteristics: $V_{CC1}$ and $V_{CC2}$ at 2.7 V (ISO7631FM Only)

$V_{CC1}$ and $V_{CC2}$ at 2.7 V (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | M-Grade | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **ISO7631F** | | | | | | |
| $I_{CC1}$ | Disable | EN1 = EN2 = 0 V | | 1.5 | 2.4 | mA |
| $I_{CC2}$ | | | | 2.2 | 3.2 | mA |
| $I_{CC1}$ | DC to 1 Mbps | DC Signal: $V_I = V_{CC}$ or 0 V<br>AC Signal: All channels switching with square wave clock input; $C_L$ = 15 pF | | 1.6 | 2.5 | mA |
| $I_{CC2}$ | | | | 2.3 | 3.2 | mA |
| $I_{CC1}$ | 10 Mbps | | | 2 | 2.9 | mA |
| $I_{CC2}$ | | | | 3 | 3.9 | mA |
| $I_{CC1}$ | 25 Mbps | | | 2.7 | 3.7 | mA |
| $I_{CC2}$ | | | | 3.9 | 4.9 | mA |
| $I_{CC1}$ | 100 Mbps | | | 5.7 | 6.8 | mA |
| $I_{CC2}$ | | | | 8.6 | 12 | mA |

## 7.16 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5 V ± 10%

$V_{CC1}$ and $V_{CC2}$ at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISO7631F, ISO7641F** | | | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 16 | 3.5 | 7 | 10.5 | 11 | 17 | 28 | ns |
| PWD(1) | Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 16 | | | 2 | | | 3 | ns |
| $t_{sk(o)}$(2) | Channel-to-channel output skew time | Same-direction Channels | | | 2 | | | 3 | ns |
| | | Opposite-direction Channels | | | 3 | | | 4 | |
| $t_{sk(pp)}$(3) | Part-to-part skew time | | | | 4.5 | | | 13 | ns |
| $t_r$ | Output signal rise time | See Figure 16 | | 1.6 | | | 2.8 | | ns |
| $t_f$ | Output signal fall time | See Figure 16 | | 1 | | | 2.9 | | ns |
| $t_{PHZ}$ | Disable Propagation Delay, high-to-high impedance output | See Figure 17 | | 5 | 16 | | 8 | 20 | ns |
| $t_{PLZ}$ | Disable Propagation Delay, low-to-high impedance output | See Figure 17 | | 5 | 16 | | 7 | 20 | ns |
| $t_{PZH}$ | Enable Propagation Delay, high impedance-to-high output | See Figure 17 | | 4 | 16 | | 11000 | 22000(4) | ns |
| $t_{PZL}$ | Enable Propagation Delay, high impedance-to-low output | See Figure 17 | | 4 | 16 | | 8 | 20 | ns |
| $t_{fs}$ | Fail-safe output delay time from input data or power loss | See Figure 18 | | 9.5 | | | 9 | | µs |

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

## 7.17 Switching Characteristics: $V_{CC1}$ at 5 V ± 10% and $V_{CC2}$ at 3.3 V ± 10%

$V_{CC1}$ at 5 V ± 10% and $V_{CC2}$ at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISO7631F, ISO7641F** | | | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 16 | 4 | 8 | 13 | 11 | 18 | 32 | ns |
| PWD(1) | Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 16 | | | 2 | | | 3.5 | ns |
| $t_{sk(o)}$(2) | Channel-to-channel output skew time | Same-direction Channels | | | 2.5 | | | 4.5 | ns |
| | | Opposite-direction Channels | | | 3.5 | | | 5.5 | |
| $t_{sk(pp)}$(3) | Part-to-part skew time | | | | 6 | | | 15 | ns |
| $t_r$ | Output signal rise time | See Figure 16 | | 2 | | | 3.6 | | ns |
| $t_f$ | Output signal fall time | See Figure 16 | | 1.2 | | | 3.3 | | ns |
| $t_{PHZ}$ | Disable Propagation Delay, high-to-high impedance output | See Figure 17 | | 6.5 | 17 | | 9 | 20 | ns |
| $t_{PLZ}$ | Disable Propagation Delay, low-to-high impedance output | See Figure 17 | | 6.5 | 17 | | 8 | 20 | ns |
| $t_{PZH}$ | Enable Propagation Delay, high impedance-to-high output | See Figure 17 | | 5.5 | 17 | | 11000 | 22000(4) | ns |
| $t_{PZL}$ | Enable Propagation Delay, high impedance-to-low output | See Figure 17 | | 5.5 | 17 | | 10 | 30 | ns |
| $t_{fs}$ | Fail-safe output delay time from input data or power loss | See Figure 18 | | 9.5 | | | 8.5 | | µs |

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

## 7.18 Switching Characteristics: $V_{CC1}$ at 3.3 V ± 10% and $V_{CC2}$ at 5 V ± 10%

$V_{CC1}$ at 3.3 V ± 10% and $V_{CC2}$ at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISO7631F, ISO7641F** | | | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 16 | 4 | 7.5 | 12.5 | 11 | 18.5 | 32 | ns |
| PWD(1) | Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 16 | | | 2 | | | 2.5 | ns |
| $t_{sk(o)}$(2) | Channel-to-channel output skew time | Same-direction Channels | | | 2.5 | | | 4.5 | ns |
| | | Opposite-direction Channels | | | 3.5 | | | 5.5 | |
| $t_{sk(pp)}$(3) | Part-to-part skew time | | | | 6 | | | 15 | ns |
| $t_r$ | Output signal rise time | See Figure 16 | | 1.7 | | | 2.9 | | ns |
| $t_f$ | Output signal fall time | See Figure 16 | | 1.1 | | | 2.9 | | ns |
| $t_{PHZ}$ | Disable Propagation Delay, high-to-high impedance output | See Figure 17 | | 5.5 | 17 | | 8 | 20 | ns |
| $t_{PLZ}$ | Disable Propagation Delay, low-to-high impedance output | See Figure 17 | | 5.5 | 17 | | 7 | 20 | ns |
| $t_{PZH}$ | Enable Propagation Delay, high impedance-to-high output | See Figure 17 | | 4.5 | 17 | | 11000 | 22000(4) | ns |
| $t_{PZL}$ | Enable Propagation Delay, high impedance-to-low output | See Figure 17 | | 4.5 | 17 | | 8 | 30 | ns |
| $t_{fs}$ | Fail-safe output delay time from input data or power loss | See Figure 18 | | 9.5 | | | 7.5 | | µs |

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

## 7.19 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V ± 10%

$V_{CC1}$ and $V_{CC2}$ at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | M-Grade | | | C-Grade | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ISO7631F, ISO7641F** | | | | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 16 | 4 | 8.5 | 14 | 12 | 23 | 35 | ns |
| PWD(1) | Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 16 | | | 2 | | | 3 | ns |
| $t_{sk(o)}$(2) | Channel-to-channel output skew time | Same-direction Channels | | | 3 | | | 5 | ns |
| | | Opposite-direction Channels | | | 4 | | | 6 | |
| $t_{sk(pp)}$(3) | Part-to-part skew time | | | | 6.5 | | | 16 | ns |
| $t_r$ | Output signal rise time | See Figure 16 | | 2 | | | 3.7 | | ns |
| $t_f$ | Output signal fall time | See Figure 16 | | 1.3 | | | 3.4 | | ns |
| $t_{PHZ}$ | Disable Propagation Delay, high-to-high impedance output | See Figure 17 | | 6.5 | 17 | | 9 | 20 | ns |
| $t_{PLZ}$ | Disable Propagation Delay, low-to-high impedance output | See Figure 17 | | 6.5 | 17 | | 8 | 20 | ns |
| $t_{PZH}$ | Enable Propagation Delay, high impedance-to-high output | See Figure 17 | | 5.5 | 17 | | 11000 | 22000(4) | ns |
| $t_{PZL}$ | Enable Propagation Delay, high impedance-to-low output | See Figure 17 | | 5.5 | 17 | | 10 | 30 | ns |
| $t_{fs}$ | Fail-safe output delay time from input data or power loss | See Figure 18 | | 9.2 | | | 7.5 | | µs |

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

## 7.20 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 2.7 V

$V_{CC1}$ and $V_{CC2}$ at 2.7 V (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | M-Grade | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **ISO7631F, ISO7641F** | | | | | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 16 | 5 | 8 | 16 | ns |
| PWD(1) | Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 16 | | | 2.5 | ns |
| $t_{sk(o)}$(2) | Channel-to-channel output skew time | Same-direction Channels | | | 4 | ns |
| | | Opposite-direction Channels | | | 5 | |
| $t_{sk(pp)}$(3) | Part-to-part skew time | | | | 8 | ns |
| $t_r$ | Output signal rise time | See Figure 16 | | 2.3 | | ns |
| $t_f$ | Output signal fall time | See Figure 16 | | 1.8 | | ns |
| $t_{PHZ}$ | Disable Propagation Delay, high-to-high impedance output | See Figure 17 | | 8 | 18 | ns |
| $t_{PLZ}$ | Disable Propagation Delay, low-to-high impedance output | See Figure 17 | | 8 | 18 | ns |
| $t_{PZH}$ | Enable Propagation Delay, high impedance-to-high output | See Figure 17 | | 7 | 18 | ns |
| $t_{PZL}$ | Enable Propagation Delay, high impedance-to-low output | See Figure 17 | | 7 | 18 | ns |
| $t_{fs}$ | Fail-safe output delay time from input data or power loss | See Figure 18 | | 8.5 | | µs |

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 7.21 Typical Characteristics

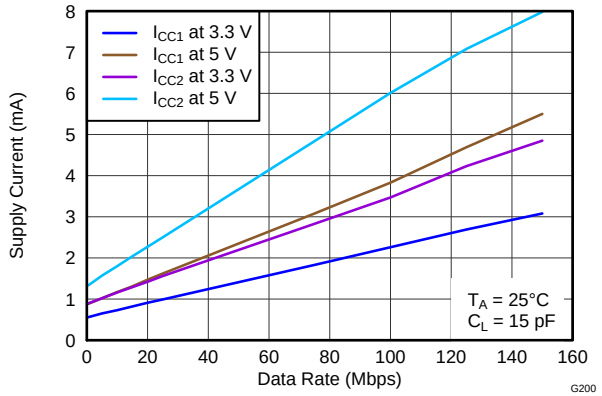



**Figure 1. ISO7631FM Supply Current Per Channel vs Data Rate**

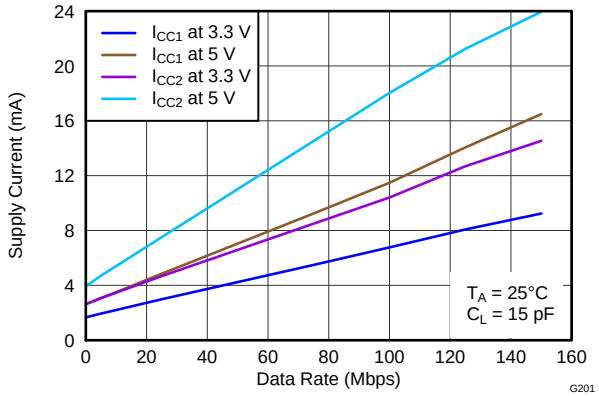



**Figure 2. ISO7631FM Supply Current For All Channels vs Data Rate**

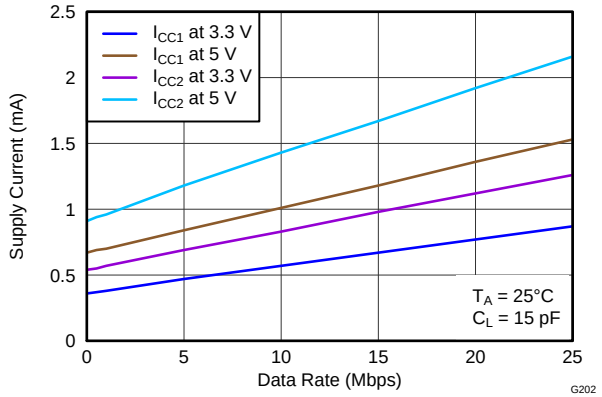



**Figure 3. ISO7631FC Supply Current Per Channel vs Data Rate**

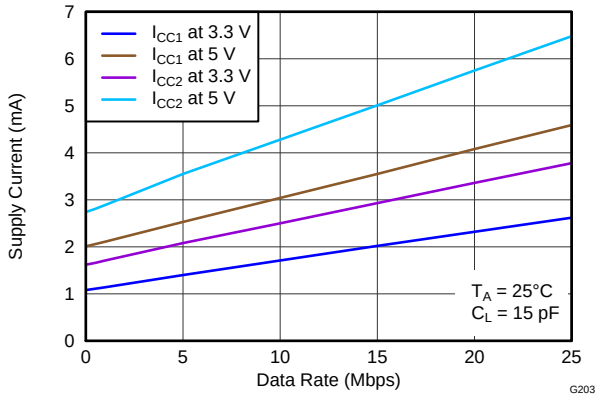



**Figure 4. ISO7631FC Supply Current For All Channels vs Data Rate**

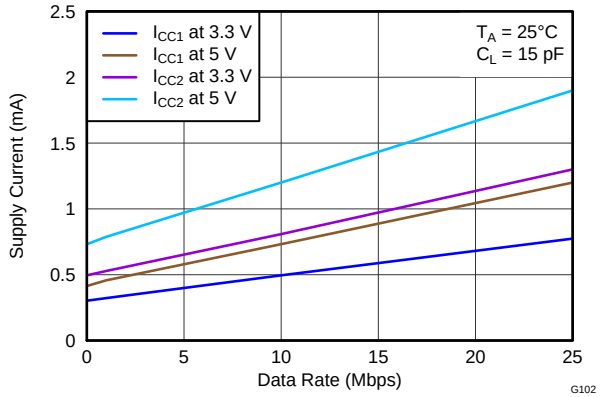



**Figure 5. ISO7641FC Supply Current Per Channel vs Data Rate**

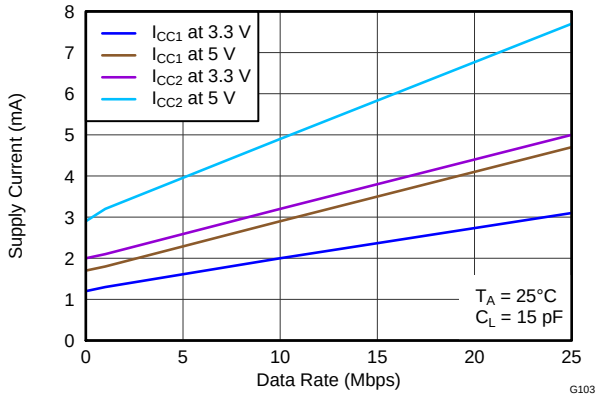



**Figure 6. ISO7641FC Supply Current For All Channels vs Data Rate**

## Typical Characteristics (continued)

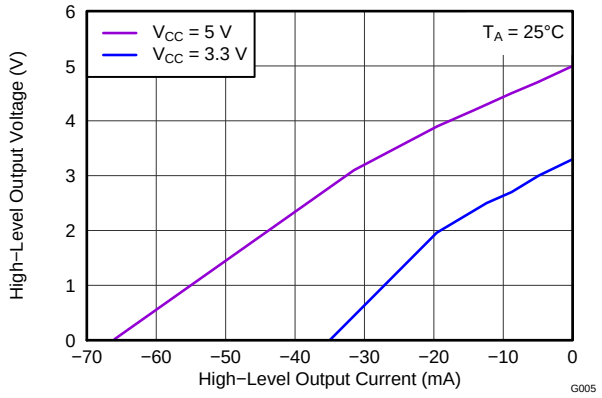



**Figure 7. M-Grade High-Level Output Voltage vs High-Level Output Current**

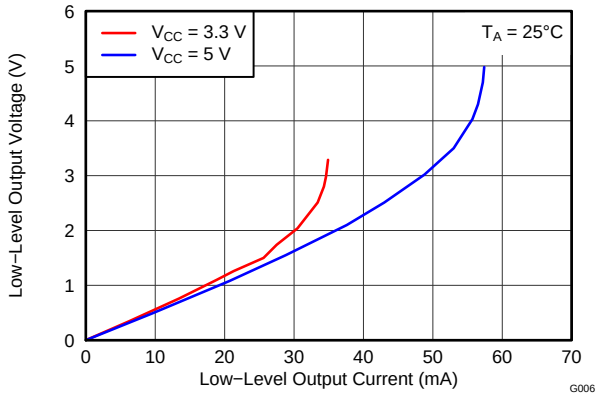



**Figure 8. M-Grade Low-Level Output Voltage vs Low-Level Output Current**

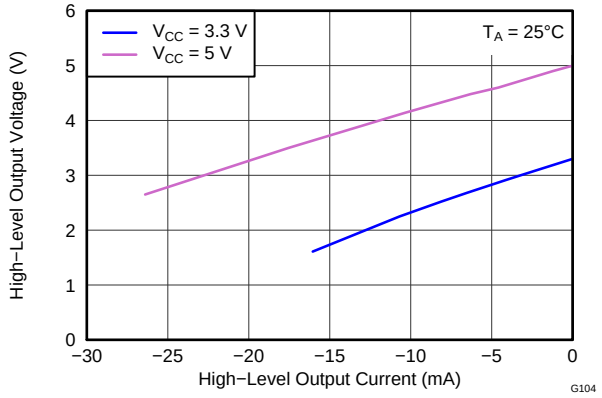



**Figure 9. C-Grade High-Level Output Voltage vs High-Level Output Current**

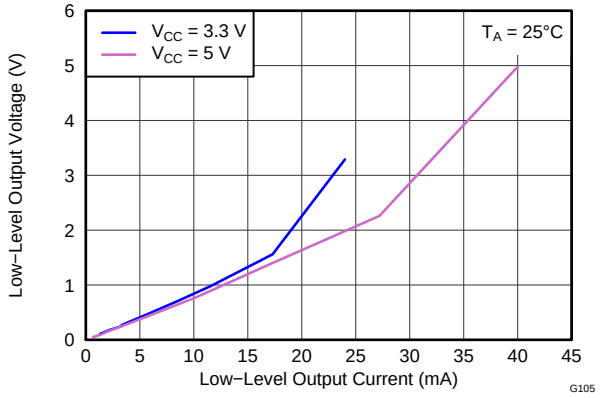



**Figure 10. C-Grade Low-Level Output Voltage vs Low-Level Output Current**

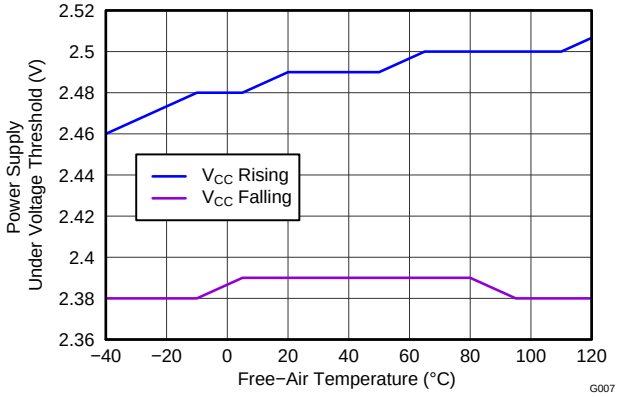



**Figure 11. $V_{CC}$ Undervoltage Threshold vs Free Air Temperature**

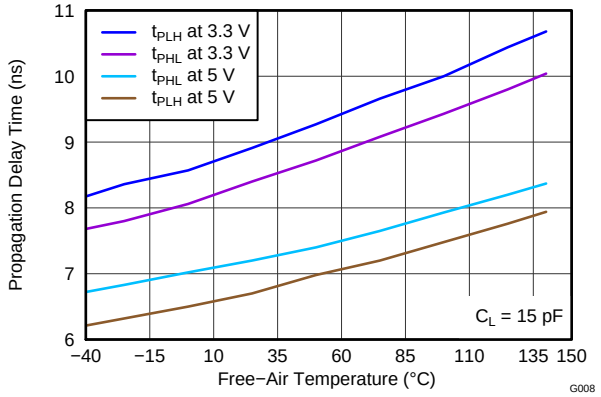



**Figure 12. M-Grade Propagation Delay Time vs Free Air Temperature**

## Typical Characteristics (continued)

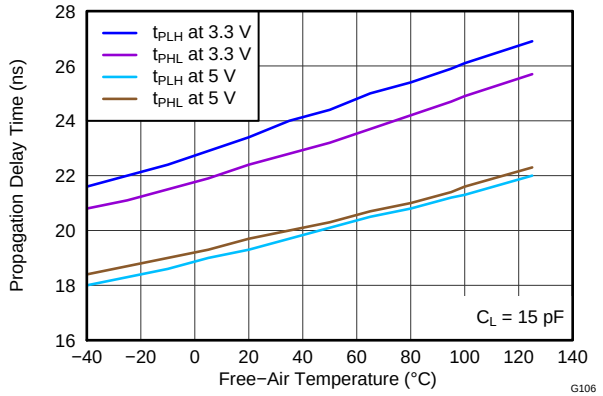



**Figure 13. C-Grade Propagation Delay Time vs Free Air Temperature**

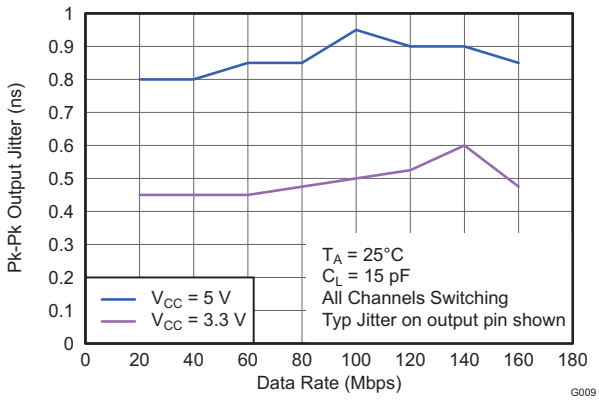



**Figure 14. M-Grade Output Jitter vs Data Rate**

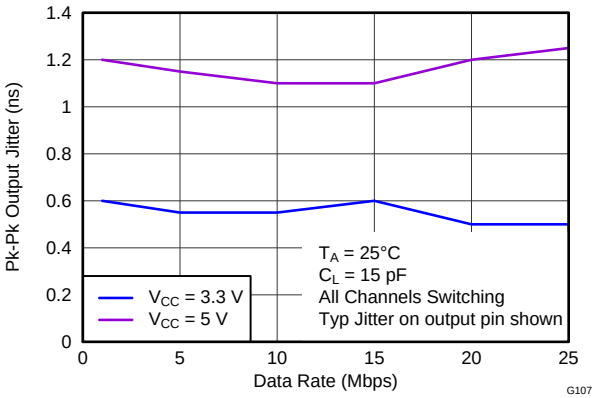
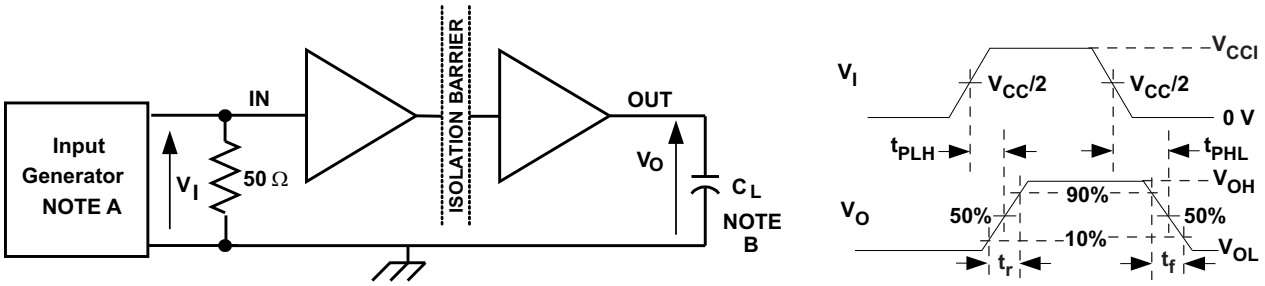



**Figure 15. C-Grade Output Jitter vs Data Rate**

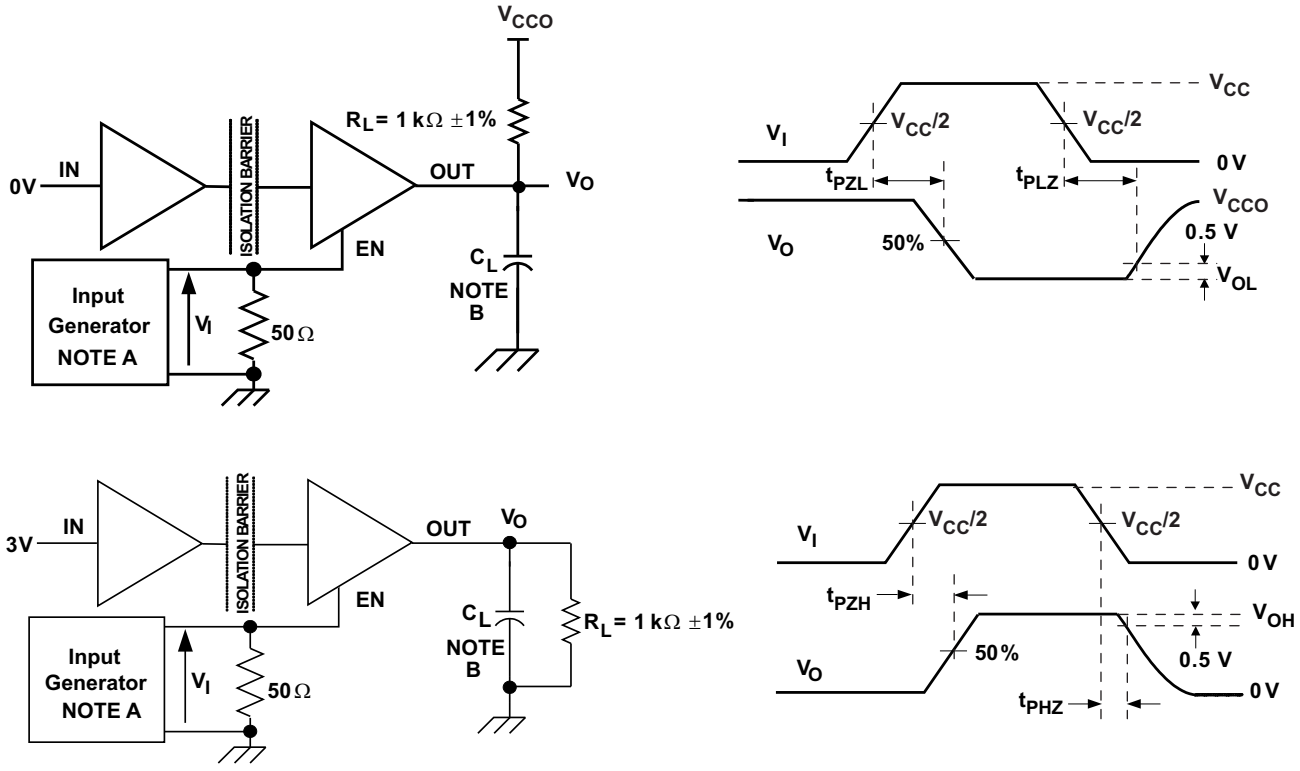
# 8 Parameter Measurement Information




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3ns, $Z_O$ = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 16. Switching Characteristics Test Circuit and Voltage Waveforms**

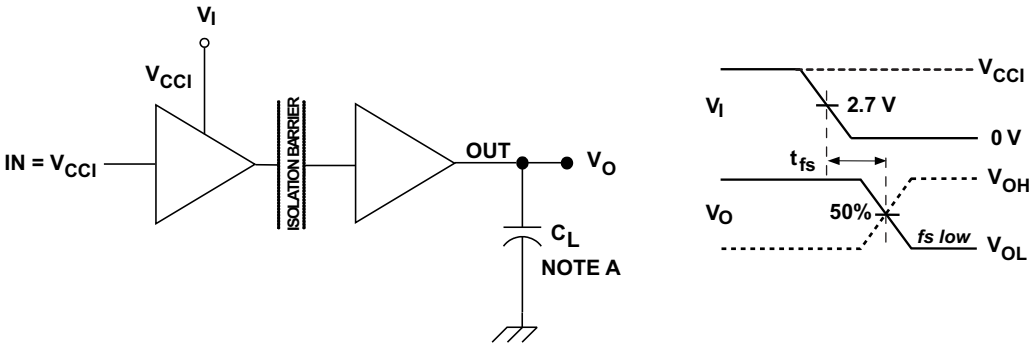



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50 Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

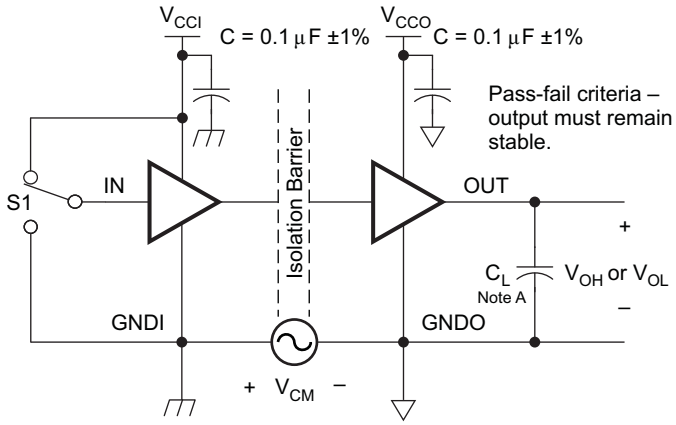
**Figure 17. Enable/Disable Propagation Delay Time Test Circuit and Waveform**

## Parameter Measurement Information (continued)




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 18. Failsafe Delay Time Test Circuit and Voltage Waveforms**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 19. Common-Mode Transient Immunity Test Circuit**

# 9 Detailed Description

## 9.1 Overview

The isolator in Figure 20 is based on a capacitive, isolation-barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

## 9.2 Functional Block Diagram

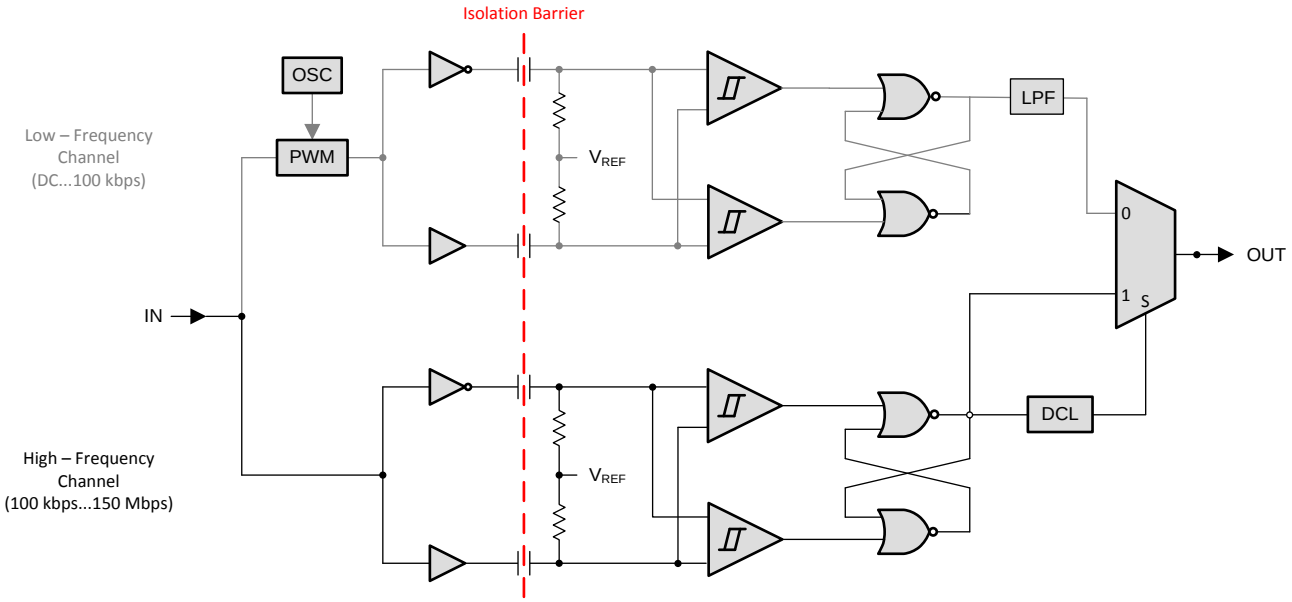



**Figure 20. ISO7631FM Conceptual Block Diagram**

## Functional Block Diagram (continued)

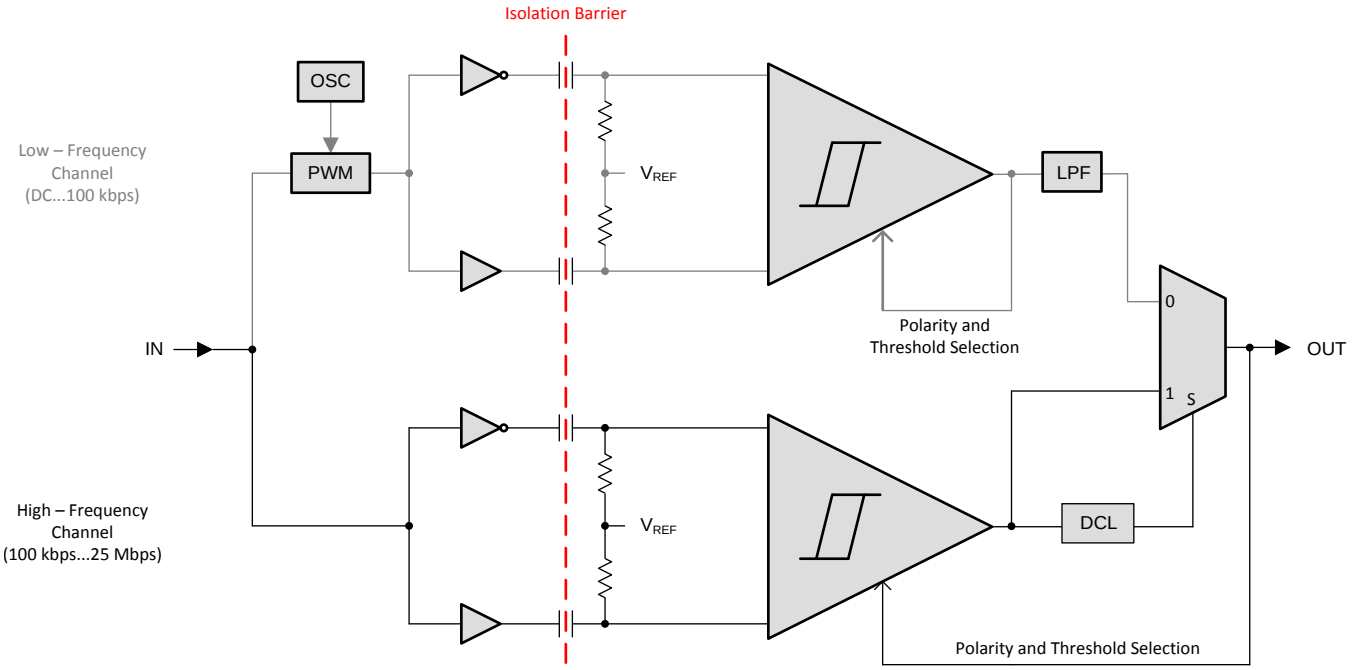



**Figure 21. ISO7631FC and ISO7641FC Conceptual Block Diagram**

## 9.3 Feature Description

### 9.3.1 Package Insulation and Safety-Related Specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| L(I01) | Minimum air gap (Clearance) | Shortest terminal to terminal distance through air | 8 | | | mm |
| L(I02) (1) | Minimum external tracking (Creepage) | Shortest terminal to terminal distance across the package surface | 8 | | | mm |
| CTI | Tracking resistance (Comparative Tracking Index) | DIN EN 60112 (VDE 0303-11); IEC 60112 | ≥400 | | | V |
| DTI | Minimum Internal Gap (Internal Clearance) | Distance through the insulation | 0.014 | | | mm |
| $C_I$ (2) | Input capacitance | $V_I = V_{CC}/2 + 0.4 \sin(2\pi ft)$, f = 1MHz, $V_{CC}$ = 5 V | | 2 | | pF |

(1) Per JEDEC package dimensions.
(2) Measured from input pin to ground.

**NOTE**

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

**Table 1. DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics(1)**

| PARAMETER | | TEST CONDITIONS | SPECIFICATION | UNIT |
|---|---|---|---|---|
| $V_{IORM}$ | Maximum working insulation voltage | | 1414 | $V_{PEAK}$ |
| $V_{PR}$ | Input-to-output test voltage | After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC | 1697 | $V_{PEAK}$ |
| | | Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial Discharge < 5 pC | 2262 | |
| | | Method b1, 100% Production test $V_{PR} = V_{IORM}$ x 1.875, t = 1 s Partial discharge < 5 pC | 2652 | |
| $V_{IOTM}$ | Maximum transient overvoltage | $V_{TEST} = V_{IOTM}$ t = 60 sec (Qualification) t = 1 sec (100% Production) | 4242 | $V_{PEAK}$ |
| $R_{IO}$ (2) | Isolation resistance, Input to Output | $V_{IO}$ = 500 V, $T_A$ = 25°C | $>10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | $>10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | $>10^{9}$ | |
| $C_{IO}$ (2) | Barrier capacitance, Input to Output | $V_I$ = 0.4 sin (2πft), f = 1MHz | 2 | pF |
| | Pollution degree | | 2 | |

(1) Climatic Classification 40/125/21
(2) All pins on each side of the barrier tied together creating a two-terminal device.

**Table 2. IEC 60664-1 Ratings Table**

| PARAMETER | TEST CONDITIONS | SPECIFICATION |
|---|---|---|
| Material Group | | II |
| Installation classification / Overvoltage category for basic insulation | Rated mains voltage ≤ 300 $V_{RMS}$ | I–IV |
| | Rated mains voltage ≤ 600 $V_{RMS}$ | I–III |
| | Rated mains voltage ≤ 1000 $V_{RMS}$ | I–II |

### *9.3.1.1 Regulatory Information*

| VDE | TUV | CSA | UL | CQC |
|---|---|---|---|---|
| Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07 | Certified according to EN/UL/CSA 60950-1 and 61010-1 | Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 | Recognized under 1577 Component Recognition Program | Certified according to GB4943.1-2011 |
| Basic Insulation Maximum Transient Overvoltage, 4242 $V_{PK}$ Maximum Working Voltage, 1414 $V_{PK}$ | 3000 $V_{RMS}$ Reinforced Insulation, 400 $V_{RMS}$ maximum working voltage 3000 $V_{RMS}$ Basic Insulation, 600 $V_{RMS}$ maximum working voltage | 3000 $V_{RMS}$ Isolation Rating | Single Protection, 2500 $V_{RMS}$ (1) | Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 $V_{RMS}$ Maximum Working Voltage |
| Certificate number: 40016131 | Certificate number: U8V 13 09 77311 010 | Master contract number: 220991 | File number: E181974 | Certificate number: CQC14001109542 |

(1) Production tested ≥ 3000 $V_{RMS}$ for 1 second in accordance with UL 1577.

### 9.3.1.2 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | DW-16 | $\theta_{JA}$ = 77.5 °C/W, $V_I$ = 5.5V, $T_J$ = 150°C, $T_A$ = 25°C | | | 293 | mA |
| | | | $\theta_{JA}$ = 77.5 °C/W, $V_I$ = 3.6V, $T_J$ = 150°C, $T_A$ = 25°C | | | 448 | |
| | | | $\theta_{JA}$ = 77.5 °C/W, $V_I$ = 2.7V, $T_J$ = 150°C, $T_A$ = 25°C | | | 597 | |
| $T_S$ | Maximum safety temperature | | | | | 150 | °C |

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

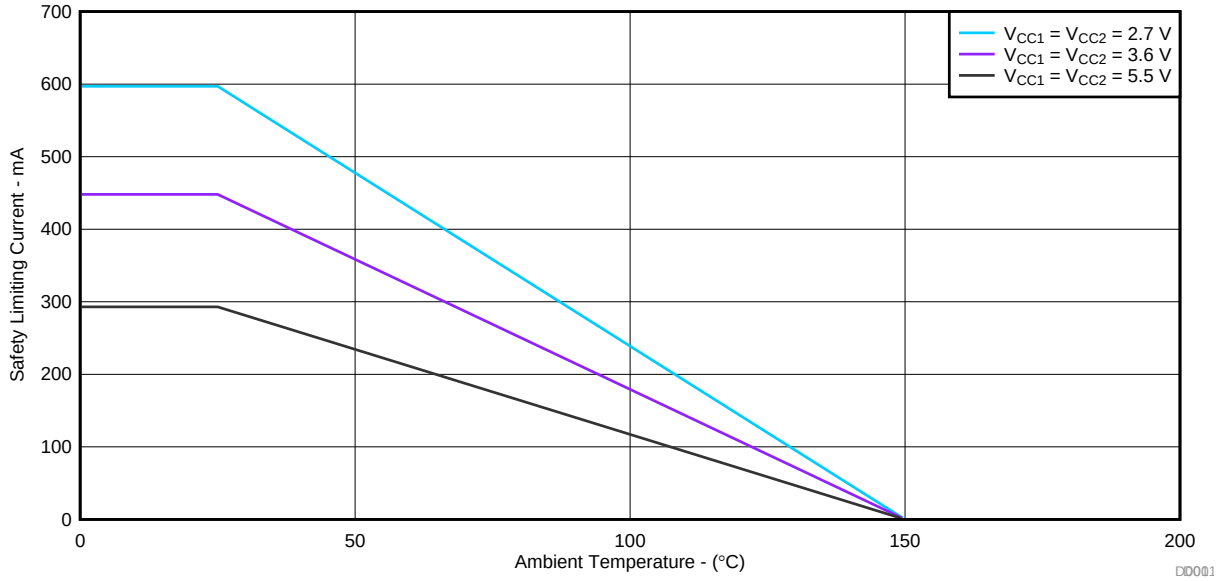



**Figure 22. Thermal Derating Curve for Safety Limiting Current per VDE**

## 9.4 Device Functional Modes

**Table 3. Function Table(1)**

| INPUT $V_{CC}$ | OUTPUT $V_{CC}$ | INPUT (INx) | OUTPUT ENABLE (ENx) | OUTPUT (OUTx) |
|---|---|---|---|---|
| PU | PU | H | H or Open | H |
| | | L | H or Open | L |
| | | X | L | Z |
| | | Open | H or Open | L |
| PD | PU | X | H or Open | L |
| PD | PU | X | L | Z |
| PU | PD | X | X | Undetermined |

(1) PU = Powered Up($V_{CC}$ ≥ 2.7 V); PD = Powered Down ($V_{CC}$ ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

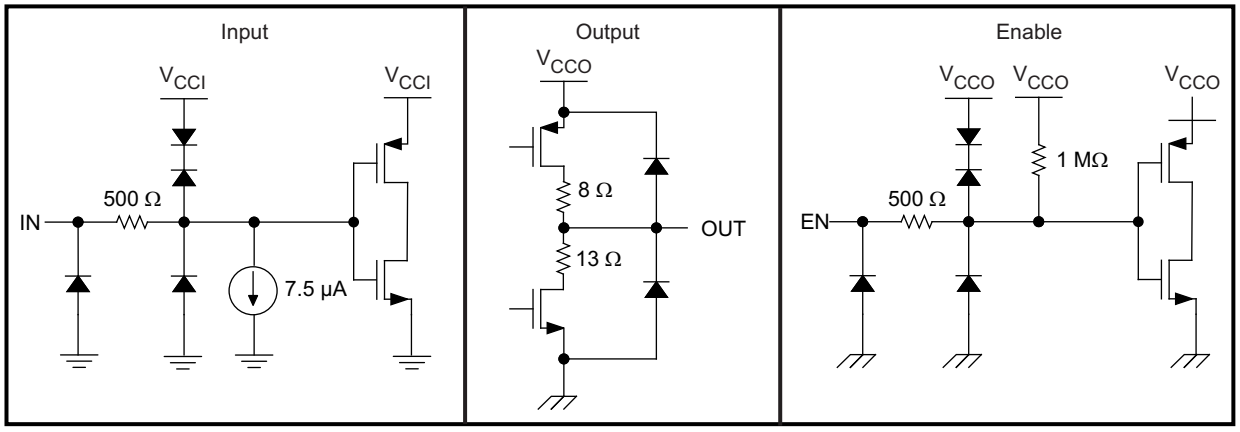



**Figure 23. Device I/O Schematics**

## 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

ISO7641FC uses single-ended TTL-logic switching technology. It has a supply voltage range from 3 V to 5.5 V for both supplies, $V_{CC1}$ and $V_{CC2}$. When designing with digital isolators, it is important to note that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

## 10.2 Typical Application

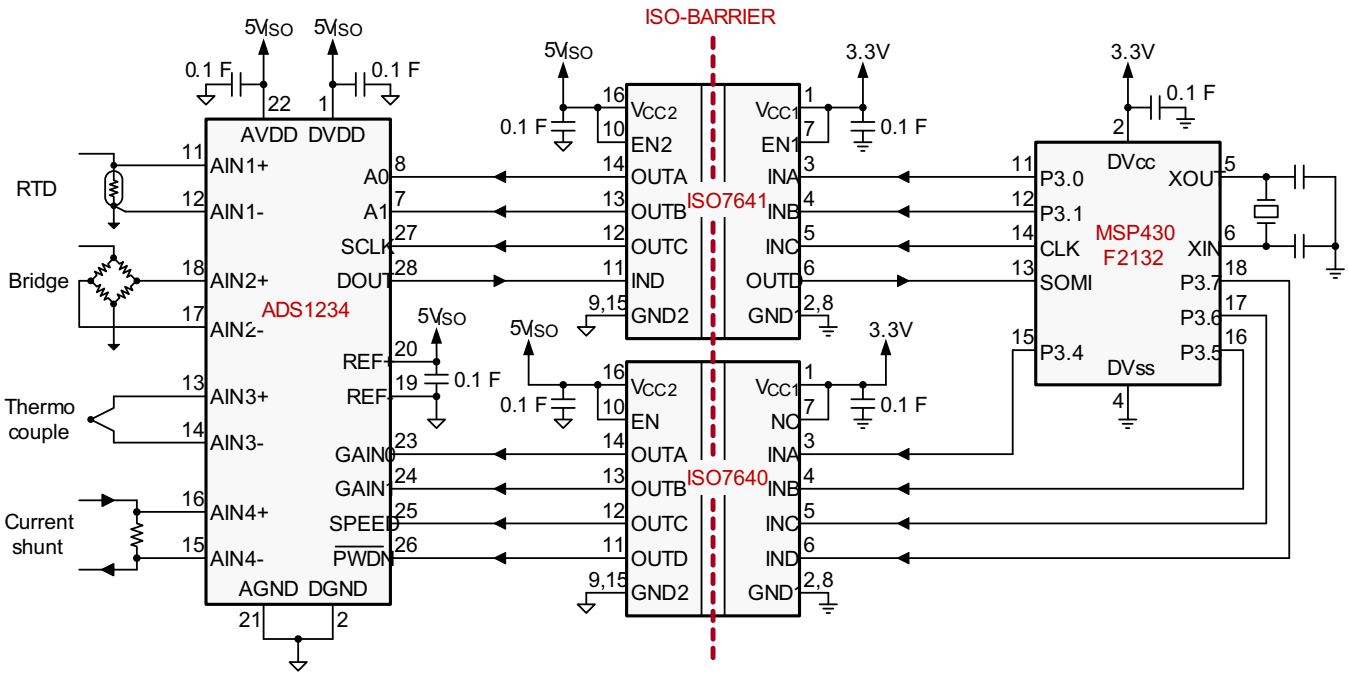



**Figure 24. Isolated Data Acquisition System for Process Control**

### 10.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO76xx device only requires two external bypass capacitors to operate.

## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

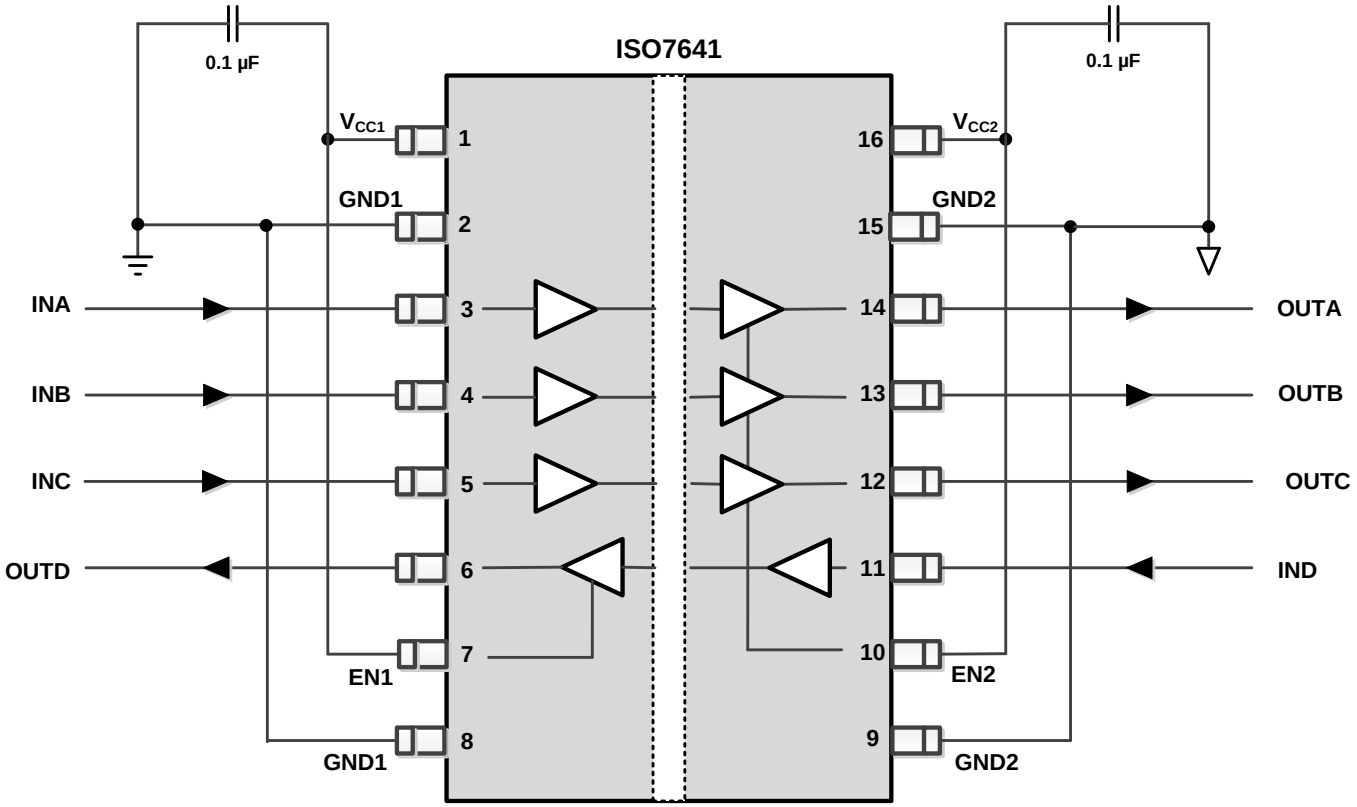



**Figure 25. Typical ISO7641FC Circuit Hookup**

#### *10.2.2.1 Typical Supply Current Equations*

(Calculated based on room temperature and typical Silicon process)

**ISO7631FM:**

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 1.8072 + 0.0244 \times f + 0.0016 \times f \times C_L \quad (1)$$

$$I_{CC2} = 2.4625 + 0.0252 \times f + 0.0033 \times f \times C_L \quad (2)$$

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 2.3183 + 0.04 \times f + 0.0025 \times f \times C_L \quad (3)$$

$$I_{CC2} = 3.2582 + 0.0403 \times f + 0.0049 \times f \times C_L \quad (4)$$

**ISO7631FC:**

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 1.1762 + 0.0325 \times f + 0.0017 \times f \times C_L \quad (5)$$

$$I_{CC2} = 1.5285 + 0.0299 \times f + 0.0033 \times f \times C_L \quad (6)$$

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 1.6001 + 0.0528 \times f + 0.0025 \times f \times C_L \quad (7)$$

$$I_{CC2} = 2.2032 + 0.0475 \times f + 0.005 \times f \times C_L \quad (8)$$

**ISO7641FC:**

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 1.2162 + 0.0462 \times f + 0.0017 \times f \times C_L \quad (9)$$

$$I_{CC2} = 1.8054 + 0.0411 \times f + 0.005 \times f \times C_L \quad (10)$$

## Typical Application (continued)

(Calculated based on room temperature and typical Silicon process)

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 1.6583 + 0.0757 \times f + 0.0025 \times f \times C_L \quad (11)$$

$$I_{CC2} = 2.5008 + 0.0655 \times f + 0.0076 \times f \times C_L \quad (12)$$

$I_{CC1}$ and $I_{CC2}$ are typical supply currents measured in mA; f is data rate measured in Mbps; $C_L$ is the capacitive load on each channel measured in pF.

### 10.2.3 Application Curves

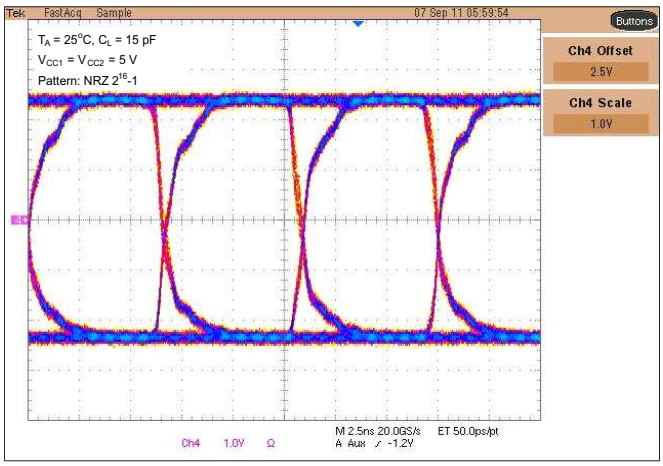



**Figure 26. M-Grade Typical Eye Diagram at 150 Mbps, 5 V Operation**

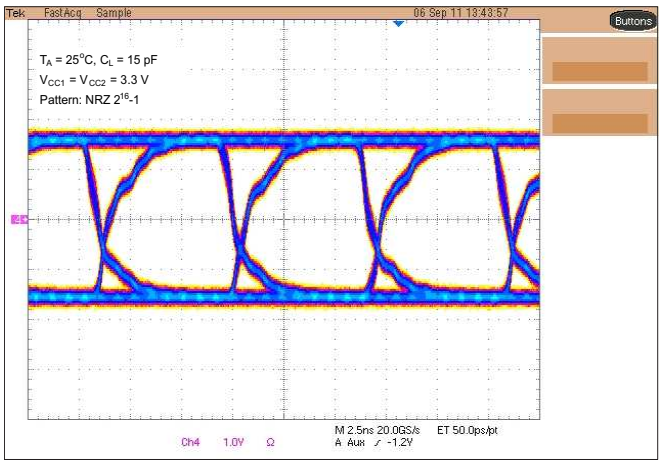



**Figure 27. M-Grade Typical Eye Diagram at 150 Mbps, 3.3 V Operation**

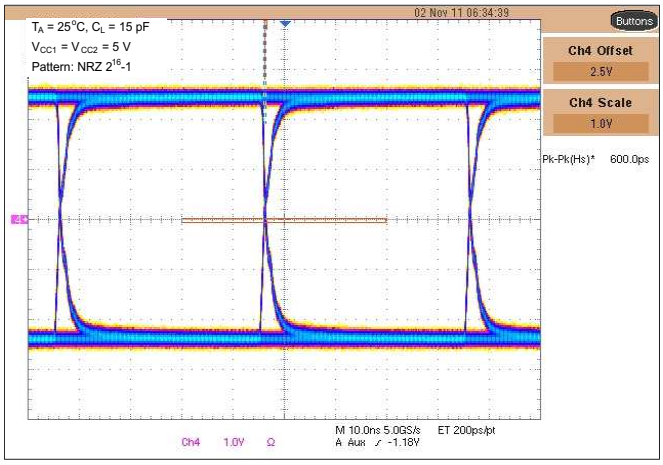



**Figure 28. C-Grade Typical Eye Diagram at 25 Mbps, 5 V Operation**

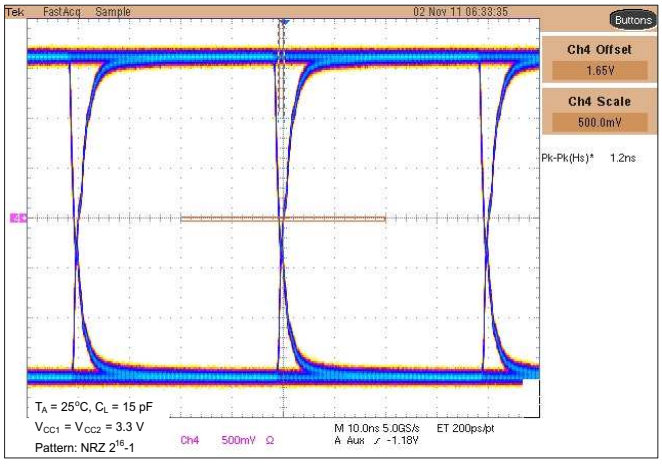



**Figure 29. C-Grade Typical Eye Diagram at 25 Mbps, 3.3 V Operation**

# 11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins ($V_{CC1}$ and $V_{CC2}$). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

# 12 Layout

## 12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 30). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in$^2$.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

**NOTE**

For detailed layout recommendations, see *Digital Isolator Design Guide*, SLLA284.

## 12.2 Layout Example

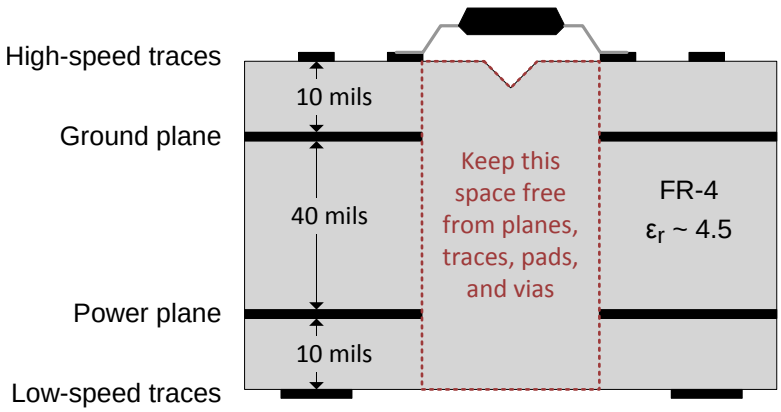



**Figure 30. Recommended Layer Stack**

# 13 Device and Documentation Support

## 13.1 Documentation Support

### 13.1.1 Related Documentation

For related documentation, see the following:

- *Digital Isolator Design Guide*, SLLA284
- *Transformer Driver for Isolated Power Supplies*, SLLSEA0
- Isolation Glossary, SLLA353

## 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| ISO7631FM | Click here | Click here | Click here | Click here | Click here |
| ISO7631FC | Click here | Click here | Click here | Click here | Click here |
| ISO7641FC | Click here | Click here | Click here | Click here | Click here |

## 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.4 Trademarks

DeviceNet, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7631FCDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7631FC | Samples |
| ISO7631FCDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7631FC | Samples |
| ISO7631FMDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7631FM | Samples |
| ISO7631FMDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7631FM | Samples |
| ISO7641FCDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7641FC | Samples |
| ISO7641FCDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO7641FC | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

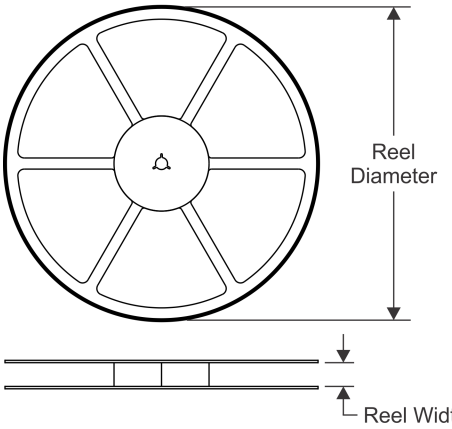
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

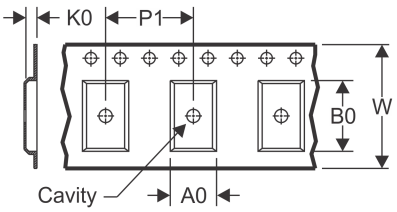
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

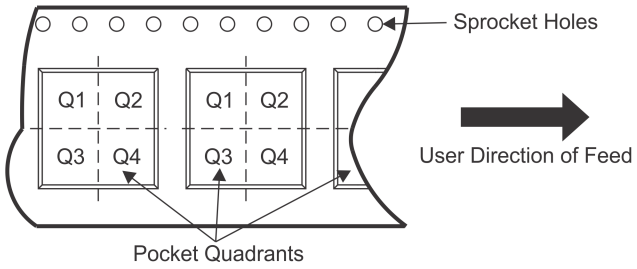



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

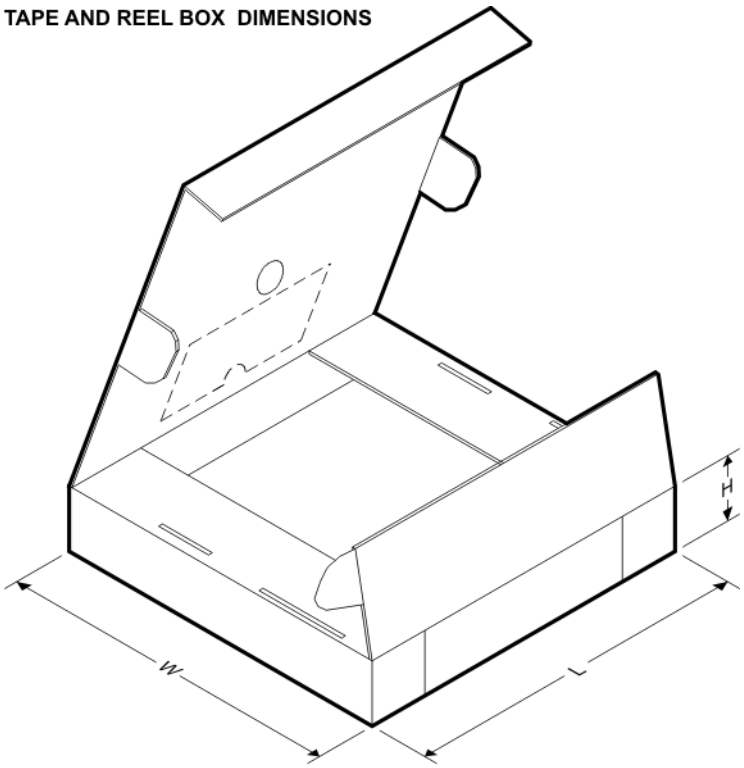
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7631FCDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7631FMDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7641FCDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

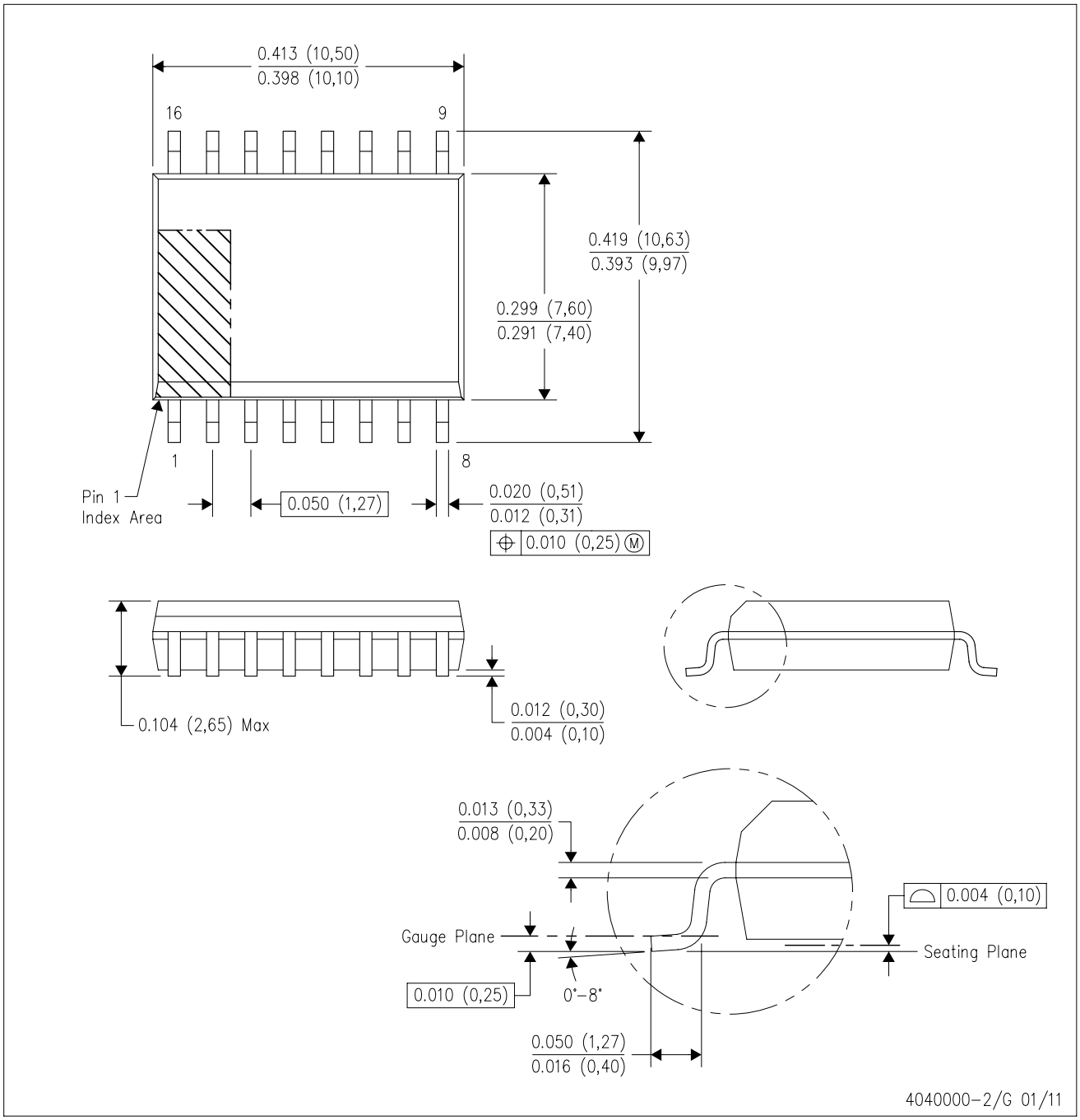
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

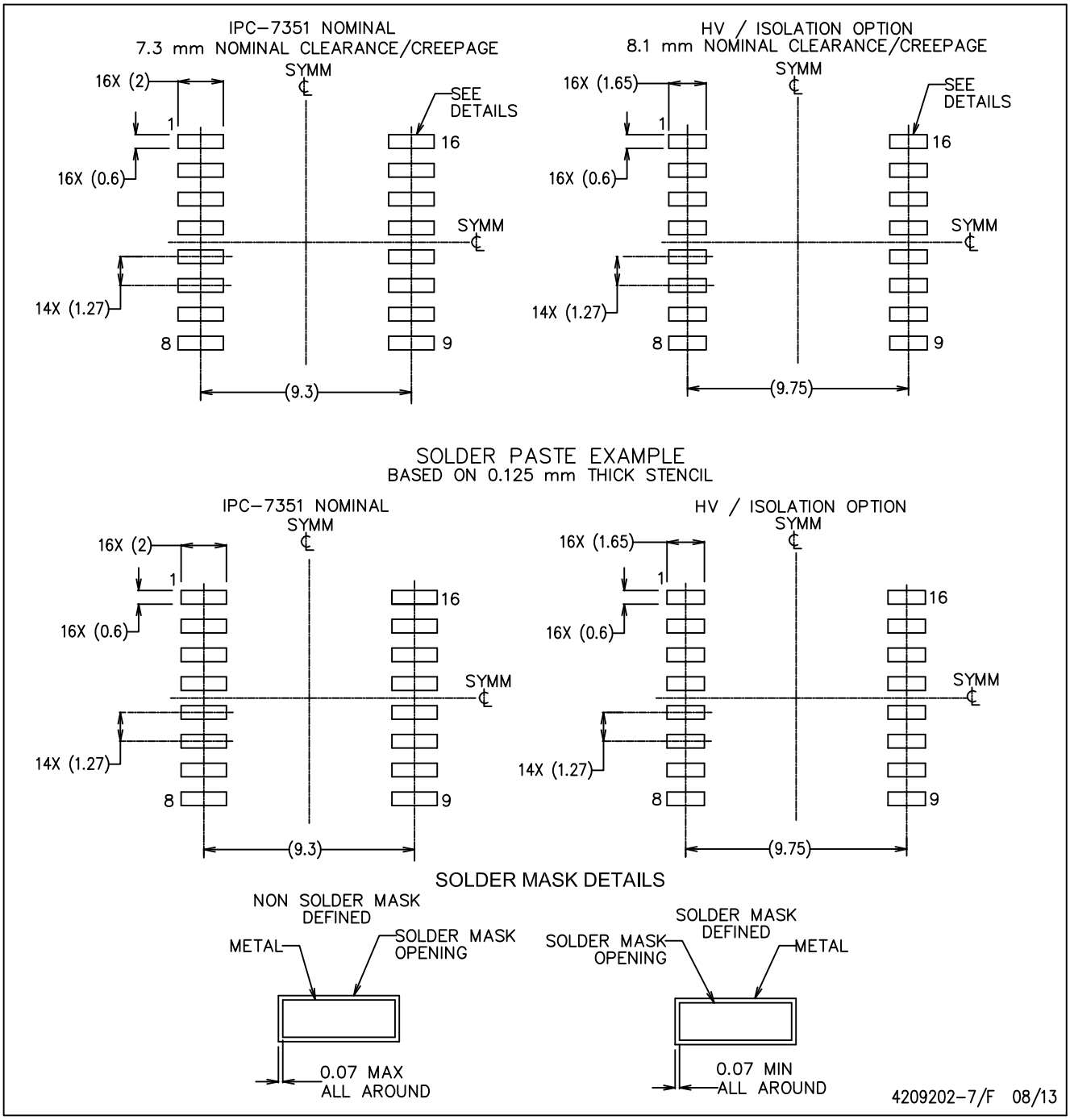
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7631FCDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7631FMDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| ISO7641FCDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

# DW (R-PDSO-G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
E. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
F. Board assembly site may have different recommendations for stencil design.

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