# ISO7041 Ultra-Low Power Four-Channel Digital Isolator

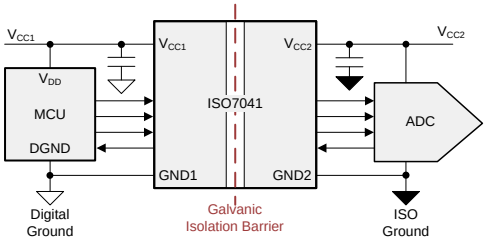
## 1 Features

- Ultra-Low Power Consumption
  - 4.4 μA per Channel Quiescent Current (3.3 V)
  - 16 μA per Channel at 100 kbps (3.3 V)
  - 126 μA per Channel at 1 Mbps (3.3 V)
- Robust Isolation Barrier
  - >100-Year Projected Lifetime
  - 3000 $V_{RMS}$ Isolation Rating
  - ±100 kV/μs Typical CMTI
- Wide Supply Range: 2.25 V to 3.63 V
- Wide Temperature Range: –40°C to +125°C
- Small 16-QSOP Package (16-DBQ)
- Signaling Rate: Up to 2 Mbps
- Default Output *High* (ISO7041) and *Low* (ISO7041F) Options
- Robust Electromagnetic Compatibility (EMC)
  - System-Level ESD, EFT, and Surge Immunity
  - Very Low Emissions
- Safety-Related Certifications (Planned):
  - UL 1577 Component Recognition Program
  - DIN V VDE V 0884-11
  - CQC, TUV and CSA Certifications
  - IECEx (IEC 60079-0 & IEC 60079-11) and ATEX (EN 60079-11)

## 2 Applications

- 4-mA to 20-mA Loop Powered Field Transmitters
- Factory Automation, Process Automation
- Programmable Logic Controller (PLC)
- Low-Power GPIO, UART and SPI Isolation

**Simplified Application Schematic**




## 3 Description

The ISO7041 device is an ultra-low power, multichannel digital isolator that can be used to isolate CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide ($SiO_2$) insulation barrier. Innovative edge based architecture combined with an ON-OFF keying modulation scheme allows these isolators to consume very-low power while meeting 3000-$V_{RMS}$ isolation rating per UL1577. The per channel dynamic current consumption of the device is under 130 μA/Mbps and the per channel static current consumption is 4.4 μA at 3.3 V.

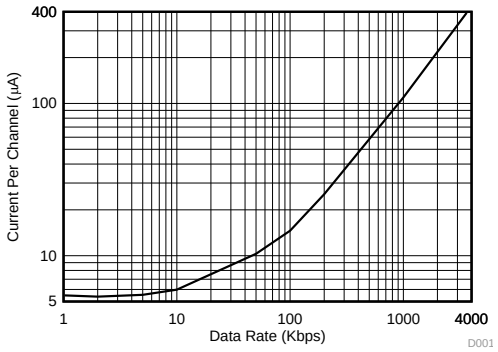
The device can operate as low as 2.25 V, as high as 3.63 V, and is fully functional with different supply voltages on each side of isolation barrier. The four channel isolator comes in a 16-QSOP package with three forward-direction channels and one reverse-direction channel in a 16-QSOP package. The device has default output high and low options. If the input power or signal is lost, default output is *high* for the ISO7041 device and *low* for the ISO7041F device with the F suffix. See the *Device Functional Modes* section for more information.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ISO7041 | QSOP (16) | 4.90 mm × 3.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Data Rate vs Power Consumption at 3.3 V**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| August 2018 | * | Initial release. |


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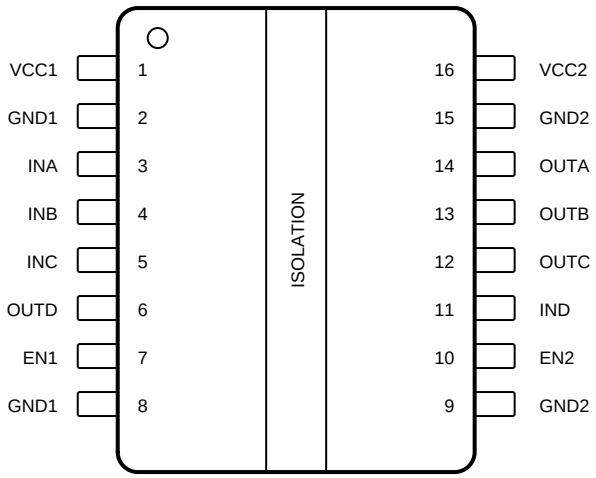
# 5 Pin Configuration and Functions

**ISO7041 DBQ Package**
**16-Pin QSOP**
**Top View**




Not to scale

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN1 | 7 | I | Refresh enable 1. Refresh is enabled when the EN1 pin is connected to GND1. Disable refresh by connecting the EN1 pin high to $V_{CC1}$. EN1 and EN2 must be connected to the same logic state to enable or disable refresh. |
| EN2 | 10 | I | Refresh enable 2. Refresh is enabled when the EN2 pin is connected to GND2. Disable refresh by connecting the EN2 pin high to $V_{CC2}$. EN1 and EN2 must be connected to the same logic state to enable or disable refresh. |
| GND1 | 2 | — | Ground connection for $V_{CC1}$ |
| | 8 | | |
| GND2 | 9 | — | Ground connection for $V_{CC2}$ |
| | 15 | | |
| INA | 3 | I | Input, channel A |
| INB | 4 | I | Input, channel B |
| INC | 5 | I | Input, channel C |
| IND | 11 | I | Input, channel D |
| OUTA | 14 | O | Output, channel A |
| OUTB | 13 | O | Output, channel B |
| OUTC | 12 | O | Output, channel C |
| OUTD | 6 | O | Output, channel D |
| $V_{CC1}$ | 1 | — | Power supply, side 1 |
| $V_{CC2}$ | 16 | — | Power supply, side 2 |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage | $V_{CC1}$ to GND1 | -0.5 | 6 | V |
| | $V_{CC2}$ to GND2 | -0.5 | 6 | |
| Input/Output Voltage | INx to GNDx | -0.5 | $V_{CCX}$ + 0.5 | V |
| | OUTx to GNDx | -0.5 | $V_{CCX}$ + 0.5 | |
| | ENx to GNDx | -0.5 | $V_{CCX}$ + 0.5 | |
| Output Current | Io | -15 | 15 | mA |
| Temperature | Operating junction temperature, $T_J$ | -40 | 150 | °C |
| | Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±6000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$ (1) | Supply Voltage Side 1 | | 2.25 | | 3.63 | V |
| $V_{CC2}$ (1) | Supply Voltage Side 2 | | 2.25 | | 3.63 | V |
| $V_{IH}$ | High level Input voltage | | 0.7 x $V_{CCI}$ | | $V_{CCI}$ | V |
| $V_{IL}$ | Low level Input voltage | | 0 | | 0.3 x $V_{CCI}$ | V |
| $I_{OH}$ | High level output current | $V_{CCO}$ = 3.3 V | -2 | | | mA |
| | | $V_{CCO}$ = 2.5 V | -1 | | | mA |
| $I_{OL}$ | Low level output current | $V_{CCO}$ = 3.3 V | | | 2 | mA |
| | | $V_{CCO}$ = 2.5 V | | | 1 | mA |
| DR | Data Rate | | 0 | | 2 | Mbps |
| $T_A$ | Ambient temperature | | -40 | | 125 | °C |

(1) $V_{CC1}$ and $V_{CC2}$ can be set indepentent of one another

## 6.4 Thermal Information

| THERMAL METRIC(1) | | ISO7041 DBQ (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 87.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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## Thermal Information (continued)

| THERMAL METRIC(1) | | ISO7041 DBQ (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 33.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 48.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

## 6.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 3.63$ V, $T_J = 150°C$, $C_L =$ 15 pF, Input a 1-MHz 50% duty cycle square wave | | | TBD | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | TBD | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | TBD | mW |

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## 6.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | SPECIFICATIONS | UNIT |
|---|---|---|---|---|
| | | | QSOP-16 | |
| **IEC 60664-1** | | | | |
| CLR | External clearance(1) | Side 1 to side 2 distance through air | >3.7 | mm |
| CPG | External Creepage(1) | Side 1 to side 2 distance across package surface | >3.7 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | 17 | µm |
| CTI | Comparative tracking index | IEC 60112; UL 746A | >600 | V |
| | Material Group | According to IEC 60664-1 | I | |
| | Overvoltage category | Rated mains voltage ≤ 600 $V_{RMS}$ | I-IV | |
| **DIN V VDE V 0884-11:2017-01** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 566 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum isolation working voltage | AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; See Figure 10 | 400 | $V_{RMS}$ |
| | | DC voltage | 566 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$ , t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production) | 4242 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage | Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 6400\ V_{PK}$ (qualification) | 4000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(2) | Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m$ = 10 s | ≤ 5 | pC |
| | | Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$ , $t_m$ = 10 s | ≤ 5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini}$ = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$ , $t_m$ = 1 s | ≤ 5 | |
| $C_{IO}$ | Barrier capacitance, input to output(3) | $V_{IO}$ = 0.4 × sin (2 πft), f = 1 MHz | 1.5 | pF |
| $R_{IO}$ | Insulation resistance, input to output(3) | $V_{IO}$ = 500 V, $T_A$ = 25°C | > $10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 150°C | > $10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | > $10^9$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/ 21 | |
| **UL 1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO}$ , t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ , t = 1 s (100% production) | 3000 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Apparent charge is electrical discharge caused by a partial discharge (pd).
(3) All pins on each side of the barrier tied together creating a two-pin device.

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## 6.7 Safety-Related Certifications

| VDE | CSA | UL | CQC | TUV | CSA/Sira |
|---|---|---|---|---|---|
| Plan to certify according to DIN V VDE V 0884-11:2017- 01 | Plan to certify according to IEC 60950-1, and IEC 60601-1 | Plan to certify according to UL 1577 Component Recognition Program | Plan to certify according to GB4943.1-2011 | Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 | Plan to certify for use in intrinsic safety (IS) to IS applications under ATEX and IECEx |
| Maximum transient isolation voltage, 4242 $V_{PK}$; Maximum repetitive peak isolation voltage, 566 $V_{PK}$; Maximum surge isolation voltage, 4000 $V_{PK}$ | CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., for pollution degree 2, material group I $V_{RMS}$ basic isolation ---------- CSA 60601- 1:14 and IEC 60601-1 Ed. 3.1, 2 MOPP (Means of Patient Protection) TBD maximum working voltage | Single protection, 3000 $V_{RMS}$ | Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 250 $V_{RMS}$ maximum working voltage | 3000 $V_{RMS}$ Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 300 $V_{RMS}$ 3000 $V_{RMS}$ Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A 12:2011/A2:2013 up to working voltage of 370 $V_{RMS}$ | ATEX: EN 60079-0:2012+A11:2013 and EN 60079-11:2012 IECEx:IEC 60079-0:2011 (6th Ed) and IEC60079-11:2011 (6th Ed) II 1G Ex ia IIC Ga |
| Certificate planned | Certificate planned | Certificate planned | Certificate planned | Certificate planned | Certificate planned |

## 6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **16-QSOP PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 87°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 399 | mA |
| | | $R_{\theta JA}$ = 87°C/W, $V_I$ = 2.75 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 522 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 87°C/W, $T_J$ = 150°C, $T_A$ = 25°C | | | 1435 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where $V_I$ is the maximum input voltage.

## 6.9 Electrical Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+(IN)}$ | Rising input switching threshold | | | | 0.7 x $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -2mA | $V_{CCO}$ - 0.3 | $V_{CCO}$ - 0.2 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2mA | | 0.2 | 0.3 | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 1 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx | -1 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, $V_{CM}$ = 1200 V | 50 | 100 | | kV/us |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$

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## Electrical Characteristics 3.3V Supply (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_i$ | Input Capacitance(2) | $V_I = V_{CC}/2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, $V_{CC}$ = 3.63 V | | 2 | | pF |

(2) Measured from input pin to ground.

## 6.10 Supply Current Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO7041** | | | | | | |
| $I_{CC1}$ | Side 1 Supply Current, Refresh Disabled | DC Signal | | 5.5 | 10.5 | µA |
| | | 10kbps, No Load | | 8.3 | 14.7 | µA |
| | | 100kbps, No Load | | 36.9 | 51.3 | µA |
| | | 1Mbps, No Load | | 323.4 | 418.8 | µA |
| | Side 1 Supply Current, Refresh Enabled | Inputs in Fail safe | | 7.2 | 13 | µA |
| | | Inputs in Non-Fail safe | | 8.4 | 15.8 | µA |
| | | 10kbps, No Load | | 9.5 | 16.6 | µA |
| | | 100kbps, No Load | | 36.9 | 51.3 | µA |
| | | 1Mbps, No Load | | 322.3 | 418.8 | µA |
| $I_{CC2}$ | Side 2 Supply Current, Refresh Disabled | DC Signal | | 9.8 | 15.9 | µA |
| | | 10kbps, No Load | | 11.6 | 18.3 | µA |
| | | 100kbps, No Load | | 27.1 | 38.2 | µA |
| | | 1Mbps, No Load | | 183.7 | 238.8 | µA |
| | Side 2 Supply Current, Refresh Enabled | Inputs in Fail safe | | 10.5 | 15.9 | µA |
| | | Inputs in Non-Fail safe | | 10.9 | 17.8 | µA |
| | | 10kbps, No Load | | 11.7 | 18.7 | µA |
| | | 100kbps, No Load | | 27.1 | 38.2 | µA |
| | | 1Mbps, No Load | | 182.6 | 238.8 | µA |
| $I_{CC1(ch)} + I_{CC2(ch)}$ | Total Supply Current Per Channel, Refresh Disabled | DC Signal | | 3.8 | 6.5 | µA |
| | | 10kbps, No Load | | 5.0 | 8.1 | µA |
| | | 100kbps, No Load | | 16.1 | 21.5 | µA |
| | | 1Mbps, No Load | | 126.5 | 156 | µA |
| | Total Supply Current Per Channel, Refresh Enabled | Inputs in Fail safe | | 4.4 | 7.4 | µA |
| | | Inputs in Non-Fail safe | | 4.8 | 8.4 | µA |
| | | 10kbps, No Load | | 5.3 | 8.7 | µA |
| | | 100kbps, No Load | | 16.1 | 21.5 | µA |
| | | 1Mbps, No Load | | 126.5 | 156 | µA |

## 6.11 Electrical Characteristics 2.5V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+(IN)}$ | Rising input switching threshold | | | | 0.7 x $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 x $V_{CCI}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -1mA | $V_{CCO}$ - 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1mA | | | 0.2 | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 x $V_{CCI}$ | | | V |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$

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## Electrical Characteristics 2.5V Supply (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{IH}$ | High-level input current | $V_{IH} = V_{CCI}$ (1) at INx | | | 1 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 V at INx | -1 | | | µA |
| CMTI | Common mode transient immunity | $V_I = V_{CC}$ or 0 V, $V_{CM}$ = 1200 V | 50 | 100 | | kV/us |
| $C_i$ | Input Capacitance(2) | $V_I = V_{CC}/2 + 0.4\times\sin(2\pi ft)$, f = 1 MHz, $V_{CC}$ = 2.5 V | | 2 | | pF |

(2) Measured from input pin to ground.

## 6.12 Supply Current Characteristics 2.5V Supply

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO7041** | | | | | | |
| $I_{CC1}$ | Side 1 Supply Current, Refresh Disabled | DC Signal | | 5.1 | 9.3 | µA |
| | | 10kbps, No Load | | 8.6 | 13.2 | µA |
| | | 100kbps, No Load | | 35.6 | 47.1 | µA |
| | | 1Mbps, No Load | | 306.9 | 387.6 | µA |
| | Side 1 Supply Current, Refresh Enabled | Inputs in Fail safe | | 6.7 | 11.7 | µA |
| | | Inputs in Non-Fail safe | | 7.9 | 14.1 | µA |
| | | 10kbps, No Load | | 8.7 | 15.2 | µA |
| | | 100kbps, No Load | | 35.6 | 47.1 | µA |
| | | 1Mbps, No Load | | 305.8 | 387.6 | µA |
| $I_{CC2}$ | Side 2 Supply Current, Refresh Disabled | DC Signal | | 9.4 | 14.8 | µA |
| | | 10kbps, No Load | | 11.1 | 17.0 | µA |
| | | 100kbps, No Load | | 25.1 | 34.9 | µA |
| | | 1Mbps, No Load | | 167.2 | 216 | µA |
| | Side 2 Supply Current, Refresh Enabled | Inputs in Fail safe | | 10.0 | 14.8 | µA |
| | | Inputs in Non-Fail safe | | 10.5 | 16.6 | µA |
| | | 10kbps, No Load | | 11.1 | 18.3 | µA |
| | | 100kbps, No Load | | 25.1 | 34.9 | µA |
| | | 1Mbps, No Load | | 166.1 | 216 | µA |
| $I_{CC1(ch)} + I_{CC2(ch)}$ | Total Supply Current Per Channel, Refresh Disabled | DC Signal | | 3.6 | 6.0 | µA |
| | | 10kbps, No Load | | 4.8 | 7.4 | µA |
| | | 100kbps, No Load | | 15.0 | 19.5 | µA |
| | | 1Mbps, No Load | | 118.8 | 141.6 | µA |
| | Total Supply Current Per Channel, Refresh Enabled | Inputs in Fail safe | | 4.2 | 6.8 | µA |
| | | Inputs in Non-Fail safe | | 4.6 | 7.6 | µA |
| | | 10kbps, No Load | | 4.9 | 8.2 | µA |
| | | 100kbps, No Load | | 15.0 | 19.5 | µA |
| | | 1Mbps, No Load | | 117.7 | 141.6 | µA |

## 6.13 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 1 | | 140 | 175 | ns |
| $t_{UI}$ | Minimum pulse width | | 500 | | | ns |
| PWD | Pulse width distortion | | | | 10 | ns |

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## Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{sk(o)}$ | Channel to channel output skew time | Same-direction channels | | | 10 | ns |
| | | Opposite-direction channels | | | 10 | ns |
| $t_{sk(p-p)}$ | Part to part skew time | | | | 70 | ns |
| $t_R$ | Output signal rise time | See Figure 1 | | | 5 | ns |
| $t_F$ | Output signal fall time | | | | 5 | ns |
| $t_{DO}$ | Default output delay time from input power loss | Refresh enabled, See Figure 3 | | 400 | 750 | us |
| $t_{PU}$ | Time from UVLO to valid output data | | 1 | | 5 | ms |
| $F_R$ | Refresh rate | | 5 | 10 | | kbps |

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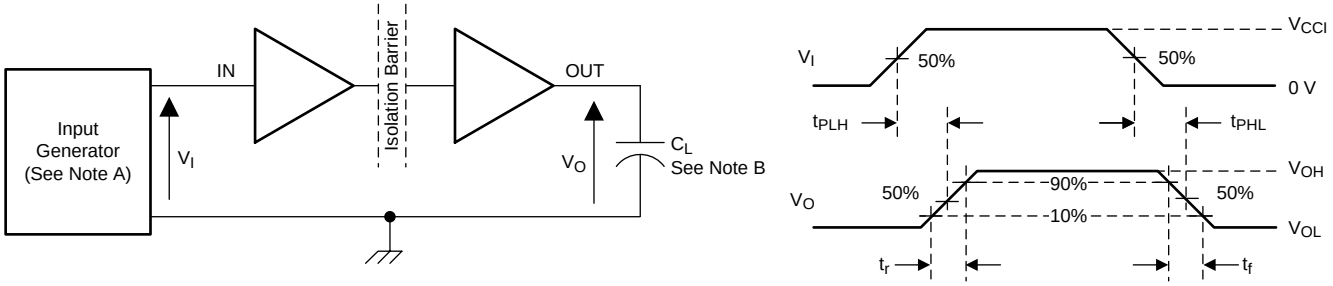
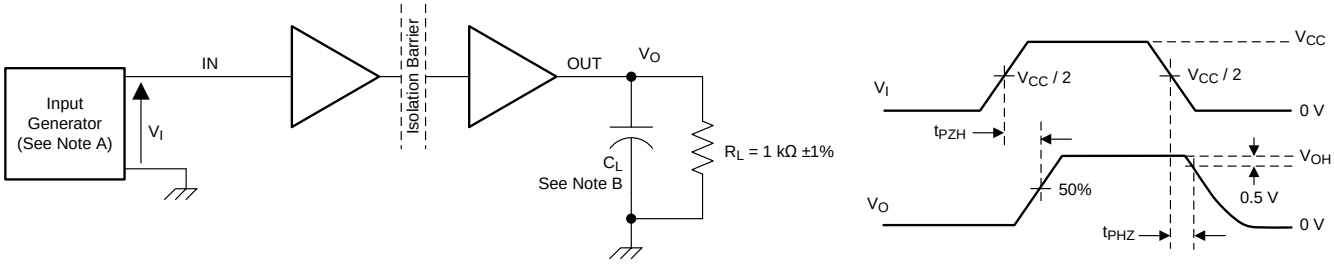
# 7 Parameter Measurement Information




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3ns, $Z_O$ = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

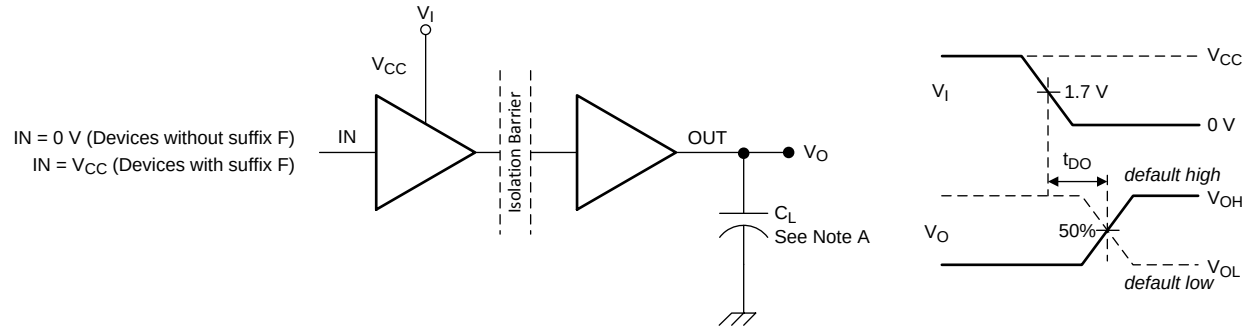
**Figure 1. Switching Characteristics Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 2. Propagation Delay Time Test Circuit and Waveform**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

**Figure 3. Default Output Delay Time Test Circuit and Voltage Waveforms**

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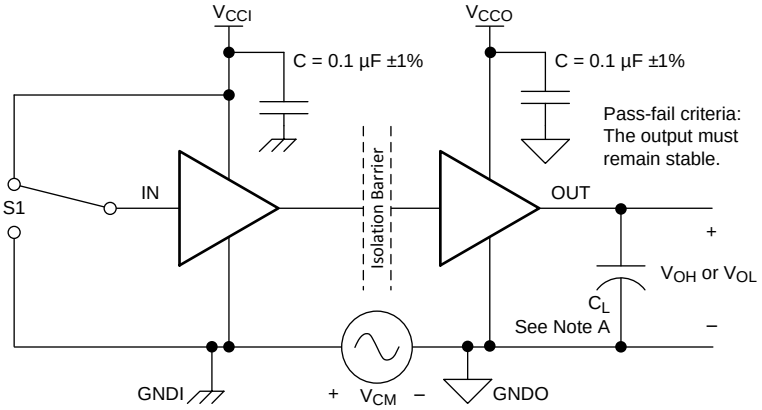
## Parameter Measurement Information (continued)




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 4. Common-Mode Transient Immunity Test Circuit**

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# 8 Detailed Description

## 8.1 Overview

The ISO7041 device uses edge encoding of data with an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide isolation barrier. The transmitter uses a high frequency carrier signal to pass data across the barrier representing a signal edge transition. Using this method achieves very low power consumption and high immunity. The receiver demodulates the carrier signal after advanced signal conditioning and produces the output through a buffer stage. For low data rates, a refresh logic option is available to make sure the output state matches the input state. The ENx pins of side A and side B must be tied low to enable refresh or high to disable refresh. Advanced circuit techniques are used to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 5, shows a functional block diagram of a typical channel.

## 8.2 Functional Block Diagram

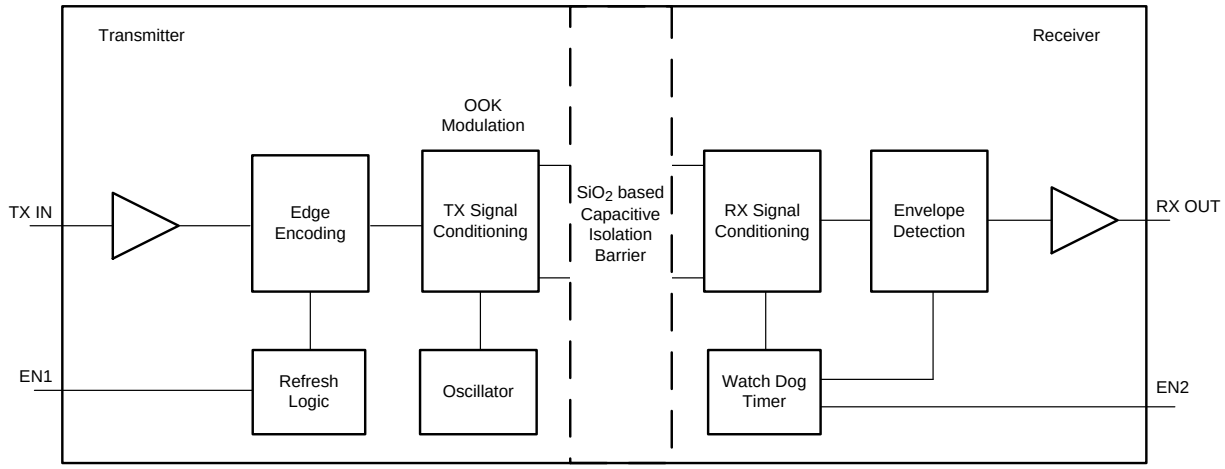


**Figure 5. Conceptual Block Diagram of a Digital Capacitive Isolator**

## 8.3 Feature Description

Table 1 shows an overview of the device features.

**Table 1. Device Features**

| PART NUMBER | CHANNEL DIRECTION | MAXIMUM DATA RATE | DEFAULT OUTPUT | PACKAGE | RATED ISOLATION(1) |
|---|---|---|---|---|---|
| ISO7041 | 3 Forward, 1 Reverse | 2 Mbps | High | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |
| ISO7041 with F suffix | 3 Forward, 1 Reverse | 2 Mbps | Low | DBQ-16 | 3000 $V_{RMS}$ / 4242 $V_{PK}$ |

(1) See for detailed isolation ratings.

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### 8.3.1 Refresh Enable

The ISO7041 uses an edge based encoding scheme to transfer an input signal change across the isolation barrier versus sending across the DC state. Enabling the refresh feature consistently validates that the DC output state of each isolator channel matches the DC input state. An internal watchdog timer monitors for activity on the individual inputs and transmits the logic state when there is no input signal transition for more than 100 µs. This ensures that the input and output state of the isolator always match. Tie both EN1 and EN2 to their respective grounds to enable refresh.

Disable refresh by tying both EN1 and EN2 to their respective VCC power supplies. Disabling refresh will further decrease the power consumption of the device but the DC state is not guaranteed at startup. System level solutions can be implemented to ensure the isolator channel output matches the input at startup. For example, at start up, an immediate full transition of the input signals from high to low and low to high on the individual isolator lines would allow the states of the outputs to properly track the inputs.

### 8.3.2 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO70xx family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

The device has no issue being able to meet either CISPR 22 Class A and CISPR22 Class B standards in an unshielded environment.

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## 8.4 Device Functional Modes

Table 2 shows the functional modes for the device.

**Table 2. Function Table(1)**

| $V_{CCI}$ | $V_{CCO}$ | INPUT (INx)(2) | REFRESH ENABLE (ENx) | OUTPUT (OUTx) | COMMENTS |
|---|---|---|---|---|---|
| PU | PU | H | L | H | Normal Operation:<br>A channel output assumes the logic state of its input. |
| | | L | L | L | |
| | | X | H | Undetermined | The device needs an input signal transition to validate the output tracks the input state. Without a signal edge transition, the output will be in an undetermined state. |
| PD | PU | X | L | Default | When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for the device without the F suffix and *Low* for device with the F suffix.<br>When $V_{CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input.<br>When $V_{CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state. |
| | | | H | Undetermined | When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the previous state of the output before $V_{CCI}$ powered down. |
| X | PD | X | L | Undetermined | When $V_{CCO}$ is unpowered, a channel output is undetermined(3).<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input. |
| | | | H | Undetermined | When $V_{CCO}$ is unpowered, a channel output is undetermined(3).<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the selected default option. |
| X | X | X | Open | Undetermined | When ENx is unconnected or open, the device output will be in an undetermined and unknown state. ENx must be connected high or low for the device to behave correctly. |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$; PU = Powered up ($V_{CC} \geq 2.25$ V); PD = Powered down ($V_{CC} \leq 1.54$); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) A strongly driven input signal can weakly power the floating $V_{CC}$ through an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 2.25 V < $V_{CCI}$, $V_{CCO}$ < 2.25 V.

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### 8.4.1 Device I/O Schematics

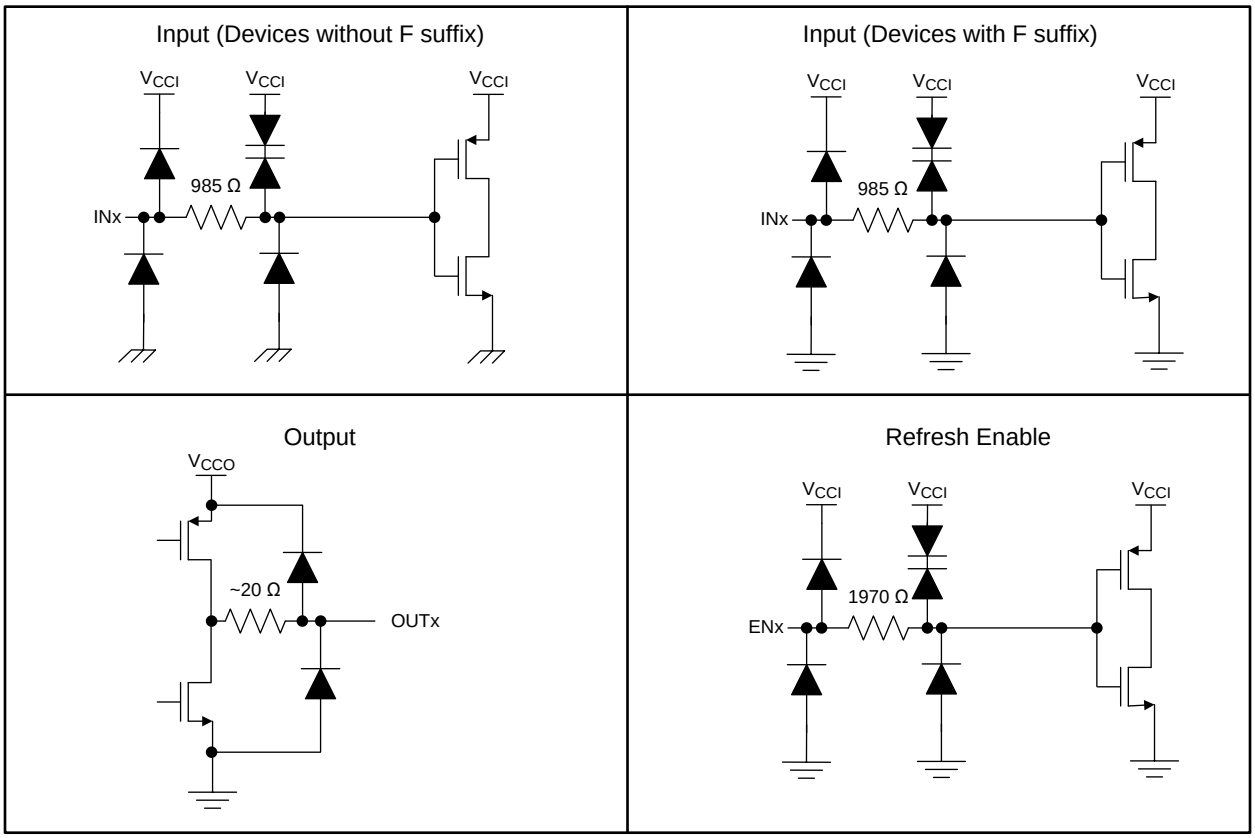


**Figure 6. Device I/O Schematics**

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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The ISO7041 device is an ultra-low power digital isolator. The device uses single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 3.63 V for both supplies, $V_{CC1}$ and $V_{CC2}$, and can be set irrespective of one another. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

## 9.2 Typical Application

Figure 7 shows the isolated serial peripheral interface (SPI).

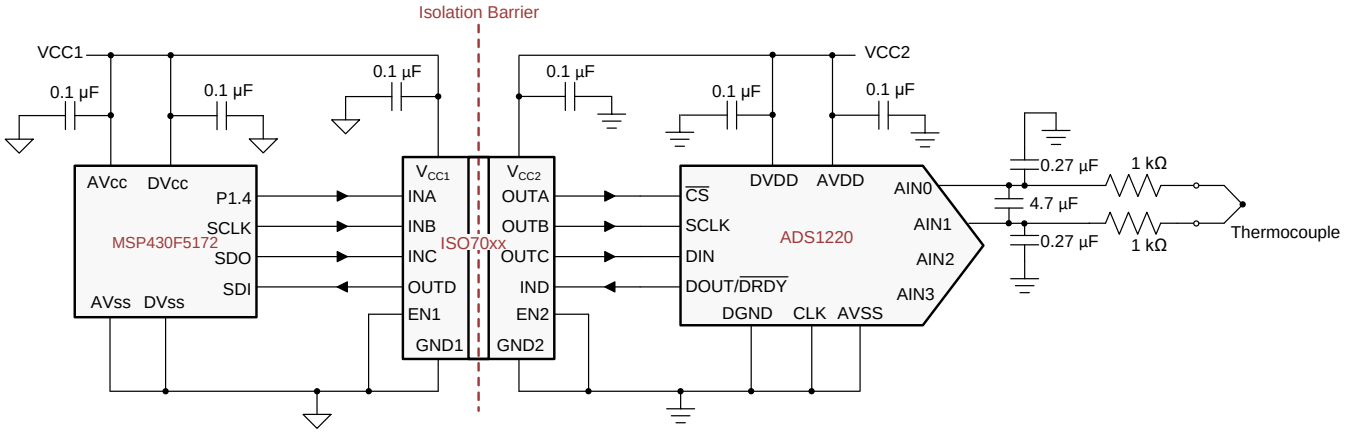


**Figure 7. Isolated SPI for a Temperature Field Transmitter**

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## Typical Application (continued)

### 9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 3.

**Table 3. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Supply voltage, $V_{CC1}$ and $V_{CC2}$ | 2.25 V to 3.63 V |
| Decoupling capacitor between $V_{CC1}$ and GND1 | 0.1 µF |
| Decoupling capacitor from $V_{CC2}$ and GND2 | 0.1 µF |

### 9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the device only require two external bypass capacitors to operate.

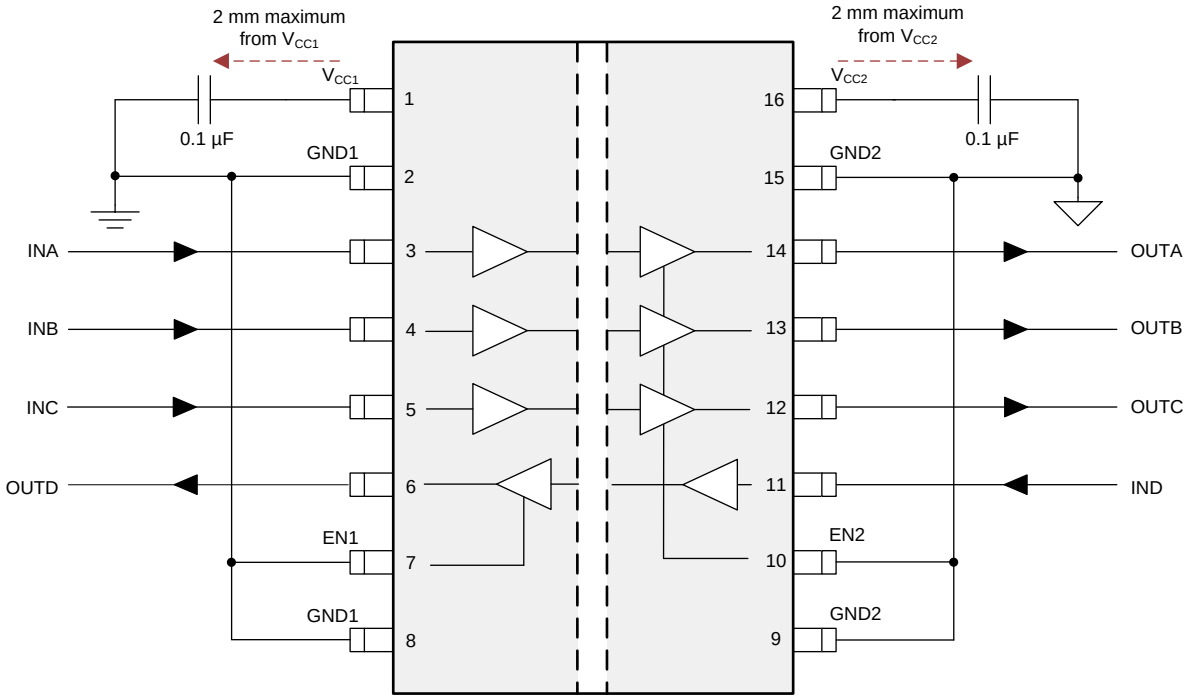


**Figure 8. Typical ISO7041 Circuit Hook-up**

### 9.2.3 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see Figure 9 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm) and a minimum insulation lifetime of 20 years. VDE standard also requires additional safety margin of 20% for working voltage and 87.5% for insulation lifetime which translates into minimum required life time of 37.5 years.

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Figure 10 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of these devices is 400 VRMS with a lifetime of >100 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of the DBQ-16 package specified up to 400 VRMS. At the lower working voltages, the corresponding insulation barrier life time is much longer.

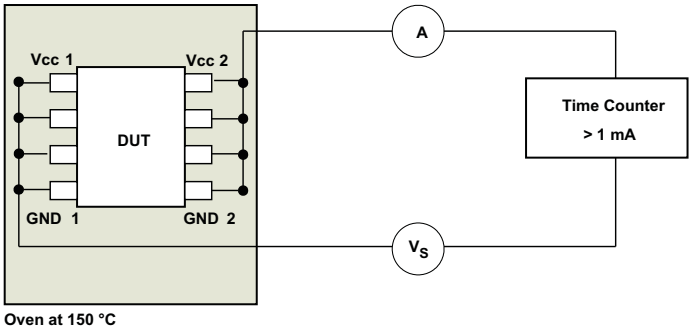


**Figure 9. Test Setup for Insulation Lifetime Measurement**

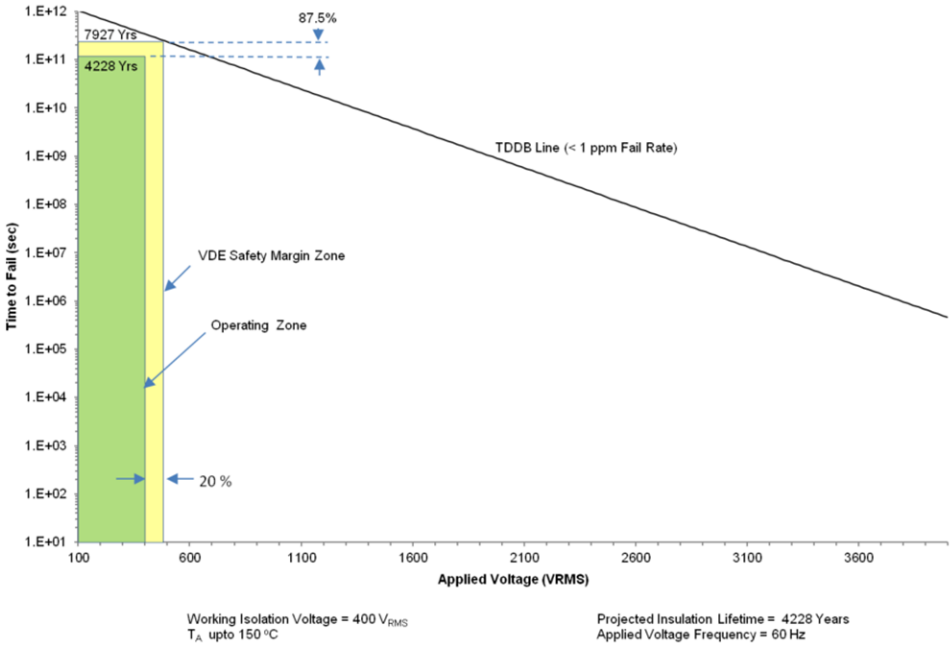


**Figure 10. Insulation Lifetime Projection Data**

## 10 Power Supply Recommendations

Put a 0.1-µF bypass capacitor at the input and output supply pins ($V_{CC1}$ and $V_{CC2}$) to make sure that operation is reliable at data rates and supply voltage. Put the capacitors as near to the supply pins as possible. If only one primary-side power supply is available in an application, use a transformer driver to help generate the isolated power for the secondary-side. Texas Instruments recommends the SN6501 device or SN6505A device. Refer to the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet for detailed power supply design and transformer selection recommendations.

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# 11 Layout

## 11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 11). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in$^2$.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the *Digital Isolator Design Guide* for detailed layout recommendations,.

### 11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 11.2 Layout Example

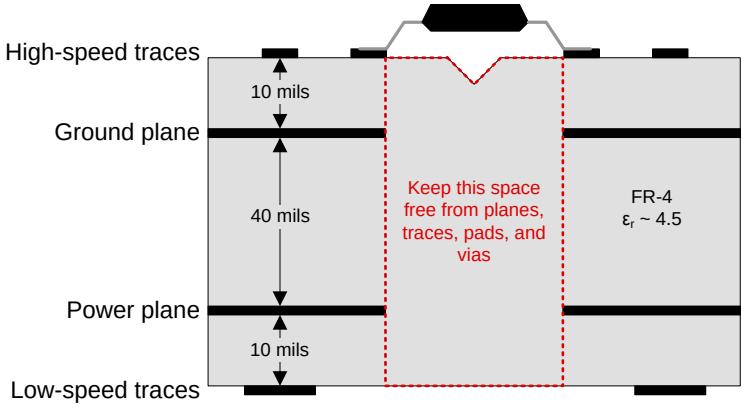


**Figure 11. Recommended Layer Stack**

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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *ADS1220 4-Channel, 2-kSPS, Low-Power, 24-Bit ADC with Integrated PGA and Reference* data sheet
- Texas Instruments, *ADS122U04 24-Bit, 4-Channel, 2-kSPS, Delta-Sigma ADC With UART Interface* data sheet
- Texas Instruments, *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet
- Texas Instruments, *Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications* TI Design
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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## 12.4 Trademarks

E2E is a trademark of Texas Instruments.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7041DBQ | PREVIEW | SSOP | DBQ | 16 | 1500 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISO7041DBQR | PREVIEW | SSOP | DBQ | 16 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISO7041FDBQ | PREVIEW | SSOP | DBQ | 16 | 1500 | TBD | Call TI | Call TI | -40 to 125 | | |
| ISO7041FDBQR | PREVIEW | SSOP | DBQ | 16 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | |
| XISO7041DBQR | ACTIVE | SSOP | DBQ | 16 | 2500 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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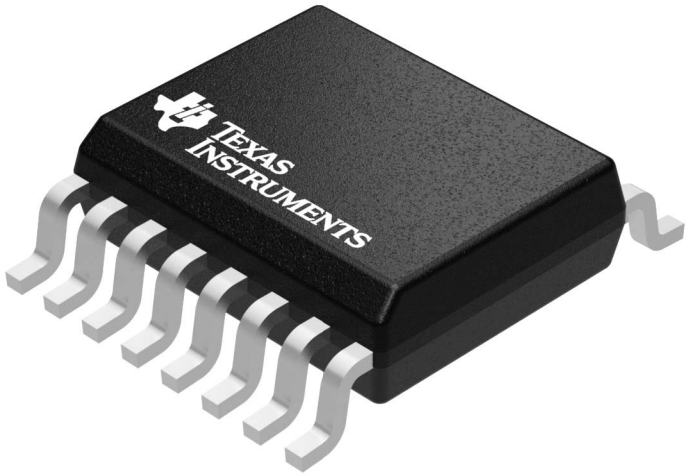
# GENERIC PACKAGE VIEW

## DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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