IS2020/21/23/25 SoC

Bluetooth® 4.1 Stereo Audio SOC

Features

System Specification
- Compliant with Bluetooth Specification v.4.1 (EDR) in 2.4 GHz ISM band
- It supports following profiles :
  - HFP 1.6
  - HSP 1.1
  - A2DP 1.2
  - AVRCP 1.5
  - SPP 1.0
  - PBAP 1.0

Baseband Hardware
- 16MHz main clock input
- Built-in internal ROM for program memory
- Support to connect to two hosts (phones, tablets…) with HFP or A2DP profiles simultaneously
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels
- Fast Connection supported

RF Hardware
- Fully Bluetooth 4.1 (EDR) system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- Max. +4dBm output power with 20 dB level control from register control.
- Built-in T/R switch for Class 2/3 application
- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.
- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with built-in digital trimming for temperature/process variations.

Audio processor
- Support 64 kb/s A-Law or μ-Law PCM format, or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.
- Noise suppression
- Echo suppression
- SBC and optional AAC decoding

- Packet loss concealment
- Build-in four languages (Chinese/ English/ Spanish/ French) voice prompts and 20 events for each one (This function can be set up in "IS20XXS_UI" tool.)
- Support SCMS-T

Audio Codec
- 20 bit DAC and 16 bit ADC codec
- 98dB SNR DAC playback
- Built-in 2 channel 2.3W class-D amplifier for a 4Ω speaker (for IS2025S only)

Peripherals
- Built-in Lithium-ion battery charger (up to 350mA)
- Integrate 3V, 1.8V configurable switching regulator and LDO
- Built-in ADC for battery monitor and voltage sense.
- A line-in port for external audio input
- Two LED drivers

Flexible HCI interface
- High speed HCI-UART (Universal Asynchronous Receiver Transmitter) interface (up to 921600bps)

Package
- 5x6.5mm² 48QFN package (IS2021S)
- 7x7mm² 56QFN package (IS2020S, IS2023S)
- 8x8mm² 68QFN package (IS2025S)

Description

Stereo Audio Chip is a compact, highly integrated, CMOS single-chip RF and baseband IC for Bluetooth v4.1 with Enhanced Data Rate 2.4GHz applications. This chip is fully compliant with Bluetooth specification and completely backward-compatible with Bluetooth 3.0, 2.0 or 1.2 systems.

It incorporates Bluetooth 1M/2M/3Mbps RF, single-cycle 8bit MCU, TX/RX modem, 5-port memory controller, task/hopping controller,

UART interface, and MICROCHIP's own Bluetooth software stack to achieve the required BT v4.1 with EDR functions.

To provide the superior audio and voice quality, it also integrates a DSP co-processor, a PLL, and a CODEC dedicated for voice and audio applications.

For voice, not only basic CVSD encoding and decoding but also enhanced noise reduction and echo cancellation are implemented by the built-in DSP to achieve better quality in both sending and receiving sides. For the enhanced audio applications, SBC/AAC_LC decoding functions can be also carried out by DSP to satisfy Bluetooth A2DP requirements.

In addition, to minimize the external components required for portable devices, a battery voltage sensor, battery charger, a switching regulator and LDO are integrated to reduce system BOM cost for various Bluetooth applications.

As the market of portable/wireless speakers demand is increasing, a stereo 2 channels 2.3W class-D amplifier which provides up to 100dB SNR is also built-in to reduce BOM cost and PCB area.

Applications

- Stereo headsets
- Portable speakerphones

Table of Contents

Abbreviations List:

HFP: Hands-free Profile
AVRCP: Audio Video Remote Control Profile
A2DP: Advanced Audio Distribution Profile
PBAP: Phone Book Access Profile
HSP: Headset Profile
SPP: Serial Port Profile
NFC: Near Field Communication
CDA: Class D Amplifier
SCMS-T: Serial Copy Management System

1.0 DEVICE OVERVIEW

The stereo audio chip series include IS2020S, IS2021S, IS2023S, and IS2025S chip. The chip integrates Bluetooth 4.1 radio transceiver, PMU, DSP and 2-channel CDA (Class D Amplifier). Figure 1-1 shows the application block diagram.

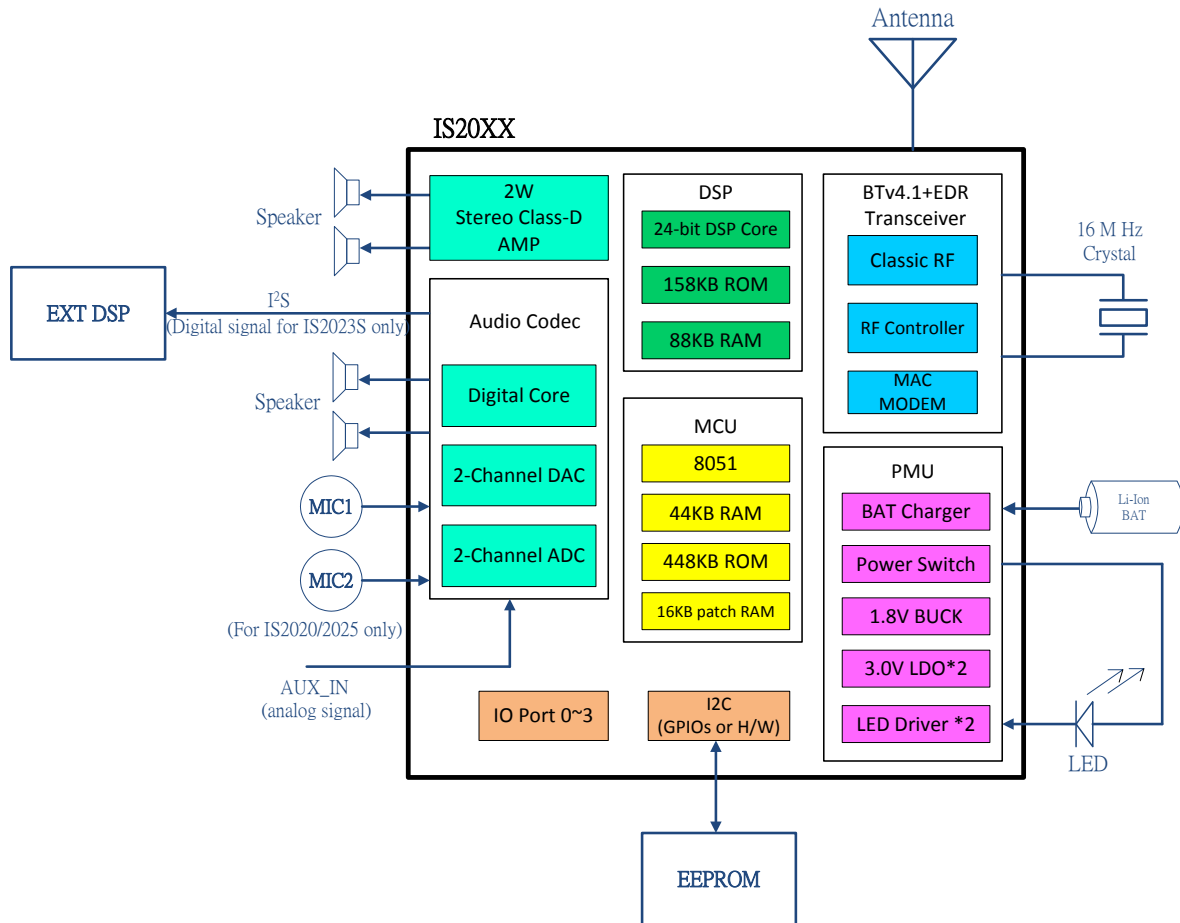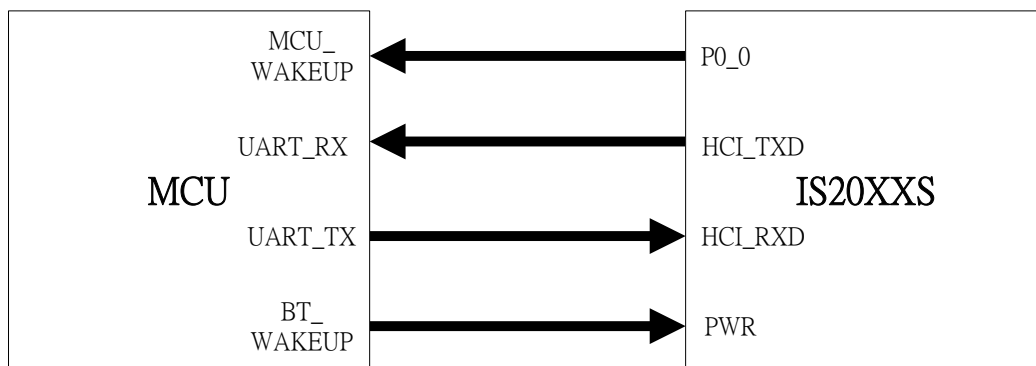**FIGURE 1-1: APPLICATION BLOCK DIAGRAM**

FIGURE 1-2: INTERFACE BETWEEN MCU AND IS20XX CHIP

2.0 KEY FEATURES TABLE

Feature Chip	IS2020S	IS2021S	IS2023S	IS2025S
Application	Headset / Speaker	Headset	I²S Speaker	Speaker
Stereo/Mono	Stereo	Stereo	Stereo	Stereo
Pin count	56	48	56	68
Dimension (mm²)	7X7	5X6.5	7X7	8X8
Audio DAC output	2-ch	2-ch	X	2-ch
DAC (single-end) SNR @2.8V (dB)	-98	-98	X	-98
DAC (cap-less) SNR @2.8V (dB)	-96	-96	X	-96
ADC SNR @2.8V (dB)	-90	-90	-90	-90
I²S digital interface	X	X	√	X
Analog Aux- in	√	X	√	√
Mono MIC	2	1	1	2
Support external audio AMP	√	X	X	√
Build-in Class-D amplifier	X	X	X	2-ch
UART	√	√	√	√
LED Driver	2	2	2	2
Internal DC-DC step-down regulator	√	√	√	√
DC 5V Adaptor Input	√	√	√	√
Battery Charger (350mA max)	√	√	√	√
IO Pin for Application	9	8	X	10
Button support	6	6	6	6
Support NFC application	√	√	√	√
Voice prompt	√	√	√	√
Multi-tone	√	√	√	√
Internal DSP sound effect	√	√	X	√
Profile				
HFP	1.6	1.6	1.6	1.6
AVRCP	1.5	1.5	1.5	1.5
A2DP	1.2	1.2	1.2	1.2
PBAP	1.0	1.0	1.0	1.0
HSP	1.1	1.1	1.1	1.1
SPP	1.0	1.0	1.0	1.0
Build-in EEPROM	X	□√(128k)	X	X

Note: "√" means support the feature.

"X" means no support the feature.

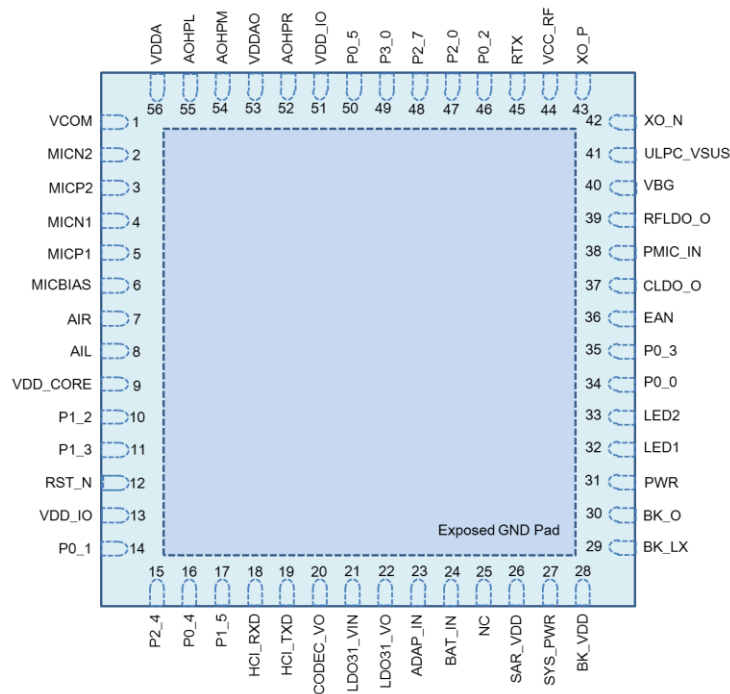## 3.0 PIN DESCRIPTION AND POWER SUPPLY

3.1 PIN ASSIGNMENT

TABLE 3-1: IS2020S PIN DESCRIPTION

Pin No.	Pin type	Name	Description
1	P	VCOM	Internal biasing voltage for CODEC
2	I	MICN2	Mic 2 mono differential analog negative input
3	I	MICP2	Mic 2 mono differential analog positive input
4	I	MICN1	Mic 1 mono differential analog negative input
5	I	MICP1	Mic 1 mono differential analog positive input
6	P	MIC_BIAS	Electric microphone biasing voltage
7	I	AIR	R-channel single-ended analog inputs
8	I	AIL	L-channel single-ended analog inputs
9	P	VDD_CORE	Core 1.2V power input; Connect to CLDO_O pin
10	O	P1_2	IO pin, default pull-high input EEPROM clock SCL
11	I/O	P1_3	IO pin, default pull-high input EEPROM data SDA
12	I	RST_N	System Reset Pin, active when rising edge.
13	P	VDD_IO	I/O power supply input (2.7~3.3V); Connect to LDO31_VO pin
14	I/O	P0_1	IO pin, default pull-high input (Note 1) 1. FWD key when class 2 RF (default), active low. 2. Class1 TX Control signal of external RF T/R switch, active high.
15	I	P2_4	IO pin, default pull-high input System Configuration,

Pin No.	Pin type	Name	Description
			L: Boot Mode with P2_0 low combination

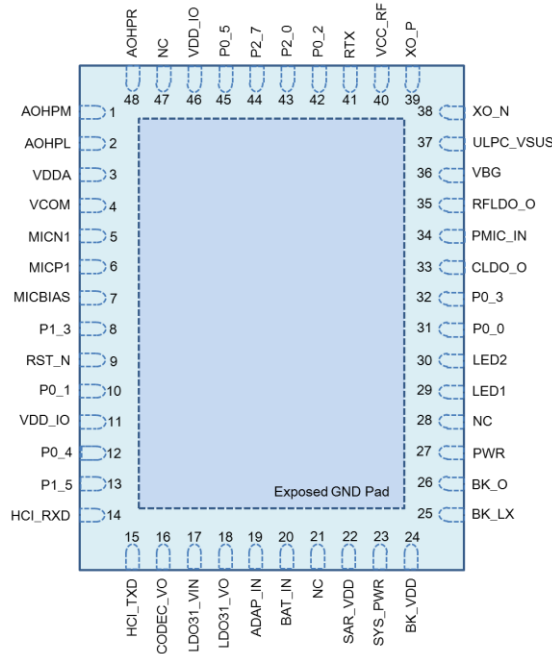| Pin No.	Pin type	Name	Description
16	I/O	P0_4	IO pin, default pull-high input. (Note 1) 1. NFC detection pin, active low. 2. Out_Ind_0
17	I/O	P1_5	IO pin, default pull-high input (Note 1) 1. NFC detection pin, active low. 2. Out_Ind_0 3. Slide Switch Detector, active low. 4. Buzzer Signal Output
18	I	HCI_RXD	HCI-UART RX data
19	O	HCI_TXD	HCI-UART TX data
20	P	CODEC_VO	3.1V LDO output for CODEC power
21	P	LDO31_VIN	3.1V LDO input; Connect to SYS_PWR pin
22	P	LDO31_VO	3.1V LDO output
23	P	ADAP_IN	5V power adaptor input
24	P	BAT_IN	3.3V~4.2V Li-Ion battery input
25	-	NC	No Connection
26	P	SAR_VDD	SAR 1.8V input; Connect to BK_O pin
27	P	SYS_PWR	Power Output which come from BAT_IN or ADAP_IN
28	P	BK_VDD	1.8V buck VDD Power Input; Connect to SYS_PWR pin
29	P	BK_LX	1.8V buck pin for switch
30	P	BK_O	1.8V buck feedback input
31	I	PWR	Multi-Function Push Button and power on key
32	I	LED2	LED Driver 2
33	I	LED1	LED Driver 1
34	I/O	P0_0	IO pin, default pull-high input (Note 1) 1. Slide Switch Detector, active low. 2. UART TX_IND, active low.
35	I/O	P0_3	IO pin, default pull-high input (Note 1) 1. REV key (default), active low. 2. Buzzer Signal Output 3. Out_Ind_1 4. Class1 RX Control signal of external RF T/R switch, active high.
36	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash
37	P	CLDO_O	1.2V core LDO output
38	P	PMIC_IN	PMU blocks power input; Connect to BK_O pin
39	P	RFLDO_O	1.28V RF LDO output
40	P	VBG	Bandgap output reference for decoupling interference
41	P	ULPC_VSUS	ULPC 1.2V output power.

Pin No.	Pin type	Name	Description
42	I	XO_N	16MHz Crystal input negative
43	I	XO_P	16MHz Crystal input positive
44	P	VCC_RF	RF power input (1.28V) for both synthesizer and TX/RX block

Pin No.	Pin type	Name	Description
45	I/O	RTX	RF RTX path
46	I	P0_2	IO pin, default pull-high input (Note 1) Play/Pause key (default), active low.
47	I	P2_0	IO pin, default pull-high input System Configuration, H: Application L: Baseband(IBDK Mode)
48	I	P2_7	IO pin, default pull-high input (Note 1) Volume up key (default), active low.
49	I	P3_0	IO pin, default pull-high input (Note 1) Line-in Detector (default), active low.
50	I	P0_5	IO pin, default pull-high input (Note 1) Volume down (default), active low.
51	P	VDD_IO	I/O power supply input (2.7~3.3V); Connect to LDO31_VO pin
52	O	AOHPR	R-channel analog headphone output
53	P	VDDAO	Positive power supply dedicated to CODEC output amplifiers; Connect to CODEC_VO pin
54	O	AOHPM	Headphone common mode output/sense input.
55	O	AOHPL	L-channel analog headphone output
56	P	VDDA	Positive power supply/reference voltage for CODEC; Connect to CODEC_VO pin
57	P	EP	Exposed pad as ground

* I: signal input pin
* O: signal output pin
* I/O: signal input/output pin
* P: power pin

Note 1: These button or functions can be setup by "IS20XXS_UI" tool.

TABLE 3-2: IS2021S PIN DESCRIPTION

Pin No.	Pin type	Name	Description
1	O	AOHPM	Headphone common mode output/sense input.
2	O	AOHPL	L-channel analog headphone output
3	P	VDDA	Positive power supply/reference voltage for CODEC; Connect to CODEC_VO pin
4	P	VCOM	Internal biasing voltage for CODEC
5	I	MICN1	Mic 1 mono differential analog negative input
6	I	MICP1	Mic 1 mono differential analog positive input
7	P	MIC_BIAS	Electric microphone biasing voltage
8	I/O	P1_3	IO pin, default pull-high input EEPROM data SDA
9	I	RST_N	System Reset Pin, active when rising edge.
10	I/O	P0_1	IO pin, default pull-high input (Note 1) 1. FWD key when class 2 RF, active low. 2. Class1 TX Control signal of external RF T/R switch, active high.
11	P	VDD_IO	I/O power supply input (2.7~3.3V); Connect to LDO31_VO pin
12	I/O	P0_4	IO pin, default pull-high input. (Note 1) 1. NFC detection pin, active low. 2. Out_Ind_0
13	I/O	P1_5	IO pin, default pull-high input (Note 1) 1. NFC detection pin, active low. 2. Out_Ind_0

Pin No.	Pin type	Name	Description
			3. Slide Switch Detector, active low. 4. Buzzer Signal Output
14	I	HCI_RXD	HCI-UART RX data
15	O	HCI_TXD	HCI-UART TX data

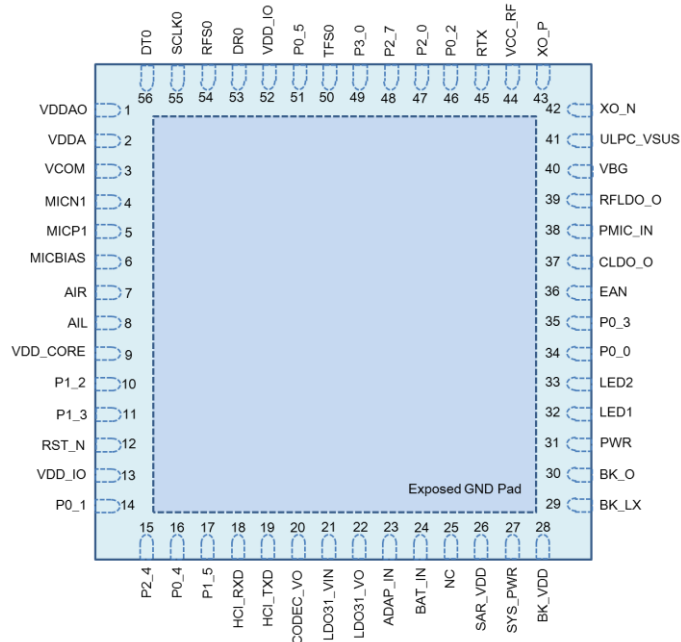| Pin No.	Pin type	Name	Description
16	P	CODEC_VO	3.1V LDO output for CODEC power
17	P	LDO31_VIN	3.1V LDO input; Connect to SYS_PWR pin
18	P	LDO31_VO	3.1V LDO output
19	P	ADAP_IN	5V power adaptor input
20	P	BAT_IN	3.3~4.2V Li-Ion battery input
21	-	NC	No Connection
22	P	SAR_VDD	SAR 1.8V input; Connect to BK_O pin
23	P	SYS_PWR	Power Output which come from BAT_IN or ADAP_IN
24	P	BK_VDD	1.8V buck VDD Power Input; Connect to SYS_PWR pin
25	P	BK_LX	1.8V buck pin for switch
26	P	BK_O	1.8V buck feedback input
27	I	PWR	Multi-Function Push Button and power on key
28	-	NC	No Connection
29	I	LED2	LED Driver 2
30	I	LED1	LED Driver 1
31	I/O	P0_0	IO pin, default pull-high input (Note 1) 1. Slide Switch Detector, active low. 2. UART TX_IND, active low.
32	I/O	P0_3	IO pin, default pull-high input (Note 1) 1. REV key (default), active low. 2. Buzzer Signal Output 3. Out_Ind_1 4. Class1 RX Control signal of external RF T/R switch, active high.
33	P	CLDO_O	1.2V core LDO output
34	P	PMIC_IN	PMU blocks power input; Connect to BK_O pin
35	P	RFLDO_O	1.28V RF LDO output
36	P	VBG	Bandgap output reference for decoupling interference
37	P	ULPC_VSUS	ULPC 1.2V output power.
38	I	XO_N	16MHz Crystal input negative
39	I	XO_P	16MHz Crystal input positive
40	P	VCC_RF	RF power input (1.28V) for both synthesizer and TX/RX block; Connect to RFLDO_O pin
41	I/O	RTX	RF RTX path
42	I	P0_2	IO pin, default pull-high input (Note 1) Play/Pause key (default), active low.

Pin No.	Pin type	Name	Description
43	I	P2_0	IO pin, default pull-high input (Note 1) System Configuration, H: Application L: Baseband(IBDK Mode)
44	I	P2_7	IO pin, default pull-high input (Note 1) Volume up key (default), active low.
45	I	P0_5	IO pin, default pull-high input (Note 1) Volume down (default), active low.

Pin No.	Pin type	Name	Description
46	P	VDD_IO	I/O power supply input (2.7~3.3V); Connect to LDO31_VO pin
47	-	NC	No Connection.
48	O	AOHPR	R-channel analog headphone output
49	P	EP	Exposed pad as ground

* I: signal input pin
* O: signal output pin
* I/O: signal input/output pin
* P: power pin

Note 1: These button or functions can be setup by "IS20XXS_UI" tool.

TABLE 3-3: IS2023S PIN DESCRIPTION

Pin No.	Pin type	Name	Description
1	P	VDDAO	Positive power supply dedicated to CODEC output amplifiers; Connect to CODEC_VO pin
2	P	VDDA	Positive power supply/reference voltage for CODEC; Connect to CODEC_VO pin
3	P	VCOM	Internal biasing voltage for CODEC
4	I	MICN1	Mic 1 mono differential analog negative input
5	I	MICP1	Mic 1 mono differential analog positive input
6	P	MIC_BIAS	Electric microphone biasing voltage
7	I	AIR	R-channel single-ended analog inputs
8	I	AIL	L-channel single-ended analog inputs
9	P	VDD_CORE	Core 1.2V power input; Connect to CLDO_O pin
10	O	P1_2	IO pin, default pull-high input EEPROM clock SCL
11	I/O	P1_3	IO pin, default pull-high input EEPROM data SDA
12	I	RST_N	System Reset Pin, active when rising edge.
13	P	VDD_IO	I/O power supply input (2.7~3.3V); Connect to LDO31_VO pin
14	I/O	P0_1	IO pin, default pull-high input

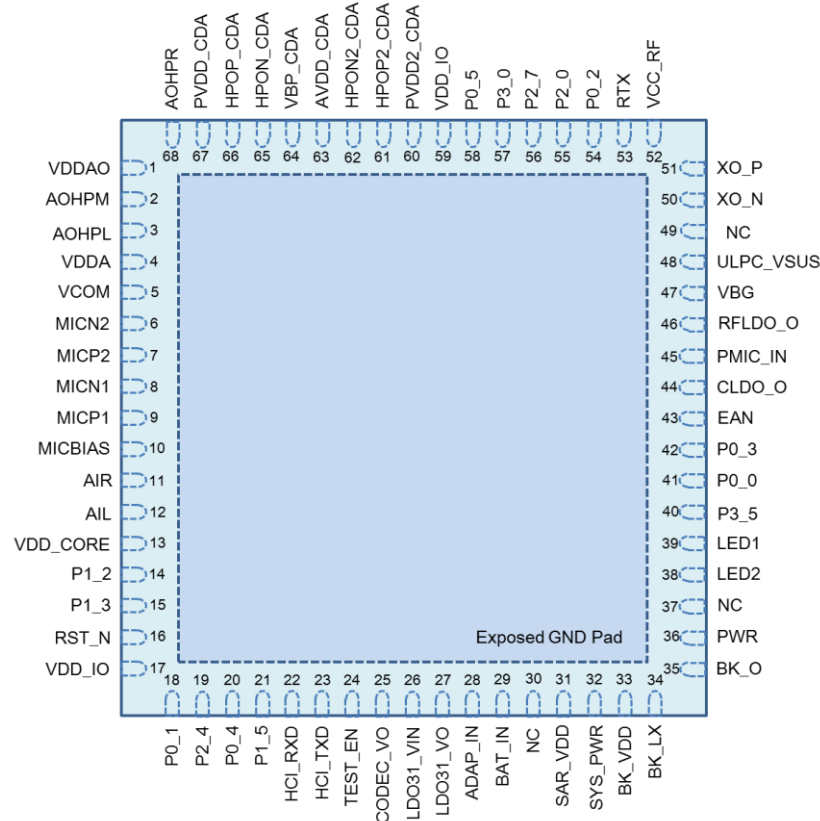| Pin No.	Pin type	Name	Description
15	I	P2_4	IO pin, default pull-high input System Configuration, L: Boot Mode with P2_0 low combination
16	I/O	P0_4	IO pin, default pull-high input.
17	I/O	P1_5	IO pin, default pull-high input
18	I	HCI_RXD	HCI-UART RX data
19	O	HCI_TXD	HCI-UART TX data
20	P	CODEC_VO	3.1V LDO output for CODEC power
21	P	LDO31_VIN	3.1V LDO input; Connect to SYS_PWR pin
22	P	LDO31_VO	3.1V LDO output
23	P	ADAP_IN	5V power adaptor input
24	P	BAT_IN	3.3~4.2V Li-ion battery input
25	-	NC	No Connection
26	P	SAR_VDD	SAR 1.8V input; Connect to BK_O pin
27	P	SYS_PWR	Power Output which come from BAT_IN or ADAP_IN
28	P	BK_VDD	1.8V buck VDD Power Input; Connect to SYS_PWR pin
29	P	BK_LX	1.8V buck pin for switch
30	P	BK_O	1.8V buck feedback input
31	I	PWR	1. Multi-Function Push Button and power on key 2. UART RX_IND
32	I	LED2	LED Driver 2
33	I	LED1	LED Driver 1
34	I/O	P0_0	IO pin, default pull-high input (Note 1) UART TX_IND
35	I/O	P0_3	IO pin, default pull-high input
36	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash
37	P	CLDO_O	1.2V core LDO output
38	P	PMIC_IN	PMU blocks power input; Connect to BK_O pin
39	P	RFLDO_O	1.28V RF LDO output
40	P	VBG	Bandgap output reference for decoupling interference
41	P	ULPC_VSUS	ULPC 1.2V output power.
42	I	XO_N	16MHz Crystal input negative
43	I	XO_P	16MHz Crystal input positive
44	P	VCC_RF	RF power input (1.28V) for both synthesizer and TX/RX block; Connect to RFLDO_O pin
45	I/O	RTX	RF RTX path
46	I/O	P0_2	IO pin, default pull-high input
47	I	P2_0	IO pin, default pull-high input System Configuration, H: Application L: Baseband(IBDK Mode)

Pin No.	Pin type	Name	Description
48	I/O	P2_7	IO pin, default pull-high input
49	I/O	P3_0	IO pin, default pull-high input
50	I/O	TFS0	I²S interface: ADC Left/Right Clock
51	I/O	P0_5	IO pin, default pull-high input
52	P	VDD_IO	I/O power supply input (2.7~3.3V); Connect to LDO31_VO pin
53	I/O	DR0	I²S interface: DAC Digital Left/Right Data
54	I/O	RFS0	I²S interface: DAC Left/Right Clock
55	I/O	SCLK0	I²S interface: Bit Clock
56	I/O	DT0	I²S interface: ADC Digital Left/Right Data
57	P	EP	Exposed pad as ground

* I: signal input pin
* O: signal output pin
* I/O: signal input/output pin
* P: power pin

Note 1: These button or functions can be setup by "IS20XXS_UI" tool.

TABLE 3-4: IS2025S PIN DESCRIPTION

Pin No.	Pin type	Name	Description
1	P	VDDAO	Positive power supply dedicated to CODEC output amplifiers; Connect to CODEC_VO pin
2	O	AOHPM	Headphone common mode output/sense input.
3	O	AOHPL	L-channel analog headphone output
4	P	VDDA	Positive power supply/reference voltage for CODEC; Connect to CODEC_VO pin
5	P	VCOM	Internal biasing voltage for CODEC
6	I	MICN2	Mic 2 mono differential analog negative input
7	I	MICP2	Mic 2 mono differential analog positive input
8	I	MICN1	Mic 1 mono differential analog negative input
9	I	MICP1	Mic 1 mono differential analog positive input
10	P	MIC_BIAS	Electric microphone biasing voltage

Pin No.	Pin type	Name	Description
11	I	AIR	R-channel single-ended analog inputs
12	I	AIL	L-channel single-ended analog inputs
13	P	VDD_CORE	Core 1.2V power input; Connect to CLDO_O pin
14	O	P1_2	IO pin, default pull-high input EEPROM clock SCL
15	I/O	P1_3	IO pin, default pull-high input EEPROM data SDA

Pin No.	Pin type	Name	Description
16	I	RST_N	System Reset Pin, active when rising edge.
17	P	VDD_IO	I/O power supply input (2.7~3.3V); Connect to LDO31_VO pin
18	I/O	P0_1	IO pin, default pull-high input (Note 1) 1. FWD key when class 2 RF, active low. 2. Class1 TX Control signal of external RF T/R switch, active high.
19	I	P2_4	IO pin, default pull-high input System Configuration, L: Boot Mode with P2_0 low combination
20	I/O	P0_4	IO pin, default pull-high input. (Note 1) 1. NFC detection pin, active low. 2. Out_Ind_0
21	I/O	P1_5	IO pin, default pull-high input (Note 1) 1. NFC detection pin, active low. 2. Out_Ind_0 3. Slide Switch Detector, active low. 4. Buzzer Signal Output
22	I	HCI_RXD	HCI-UART RX data
23	O	HCI_TXD	HCI-UART TX data
24	I	TEST_EN	Scan chain test enable pin, active high.
25	P	CODEC_VO	3.1V LDO output for CODEC power
26	P	LDO31_VIN	3.1V LDO input; Connect to SYS_PWR pin
27	P	LDO31_VO	3.1V LDO output
28	P	ADAP_IN	5V power adaptor input
29	P	BAT_IN	3.3~4.2V Li-Ion battery input
30	-	NC	No Connection
31	P	SAR_VDD	SAR 1.8V input; Connect to BK_O pin
32	P	SYS_PWR	Power Output which come from BAT_IN or ADAP_IN
33	P	BK_VDD	1.8V buck VDD Power Input; Connect to SYS_PWR pin
34	P	BK_LX	1.8V buck pin for switch
35	P	BK_O	1.8V buck feedback input
36	I	PWR	Multi-Function Push Button and power on key
37	-	NC	No Connection

Pin No.	Pin type	Name	Description
38	I	LED2	LED Driver 2
39	I	LED1	LED Driver 1
40	I/O	P3_5	IO pin, default pull-high input
41	I/O	P0_0	IO pin, default pull-high input (Note 1) 1. Slide Switch Detector, active low. 2. UART TX_IND, active low.
42	I/O	P0_3	IO pin, default pull-high input (Note 1) 1. REV key (default), active low. 2. Buzzer Signal Output 3. Out_Ind_1 4. Class1 RX Control signal of external RF T/R switch, active high.

Pin No.	Pin type	Name	Description
43	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash
44	P	CLDO_O	1.2V core LDO output
45	P	PMIC_IN	PMU blocks power input.
46	P	RFLDO_O	1.28V RF LDO output
47	P	VBG	Bandgap output reference for decoupling interference
48	P	ULPC_VSUS	ULPC 1.2V output power, maximum loading 1mA.
49	-	NC	No Connection.
50	I	XO_N	16MHz Crystal input negative
51	I	XO_P	16MHz Crystal input positive
52	P	VCC_RF	RF power input for both synthesizer and TX/RX block
53	I/O	RTX	RF RTX path
54	I/O	P0_2	GPIO, default pull-high input (Note 1) Play/Pause key as the default setting
55	I/O	P2_0	GPIO, default pull-high input (Note 1) 1. KEY PIN for FT Test 2. System Configuration, H: Application L: Baseband(IBDK Mode) 3. Buzzer Signal Output
56	I/O	P2_7	GPIO, default pull-high input (Note 1) Volume up key (default)
57	I/O	P3_0	GPIO, default pull-high input (Note 1) Line-in Detector
58	I/O	P0_5	GPIO, default pull-high input (Note 1) Volume down (default)
59	P	VDD_IO	I/O power supply input
60	P	PVDD2_CDA	Supply voltage of power stage ch-2 .
61	O	HPOP2_CDA	Positive BTL output of channel-2
62	O	HPON2_CDA	Negative BTL output of channel-2
63	P	AVDD_CDA	Supply voltage of audio amplifier.
64	P	VBP_CDA	Reference voltage output.
65	O	HPON_CDA	Negative BTL output of channel-1

Pin No.	Pin type	Name	Description
66	O	HPOP_CDA	Positive BTL output of channel-1
67	P	PVDD_CDA	Supply voltage of power stage ch-1
68	O	AOHPR	R-channel analog headphone output
69	P	EP	Exposed pad as ground

* I: signal input pin
* O: signal output pin
* I/O: signal input/output pin
* P: power pin

Note 1: These button or functions can be setup by "IS20XXS_UI" tool.

3.2 POWER SUPPLY

The device is powered via BAT pin input. If a battery is not connected, an external power supply needs to provide to this input. Figure 3-1 shows the PCB connections from BAT pin to other voltage supply pins of the chip.

FIGURE 3-1: POWER TREE DIAGRAM
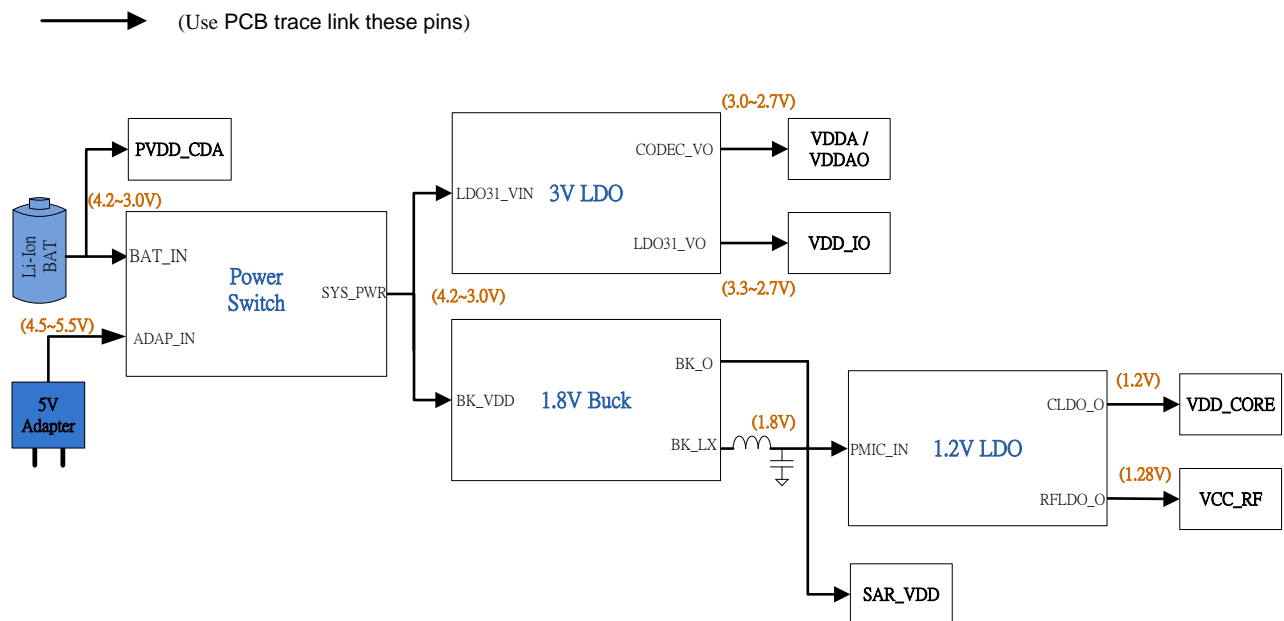
4.0 TRANSCEIVER

The stereo audio chip is designed and optimized for Bluetooth 2.4 GHz system. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock for synchronize with another device.

4.1 TRANSMITTER

The internal PA has a maximum output power of +4dBm with 20dB power level control. This is applied into Class2/3 radios without external RF PA.

The transmitter directly performs IQ conversion to minimize the frequency drift, and it can excess 20dB power range with temperature compensation mechanism.

4.2 RECEVIER

The LNA operates with TR-combined mode for single port application. It can save a pin on package and without an external TX/RX switch.

The ADC is utilized to sample the input analog wave and convert into digital signal for de-modulator analysis. A channel filter has been integrated into receiver channel before the ADC, which to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject image frequency for low-IF architecture. This filter for low-IF architecture is intent to reduce external BPF component for super heterodyne architecture.

RSSI signal is feedback to the processor to control the RF output power to make a good tradeoff for effective distance and current consumption.

4.3 SYNTHESIZER

A synthesizer generates a clock for radio transceiver operation. There is a VCO inside with tunable internal LC tank. It can reduce variation for components. A crystal oscillation with internal digital trimming circuit provides a stable clock for synthesizer.

4.4 MODEM

For Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v2.0 with EDR specification.

For Bluetooth v2.0 with EDR specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v2.0 with EDR specification. For the viewpoint of baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8DPSK.

4.5 AFH (Adaptive Frequency Hopping)

Stereo audio chip have AFH function to avoid RF interference. It has an algorithm to check the interference nearby and choice clear channel to transceiver Bluetooth signal.

5.0 MICROPROCESSOR

A single-cycle 8-bit MCU is built into the stereo audio chip to execute the Bluetooth protocols. It operates from 16MHz to higher frequency where the firmware can dynamically adjust the tradeoff between the computing power and the power consumption. The MCU firmware is hard-wired in ROM to minimize the firmware execution power consumption and to save the external flash cost.

5.1 MEMORY

A synchronous single port RAM interface is used. There are sufficient ROM and RAM to fulfill the requirement of processor. A register bank, a dedicated single port memory and a flash memory are connected to the processor bus. The processor coordinates all the link control procedures and data movement using a set of pointers registers.

5.2 EXTERNAL RESET

The chip provides a watchdog timer to reset the chip. It has an integrated Power-On Reset (POR) circuit that resets all circuits to a known power-on state. This action can also be driven by an external reset signal that can be used to externally control the device, forcing it into a power-on reset state. The RST signal input is active low and no connection is required in most applications.

5.3 REFERENCE CLOCK

Stereo audio chip is composed of an integrated crystal oscillation function. It uses a 16 MHz external crystal and two specified loading capacitors to provide a high quality system reference timer source. This feature is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent loading capacitance in mass production. Frequency trim is achieved by adjusting the crystal loading capacitance through the on-chip trim capacitors Ctrim..

The value of trimming capacitance is around 200fF (200×10^{-15} F) per LSB at 5 bits word, therefore the overall adjustable clock frequency is around 40 KHz.

FIGURE 5-1: CRYSTAL CONNECTION
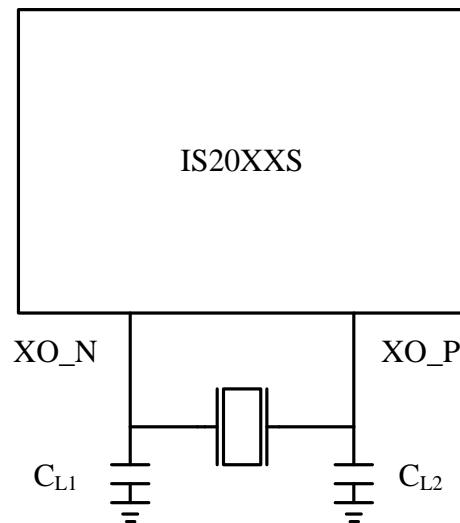
C_{trim} =200fF * (1~31) ; $C_{int} \approx$ 3pF

$C_L = [(C_{L1} * C_{L2})/(C_{L1} + C_{L2})] + (C_{trim}/2) + C_{int}$
(e.g. Set trim value as 16, then C_{trim}= 3.2pF.
For a 16M Hz crystal which C_L=9pF, we can get $C_{L1} = C_{L2}$ = 9.1pF in this case.)

For C_L selection, please refer to the datasheet of crystal vendor

6.0 AUDIO

There are a few stages for input audio and output audio. Each stage can be programmed to vary the gain response characteristics. For microphone input, both single-end input and differential input are supported. One of the important points in maintaining a high quality signal is to provide a stable bias voltage source to the condenser microphone's FET. DC blocking capacitors may be used at both positive and negative sides of input. Internally, this analog signal is converted to 16-bit 8 kHz linear PCM data.

6.1 DIGITAL SIGNAL PROCESSOR

A digital signal processor (DSP) cooperates with MCU to perform digital audio processing with some advanced features such as noise cancellation, audio output level suppression and etc. It provides audio processing with some advanced features. The DSP cancels the acoustic echo that may present in headset or speaker. All the audio processing is performed by the DSP with low power consumption. This technique effectively cancels the incoming echo signal without impact to the desired voice signal. An outgoing signal to the speaker which level exceeds the threshold (and therefore deemed likely to create echo) will be result in suppression of the signal along the input path from the microphone. Filtering is also applied to provide a smoother transition for more natural user experience.

FIGURE 6-1: BLOCK DIAGRAM OF DSP

(a)

(b)
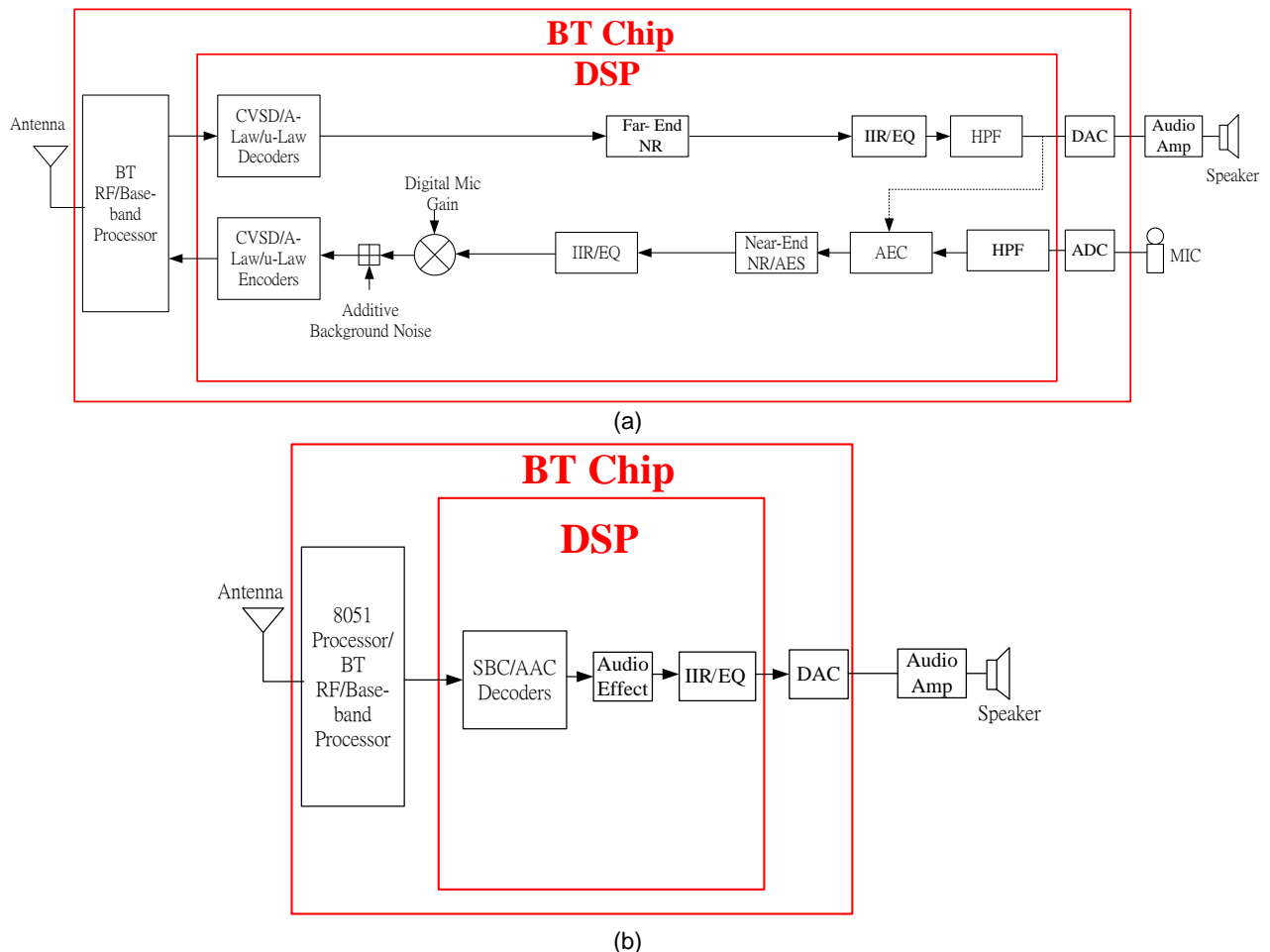
Processing flow of speakerphone applications for (a) speech and (b) audio signal processing.

There is a "DSPTool_IS20XX" can support user to set up these DSP parameter. For more detail information, please reference "BT5502_DSP_APP" document.

6.2 CLASS-D AUDIO AMPLIFIER

The class D amplifier has significant advantage in many applications because of its lower power dissipation which produces less heat. IS2025S chip has built-in a class D amplifier that reduces circuit board space and system cost. The efficiency of the amplifier extends the battery life in portable systems.

The class D amplifier is implemented by using a full-bridge output stage. A full bridge uses two half-bridge stages to drive the load differentially. It provides a good signal to noise ratio (SNR) and enough drive capability for a 4 Ohm speaker driver.

6.3 CODEC

The built-in codec has a high Signal to Noise ratio performance. This built-in codec consist of an analog to digital converter (ADC), a digital to analog converter (DAC) and additional analog circuitry.

6.4 LINE IN (Aux In)

The chip supports one analog line in from external audio source. The analog line in signal can be processed by the DSP to generate different sound effect (Multi-band Dynamic Range Compression, Audio Widening). The sound effect can be set up by DSP tool.

7.0 POWER MANAGEMENT UNIT

The on-chip Power management Unit (PMU) has two main feature; Lithium Ion battery charging and voltage regulation. A power switch is used to switch over the power source between battery and adaptor automatically. The PMU also provides driving current for 2 LEDs.

7.1 CHARGING A BATTERY

Stereo audio chip has a built-in battery charger which is optimized for lithium polymer batteries. The charger includes a current sensor for charging control, user programmable current regulation and high accuracy voltage regulation.

The charging current parameters are configured by "IS20XXS_UI" tool. Whenever the adaptor is plug-in, the charging circuit will be activated. Reviving, Pre-charging, Constant Current and Constant Voltage modes are implemented and re-charging function is also included. The maximum charging current is 350mA.

FIGURE 7-1: CHARGING CURVE
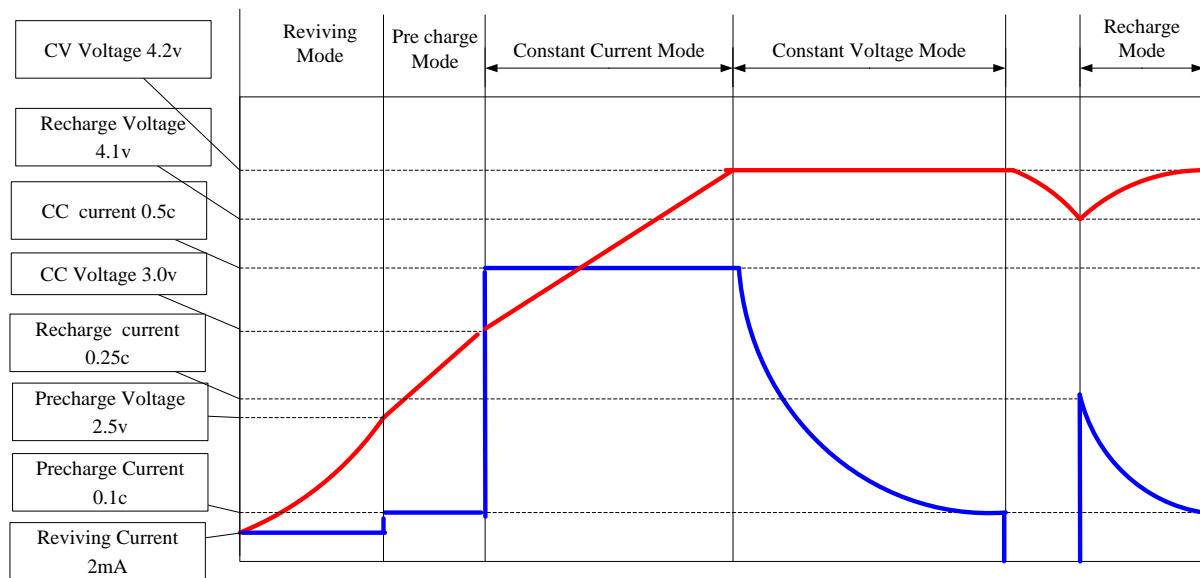
7.2 VOLTAGE MONITORING

A 10-bit Successive-Approximation-Register analog to digital converter (SAR ADC) provides one dedicated channel for battery voltage level detection. The warning level is programmable by "IS20XXS_UI" tool. This ADC provides a good resolution that MCU can control the charging process.

7.3 LDO

The built-in LDO is used to convert the battery or adaptor power for power supply. It also integrates hardware architecture to control power on/off procedure. The built-in programmable LDOs provide power for codec and digital IO pads. It is used to buffer the high input voltage from battery or adapter. This LDO needs 1uF bypass capacitor.

7.4 SWITCHING REGULATOR

The built-in programmable output voltage regulator can convert battery voltage for RF and baseband core power supply. This converter has high conversion efficiency and fast transient response.

7.5 LED DRIVER

There are two dedicate LED drivers to control the LEDs. They provide enough sink current (16 step control and 0.35mA for each step) that LED can be connected directly with IS20XXS. LED setting can be set up by "IS20XXS_UI" tool.
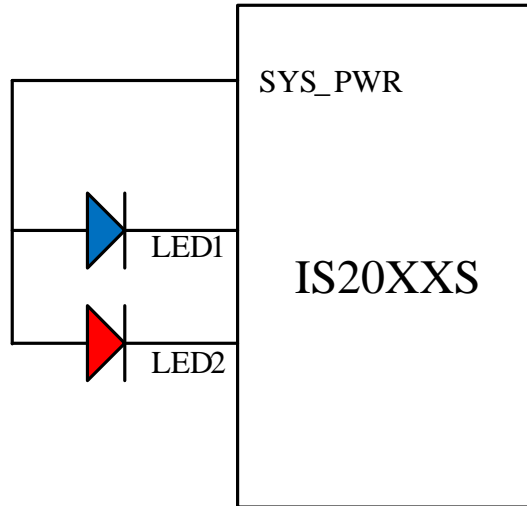
8.0 GENERAL PURPOSE IOs

Stereo audio chip provides six IOs for key functions. The corresponding key functions can be set up by "IS20XXS_UI" tool. The first button (Button 0) must be power key. The power on/off functions only can be set on PWR pin. There are four different operations (short click, long click, double click and combinations) for every button can be defined as different functions. All these function can be set up by "IS20XXS_UI" tool.

IO Pin for Buttons

Button Name	Default Functions	IO pin name
Button 0	Power / MFB	PWR
Button 1	PLAY/PAUSE	P0_2
Button 2	Volume UP	P2_7
Button 3	Volume DOWN	P0_5
Button 4	FWD	P0_1
Button 5	REV	P0_3

Note: All these function can be set up by "IS20XXS_UI" tool.

Some signals were generated to indicate or control outside devices. The most popular applications are NFC for easy pairing, external audio amplifier for louder speaker and buzzer for indication.

IOs pin for added functions

Functions	IO configurable features
Slide switch	P0_0 / P1_5
Buzzer	P0_3
NFC detect	P0_4 / P1_5
External AMP enable	P1_5

Note: All these function can be set up by "IS20XXS_UI" tool.

9.0 OPERATION WITH EXTERNAL MCU

IS20XXS support UART command set to make an external MCU to control IS20XXS chip. Here is the connection interface between IS20XXS and MCU.

FIGURE 9-1: INTERFACE BETWEEN MCU AND IS20XX CHIP
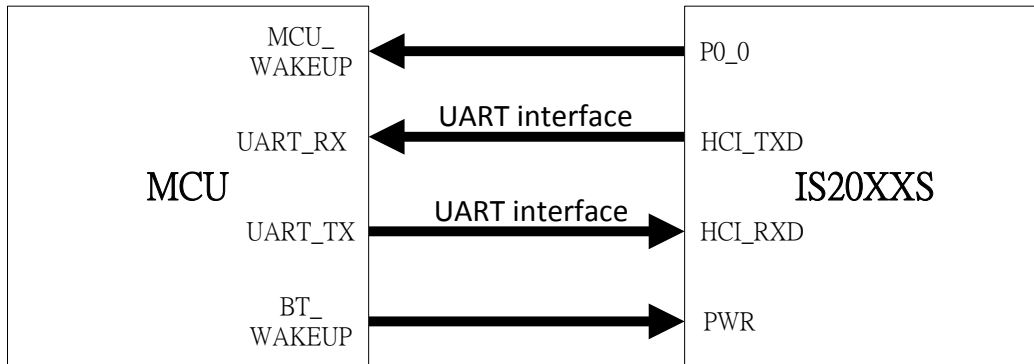
MCU can control IS20XXS chip by UART interface and wakeup IS20XXS by PWR pin. IS20XXS provide wakeup MCU function by connect to P0_0 pin of IS20XX.

"UART_CommandSet_v154" document provide all UART command which IS20XX support and "IS20XXS_UI" tool will help you to set up your system support UART command.

For more detail description, please reference "UART_CommandSet_v154" document and "IS20XXS_UI" tool.

9.1 TIMING SEQUENCE OF UART APPLICATION
FIGURE 9-2: POWER ON/OFF SEQUENCE
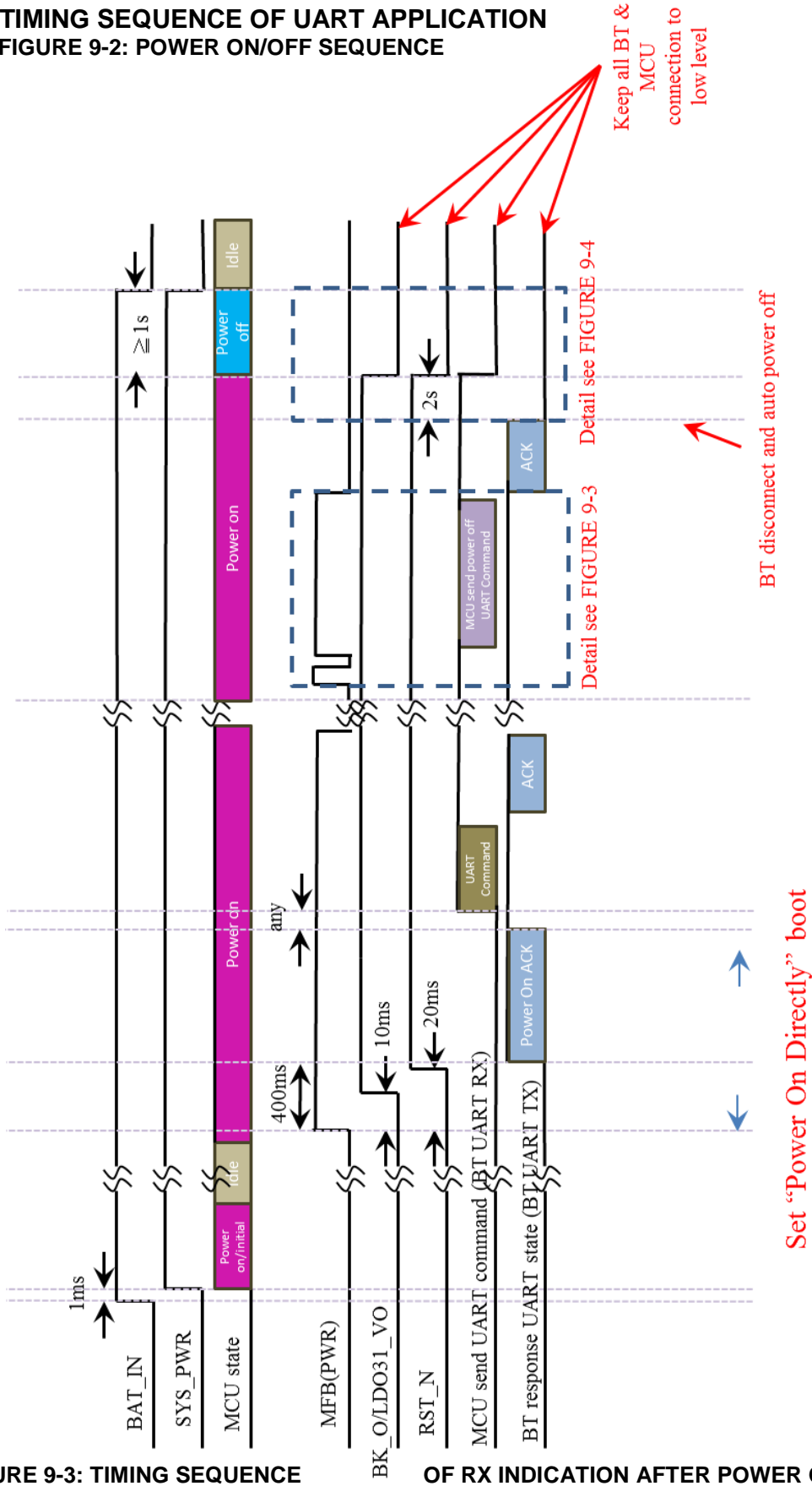
FIGURE 9-3: TIMING SEQUENCE OF RX INDICATION AFTER POWER ON

Resume 32KHz mode

MFB pulse must longer than
UART command slot time

MFB(PWR)

150ms

MCU send UART
command

UART
Command

2ms   2ms

To save power, we will
enter 32KHz mode

1ms
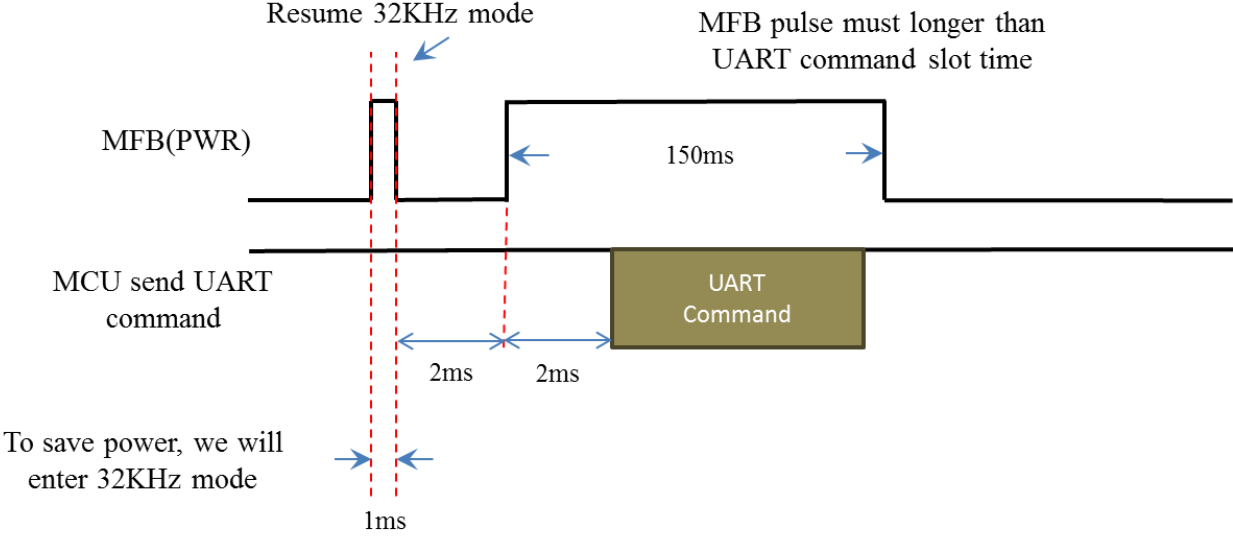
FIGURE 9-4: TIMING SEQUENCE OF POWER OFF

BT send power off ACK

BAT_IN +4V

MFB(PWR)

MCU send RST_N

BK_O

LDO31_VO

UART bus

2s   1s
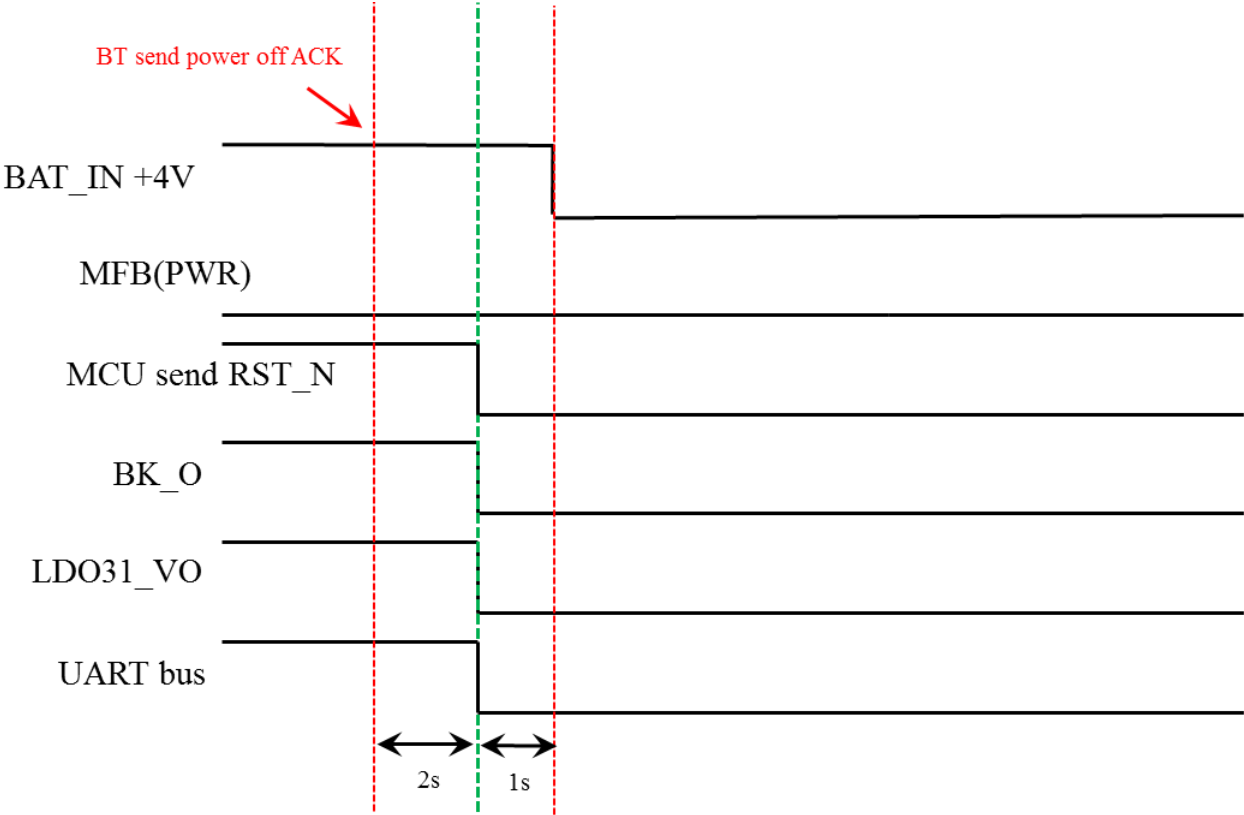
EEPROM clock= 100KHz
For a byte write, 0.01ms*32clock*2= 640us
If power drop faster than 640us, some issue may occurs, but the possibility is low

FIGURE 9-5: TIMING SEQUENCE OF POWER ON (NACK)
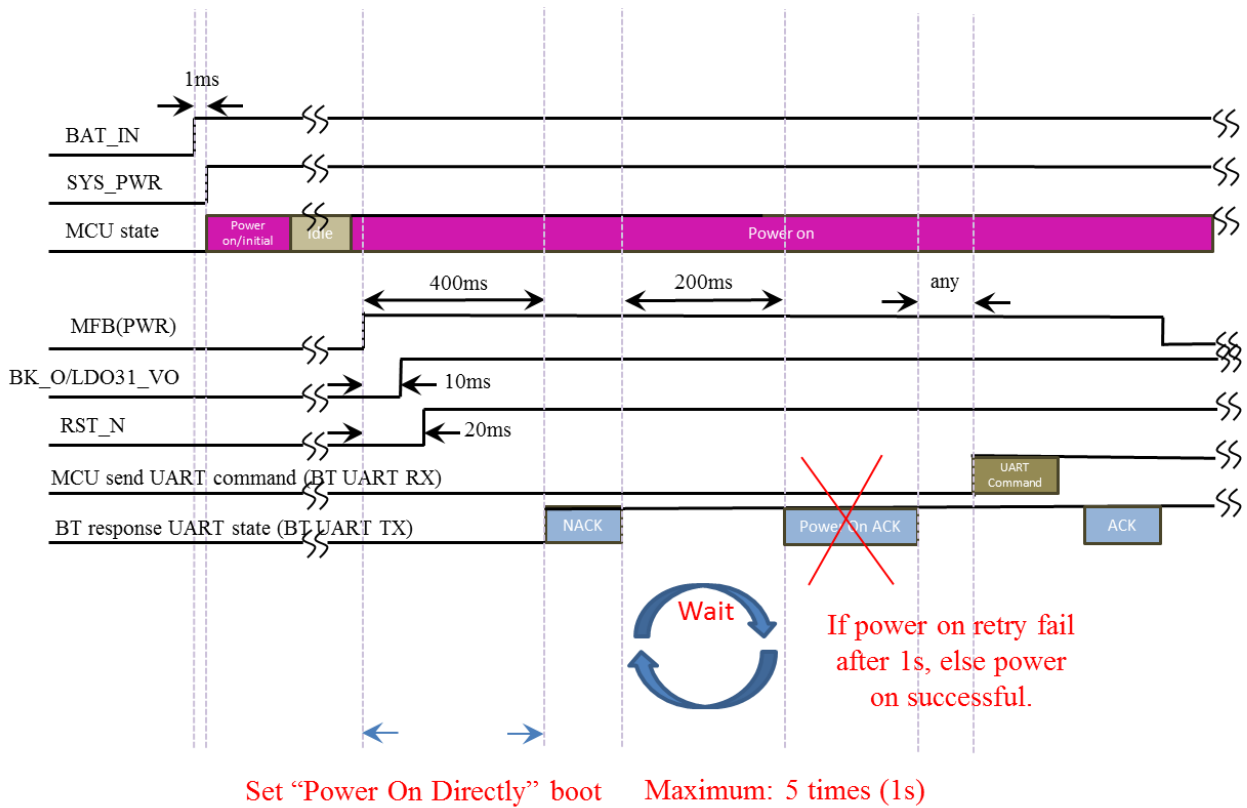
FIGURE 9-6: RESET TIMING SEQUENCE IF MODULE HANGS UP
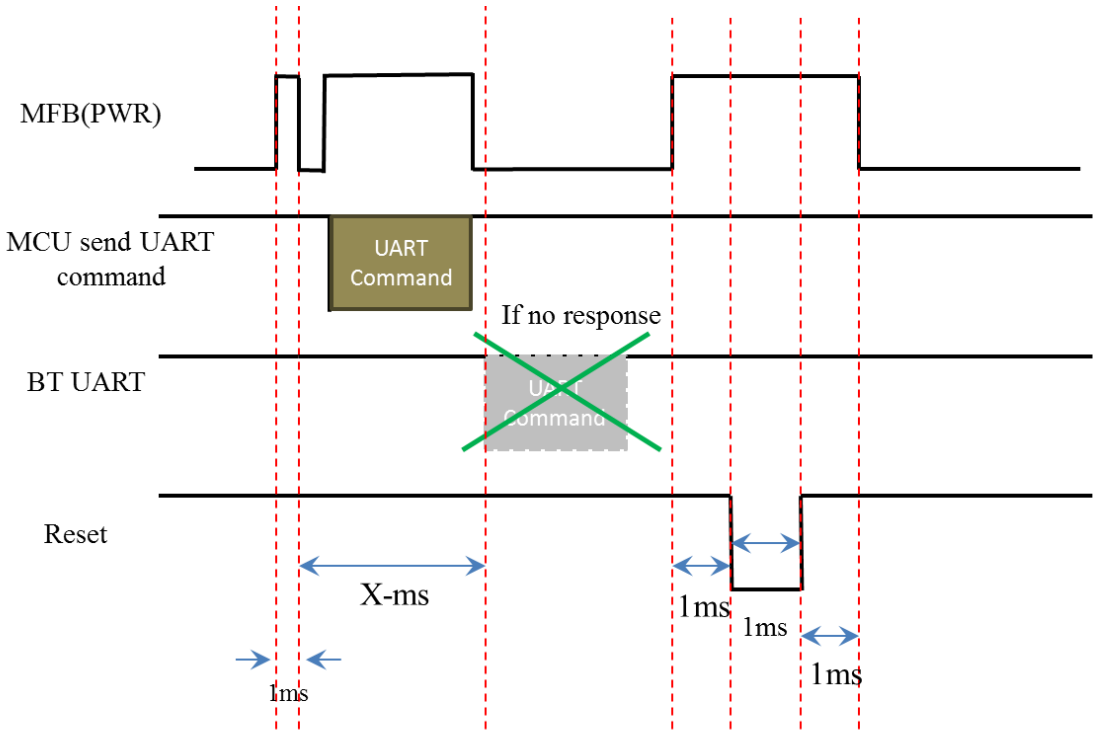
If MCU send UART command, but BT does not response within X-ms,
MCU will send a reset signal to BT to do hardware reset

FIGURE 9-7: TIMING SEQUENCE OF POWER DROP PROTECTION
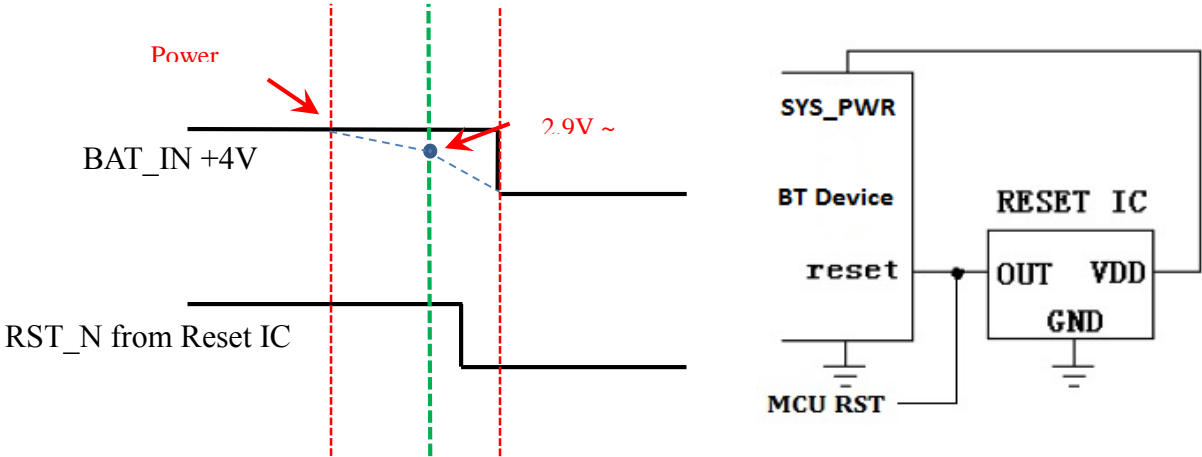
If BT's BAT use adaptor translates voltage by LDO, we recommend use "Reset IC" to avoid power off suddenly. Rest IC spec output pin must be "Open Drain" 、delay time ≦ 10ms
Recommend part: TCM809SVNB713 or G691L263T73

10.0 I²S APPLICATION

IS2023S support I²S digital audio signal output. It provide 8k Hz, 44.1k Hz and 48k Hz sampling rate; it also support 16 bits and 24bits data format. The I²S setting can be set up by "IS20XXS_UI" tool and DSP tool.
.
The I²S signal connection between IS2023S and external DSP as below:

FIGURE 10-1: MASTER MODE REFERENCE CONNECTION
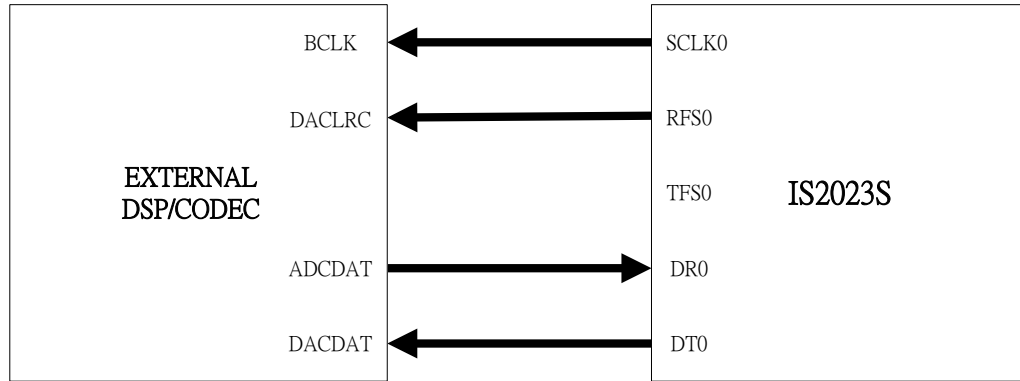
FIGURE 10-2: SLAVE MODE REFERENCE CONNECTION
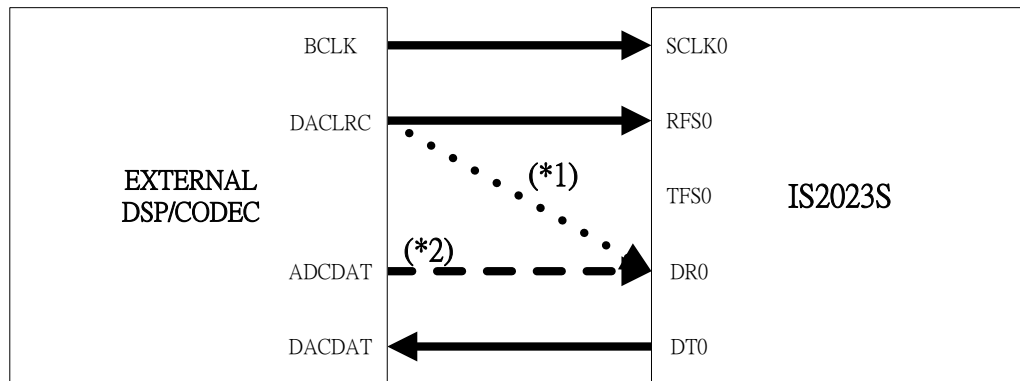
Note 1: For 002 version chip or module, system should connect line 1 in slave mode figure.
And, system not support ADC signal from external DSP/CODEC.
Note 2: For other version chip or module, system should connect line 2 in slave mode figure.

About "Mast" or "Slave" mode setting, you can use "DSP Configuration Tool" to set up system.

10.1 CLOCK AND DATA TIMING SEQUENCE

FIGURE 10-3: TIMING FOR I^{2}S MODES (both master and slave)
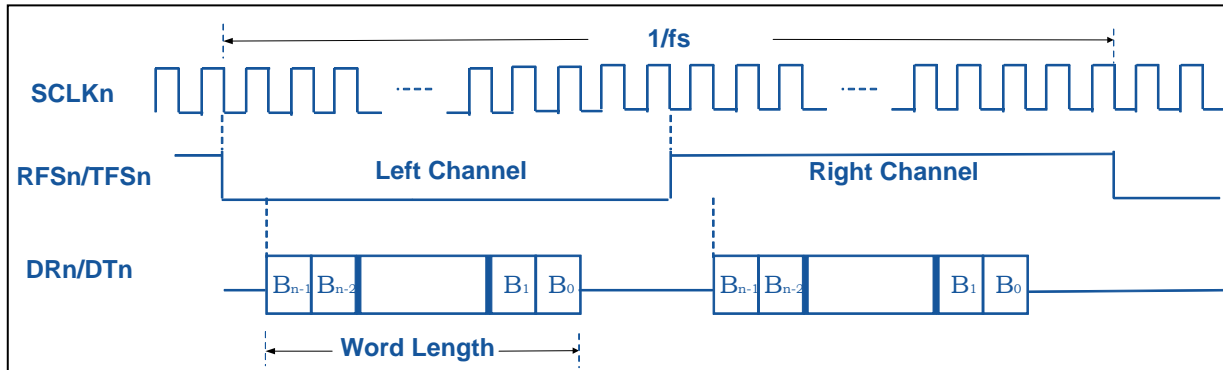
FIGURE 10-4: TIMING FOR PCM MODES (both master and slave)
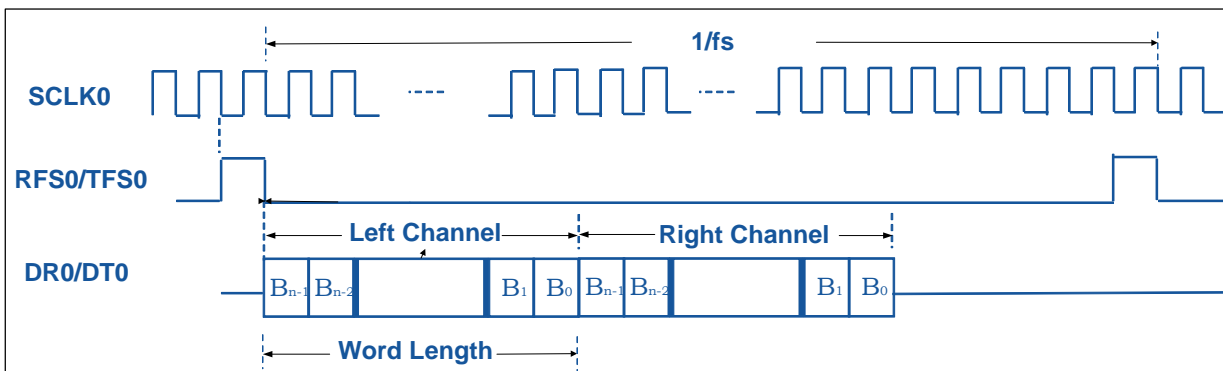
11.0 ANTENNA PLACEMENT RULE

For Bluetooth product, antenna placement will affect whole system performance.
Antenna need free space to transmit RF signal, it can't be surround by GND plane.

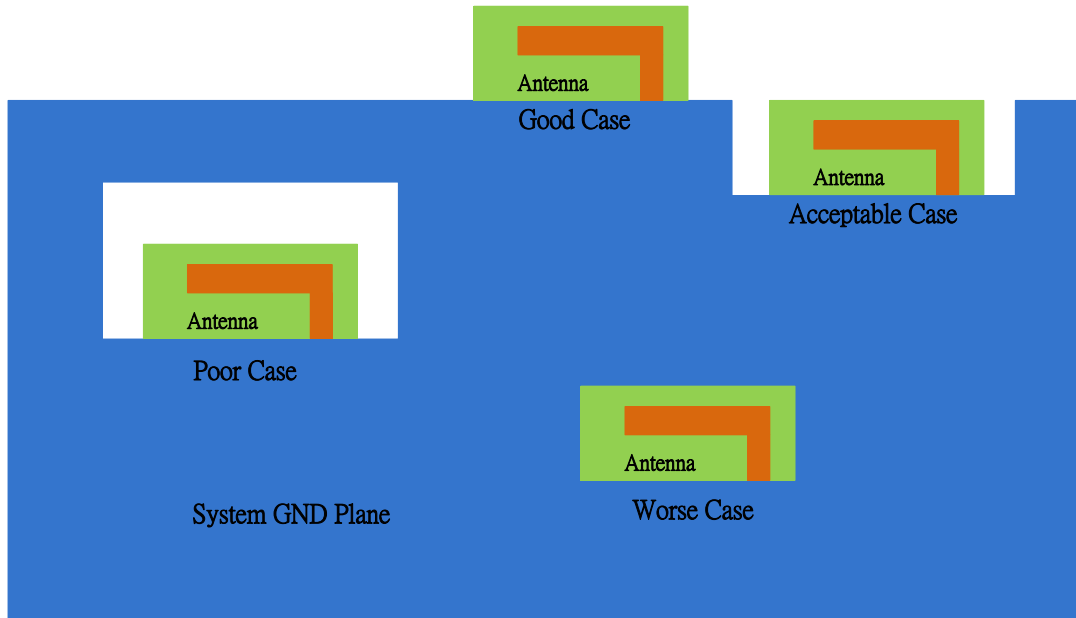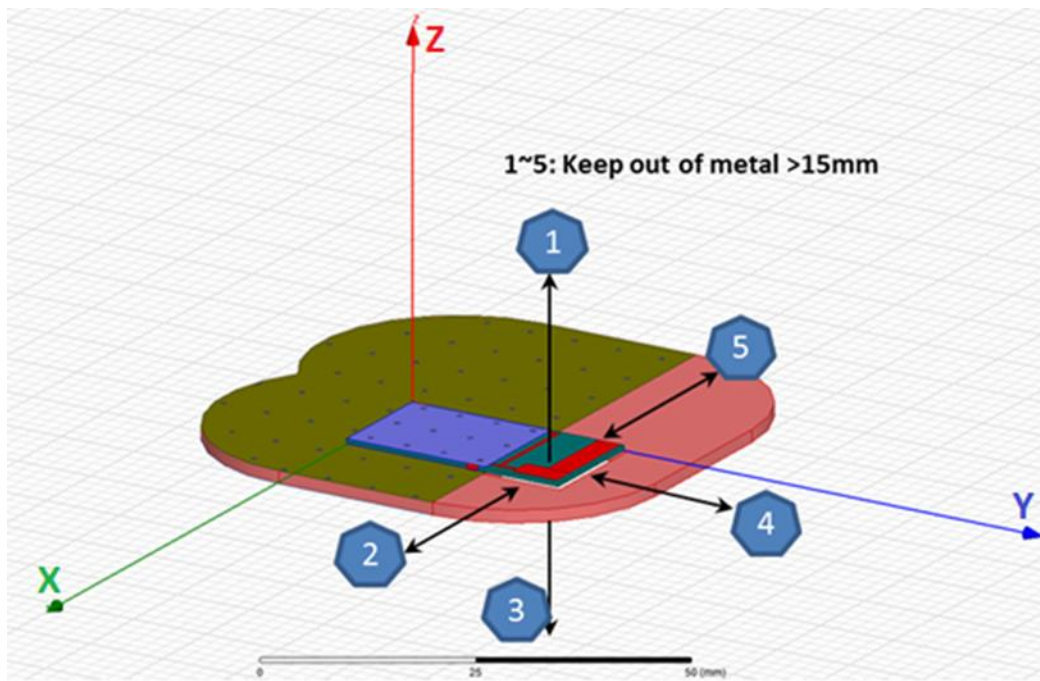Here are some examples of good and poor placement on a Main Application board with GND plane.

FIGURE 11-1: ANTENNA PLACEMENT EXAMPLES

FIGURE 11-2: KEEP OUT AREA SUGGESTION FOR ANTENNA

For more detail free space of antenna placement design, you can reference the design rule of antenna produce vendor.

12.0 SPECIFICATIONS

Table 12-1: ABSOLUTE MAXIMUM SPECIFICATION

Symbol	Parameter	Min	Max	Unit
VDD_CORE	Digital core supply voltage	0	1.35	V
VCC_RF	RF supply voltage	0	1.35	V
SAR_VDD	SAR ADC supply voltage	0	2.1	V
VDDA/VDDAO	CODEC supply voltage	0	3.3	V
VDD_IO	I/O supply voltage	0	3.6	V
BK_VDD	BUCK supply voltage	0	4.3	V
LDO31_VIN	Supply voltage	0	4.3	V
BAT_IN	Input voltage for battery	0	4.3	V
ADAP_IN	Input voltage for adaptor	0	7.0	V
T_{STORE}	Storage temperature	-65	+150	ºC
$T_{OPERATION}$	Operation temperature	-20	+70	ºC

Table 12-2: RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Typical	Max	Unit
VDD_CORE	Digital core supply voltage	1.14	1.2	1.26	V
VCC_RF	RF supply voltage	1.22	1.28	1.34	V
SAR_VDD	SAR ADC supply voltage	1.62	1.8	1.98	V
VDDA/VDDAO	CODEC supply voltage	2.7	2.8	3.0	V
VDD_IO	I/O supply voltage	2.7	3.0	3.3	V
BK_VDD	BUCK supply voltage	3	3.7	4.25	V
LDO31_VIN	Supply voltage	3	3.7	4.25	V
BAT_IN	Input voltage for battery	3	3.7	4.25	V
ADAP_IN	Input voltage for adaptor	4.5	5	5.5	V
$T_{OPERATION}$	Operation temperature	-20	+25	+70	ºC

Note:
All these supply voltage are programmable by EEPROM parameters.

Table 12-3: BUCK SWITCHING REGULATOR

Parameter	Min	Typical	Max	Unit
Input Voltage	3.0	3.7	4.25	V
Output Voltage (I_{load}=70mA, Vin=4V)	1.7	1.8	2.05	V
Output Voltage Accuracy		±5		%
Output Voltage Adjustable Step		50		mV /Step
Output Adjustment Range	-0.1		+0.25	V
Average Load Current (I_{LOAD})	120			mA
Conversion efficiency (BAT=3.8V, I_{load} = 50mA)		88		%
Quiescent Current (PFM)			40	μA
Output Current (peak)	200			mA
Shutdown Current			<1	μA

Note:
(1) Test condition: SAR_VDD=1.8V, temperature=25 ºC.
 (2) These parameters are characterized but not tested in manufacturing.

Table 12-4: LOW DROP REGULATOR

Parameter		Min	Typical	Max	Unit
Input Voltage		3.0	3.7	4.25	V
Output Voltage	$V_{OUT\ CODEC}$		2.8		V
	$V_{OUT\ IO}$		2.8		
Output Accuracy (V_{IN}=3.7V, I_{LOAD}=100mA, 27'C)			±5		%
Output current (average)				100	mA
Drop-out voltage (I_{load} = maximum output current)				300	mV
Quiescent Current (excluding load, I_{load} < 1mA)			45		μA
Shutdown Current				<1	μA

Note:
(1) Test condition: SAR_VDD=1.8V, temperature=25 ºC.
(2) These parameters are characterized but not tested in manufacturing.

Table 12-5: BATTERY CHARGER

Parameter		Min	Typical	Max	Unit
Input Voltage		4.5	5.0	5.5	V
Supply current to charger only			3	4.5	mA
Maximum Battery Fast Charge Current Note: ENX2=0	Headroom > 0.7V (ADAP_IN=5V)	170	200	240	mA
	Headroom = 0.3V (ADAP_IN=4.5V)	160	180	240	mA
Maximum Battery Fast Charge Current Note: ENX2=1	Headroom > 0.7V (ADAP_IN=5V)	330	350	420	mA
	Headroom = 0.3V (ADAP_IN=4.5V)	180	220	270	mA
Trickle Charge Voltage Threshold			3		V
Battery Charge Termination Current, (% of Fast Charge Current)			10		%

Note:

(1) Headroom = $V_{ADAP\_IN} - V_{BAT}$

(2) ENX2 is not allowed to be enabled when $V_{ADAP\_IN} - V_{BAT} > 2V$

(3) These parameters are characterized but not tested in manufacturing.

Table 12-6: LED DRIVER

Parameter	Min	Typical	Max	Unit
Open-drain Voltage			3.6	V
Programmable Current Range	0		5.25	mA
Intensity Control		16		step
Current Step		0.35		mA
Power Down Open-drain Current			1	μA
Shutdown Current			1	μA

Note:

(1) Test condition: SAR_VDD=1.8V, temperature=25 ºC.

(2) These parameters are characterized but not tested in manufacturing.

Table 12-7: AUDIO CODEC DIGITAL TO ANALOGUE CONVERTER

T= 25ºC, V$_{dd}$=3.0V, 1KHz sine wave input, Bandwidth = 20Hz~20KHz				
Parameter (Condition)	**Min.**	**Typ.**	**Max.**	**Unit**
Over-sampling rate		128		f_s
Resolution	16		20	Bits
Output Sample Rate	8		48	KHz
Signal to Noise Ratio Note: 1 (SNR @cap-less mode) for 48kHz		96		dB
Signal to Noise Ratio Note: 1 (SNR @single-end mode) for 48kHz		98		dB
Digital Gain	-54		4.85	dB
Digital Gain Resolution		2~6		dB
Analog Gain	-28		3	dB
Analog Gain Resolution		1		dB
Output Voltage Full-scale Swing (AVDD=2.8V)	495	742.5		mV rms
Maximum Output Power (16Ω load)		34.5		mW
Maximum Output Power (32Ω load)		17.2		mW
Allowed Load — Resistive	8	16	O.C.	Ω
Allowed Load — Capacitive			500	pF
THD+N (16Ω load)			0.05	%
Signal to Noise Ratio (SNR @ 16Ω load)			96	dB

Note:
(1) f$_{in}$=1KHz, B/W=20~20KHz, A-weighted, THD+N < 0.01%, 0dBFS signal, Load=100KΩ
(2) These parameters are characterized but not tested in manufacturing.

Table 12-8: AUDIO CODEC ANALOGUE TO DIGITAL CONVERTER

T= 25ºC, V_{dd}=3.0V, 1KHz sine wave input, Bandwidth = 20Hz~20KHz				
Parameter (Condition)	**Min.**	**Typ.**	**Max.**	**Unit**
Resolution			16	Bits
Output Sample Rate	8		48	KHz
Signal to Noise Ratio **Note: 1** (SNR @MIC or Line-in mode)		90		dB
Digital Gain	-54		4.85	dB
Digital Gain Resolution		2~6		dB
MIC Boost Gain		20		dB
Analog Gain			60	dB
Analog Gain Resolution		2.0		dB
Input full-scale at maximum gain (differential)		4		mV rms
Input full-scale at minimum gain (differential)		800		mV rms
3dB bandwidth		20		KHz
Microphone mode (input impedance)		24		KΩ
THD+N (microphone input) @30mVrms input		0.02		%

Note:

(1) f_{in}=1KHz, B/W=20~20KHz, A-weighted, THD+N < 1%, 150mV_{pp} input

(2) These parameters are characterized but not tested in manufacturing.

Table 12-9: DUAL-CHANNEL CLASS-D AMPLIFIER

Parameter (Condition)		Min.	Typ.	Max.	Unit
Standalone SNR (A-weighting)			100		dB
Gain			12		dB
PSRR (217Hz, 200mV on PVDD)			70		dB
Efficiency	4ohm	80		85	%
	8ohm	85		90	%
Supply Voltage		3.0	3.7	4.5	V
Load			4		ohm
Quiescent current (1 channel)			2		mA
Sample frequency			250		KHz
Over current limits			2.3		A
Shutdown current			1.0		uA

Note:
(1) Test condition: PVDD_CDA=4.2V, temperature=25 ºC.
(2) These parameters are characterized but not tested in manufacturing.

Table 12-10: SYSTEM CURRENT CONSUMPTION

System Status	Typ.	Max.	Unit
System Off Mode	2	5	uA
Standby Mode	0.8		mA
Linked Mode	0.4		mA
SCO Link	7.8		mA
A2DP Link (V_{p-p}=200mV; 1k tone signal)	10.7		mA

Note: Use IS2020 EVB as test platform.
Test condition: BAT_IN= 3.8V, link with HTC EYE cell phone; distance between cell phone and EVB: 30cm.

Table 12-11: SYSTEM CURRENT CONSUMPTION OF DIGITAL AUDIO OUTPUT(I²S)

System Status	Typ.	Max.	Unit
System Off Mode	2	5	uA
Standby Mode	0.4		mA
Linked Mode	0.4		mA
SCO Link	9.3		mA
A2DP Link (1k tone signal)	11.7		mA

Note: Use IS2023 EVB as test platform
Test condition: BAT_IN= 3.8V, link with HTC M8 cell phone; distance between cell phone and EVB: 30cm; I²S signal link with YAMAHA YDA174 EVB

Table 12-12: TRANSMITTER SECTION FOR BDR AND EDR

Parameter	Min	Typ	Max	Bluetooth specification	Unit
Maximum RF transmit power		3.0	4.0	-6 to 4	dBm
Relative transmit power	-4	-1.2	1	-4 to 1	dB

Note:
The RF Transmit power is calibrated during production using MP Tool software and MT8852 Bluetooth Test equipment.
Test condition: VCC_RF= 1.28V, temperature=25 ºC.

Table 12-13: RECEIVER SECTION FOR BDR AND EDR

	Modulation	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.1% BER	GFSK		-90		≤-70	dBm
Sensitivity at 0.01% BER	π/4 DQPSK		-91		≤-70	dBm
	8DPSK		-82		≤-70	dBm

Note:
(1) Test condition: VCC_RF= 1.28V, temperature=25 ºC.
(2) These parameters are characterized but not tested in manufacturing.

Stereo Audio SoC

13.0 REFERENCE CIRCUIT

FIGURE 13-1: IS2020S REFERENCE CIRCUIT

IS2020S/GM reference circuit
For stereo headset

FIGURE 13-2: IS2021S REFERENCE CIRCUIT

IS2021S reference circuit
For stereo headset

POWER

TEST POINT

SLIDE SWITCH

STEREO OUTPUT

Audio

MIC1

NFC

LED

ADAPTOR PLUG IN
Reset

PLAY/PAUSE

FWD

VOL_UP

REV

VOL_DN

MFB

Stereo Audio SoC
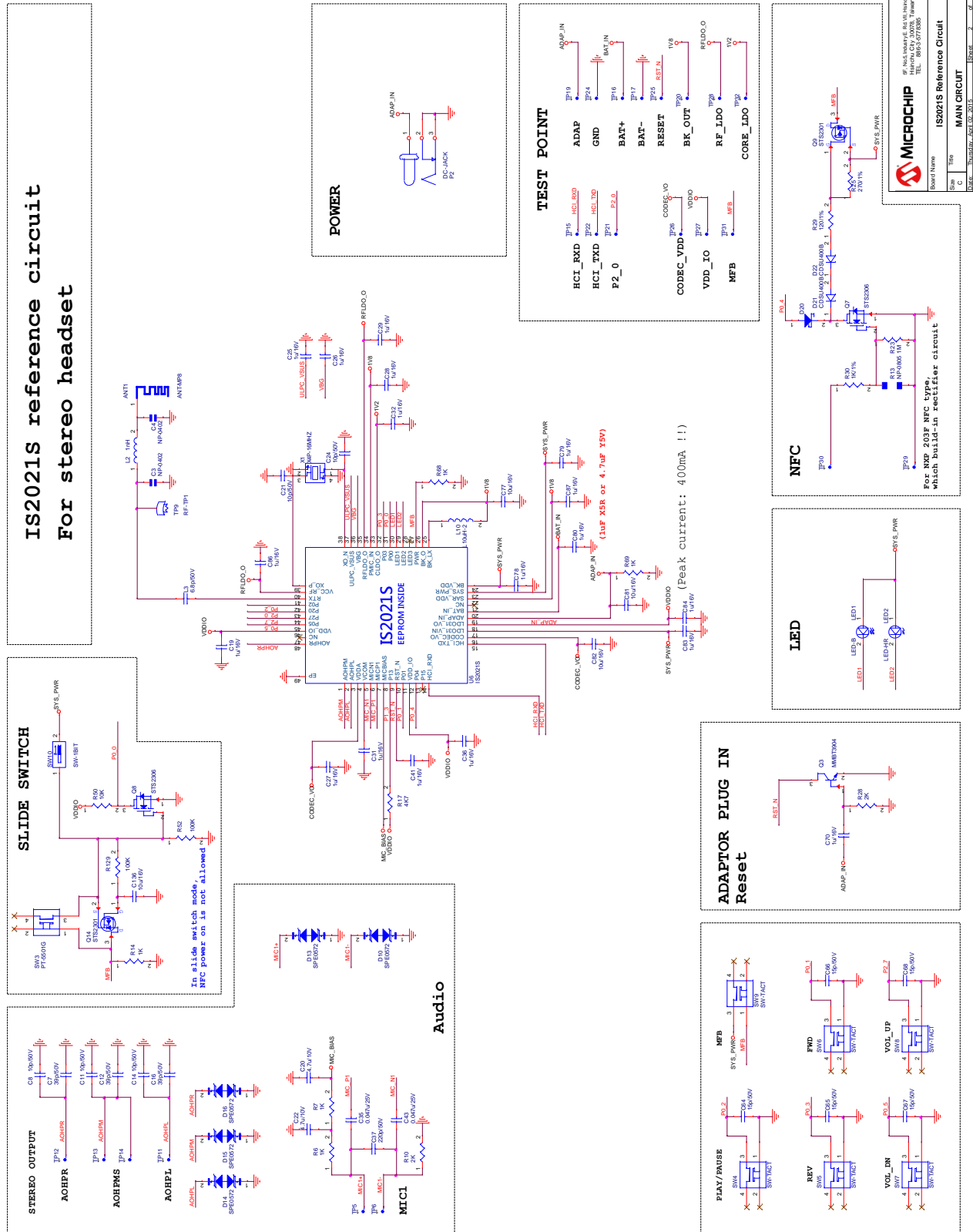
FIGURE 13-3: IS2023S REFERENCE CIRCUIT
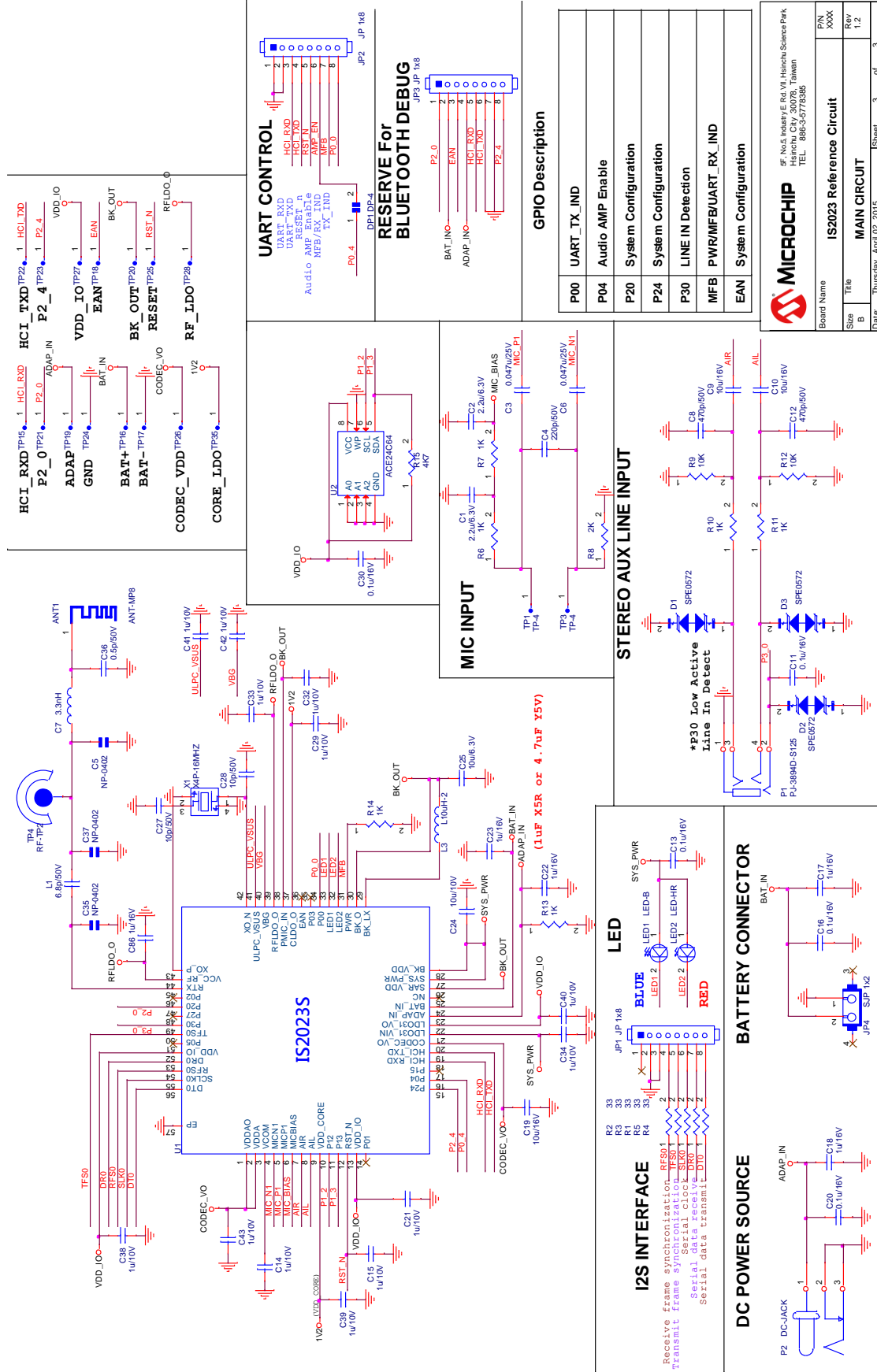
FIGURE 13-4: IS2025S REFERENCE CIRCUIT (FOR HEADSET APPLICATION)
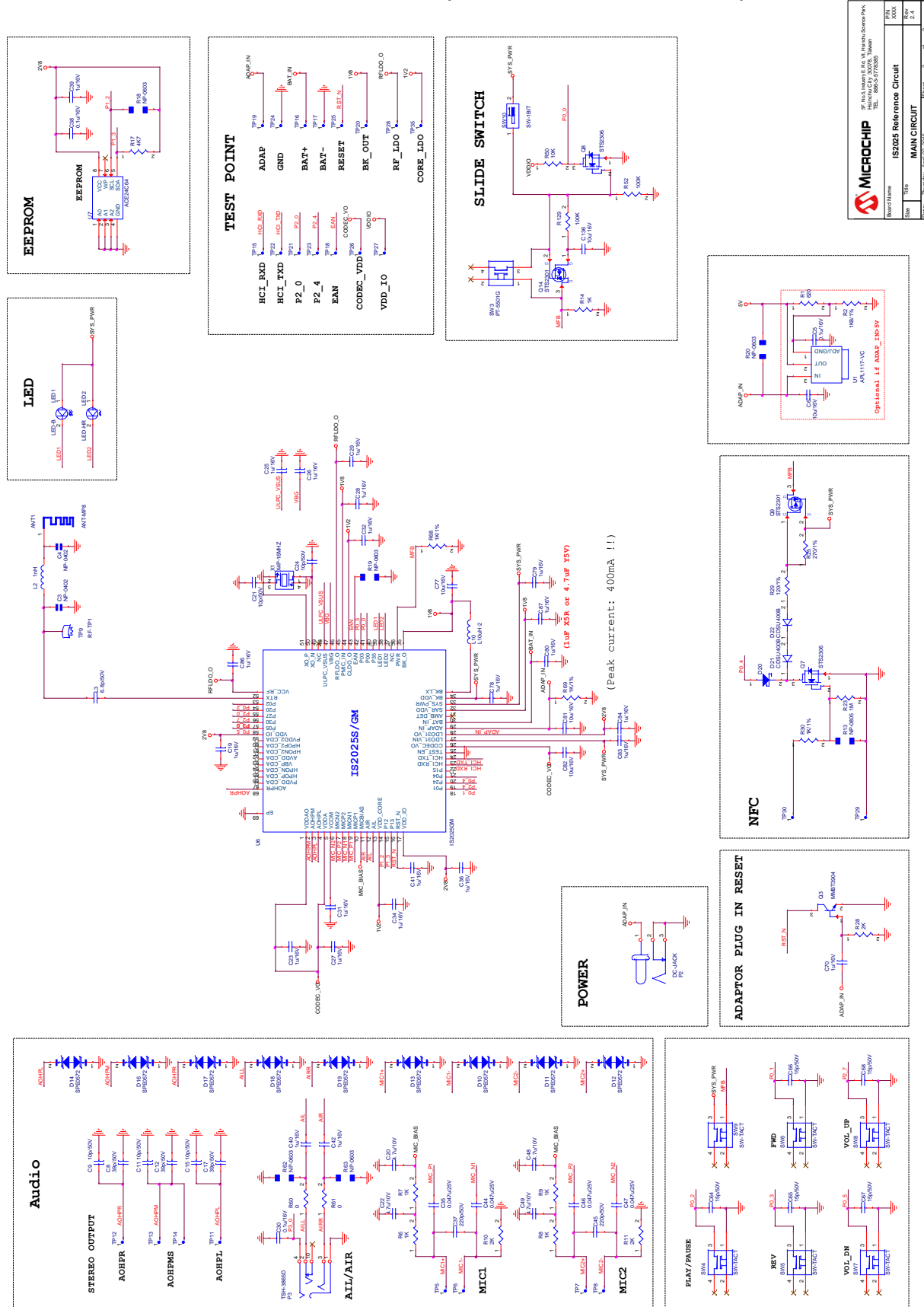
FIGURE 13-5: IS2025S REFERENCE CIRCUIT (FOR SPEAKER APPLICATION)
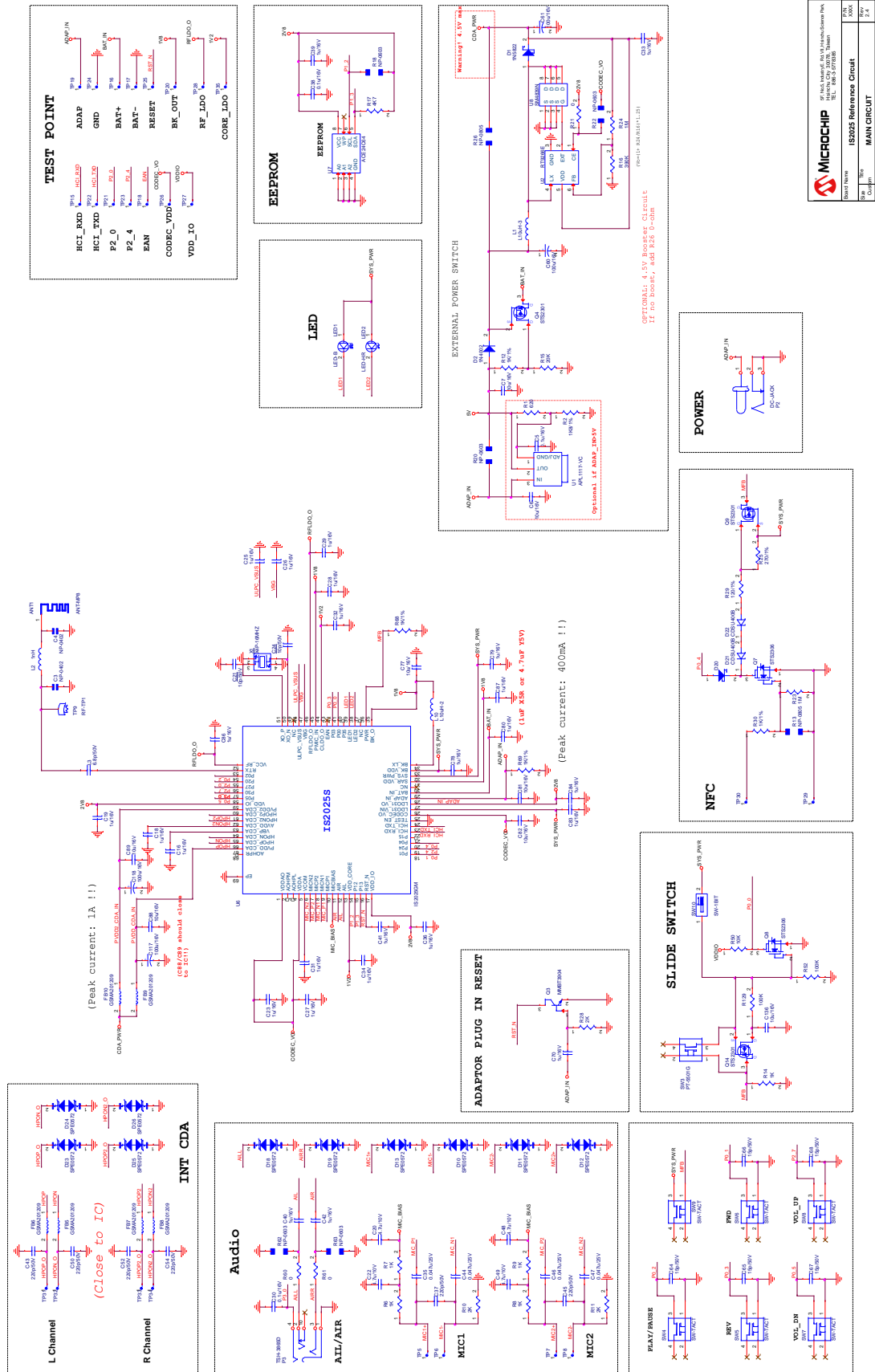
14.0 PACKAGE INFORMATION
14.1 CHIP IDENTIFICATION SYSTEM

PART NO.	X	-Y
(Chip Name)	(Package Type)	(Version)

Chip name: IS2020
                           IS2021
                           IS2023
                           IS2025

Package Type: S = QFN (Saw Type) Package

Version: e.g. "-203" is means the chip version is 203.

Examples:

a)   IS2020S-002:   002 version ROM code IS2020 chip in QFN type package.

b)   IS2025S-203:   203 version ROM code IS2025 chip in QFN type package.

14.2 PACKAGE MARKING INFORMATION

48 Lead QFN (5x6.5x0.9 mm)

Example

ISSC
IS2021S
203 (e3)
1512KT8
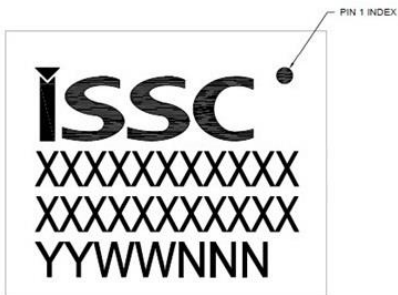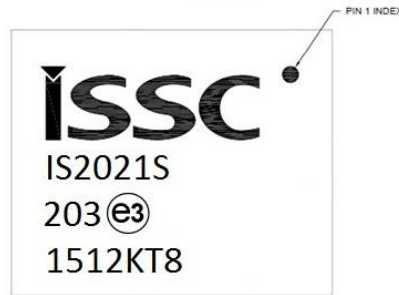
56 Lead QFN (7x7x0.9 mm)

Example

ISSC
IS2020S
203 (e3)
1512KT8

68 Lead QFN (8x8x0.9 mm)

Example

ISSC
IS2025S
203 (e3)
1512KT8
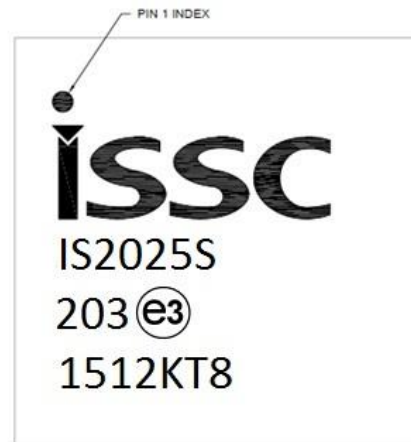
Legend:

XXX: Chip serial number version and (e3) Pb-free JEDEC designator for Matte Tin (Sn)

YY: Year code (last 2 digits of calendar year)
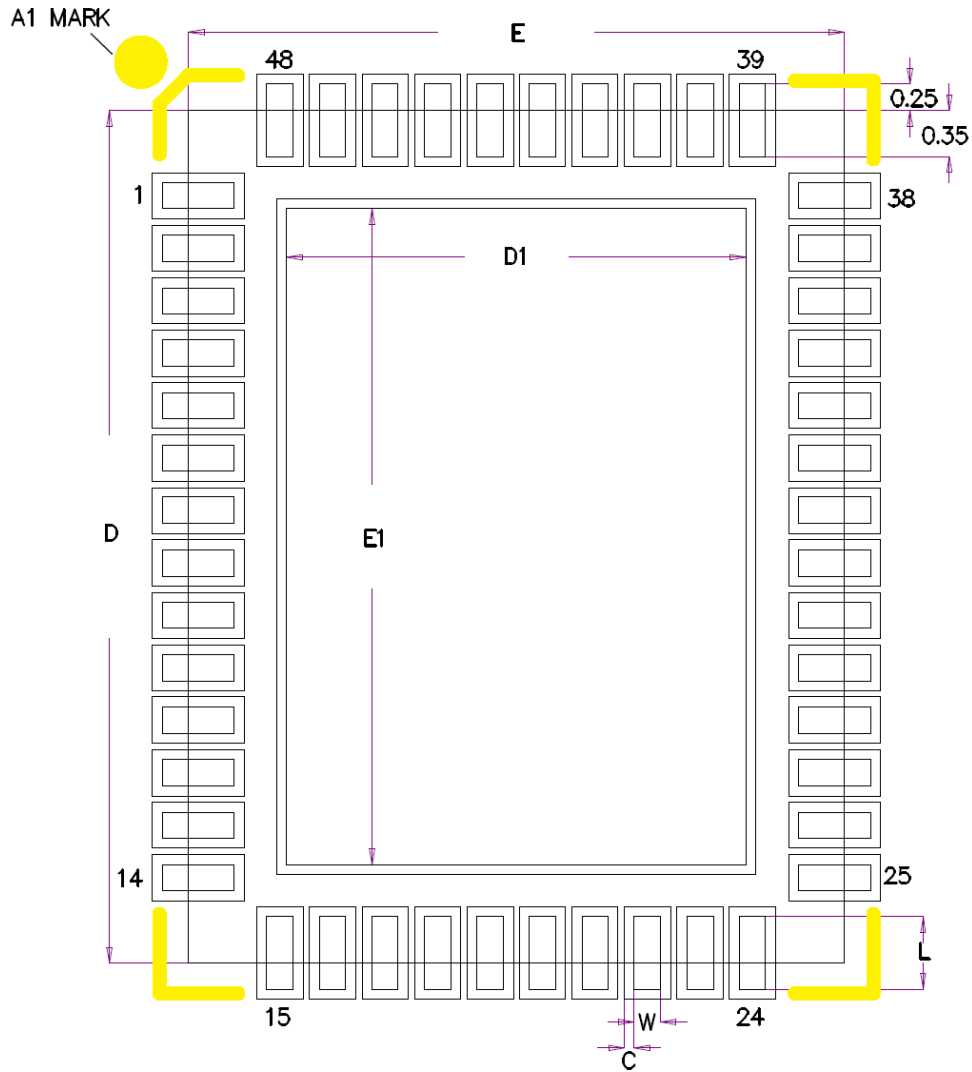WW: Week code (week of January 1 is week "1")
NNN: Alphanumeric traceability code

14.3 PACKAGE DETAIL

QFN48 5x6.5 Chip Outline (IS2021S)

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.9
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	– – –	0.65	0.67
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		5 BSC	
BODY SIZE Y	E		6.5 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	J	3.4	3.5	3.6
EP SIZE Y	K	4.9	5	5.1
LEAD LENGTH	L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ccc		0.08	
LEAD OFFSET	ddd		0.1	
EXPOSED PAD OFFSET	eee		0.1	
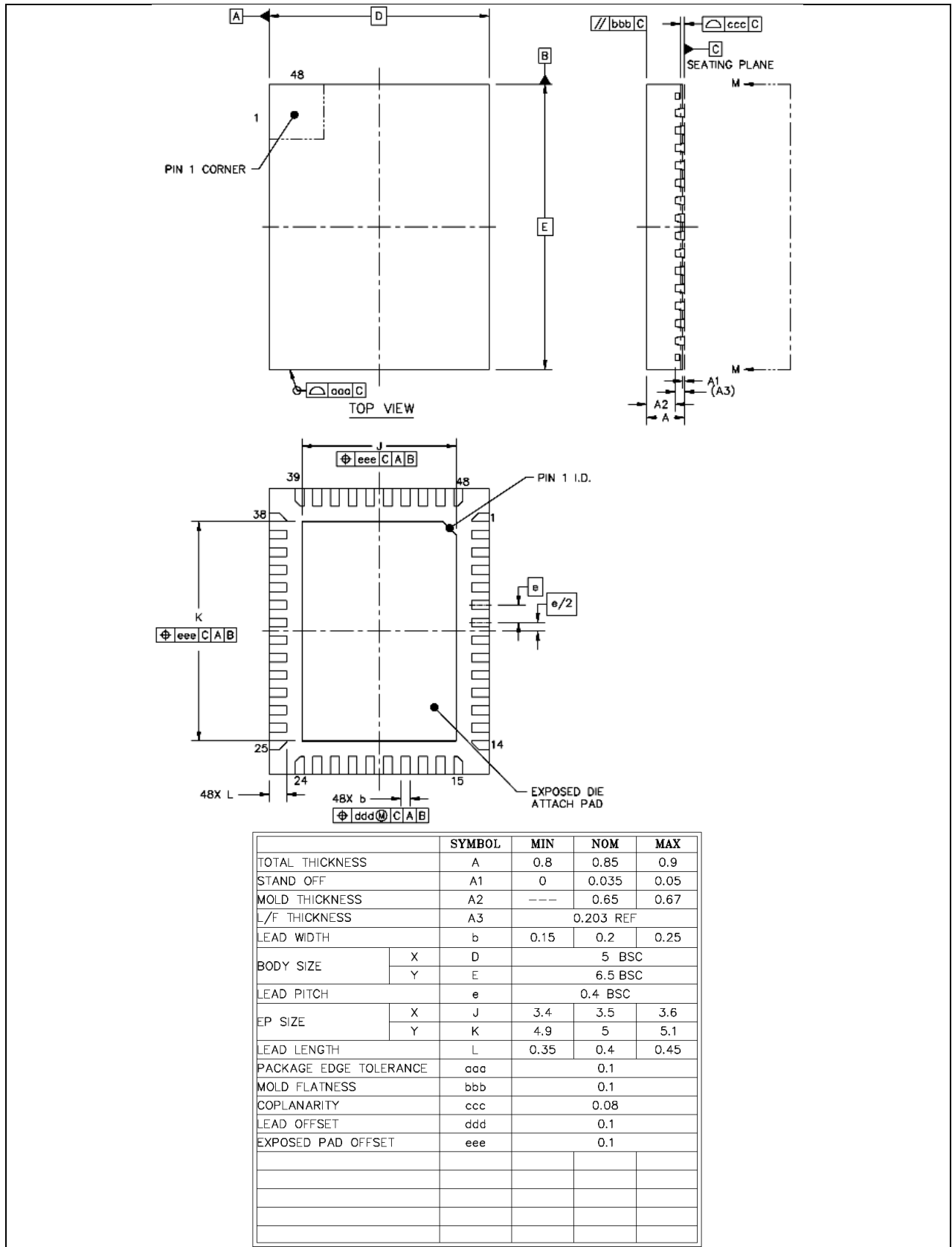
QFN48 5x6.5 PCB Footprint (IS2021S)

TOP VIEW
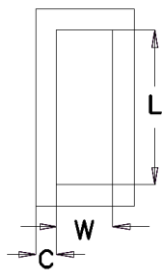
SOLDERMASK OPENING OUTSIDE OF LAND

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SILKSCREEN TOP L	A1		––	REF
SILKSCREEN TOP W	A2		––	REF
BODY SIZE	D		6.5	BSC
	E		5	BSC
EXPOSED PAD SIZE	D1		3.5	BSC
	E1		5	BSC
PEAD LENGTH	L		0.55	
PEAD WIDTH	W		0.2	
SOLDER MASKER OPEN	c		0.076	
PEAD PICTH	e		0.4	
PEAD COUNT	n1		48	

UNIT : MM

QFN56 7x7 Chip Outline (IS2020S / IS2023S)
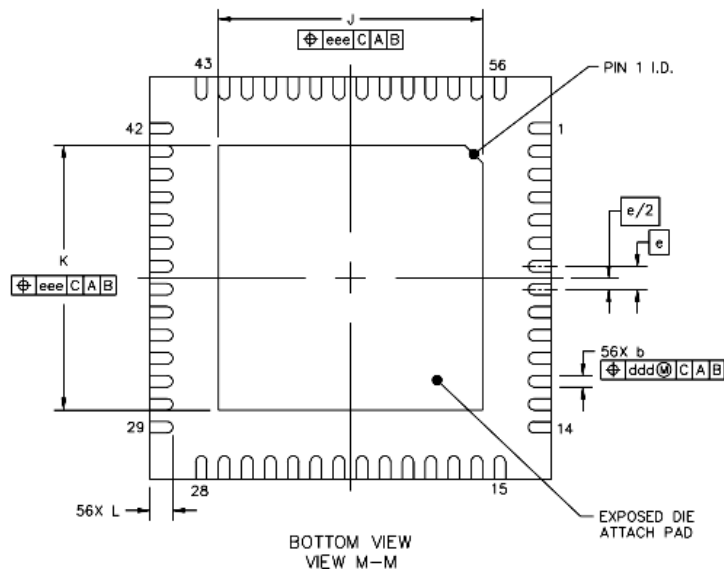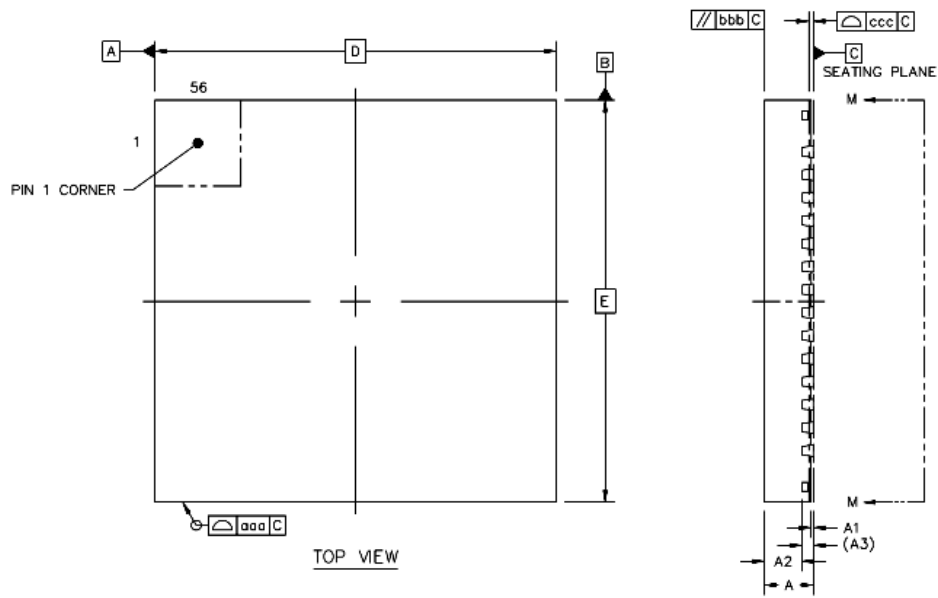
TOP VIEW

BOTTOM VIEW
VIEW M-M

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	7 BSC		
	Y	E	7 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	J	4.5	4.6	4.7
	Y	K	4.5	4.6	4.7
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

QFN68 8x8 Chip Outline (IS2025S)

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	— — —	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.5	4.6	4.7
	Y	K	4.5	4.6	4.7
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	
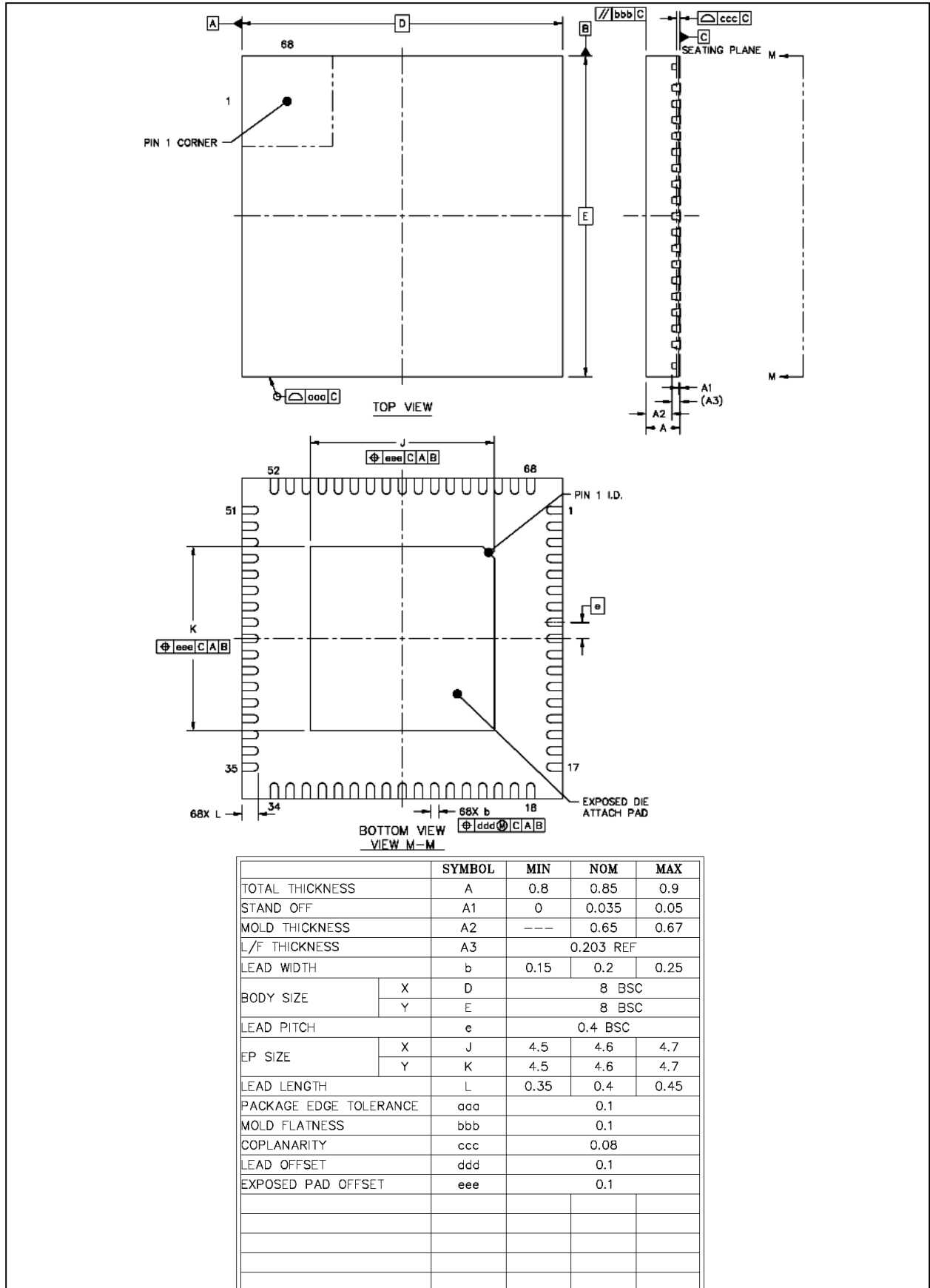
QFN68 8x8 PCB Footprint (IS2025S)
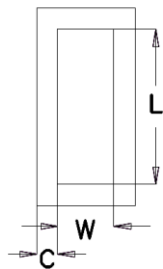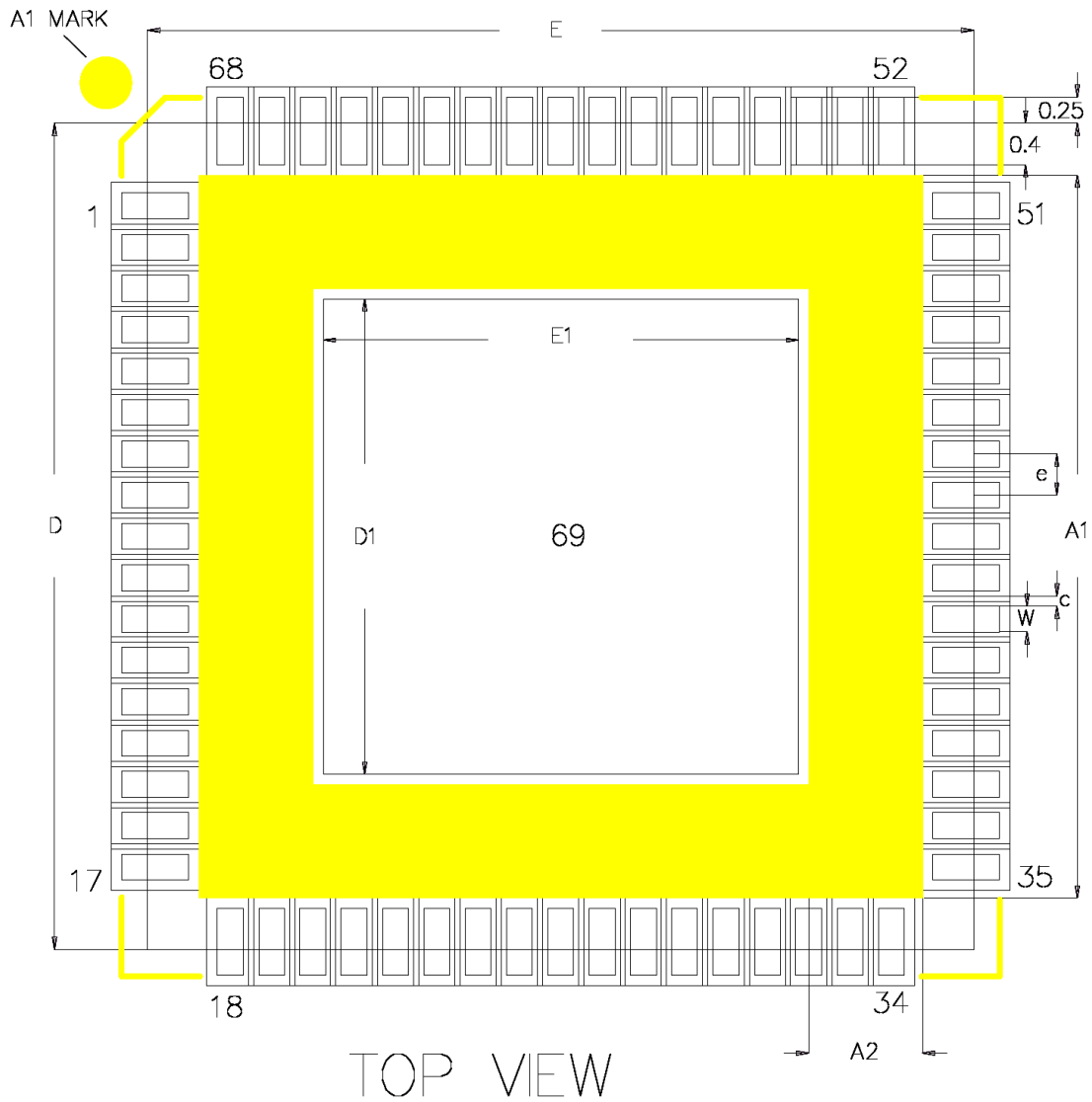
TOP VIEW

SOLDERMASK OPENING OUTSIDE OF LAND

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SILKSCREEN TOP L	A1		7	REF
SILKSCREEN TOP W	A2		1.1	REF
BODY SIZE	D		8	BSC
	E		8	BSC
EXPOSED PAD SIZE	D1		4.6	BSC
	E1		4.6	BSC
LEAD LENGTH	L		0.65	
LEAD WIDTH	W		0.25	
SOLDER MASKER OPEN	c		0.1	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		68	

UNIT : MM

15.0 REFLOW PROFILE AND STORAGE CONDITION

15.1 STENCIL OF SMT ASSEMBLY SUGGESTION

15.1.1 STENCIL TYPE & THICKNESS
Laser cutting
Stainless steel
Thickened
0.5 mm Pitch: thickness < 0.15 mm

15.1.2 APERTURE SIZE AND SHAPE FOR TERMINAL PAD
Aspect ratio (width/thickness) > 1.5
Aperture shape
 ➤ The stencil aperture is typically designed to match the pad size on the PCB.
 ➤ Oval-shaped opening should be used to get the optimum paste release.
 ➤ Rounded corners to minimize clogging.
 ➤ Positive taper walls (5o tapering) with bottom opening larger than the top.

15.1.3 APERTURE DESIGN FOR THERMAL PAD
The small multiple openings should be used in steady of one big opening.
60~80% solder paste coverage
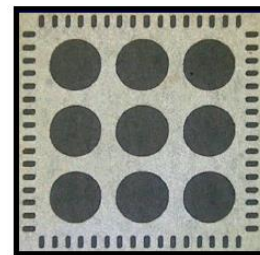Rounded corners to minimize clogging
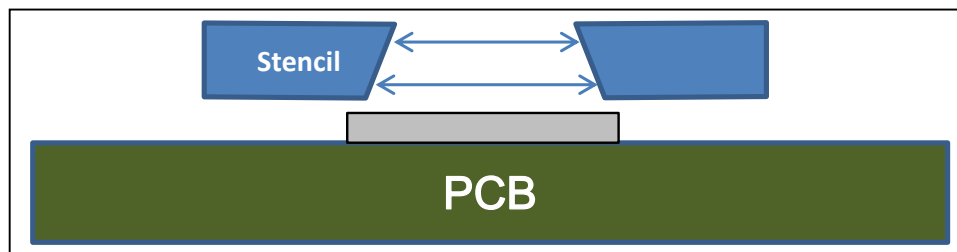Positive taper walls (5° tapering) with bottom opening larger than the top
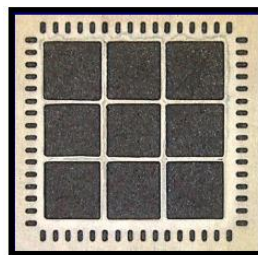
| Don't recommend
Coverage 91% | Recommend
Coverage 77% | Recommend
Coverage 65% |
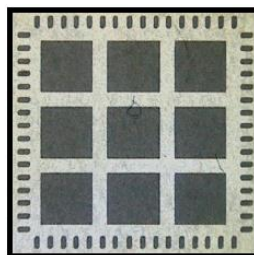
15.2 REFLOW CONDITION

1.) Follow : IPC/JEDEC J-STD-020

2.) Condition :

Average ramp-up rate (217℃ to peak): 1~2℃/sec max.

Preheat：150~200C、60~180 seconds

Temperature maintained above 217℃ : 60~150 seconds
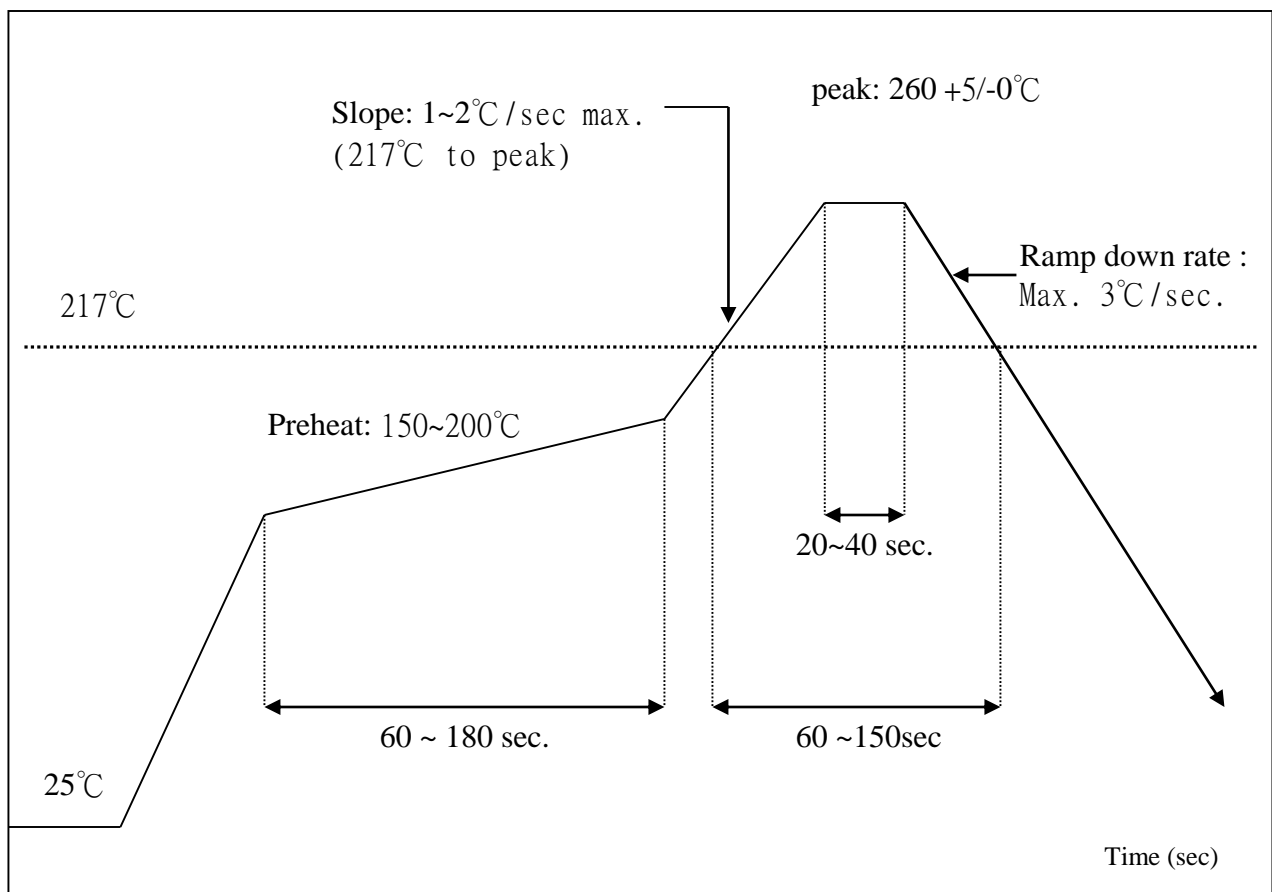
Time within 5℃ of actual peak temperature: 20 ~ 40 sec.

Peak temperature：260 +5/-0 ℃

Ramp-down rate : 3℃/sec. max.

Time 25℃ to peak temperature : 8 minutes max.

Cycle interval：5 minus

FIGURE 15-1: REFLOW PROFILE

FIGURE 15-1: REFLOW PROFILE

15.3 STORAGE CONDITION

1. Calculated shelf life in sealed bag: 24 months at < 40 ℃ and <90% relative humidity (RH)

2. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be Mounted within 168 hours of factory conditions <30℃/60% RH

FIGURE 15-2: LABEL OF CHIP BAG
(Please notice the baking requirement)

LEVEL

3

If blank, see adjacent bar code label

Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

1. Calculated shelf life in sealed bag : **24** months at < 40°C and <90% relative humidity (RH)

2. Peak package body temperature:_____°C
   If blank, see adjacent bar code label

3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be

   a) Mounted within:_____**168**_____ hours of factory conditions
      If blank, see adjacent bar code label
      ≤30°C/60% RH, or

   b) Stored per J-STD-033

4. Devices require bake, before mounting, if:

   a) Humidity Indicator Card reads >10% for level 2a - 5a devices or > 60% for level 2 devices when read at 23±5°C

   b) 3a or 3b are not met.

5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date: _____
      If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020