

### Features

- Integrated analog input Class D audio amplifier in a small 5 x 6 mm PQFN package
- High peak music power output
- No mechanical heatsink required
- Split or single power supply
- Differential or single-ended input
- Over-current, over-temperature and under voltage protections with self-reset function
- Start and stop click noise reduction
- High noise immunity
- RoHS compliant

### Typical Applications

- Home theatre systems
- Docking station audio systems
- PC audio systems
- Musical instruments
- Karaoke amplifiers
- Game consoles
- Powered speaker systems
- General purpose audio power amplifiers

### Product Summary

|                                           |                          |
|-------------------------------------------|--------------------------|
| Topology                                  | Half-Bridge, Full-Bridge |
| *IR4301 Output power (Typical, THD+N=10%) | 160 W/ 4 Ω               |
|                                           | 120 W/ 3 Ω               |
| *IR4321 Output power (Typical, THD+N=10%) | 90 W/ 4 Ω                |
|                                           | 135 W/ 2 Ω               |
| *IR4311 Output power (Typical, THD+N=10%) | 35 W/ 4 Ω                |
|                                           | 45 W/ 3 Ω                |
| *Residual noise (AES-17, IHF-A, typical)  | 250 µVrms                |
| *THD+N (1kHz, 1W, 4 Ω, typical)           | 0.02 %                   |

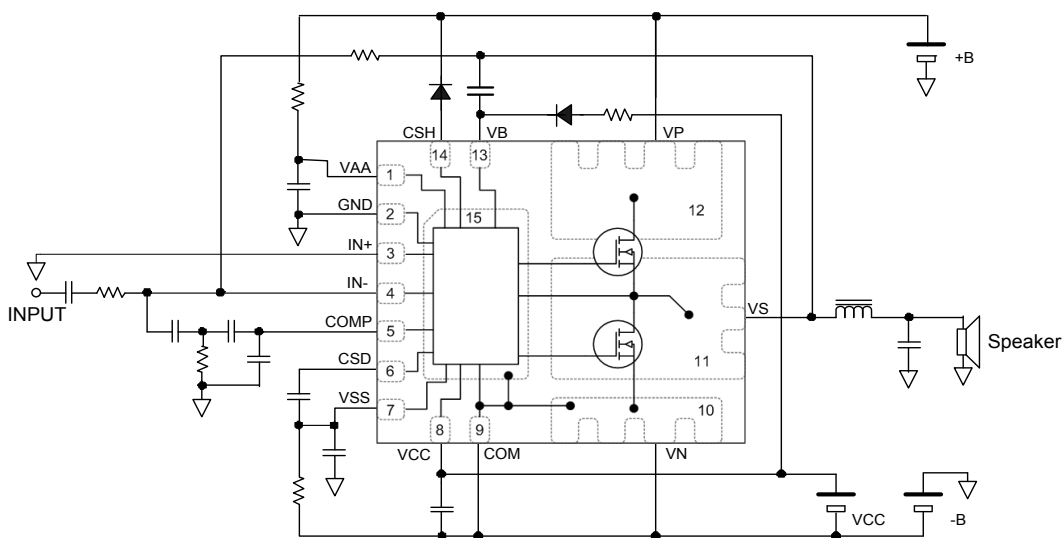
\* In typical application example

### Package



5x6mm PQFN22

### Typical Connection



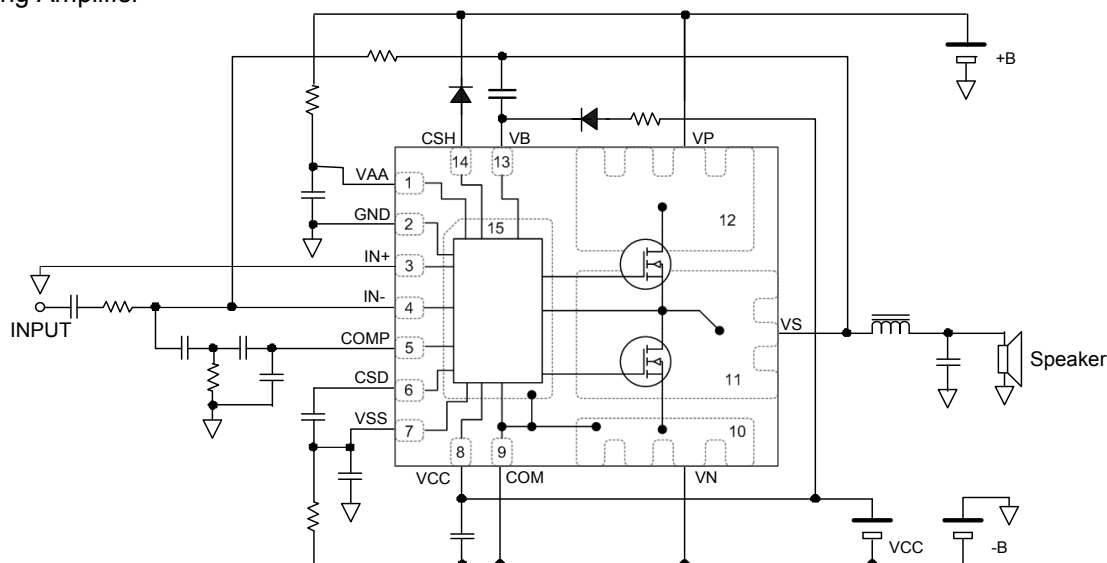
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## Description

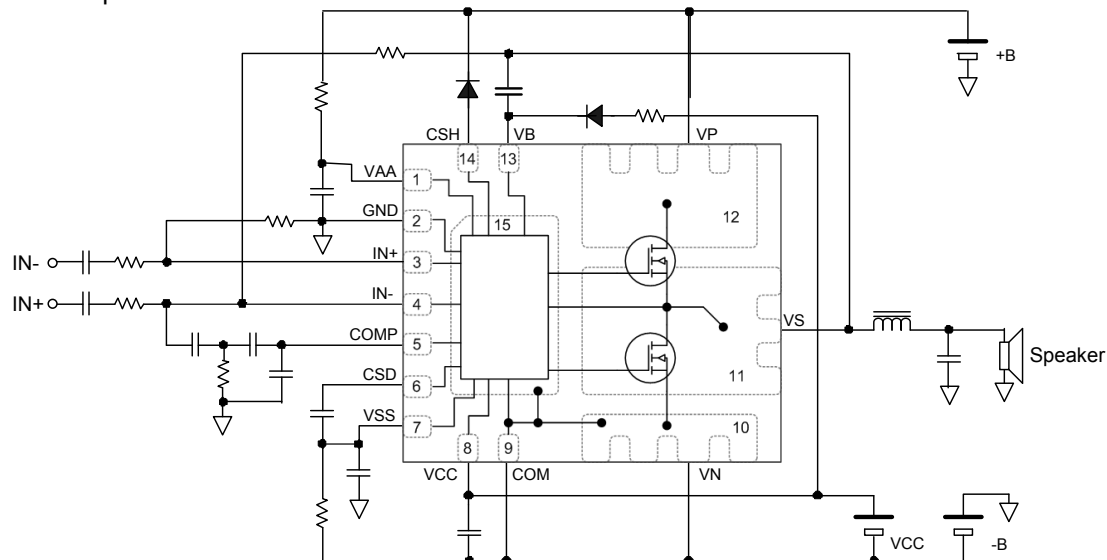
The IR43x1 integrates PWM controller and digital audio MOSFETs forming a high performance Class D audio amplifier. As a result of fully optimized MOSFETs co-packed with a dedicated controller IC, the IR43X1 operates without mechanical heatsink attached in a typical music playback usage. High voltage ratings and noise immunity in the controller IC ensures reliable operation over various environmental conditions. A small 5x6 mm PQFN package enhances the benefit of smaller size of Class D topology. The IR43x1 are a lead-free, ROHS compliant.

## Typical Connection Diagram

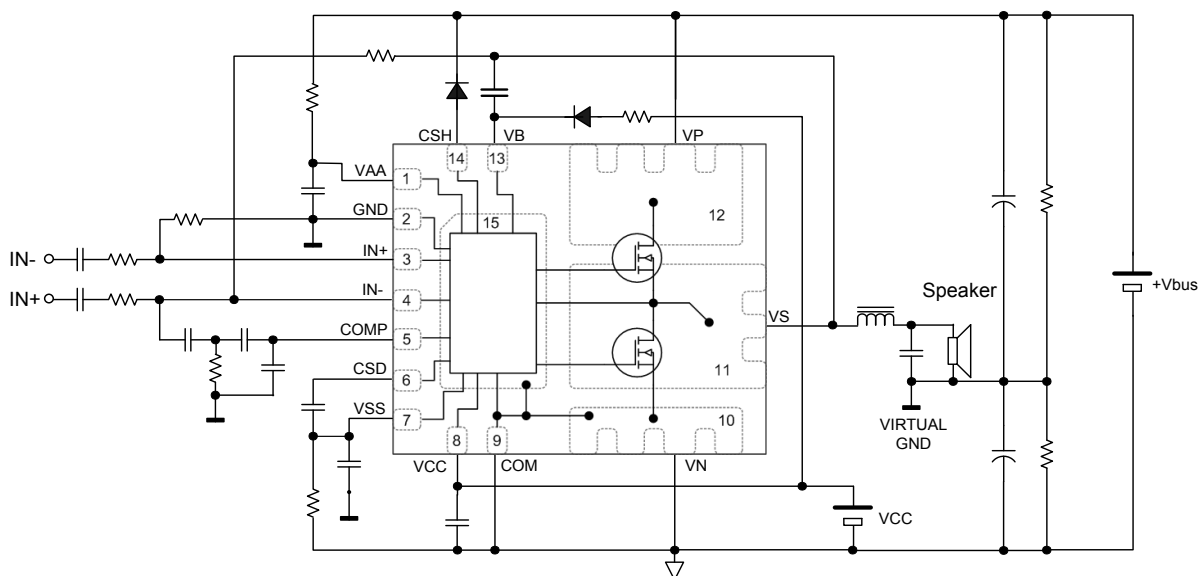
### 1. Inverting Amplifier



### 2. Differential Amplifier



### 3. Single Power Supply



### Qualification Information<sup>†</sup>

| Qualification Level        |                  | Industrial <sup>††</sup>                                                                                                                                            |
|----------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                            |                  | Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. |
| Moisture Sensitivity Level |                  | MSL2<br>(per IPC/JEDEC J-STD-020C)                                                                                                                                  |
| ESD                        | Machine Model    | Class B<br>(per JEDEC standard EIA/JESD22-A115)                                                                                                                     |
|                            | Human Body Model | Class 2<br>(per EIA/JEDEC standard JESD22-A114)                                                                                                                     |
| IC Latch-Up Test           |                  | Class I, Level A<br>(per JESD78)                                                                                                                                    |
| RoHS Compliant             |                  | Yes                                                                                                                                                                 |

<sup>†</sup> Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

<sup>††</sup> Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

<sup>†††</sup> Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM=VN; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Symbol                 | Definition                                                                                                                |        | Min                           | Max                  | Units |
|------------------------|---------------------------------------------------------------------------------------------------------------------------|--------|-------------------------------|----------------------|-------|
| V <sub>P</sub>         | VP pin positive power supply rail voltage                                                                                 | IR4301 | -                             | 80                   | V     |
|                        |                                                                                                                           | IR4321 | -                             | 60                   |       |
|                        |                                                                                                                           | IR4311 | -                             | 40                   |       |
| V <sub>B</sub>         | High side floating supply voltage                                                                                         | IR4301 | -0.3                          | 95                   |       |
|                        |                                                                                                                           | IR4321 | -0.3                          | 75                   |       |
|                        |                                                                                                                           | IR4311 | -0.3                          | 55                   |       |
| V <sub>CSH</sub>       | CSH pin input voltage                                                                                                     |        | V <sub>S</sub> -0.3           | V <sub>B</sub> +0.3  |       |
| V <sub>S</sub>         | High side floating supply voltage <sup>††</sup>                                                                           |        | V <sub>B</sub> -15            | V <sub>B</sub> +0.3  |       |
| V <sub>CC</sub>        | Low side supply voltage <sup>††</sup>                                                                                     |        | -0.3                          | 15                   |       |
| V <sub>AA</sub>        | Floating input positive supply voltage <sup>††</sup>                                                                      | IR4301 | -0.3                          | 100                  |       |
|                        |                                                                                                                           | IR4321 | -0.3                          | 70                   |       |
|                        |                                                                                                                           | IR4311 | -0.3                          | 50                   |       |
| V <sub>SS</sub>        | Floating input negative supply voltage <sup>††</sup>                                                                      |        | -1<br>(See I <sub>SSZ</sub> ) | GND +0.3             | mA    |
| V <sub>IN+</sub>       | Floating input supply ground voltage                                                                                      |        | V <sub>SS</sub> -0.3          | V <sub>AA</sub> +0.3 |       |
| I <sub>IN</sub>        | Input current between IN- and IN+ pins <sup>†</sup>                                                                       |        | -                             | ±3                   | V     |
| V <sub>CSD</sub>       | CSD pin input voltage                                                                                                     |        | V <sub>SS</sub> -0.3          | V <sub>AA</sub> +0.3 |       |
| V <sub>COMP</sub>      | COMP pin input voltage                                                                                                    |        | V <sub>SS</sub> -0.3          | V <sub>AA</sub> +0.3 | mA    |
| I <sub>AAZ</sub>       | Floating input supply zener clamp current <sup>††</sup>                                                                   |        | -                             | 20                   |       |
| I <sub>SSZ</sub>       | Floating input negative supply zener clamp current <sup>††</sup>                                                          |        | -                             | 20                   |       |
| I <sub>CCZ</sub>       | Low side supply zener clamp current <sup>†††</sup>                                                                        |        | -                             | 20                   |       |
| I <sub>BSZ</sub>       | Floating supply zener clamp current <sup>†††</sup>                                                                        |        | -                             | 20                   |       |
| dV <sub>S</sub> /dt    | Allowable V <sub>S</sub> voltage slew rate                                                                                |        | -                             | 50                   | V/ns  |
| dV <sub>SS</sub> /dt   | Allowable V <sub>SS</sub> voltage slew rate <sup>†††</sup>                                                                |        | -                             | 50                   | V/ms  |
| I <sub>D</sub> @ 25°C  | Continuous output current, from VP to VS, VS to VN, V <sub>CC</sub> =10V, V <sub>B</sub> -V <sub>S</sub> =10V             | IR4301 | -                             | 6.5                  | A     |
|                        |                                                                                                                           | IR4321 | -                             | 7.0                  |       |
|                        |                                                                                                                           | IR4311 | -                             | 3.6                  |       |
| I <sub>D</sub> @ 100°C | Continuous output current, from VP to VS, VS to VN, V <sub>CC</sub> =10V, V <sub>B</sub> -V <sub>S</sub> =10V             | IR4301 | -                             | 5.4                  |       |
|                        |                                                                                                                           | IR4321 | -                             | 5.8                  |       |
|                        |                                                                                                                           | IR4311 | -                             | 2.9                  |       |
| I <sub>DM</sub>        | Pulsed output current, from VP to VS, VS to VN, V <sub>CC</sub> =10V, V <sub>B</sub> -V <sub>S</sub> =10V <sup>††††</sup> | IR4301 | -                             | 26                   |       |
|                        |                                                                                                                           | IR4321 | -                             | 28                   |       |
|                        |                                                                                                                           | IR4311 | -                             | 15                   |       |
| Pd                     | Power dissipation <sup>††††</sup> @ T <sub>C</sub> = 25°C                                                                 | IR4301 | -                             | 31                   | W     |
|                        |                                                                                                                           | IR4321 | -                             | 31                   |       |
|                        |                                                                                                                           | IR4311 | -                             | 9                    |       |

|                   |                                                      |        |   |     |      |
|-------------------|------------------------------------------------------|--------|---|-----|------|
| Rth <sub>JC</sub> | Thermal resistance, junction to case <sup>††††</sup> | IR4301 | - | 4   | °C/W |
|                   |                                                      | IR4321 | - | 4   |      |
|                   |                                                      | IR4311 | - | 13  |      |
| T <sub>JIC</sub>  | Control IC junction temperature                      | -      | - | 150 | °C   |
| T <sub>JFET</sub> | FET junction temperature                             | -      | - | 150 |      |
| T <sub>S</sub>    | Storage Temperature                                  | -55    | - | 150 |      |
| T <sub>L</sub>    | Lead temperature (Soldering, 10 seconds)             | -      | - | 300 |      |

† IN- and IN+ contain clamping diodes between the two pins.

†† V<sub>AA</sub> -V<sub>SS</sub>, V<sub>CC</sub>-COM and V<sub>B</sub>-V<sub>S</sub> contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

††† For the rising and falling edges of step signal of 10V. V<sub>SS</sub>=15V to 200V.

†††† Per MOSFET

††††† Repetitive rating, pulse width limited by max. junction temperature

## Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The  $V_{SS}$  and  $V_S$  offset ratings are tested with supplies biased at  $COM=VN$ ,  $V_{AA}-V_{SS}=9.6V$ ,  $V_{CC}=12V$  and  $V_B-V_S=12V$ . All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

| Symbol       | Definition                                                        |        | Min.            | Max.            | Units |
|--------------|-------------------------------------------------------------------|--------|-----------------|-----------------|-------|
| $V_P$        | Positive power supply rail voltage, without heatsink              | IR4301 | -               | 62              | V     |
|              |                                                                   | IR4321 | -               | 50              |       |
|              |                                                                   | IR4311 | -               | 32              |       |
|              | Positive power supply rail voltage, with heatsink                 | IR4301 | -               | 68              |       |
|              |                                                                   | IR4321 | -               | 50              |       |
|              |                                                                   | IR4311 | -               | 32              |       |
| $V_B$        | High side floating supply absolute voltage                        |        | $V_S + 10$      | $V_S + 14$      |       |
| $V_S$        | High side floating supply offset voltage                          | IR4301 | †               | 80              |       |
|              |                                                                   | IR4321 | †               | 60              |       |
|              |                                                                   | IR4311 | †               | 40              |       |
| $V_{AA}$     | Floating input positive supply voltage <sup>††</sup>              |        | $V_{SS} + 4.5$  | $V_{SS} + 15$   |       |
| $V_{SS}$     | Floating input negative supply voltage <sup>††</sup>              | IR4301 | 0               | 80              |       |
|              |                                                                   | IR4321 | 0               | 60              |       |
|              |                                                                   | IR4311 | 0               | 40              |       |
| $I_{AAZ}$    | Floating input supply zener clamp current <sup>††</sup>           |        | 1               | 15              | mA    |
| $I_{SSZ}$    | Floating input negative supply zener clamp current <sup>††</sup>  |        | 1               | 15              |       |
| $V_{CC}$     | Low side fixed supply voltage                                     |        | 10              | 15              | V     |
| $V_{IC}$     | IN- and IN+ pins common mode input voltage                        |        | $V_{SS} + 2$    | $V_{AA} - 2$    |       |
| $V_{IN-}$    | Inverting input voltage                                           |        | $V_{IN+} - 0.5$ | $V_{IN+} + 0.5$ |       |
| $V_{CSD}$    | CSD pin input voltage                                             |        | $V_{SS}$        | $V_{AA}$        |       |
| $V_{COMP}$   | COMP pin input voltage                                            |        | $V_{SS}$        | $V_{AA}$        |       |
| $C_{COMP}$   | COMP pin phase compensation capacitor to GND                      |        | 1               | -               | nF    |
| $V_{CSH}$    | CSH pin input voltage                                             |        | $V_S$           | $V_B$           | V     |
| $dV_{SS}/dt$ | Allowable $V_{SS}$ voltage slew rate upon power-up <sup>†††</sup> |        | -               | 50              | V/ms  |
| $f_{SW}$     | Switching Frequency                                               |        | -               | 500             | kHz   |
| $T_A$        | Ambient Temperature                                               |        | -40             | 100             | °C    |

† Logic operational for  $V_S$  equal to -5V to +80V. Logic state held for  $V_S$  equal to -5V to -VBS.

†† GND input voltage is limited by  $I_{AAZ}$  and  $I_{SSZ}$ .

†††  $V_{SS}$  ramps up from 0V to 70V.

## Electrical Characteristics

$V_{CC}, V_{BS} = 12\text{ V}$ ,  $V_{SS} = V_S = V_N = \text{COM} = 0\text{ V}$ ,  $V_{AA} = 9.6\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

| Symbol                           | Definition                                                                        | Min  | Typ  | Max  | Units         | Test Conditions                                                                    |
|----------------------------------|-----------------------------------------------------------------------------------|------|------|------|---------------|------------------------------------------------------------------------------------|
| <b>Low Side Supply</b>           |                                                                                   |      |      |      |               |                                                                                    |
| $UV_{CC+}$                       | Vcc supply UVLO positive threshold                                                | 8.4  | 8.9  | 9.4  | V             |                                                                                    |
| $UV_{CC-}$                       | Vcc supply UVLO negative threshold                                                | 8.2  | 8.7  | 9.2  | V             |                                                                                    |
| $UV_{CCHYS}$                     | $UV_{CC}$ hysteresis                                                              | -    | 0.2  | -    | V             |                                                                                    |
| $I_{QCC}$                        | Low side quiescent current                                                        | -    | -    | 3    | mA            |                                                                                    |
| $I_{CC}$                         | Low side operating current                                                        | -    | 5    | -    | mA            | $f=400\text{kHz}$                                                                  |
| $V_{CLAMPL}$                     | Low side zener diode clamp voltage                                                | 14.7 | 15.3 | 16.2 | V             | $I_{CC}=5\text{mA}$                                                                |
| <b>High Side Floating Supply</b> |                                                                                   |      |      |      |               |                                                                                    |
| $UV_{BS+}$                       | High side well UVLO positive threshold                                            | 8.0  | 8.5  | 9.0  | V             |                                                                                    |
| $UV_{BS-}$                       | High side well UVLO negative threshold                                            | 7.8  | 8.3  | 8.8  | V             |                                                                                    |
| $UV_{BSHYS}$                     | $UV_{BS}$ hysteresis                                                              | -    | 0.2  | -    | V             |                                                                                    |
| $I_{QBS}$                        | High side quiescent current                                                       | -    | -    | 2.4  | mA            |                                                                                    |
| $V_{CLAMPH}$                     | High side zener diode clamp voltage                                               | 14.7 | 15.3 | 16.2 | V             | $I_{BS}=5\text{mA}$                                                                |
| <b>Floating Input Supply</b>     |                                                                                   |      |      |      |               |                                                                                    |
| $UV_{AA+}$                       | $VA+$ , $VA-$ floating supply UVLO positive threshold from $V_{SS}$               | 8.2  | 8.7  | 9.2  | V             | $V_{SS}=0\text{V}$ , GND pin floating                                              |
| $UV_{AA-}$                       | $VA+$ , $VA-$ floating supply UVLO negative threshold from $V_{SS}$               | 7.7  | 8.2  | 8.7  | V             | $V_{SS}=0\text{V}$ , GND pin floating                                              |
| $UV_{AAHYS}$                     | $UV_{AA}$ hysteresis                                                              | -    | 0.5  | -    | V             | $V_{SS}=0\text{V}$ , GND pin floating                                              |
| $I_{QAA0}$                       | Floating Input positive quiescent supply current                                  | -    | 1    | 2    | mA            | $V_{AA}=9.6\text{V}$ , $V_{SS}=0\text{V}$ , $V_{CSD}=V_{SS}$                       |
| $I_{QAA1}$                       | Floating Input positive quiescent supply current                                  | -    | 2    | 3    | mA            | $V_{AA}=9.6\text{V}$ , $V_{SS}=0\text{V}$ , $V_{CSD}=V_{AA}$                       |
| $I_{QAA2}$                       | Floating Input positive quiescent supply current                                  | -    | 2.5  | 4    | mA            | $V_{AA}=9.6\text{V}$ , $V_{SS}=0\text{V}$ , $V_{CSD}=\text{GND}$                   |
| $I_{LKM}$                        | Floating input side to Low side leakage current                                   | -    | -    | 50   | $\mu\text{A}$ | $V_{AA}=V_{SS}=V_{GND}=100\text{V}$                                                |
| $V_{CLAMPM+}$                    | $V_{AA}$ floating supply zener diode clamp voltage, positive, with respect to GND | 4.9  | 5.1  | 5.4  | V             | $I_{AA}=5\text{mA}$ , $I_{SS}=5\text{mA}$ , $V_{GND}=0\text{V}$ , $V_{CSD}=V_{SS}$ |
| $V_{CLAMPM-}$                    | $V_{SS}$ floating supply zener diode clamp voltage, negative, with respect to GND | -5.4 | -5.1 | -4.9 | V             | $I_{AA}=5\text{mA}$ , $I_{SS}=5\text{mA}$ , $V_{GND}=0\text{V}$ , $V_{CSD}=V_{SS}$ |

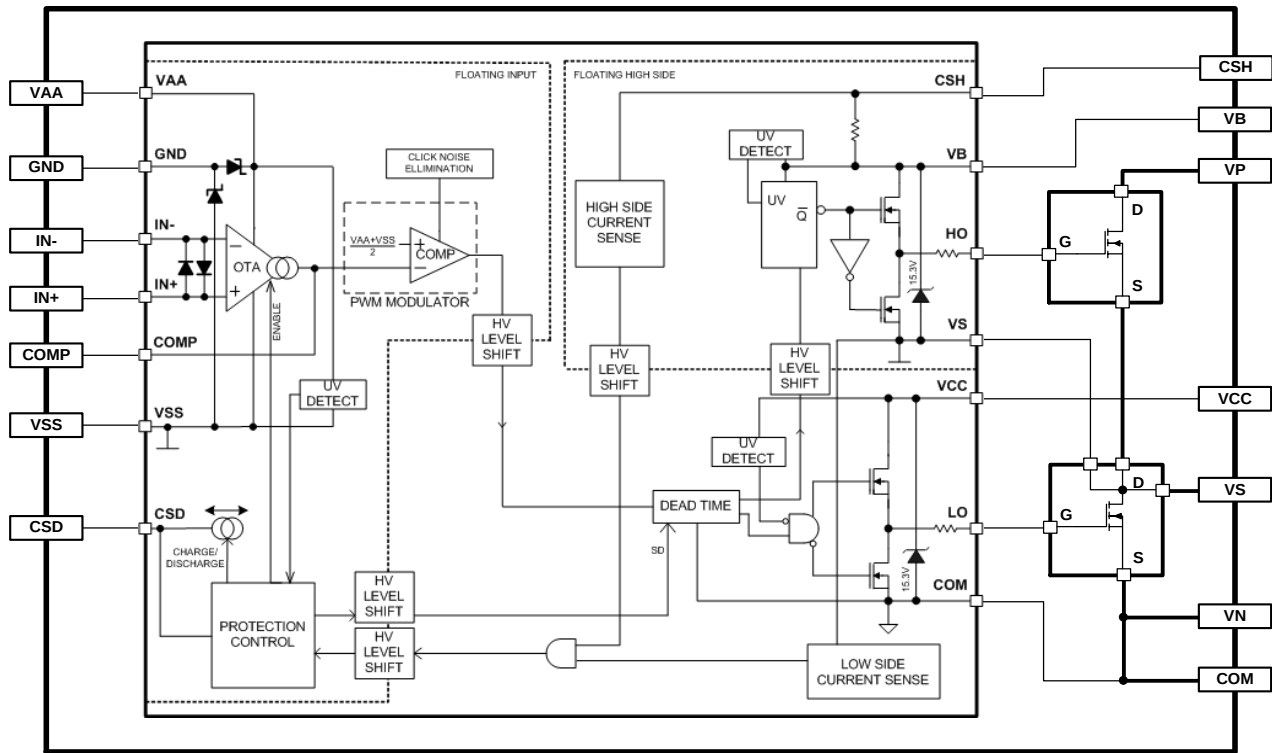
**Electrical Characteristics (cont'd)**
 $V_{CC}, V_{BS} = 12\text{ V}$ ,  $V_{SS} = V_S = V_N = \text{COM} = 0\text{V}$ ,  $V_{AA} = 9.6\text{V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

| Symbol                                                                            | Definition                                                                                                                  | Min | Typ                   | Max | Units         | Test Conditions                              |
|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|-----|-----------------------|-----|---------------|----------------------------------------------|
| <b>Audio Input</b> ( $V_{GND}=0$ , $V_{AA}=4.8\text{V}$ , $V_{SS}=-4.8\text{V}$ ) |                                                                                                                             |     |                       |     |               |                                              |
| $V_{OS}$                                                                          | Input offset voltage                                                                                                        | -18 | 0                     | 18  | mV            |                                              |
| $I_{BIN}$                                                                         | Input bias current                                                                                                          | -   | -                     | 40  | nA            |                                              |
| GBW                                                                               | Small signal bandwidth                                                                                                      | -   | 9                     | -   | MHz           | $C_{COMP}=1\text{nF}$ ,<br>$R_f=0$           |
| $g_m$                                                                             | OTA transconductance                                                                                                        | -   | 10                    | -   | mS            | $V_{IN+}=0\text{V}$ , $V_{IN-}=10\text{mV}$  |
| $G_V$                                                                             | OTA gain                                                                                                                    | 50  | -                     | -   | dB            |                                              |
| <b>PWM</b>                                                                        |                                                                                                                             |     |                       |     |               |                                              |
| $V_{th_{PWM}}$                                                                    | PWM comparator threshold in COMP                                                                                            | -   | $(V_{AA} - V_{SS})/2$ | -   | V             |                                              |
| $f_{OTA}$                                                                         | COMP pin star-up local oscillation frequency                                                                                | 0.7 | 1.0                   | 1.5 | MHz           | $V_{CSD} = \text{GND}$                       |
| $T_{on}$                                                                          | COMP to VS rising edge propagation delay                                                                                    | -   | 370                   | -   | ns            |                                              |
| $T_{off}$                                                                         | COMP to VS trailing edge propagation delay                                                                                  | -   | 320                   | -   | ns            |                                              |
| DT                                                                                | Deadtime: Low-side turn-off to High-side turn-on ( $DT_{LO-HO}$ ) & High-side turn-off to Low-side turn-on ( $DT_{HO-LO}$ ) | -   | 50                    | -   | ns            | $V_P=30\text{V}$ ,<br>$V_N=-30\text{V}$      |
| <b>Power MOSFET (FET1, FET2) (IR4301)</b>                                         |                                                                                                                             |     |                       |     |               |                                              |
| $V_{(BR)DSS}$                                                                     | Drain-to-Source breakdown voltage                                                                                           | 80  | -                     | -   | V             | $V_{GS}=0\text{V}$ ,<br>$I_D=250\mu\text{A}$ |
| $R_{DS(ON)}$                                                                      | FET on resistance                                                                                                           | -   | 39                    | 50  | m $\Omega$    | $V_{GS}=10\text{V}$ , $I_D=3.3\text{A}$      |
| Qg                                                                                | Total gate charge                                                                                                           | -   | 7.3                   | -   | nC            |                                              |
| $I_{LK0}$                                                                         | VP leakage current, $V_S=V_N$                                                                                               | -   | -                     | 20  | $\mu\text{A}$ | $V_P=80\text{V}$ , $V_{CSD}=V_{SS}$          |
| $I_{LK1}$                                                                         | VP leakage current, $V_S=V_P$                                                                                               | -   | -                     | 50  | $\mu\text{A}$ |                                              |
| <b>Power MOSFET (FET1, FET2) (IR4321)</b>                                         |                                                                                                                             |     |                       |     |               |                                              |
| $V_{(BR)DSS}$                                                                     | Drain-to-Source breakdown voltage                                                                                           | 60  | -                     | -   | V             | $V_{GS}=0\text{V}$ ,<br>$I_D=250\mu\text{A}$ |
| $R_{DS(ON)}$                                                                      | FET on resistance                                                                                                           | -   | 30                    | 40  | m $\Omega$    | $V_{GS}=10\text{V}$ , $I_D=3.3\text{A}$      |
| Qg                                                                                | Total gate charge                                                                                                           | -   | 8.3                   | -   | nC            |                                              |
| $I_{LK0}$                                                                         | VP leakage current, $V_S=V_N$                                                                                               | -   | -                     | 20  | $\mu\text{A}$ | $V_P=60\text{V}$ , $V_{CSD}=V_{SS}$          |
| $I_{LK1}$                                                                         | VP leakage current, $V_S=V_P$                                                                                               | -   | -                     | 50  | $\mu\text{A}$ |                                              |
| <b>Power MOSFET (FET1, FET2) (IR4311)</b>                                         |                                                                                                                             |     |                       |     |               |                                              |
| $V_{(BR)DSS}$                                                                     | Drain-to-Source breakdown voltage                                                                                           | 40  | -                     | -   | V             | $V_{GS}=0\text{V}$ ,<br>$I_D=250\mu\text{A}$ |
| $R_{DS(ON)}$                                                                      | FET on resistance                                                                                                           | -   | 44                    | 56  | m $\Omega$    | $V_{GS}=10\text{V}$ , $I_D=3.6\text{A}$      |
| Qg                                                                                | Total gate charge                                                                                                           | -   | 4.5                   | -   | nC            |                                              |
| $I_{LK0}$                                                                         | VP leakage current, $V_S=V_N$                                                                                               | -   | -                     | 20  | $\mu\text{A}$ | $V_P=40\text{V}$ , $V_{CSD}=V_{SS}$          |
| $I_{LK1}$                                                                         | VP leakage current, $V_S=V_P$                                                                                               | -   | -                     | 50  | $\mu\text{A}$ |                                              |

**Electrical Characteristics (cont'd)**
 $V_{CC}, V_{BS} = 12\text{ V}$ ,  $V_{SS} = V_S = V_N = \text{COM} = 0\text{ V}$ ,  $V_{AA} = 9.6\text{ V}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

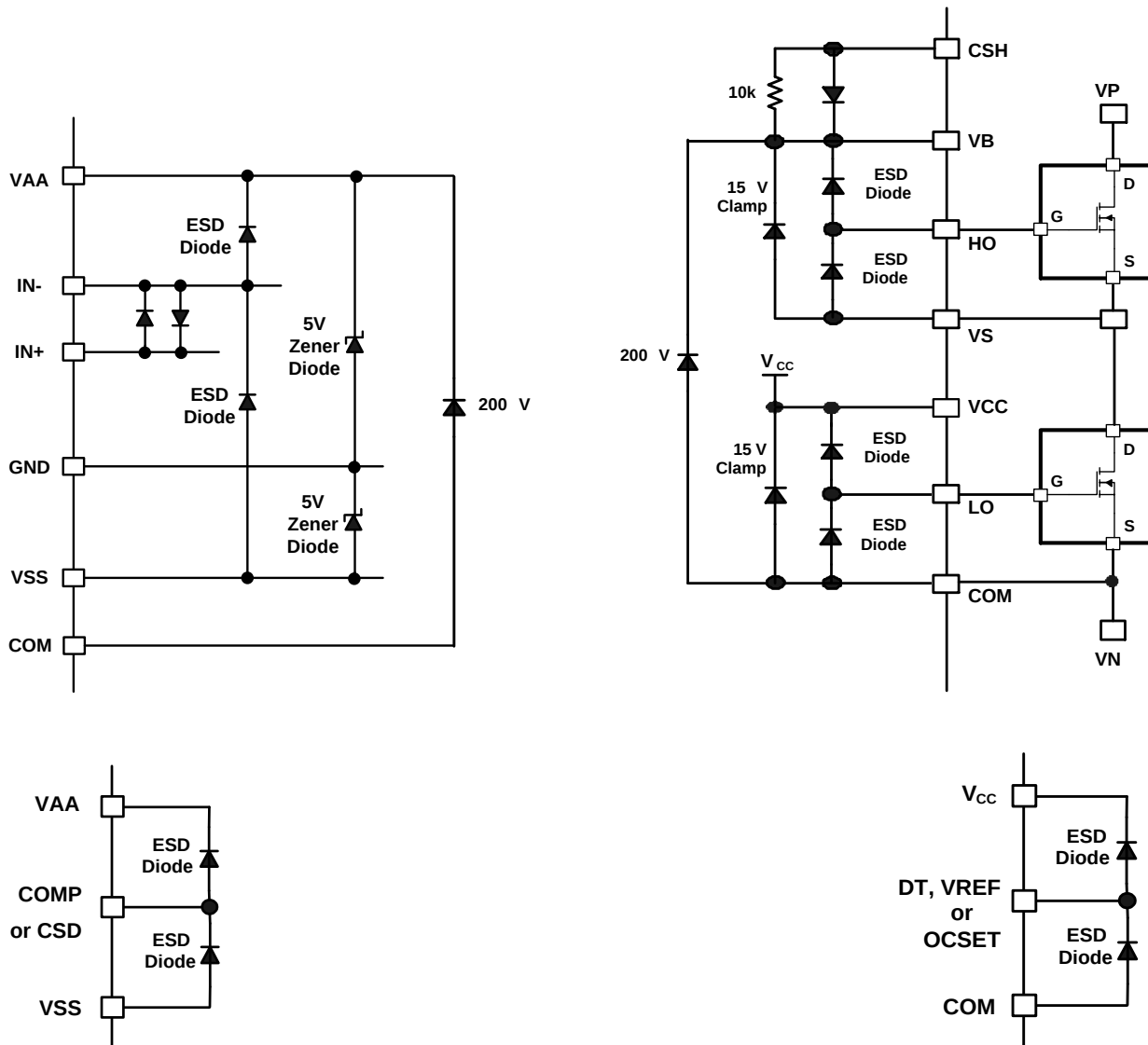
| Symbol            | Definition                                                  | Min                  | Typ                  | Max                  | Units            | Test Conditions                   |
|-------------------|-------------------------------------------------------------|----------------------|----------------------|----------------------|------------------|-----------------------------------|
| <b>Protection</b> |                                                             |                      |                      |                      |                  |                                   |
| $I_{OCP}$         | Positive OC threshold                                       | -                    | 16                   | -                    | A                |                                   |
| $I_{OCN}$         | Negative OC threshold                                       | -                    | -16                  | -                    | A                |                                   |
| $V_{th1}$         | CSD pin shutdown release threshold                          | $0.62 \times V_{AA}$ | $0.70 \times V_{AA}$ | $0.78 \times V_{AA}$ | V                |                                   |
| $V_{th2}$         | CSD pin self-reset threshold                                | $0.26 \times V_{AA}$ | $0.30 \times V_{AA}$ | $0.34 \times V_{AA}$ | V                |                                   |
| $I_{CSD+}$        | CSD pin discharge current                                   | 70                   | 100                  | 130                  | $\mu\text{A}$    | $V_{CSD} = V_{SS} + 4.8\text{ V}$ |
| $I_{CSD-}$        | CSD pin charge current                                      | 70                   | 100                  | 130                  | $\mu\text{A}$    | $V_{CSD} = V_{SS} + 4.8\text{ V}$ |
| $t_{SD}$          | Shutdown propagation delay from $V_S < V_{th1}$ to Shutdown | -                    | -                    | 250                  | ns               | $\text{COMP} = V_{SS}$            |
| $t_{OCP}$         | Propagation delay time from $I_O > I_{OCP}$ to Shutdown     | -                    | -                    | 500                  | ns               | $\text{COMP} = V_{SS}$            |
| $t_{OCN}$         | Propagation delay time from $I_O < I_{OCN}$ to Shutdown     | -                    | -                    | 500                  | ns               | $\text{COMP} = V_{SS}$            |
| $T_{SD}$          | Over temperature shutdown threshold in controller IC        | -                    | 105                  | -                    | $^\circ\text{C}$ |                                   |
| $T_{SDHYS}$       | Over temperature shutdown threshold hysteresis              | -                    | 7                    | -                    | $^\circ\text{C}$ |                                   |

## Functional Block Diagram



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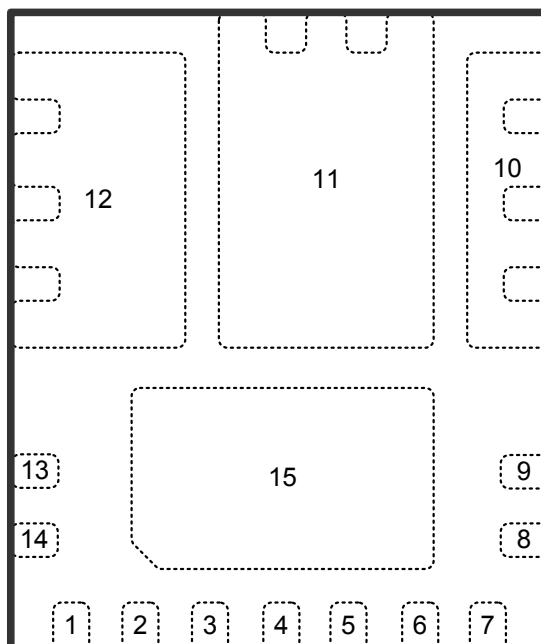
## Input/Output Pin Equivalent Circuit Diagrams



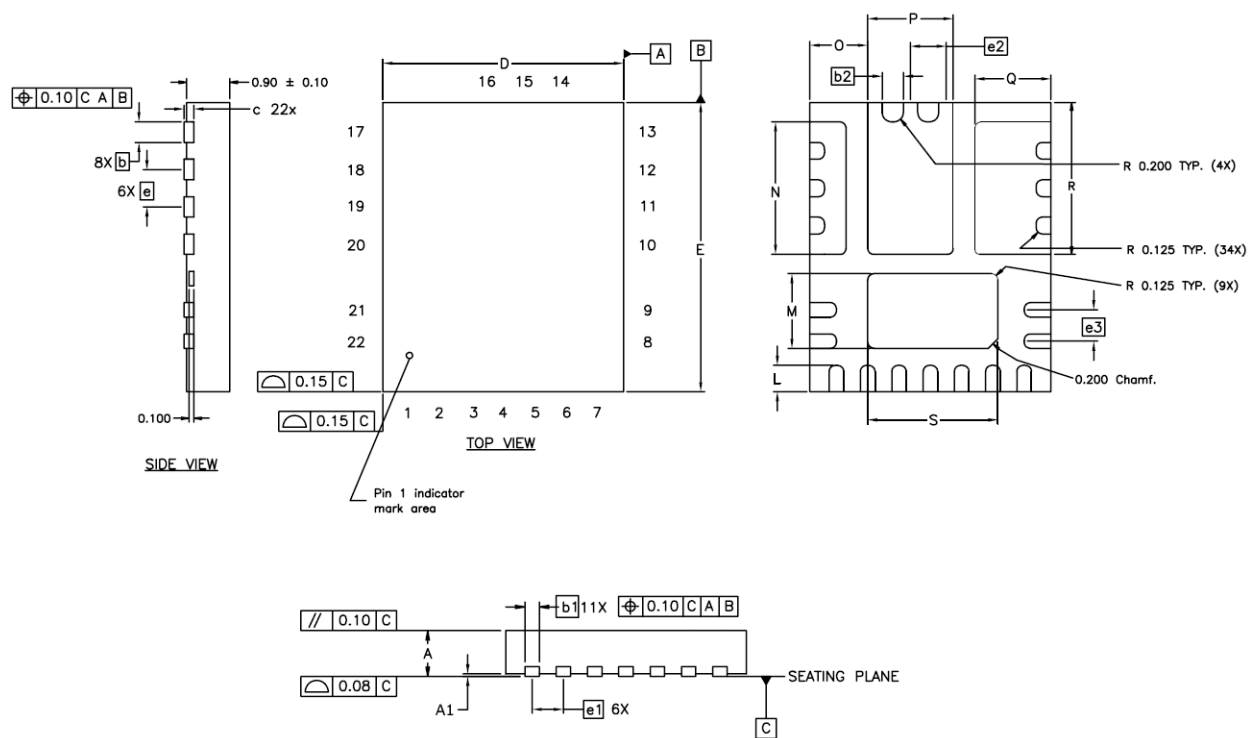
## Lead Definitions

| Pin # | Symbol | Description                                                   |
|-------|--------|---------------------------------------------------------------|
| 1     | VAA    | Floating input positive supply                                |
| 2     | GND    | GND for internal shunt zener diodes to VAA and VSS            |
| 3     | IN+    | Analog non-inverting input                                    |
| 4     | IN-    | Analog inverting input                                        |
| 5     | COMP   | PWM comparator input                                          |
| 6     | CSD    | Shutdown timing capacitor / shutdown input                    |
| 7     | VSS    | Floating input negative supply                                |
| 8     | VCC    | Low side supply                                               |
| 9     | COM    | Low side supply return, internally connected to VN            |
| 10    | VN     | Negative power supply, internally connected to COM externally |
| 11    | VS     | PWM output                                                    |
| 12    | VP     | Positive power supply                                         |
| 13    | VB     | High side floating supply, referenced to VS                   |
| 14    | CSH    | High side over current sensing input, referenced to VS        |
| 15    | SUB    | Internally connected to COM (Do not use as supply return)     |

## Lead Assignments (Top View)



## Package Details



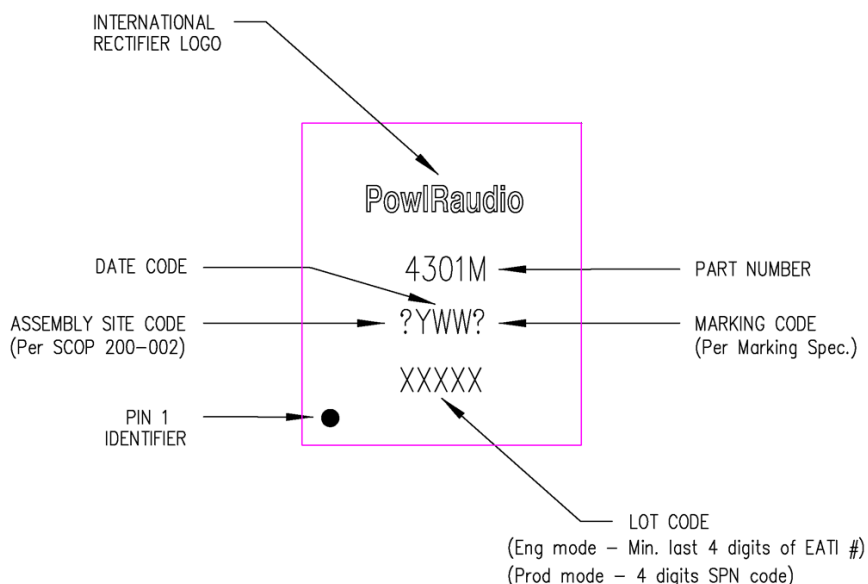
Outline PQFN 5x6 D

| DIM | MILLIMETERS |       | INCHES      |       |
|-----|-------------|-------|-------------|-------|
|     | MIN         | MAX   | MIN         | MAX   |
| A   | 0.800       | 1.000 | .0315       | .0394 |
| A1  | 0.000       | 0.050 | .0000       | .0020 |
| b   | 0.375       | 0.475 | .0148       | .0187 |
| b1  | 0.250       | 0.350 | .0098       | .0138 |
| b2  | 0.388       | 0.488 | .0153       | .0192 |
| c   | 0.203 REF.  |       | .0080 REF.  |       |
| D   | 5.000 BASIC |       | .1969 BASIC |       |
| E   | 6.000 BASIC |       | .2362 BASIC |       |
| e   | 0.775 BASIC |       | .0305 BASIC |       |
| e1  | 0.650 BASIC |       | .0256 BASIC |       |
| e2  | 0.738 BASIC |       | .0291 BASIC |       |
| e3  | 0.650 BASIC |       | .0256 BASIC |       |
| L   | 0.500       | 0.600 | .0197       | .0236 |
| M   | 1.500       | 1.600 | .0591       | .0630 |
| N   | 2.700       | 2.800 | .1063       | .1102 |
| O   | 1.150       | 1.250 | .0453       | .0492 |
| P   | 1.725       | 1.825 | .0679       | .0719 |
| Q   | 1.525       | 1.625 | .0600       | .0640 |
| R   | 3.100       | 3.200 | .1220       | .1260 |
| S   | 2.650       | 2.750 | .1043       | .1083 |

## Board Mounting Information

Refer to Application Note AN-1170 Audio Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.

## Part Marking Information



## Ordering Information

| Base Part Number | Package Type | Standard Pack |          | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
|                  |              | Form          | Quantity |                      |
| IR4301M          | PQFN22 5x6mm | Tape and Reel | 4000     | IR4301MTRPBF         |
| IR4321M          | PQFN22 5x6mm | Tape and Reel | 4000     | IR4321MTRPBF         |
| IR4311M          | PQFN22 5x6mm | Tape and Reel | 4000     | IR4311MTRPBF         |

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