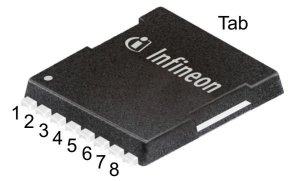
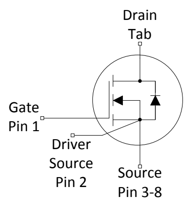
MOSFET

650V CoolMOS™ C7 Gold series (G7) Power Transistor

The C7 GOLD series (G7) for the first time brings together the benefits of the C7 GOLD CoolMOS™ technology, 4 pin Kelvin Source capability and the improved thermal properties of the TOLL package to enable a possible SMD solution for high current topologies such as PFC up to 3kW

HSOF





Features

- C7 Gold gives best in class FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$*Q_g.
- C7 Gold technology enables best in class $R_{DS(on)}$ in smallest footprint.
- TOLL package has inbuilt 4th pin Kelvin Source configuration and low parasitic source inductance (~1nH).
- TOLL package is MSL1 compliant, total Pb-free, has easy visual inspection grooved leads and is qualified for industrial applications according to JEDEC(J-STD20 and JESD22).
- TOLL SMD package combined with lead free die attach process enables improved thermal performance R_{th}.

Benefits

- C7 Gold FOM $R_{DS(on)}$*Q_g is 14% better than previous C7 650V enabling faster switching leading to higher efficiency.
- C7 Gold can reach 33mΩ in in TOLL 115mm^2 footprint, whereas previous BIC C7 650V was 45mΩ in 150mm^2 D^{2}PAK footprint.
- Reducing parasitic source inductance by Kelvin Source improves efficiency by faster switching and ease of use due to less ringing.
- TOLL package is easy to use and has the highest quality standards.
- Improved thermals enable SMD TOLL package to be used in higher current designs than has been previously possible.

Applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	33	mΩ
$Q_{g.typ}$	110	nC
$I_{D,pulse}$	245	A
$I_{D,continuous}$ @ T_j<150°C	77	A
E_{oss}@400V	13.5	µJ
Body diode di/dt	60	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPT65R033G7	PG-HSOF-8	65C7033G	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	69 44	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	245	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	289	mJ	I_D=12.5A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	1.44	mJ	I_D=12.5A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	12.5	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	391	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	69	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	245	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	1.5	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt	-	-	60	A/µs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.32	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=1.44mA
Zero gate voltage drain current	I_{DSS}	- -	- 45	2 -	µA	V_{DS}=650, V_{GS}=0V, T_j=25°C V_{DS}=650, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.029 0.072	0.033 -	Ω	V_{GS}=10V, I_D=28.9A, T_j=25°C V_{GS}=10V, I_D=28.9A, T_j=150°C
Gate resistance	R_G	-	0.85	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	5000	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	80	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	169	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	1880	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=28.9A, R_G=3.3Ω; see table 9
Rise time	t_r	-	8	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=28.9A, R_G=3.3Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	85	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=28.9A, R_G=3.3Ω; see table 9
Fall time	t_f	-	5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=28.9A, R_G=3.3Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	27	-	nC	V_{DD}=400V, I_D=28.9A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	35	-	nC	V_{DD}=400V, I_D=28.9A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	110	-	nC	V_{DD}=400V, I_D=28.9A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	V_{DD}=400V, I_D=28.9A, V_{GS}=0 to 10V

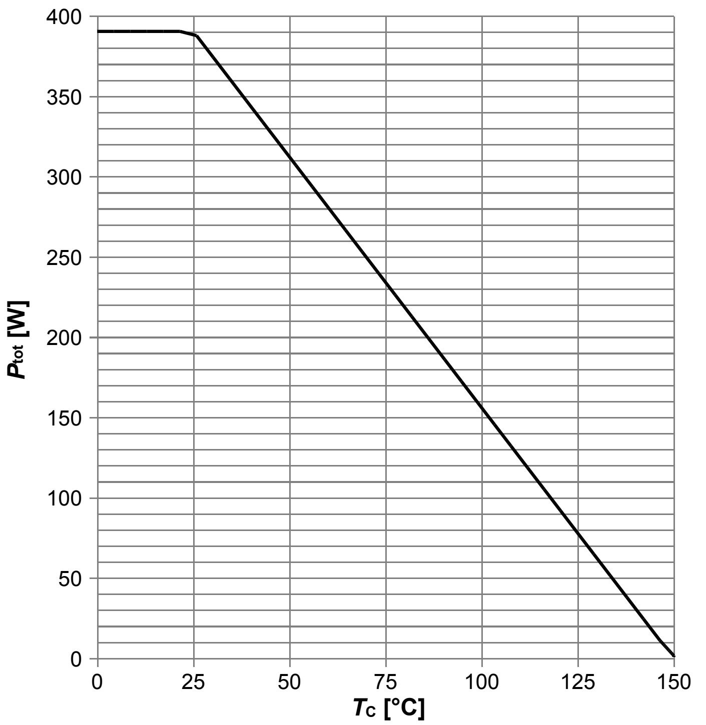
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.8	-	V	V_{GS}=0V, I_F=28.9A, T_j=25°C
Reverse recovery time	t_{rr}	-	600	-	ns	V_R=400V, I_F=28.9A, di_F/dt=60A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	9	-	µC	V_R=400V, I_F=28.9A, di_F/dt=60A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	30	-	A	V_R=400V, I_F=28.9A, di_F/dt=60A/µs; see table 8

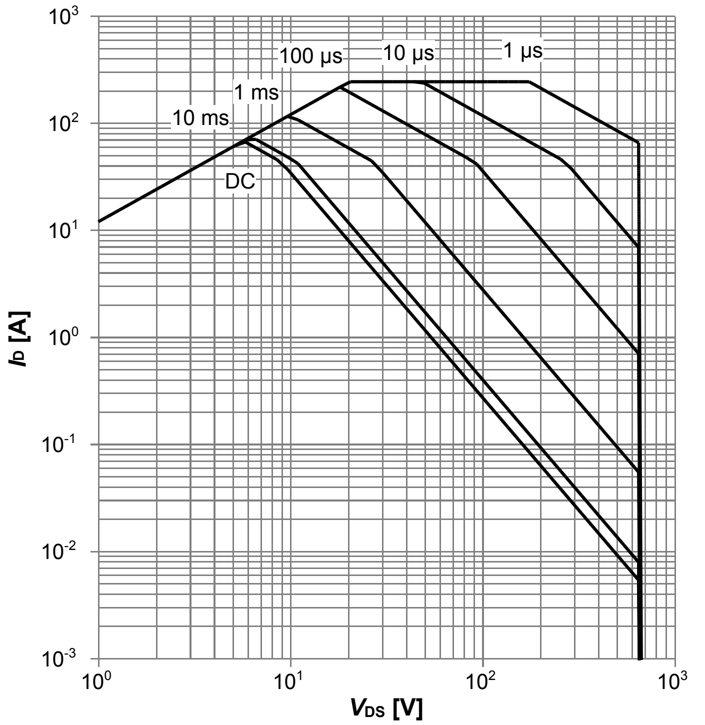
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



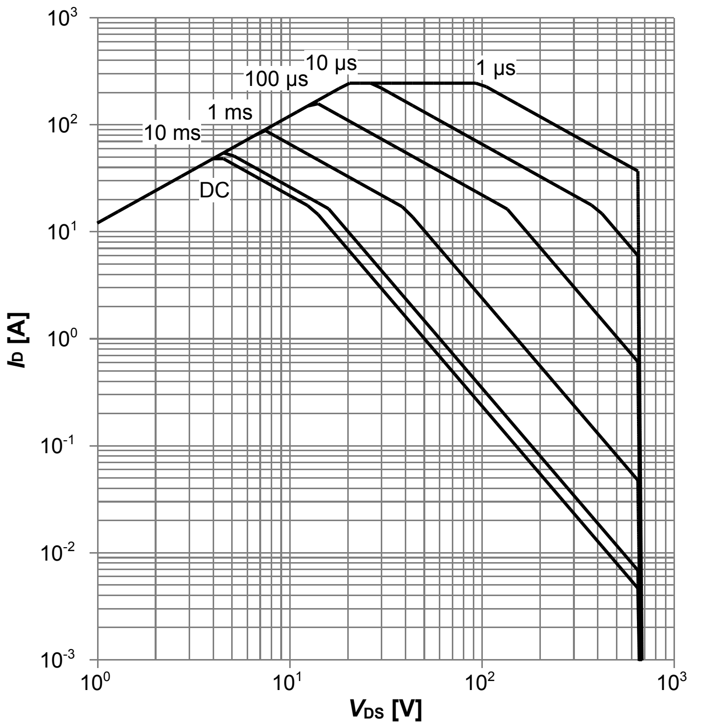
P_{tot}=f(T_C)

Diagram 2: Safe operating area



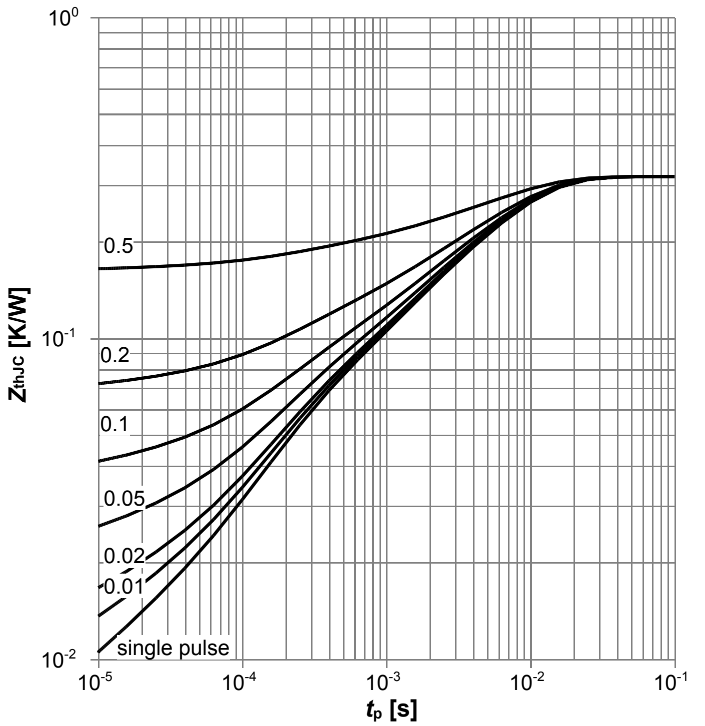
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



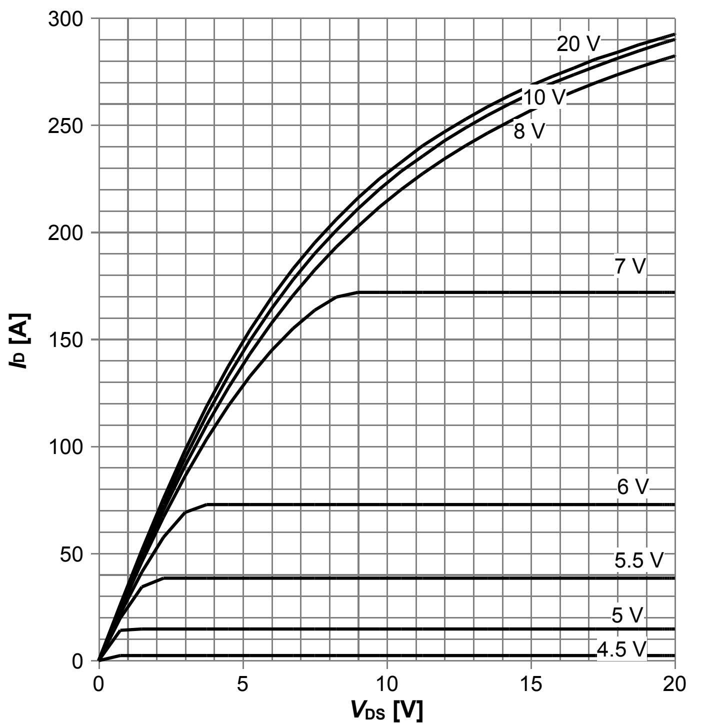
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



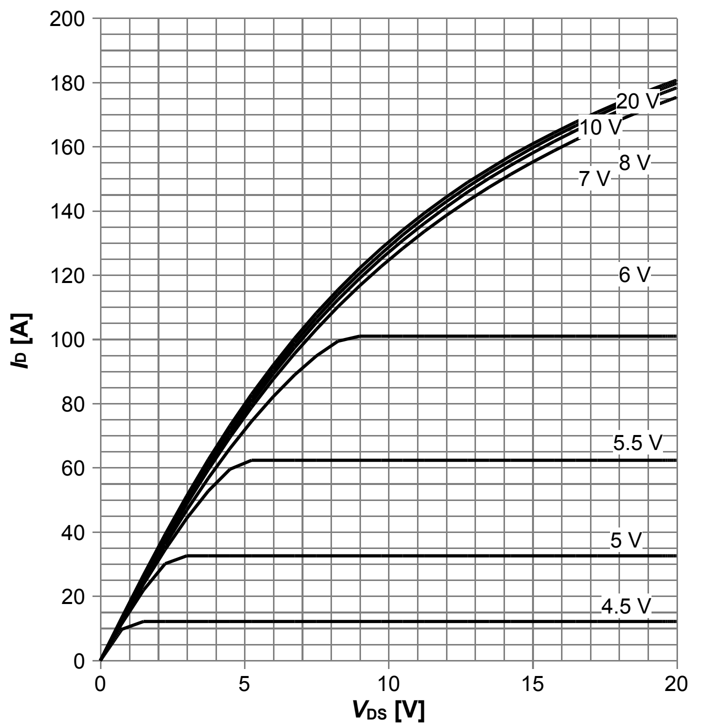
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



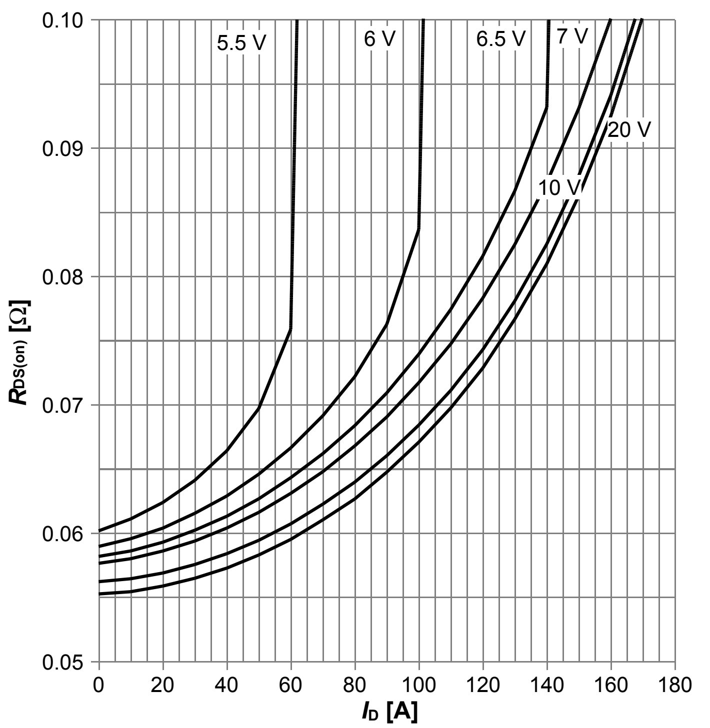
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



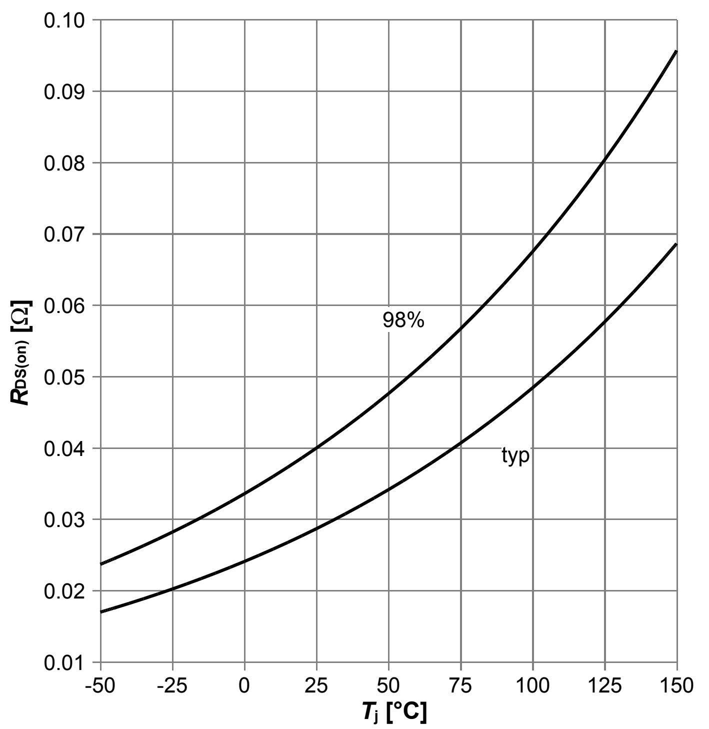
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



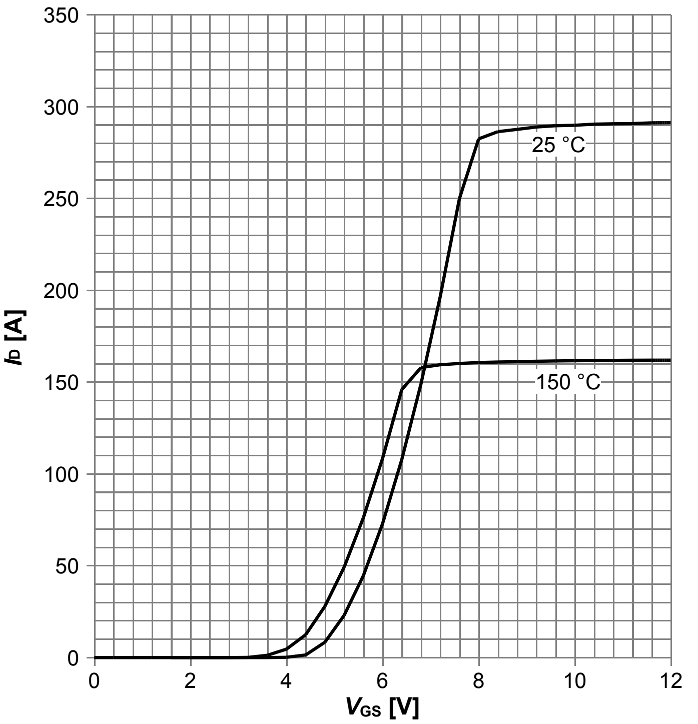
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



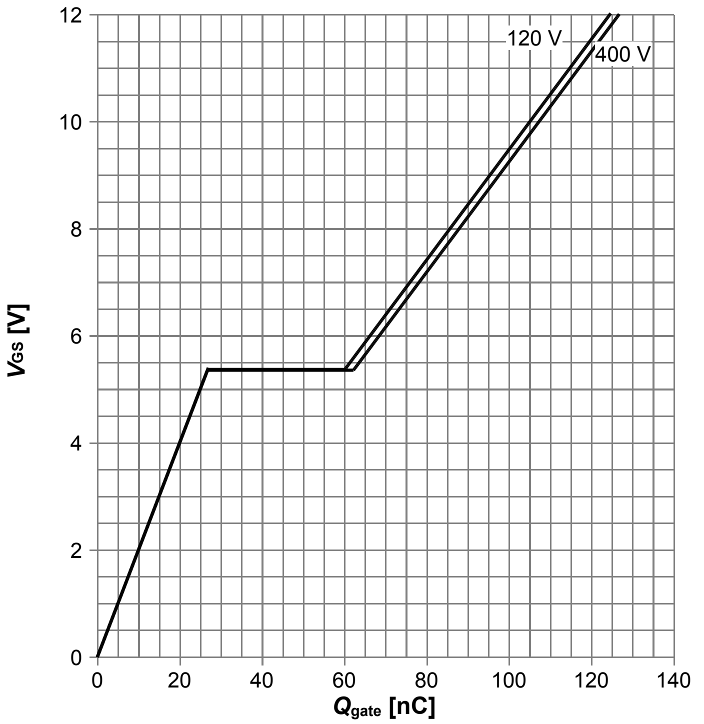
$R_{DS(on)}$=f(T_j); I_D=28.9 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



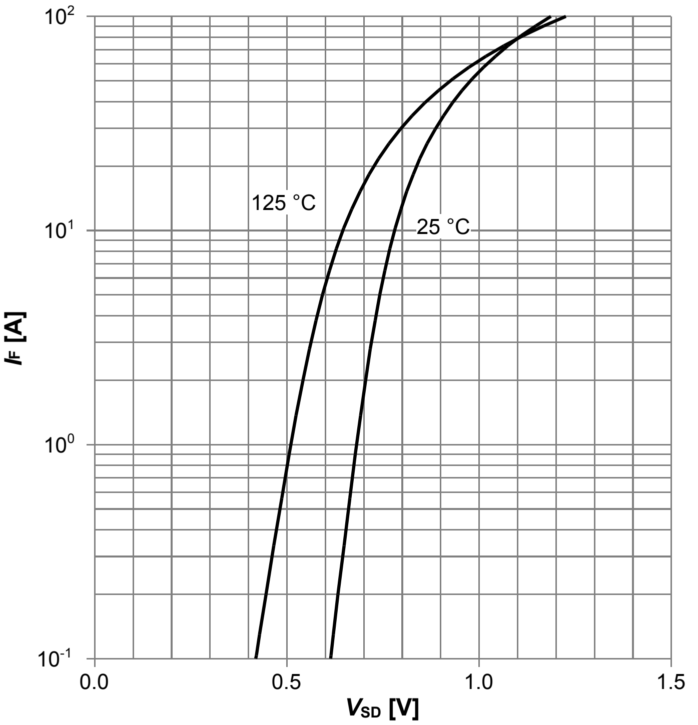
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



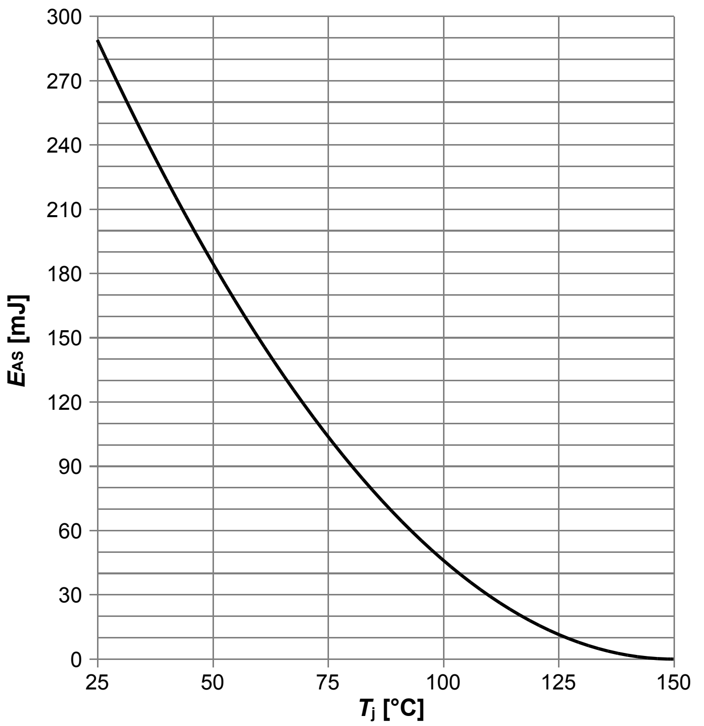
V_{GS}=f(Q_{gate}); I_D=28.9 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



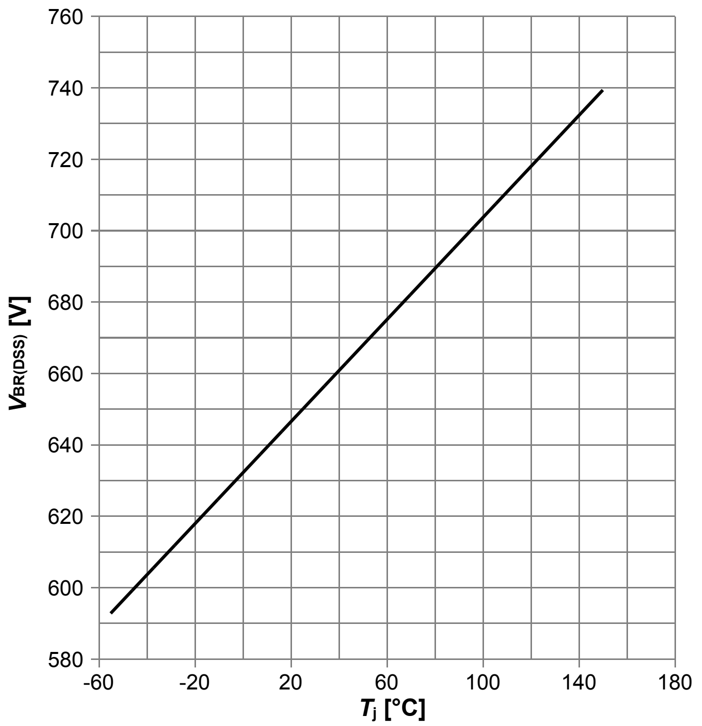
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



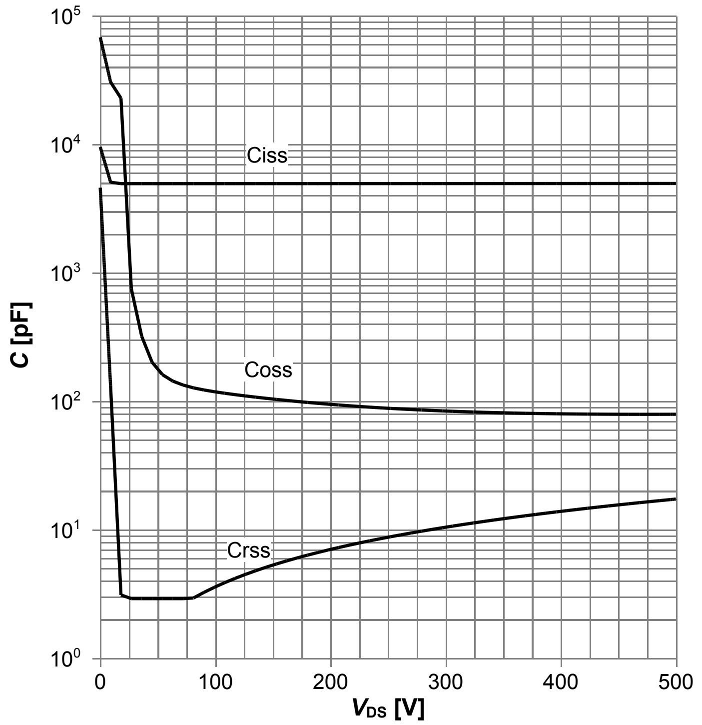
E_{AS}=f(T_j); I_D=12.5 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



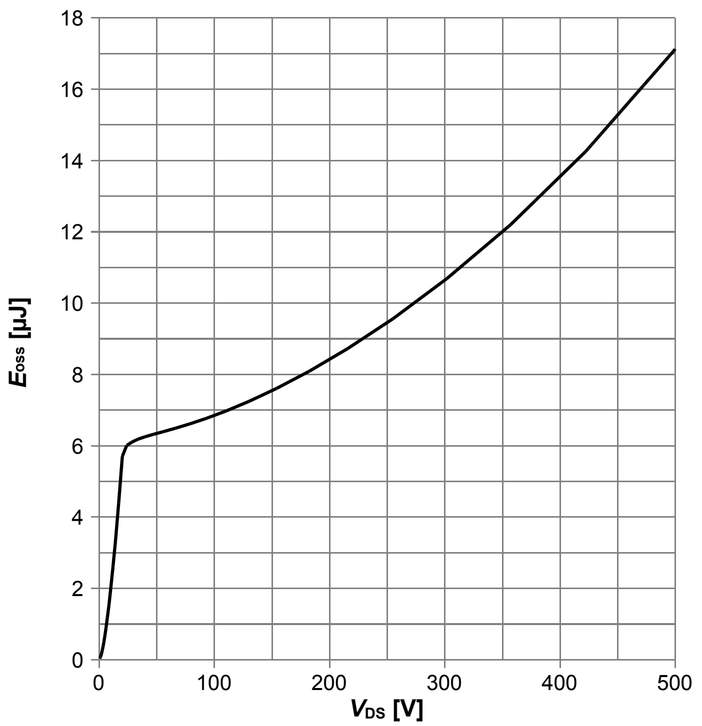
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

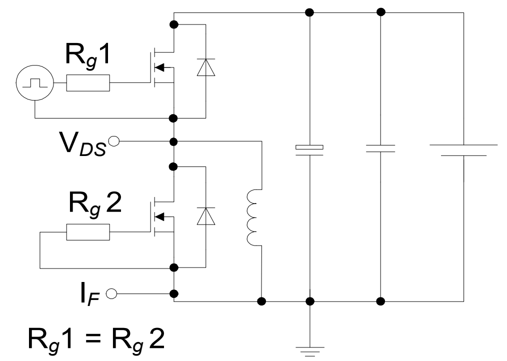
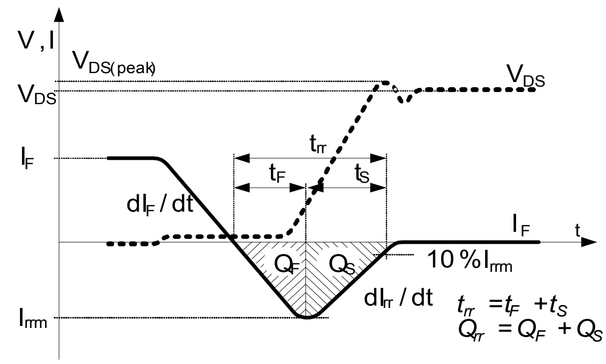
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 switching times (ss)

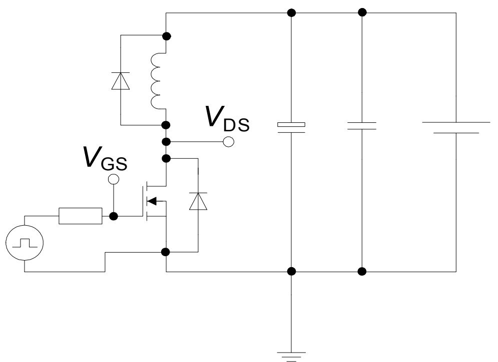
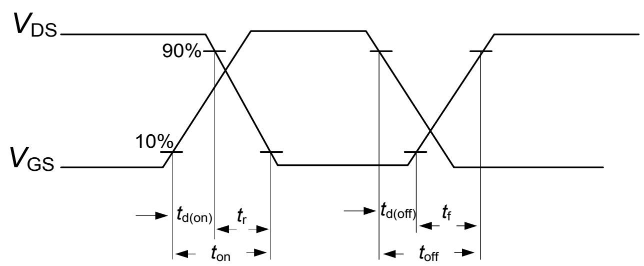
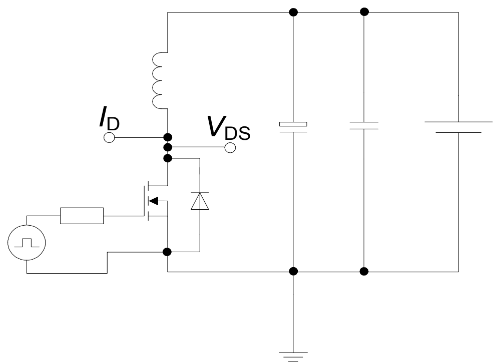
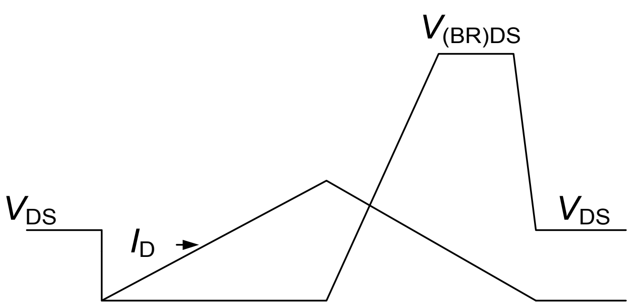
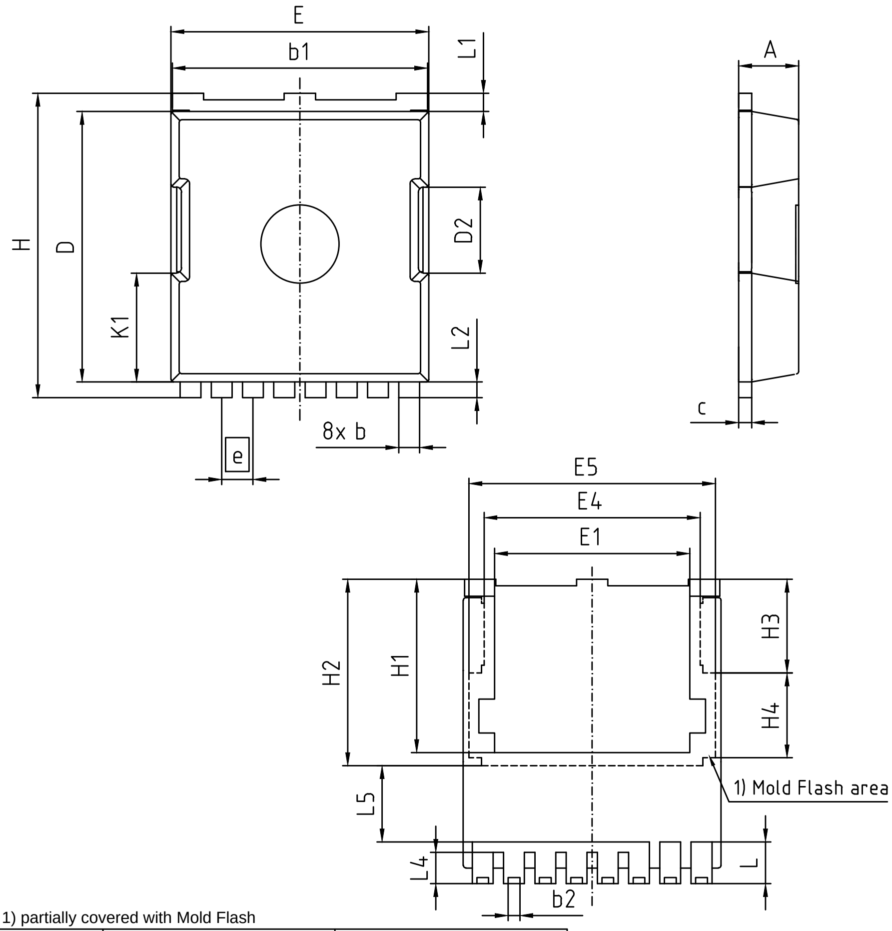
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



1) partially covered with Mold Flash

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
b	0.70	0.90	0.028	0.035
b1	9.70	9.90	0.382	0.390
b2	0.42	0.50	0.017	0.020
c	0.40	0.60	0.016	0.024
D	10.28	10.58	0.405	0.416
D2	3.30		0.130	
E	9.70	10.10	0.382	0.398
E1	7.50		0.295	
E4	8.50		0.335	
E5	9.46		0.372	
e	1.20 (BSC)		0.047 (BSC)	
H	11.48	11.88	0.452	0.468
H1	6.55	6.75	0.258	0.266
H2	7.15		0.281	
H3	3.59		0.141	
H4	3.26		0.128	
N	8		8	
K1	4.18		0.165	
L	1.40	1.80	0.055	0.071
L1	0.50	0.90	0.020	0.035
L2	0.50	0.70	0.020	0.028
L4	1.00	1.30	0.039	0.051
L5	2.62	2.81	0.103	0.111

DOCUMENT NO.
Z8B00176939

SCALE

0 2 4mm

EUROPEAN PROJECTION

ISSUE DATE
28-04-2015

REVISION
01

Figure 1 Outline PG-HSOF-8

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS™ C7 Webpage:** www.infineon.com
- **IFX CoolMOS™ C7 application note:** www.infineon.com
- **IFX CoolMOS™ C7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPT65R033G7

Revision: 2016-03-14, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2016-03-01	Release of final version
2.1	2016-03-14	Page 1 format update

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Published by
Infineon Technologies AG
81726 München, Germany

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