

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C7

650V CoolMOS™ C7 Power Transistor
IPL65R130C7

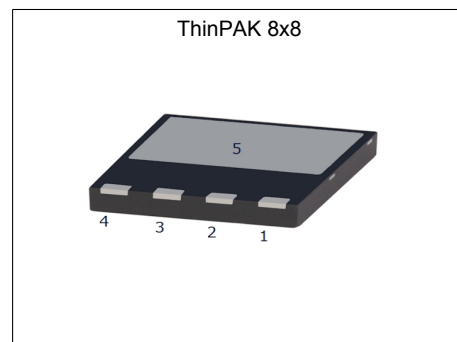
Data Sheet

Rev. 2.0
Final

1 Description

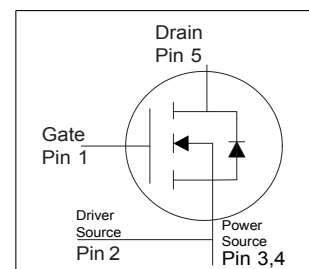
CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.



Features

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- **ThinPAK** SMD Package with very low parasitic inductance to enable fast and reliable switching with minimum of size to increase power-density
- Easy to use/drive due to **driver source pin** for better control of the gate.
- Pb-free plating, halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)



Benefits

- Enabling higher system efficiency by lower switching losses
- Enabling higher frequency / increased power density solutions
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures



Applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	130	mΩ
$Q_{g,typ}$	35	nC
$I_{D,pulse}$	75	A
$E_{oss}@400V$	4.2	μJ
Body diode di/dt	55	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPL65R130C7	PG-VSON-4	65C7130	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	15 11	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	75	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	89	mJ	$I_D=7.1\text{A}$; $V_{DD}=50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.44	mJ	$I_D=7.1\text{A}$; $V_{DD}=50\text{V}$
Avalanche current, single pulse	I_{AS}	-	-	7.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	102	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	15	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	75	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1.5	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$
Maximum diode commutation speed	di/dt	-	-	55	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_G .

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.22	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL3

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.44mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=650$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.115 0.276	0.130 -	Ω	$V_{GS}=10V$, $I_D=4.4A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=4.4A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	1	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1670	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	26	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	53	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	579	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=4.4A$, $R_G=10\Omega$
Rise time	t_r	-	5.3	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=4.4A$, $R_G=10\Omega$
Turn-off delay time	$t_{d(off)}$	-	87	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=4.4A$, $R_G=10\Omega$
Fall time	t_f	-	12	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=4.4A$, $R_G=10\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8	-	nC	$V_{DD}=400V$, $I_D=4.4A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	11	-	nC	$V_{DD}=400V$, $I_D=4.4A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	35	-	nC	$V_{DD}=400V$, $I_D=4.4A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	$V_{DD}=400V$, $I_D=4.4A$, $V_{GS}=0$ to $10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.8	-	V	$V_{GS}=0V$, $I_F=4.4A$, $T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	630	-	ns	$V_R=400V$, $I_F=15A$, $di_F/dt=55A/\mu s$
Reverse recovery charge	Q_{rr}	-	6.4	-	μC	$V_R=400V$, $I_F=15A$, $di_F/dt=55A/\mu s$
Peak reverse recovery current	I_{rrm}	-	20	-	A	$V_R=400V$, $I_F=15A$, $di_F/dt=55A/\mu s$

5 Electrical characteristics diagrams

Table 8

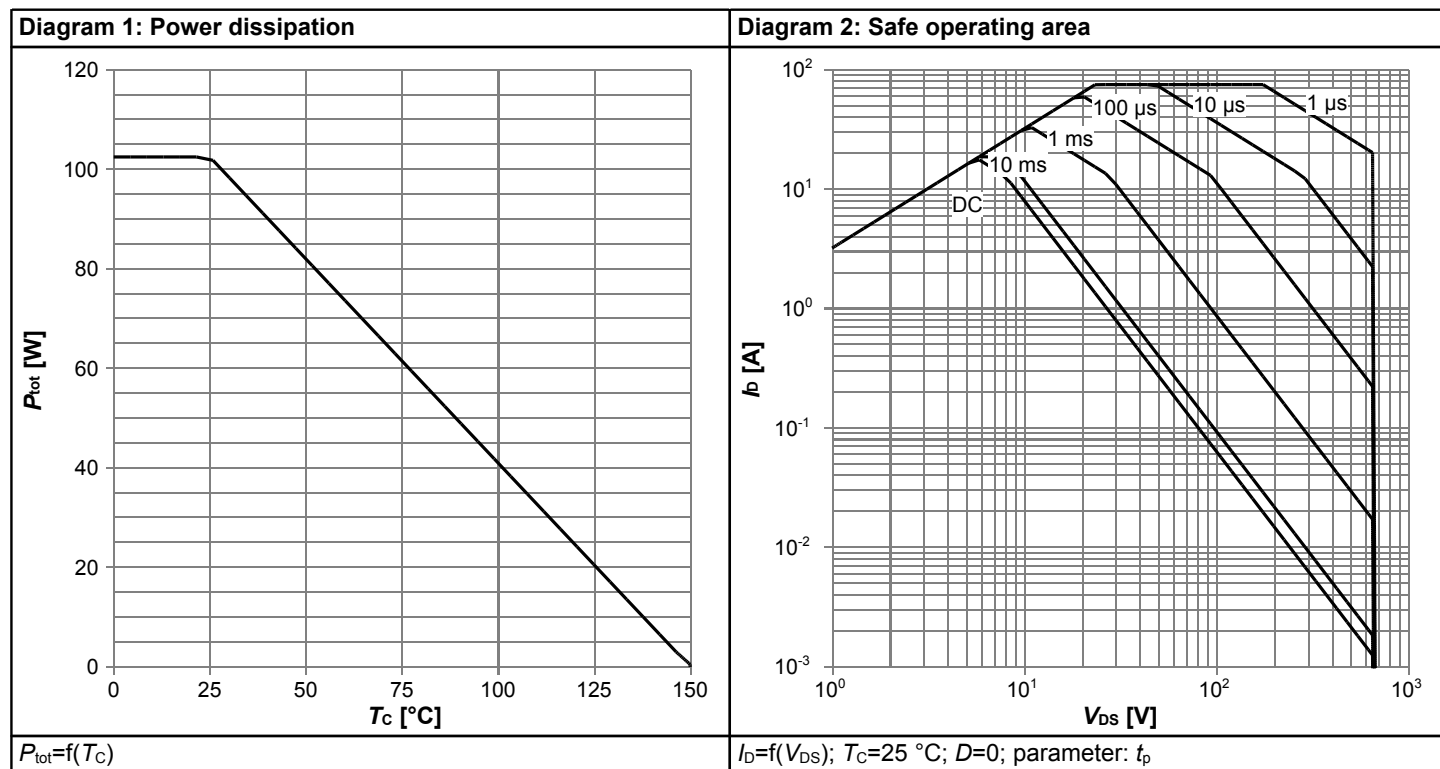


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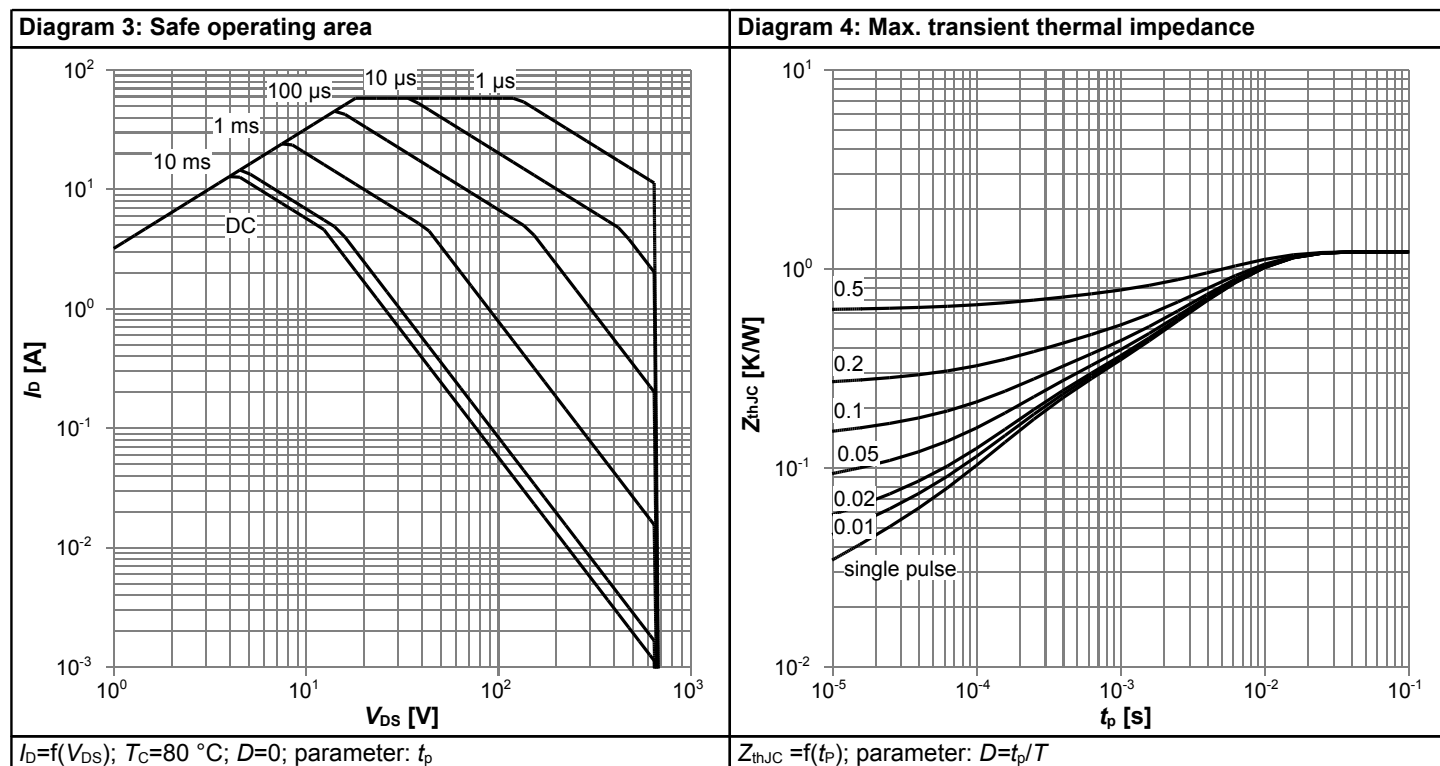


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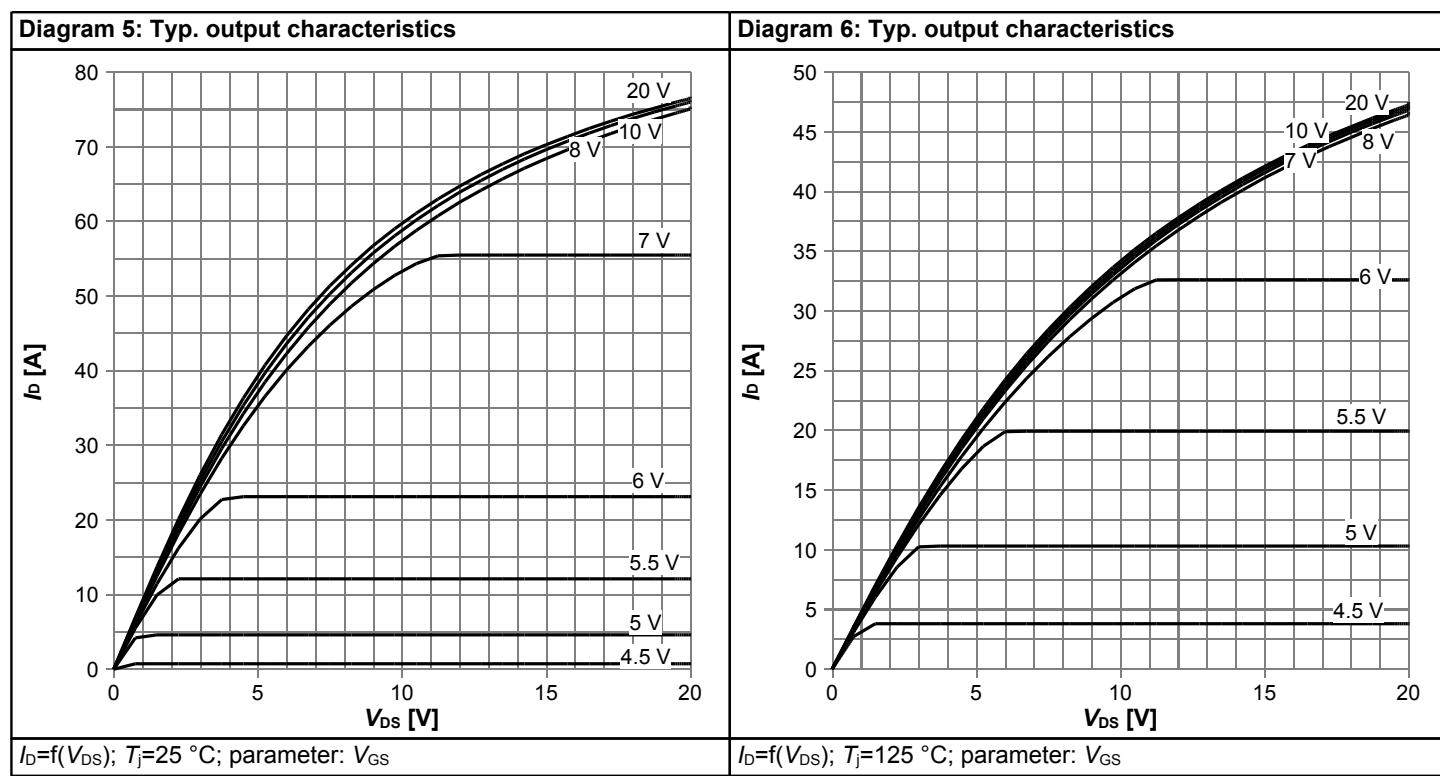


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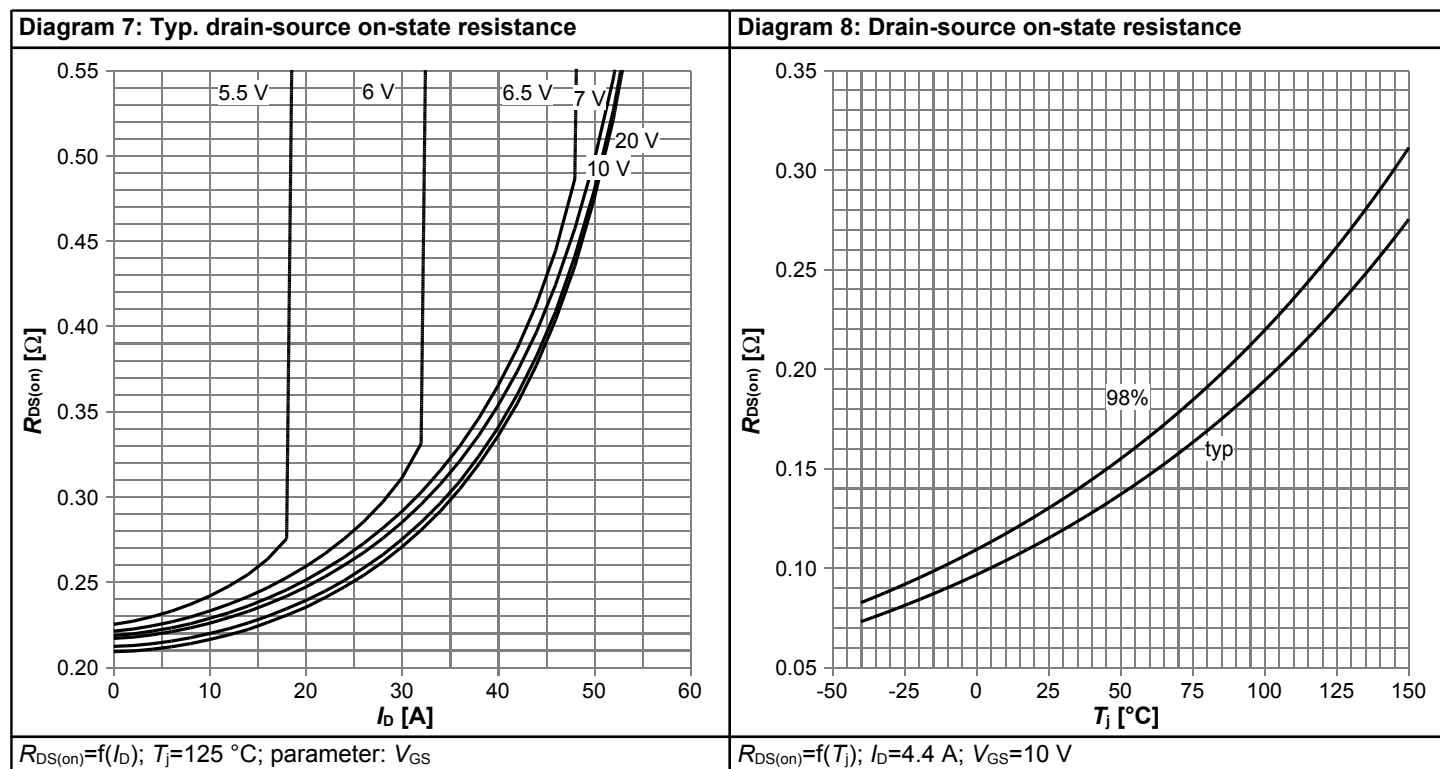


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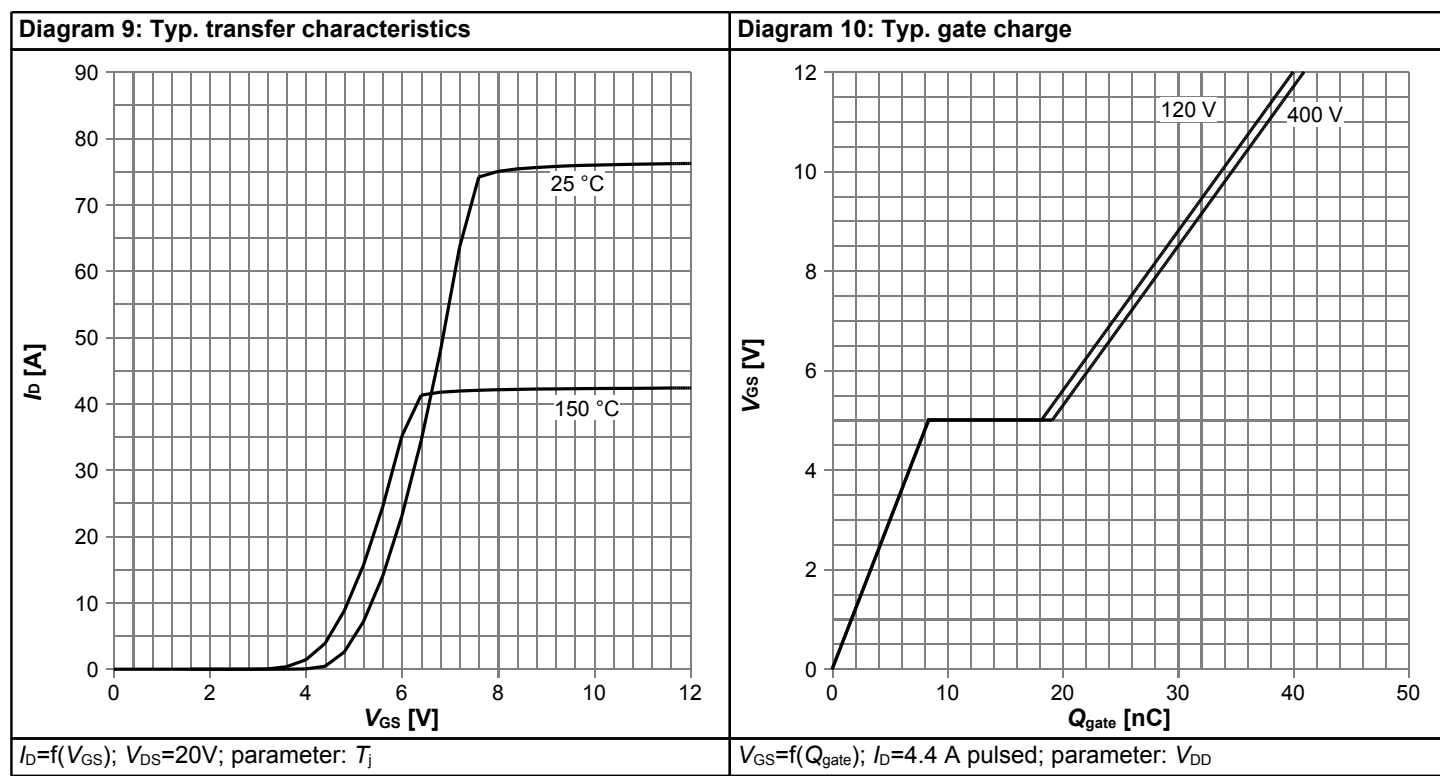


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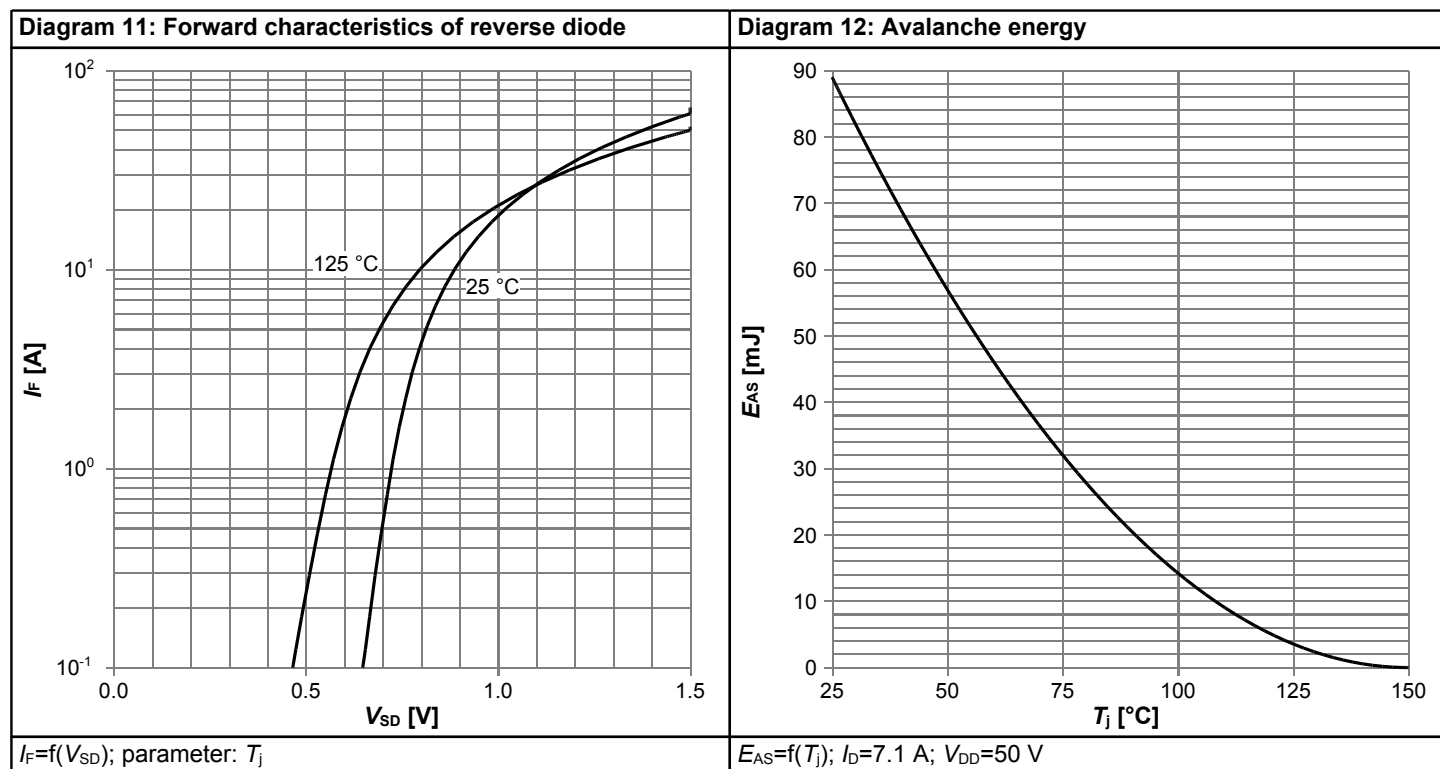


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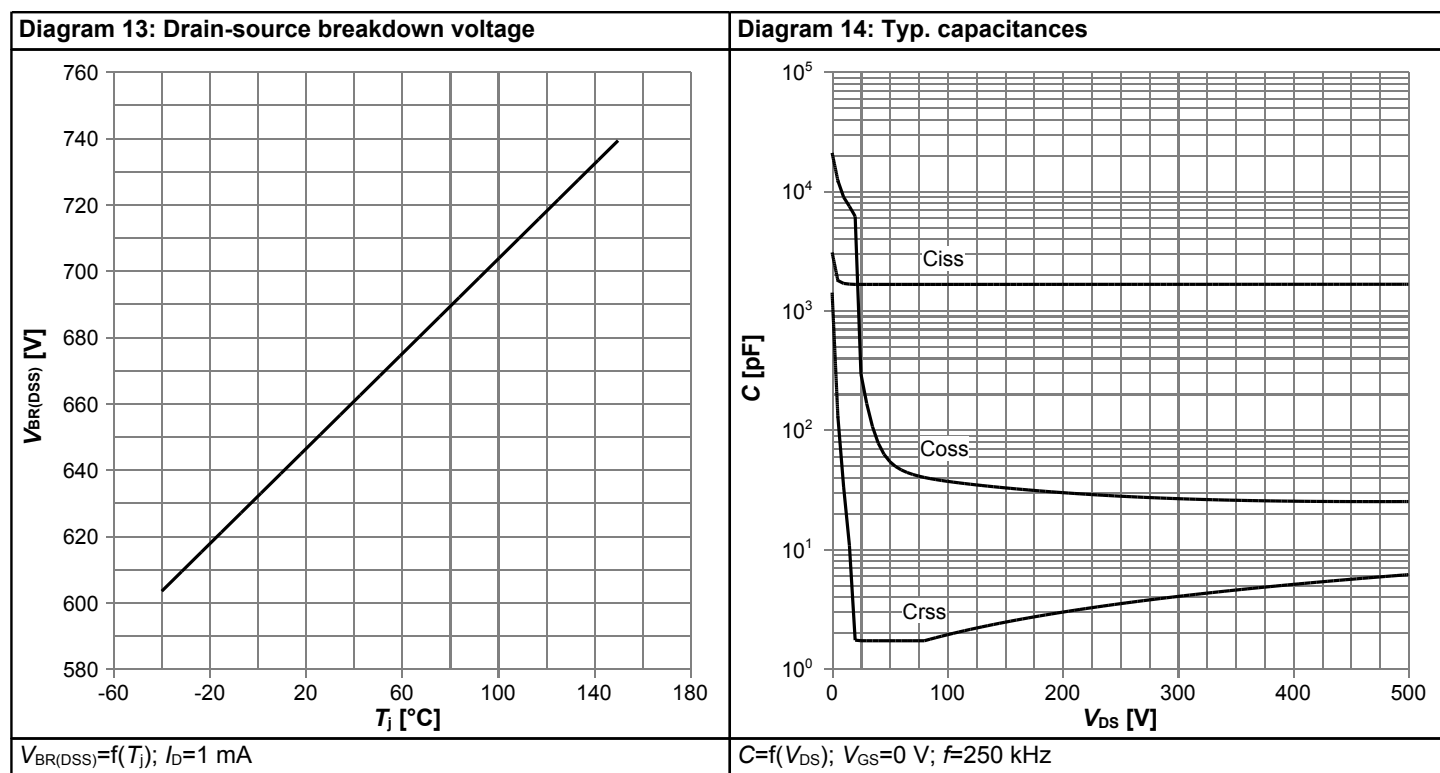
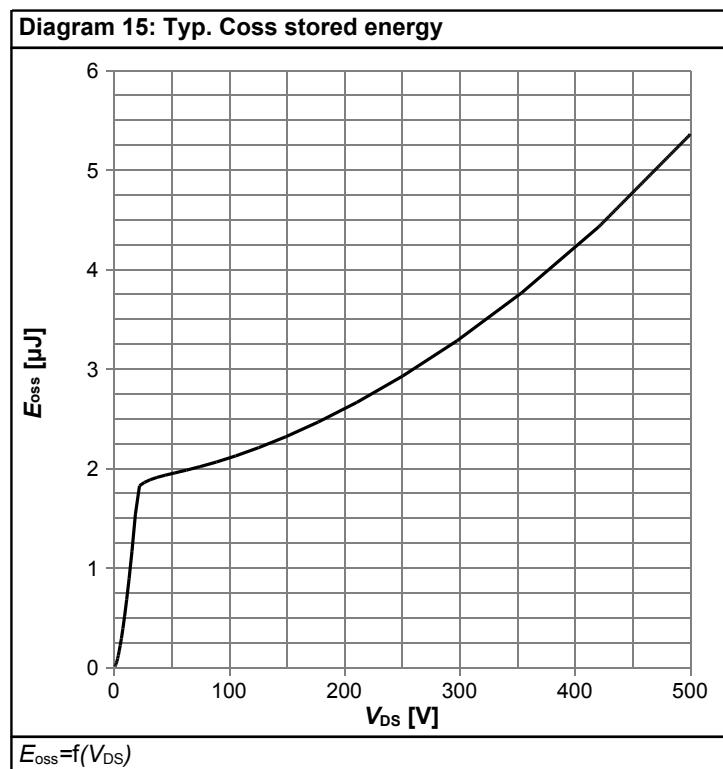


Table 15



6 Test Circuits

Table 16 Diode characteristics

Test circuit for diode characteristics

$R_{g1} = R_{g2}$

Diode recovery waveform

$t_{rr} = t_F + t_S$
 $Q_{rr} = Q_F + Q_S$

Table 17 switching times (ss)

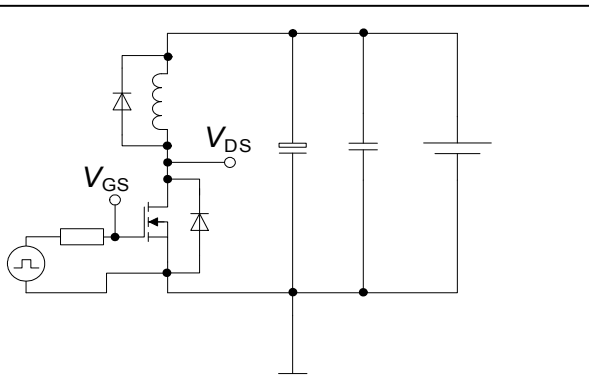
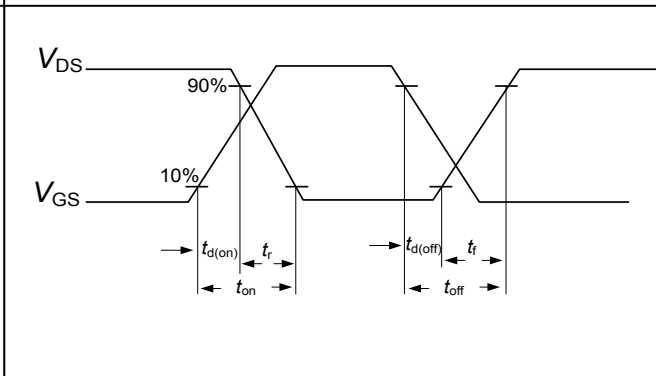
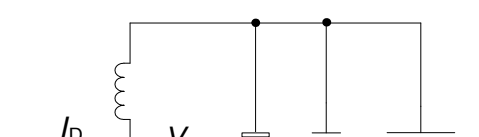
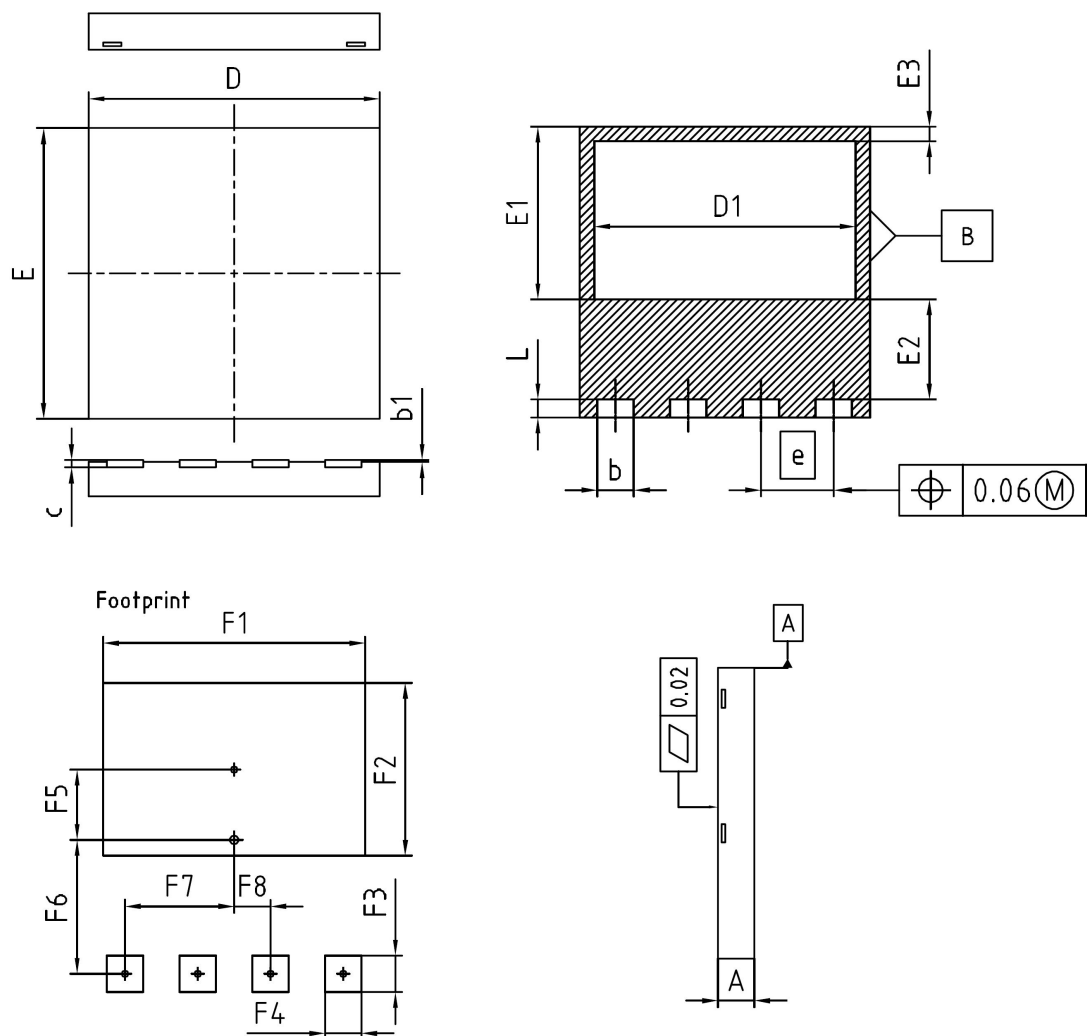
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a switching test setup for an inductive load. A MOSFET is driven by a pulse generator connected to its gate through a resistor. The drain of the MOSFET is connected to an inductor and a diode in series, which is then connected to a DC voltage source. The source of the MOSFET is connected to ground. The drain-source voltage (V_{DS}) is measured across the inductor and diode, and the gate-source voltage (V_{GS}) is measured across the gate. The diode is oriented such that it allows current to flow from the DC source to the MOSFET drain during the off-state.	 The timing diagram shows the relationship between the drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}) during switching transitions. The V_{GS} waveform is a square wave that transitions between a high level and a low level. The V_{DS} waveform shows the voltage across the load during these transitions. Key parameters are defined as follows: $t_{d(on)}$: Delay time from the 10% rise of V_{GS} to the 90% rise of V_{DS}. t_r: Rise time of V_{DS} from 90% to 100%. t_{on}: Total turn-on time, the sum of $t_{d(on)}$ and t_r. $t_{d(off)}$: Delay time from the 90% fall of V_{GS} to the 90% fall of V_{DS}. t_f: Fall time of V_{DS} from 90% to 10%. t_{off}: Total turn-off time, the sum of $t_{d(off)}$ and t_f.

Table 18 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

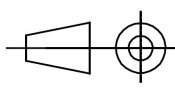
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ISSUE DATE 05-04-2010
REVISION 01

Figure 1 Outline PG-VSON-4, dimensions in mm/inches

8 Appendix A

Table 19 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPL65R130C7

Revision: 2013-04-29, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-04-29	Release of final version

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

erratum@infineon.com

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