INA199 26-V, Bidirectional, Zero-Drift, Low- or High-Side, Voltage Output Current Shunt Monitor

1 Features

- Wide Common-Mode Range: –0.3 V to 26 V
- Offset Voltage: ±150 µV (Maximum)
  (Enables shunt drops of 10-mV full-scale)
- Accuracy
  - ±1.5% Gain Error (Maximum Over Temperature)
  - 0.5-µV/°C Offset Drift (Maximum)
  - 10-ppm/°C Gain Drift (Maximum)
- Choice of Gains:
  - INA199x1: 50 V/V
  - INA199x2: 100 V/V
  - INA199x3: 200 V/V
- Quiescent Current: 100 µA (Maximum)
- Packages: SC70, UQFN-10

2 Applications

- Notebook Computers
- Cell Phones
- Qi-Compliant Wireless Charging Transmitters
- Telecom Equipment
- Power Management
- Battery Chargers
- Welding Equipment

3 Description

The INA199 series of voltage output, current shunt monitors (also called current-sense amplifiers) can sense drops across shunts at common-mode voltages from –0.3 V to 26 V, independent of the supply voltage. Three fixed gains are available: 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale.

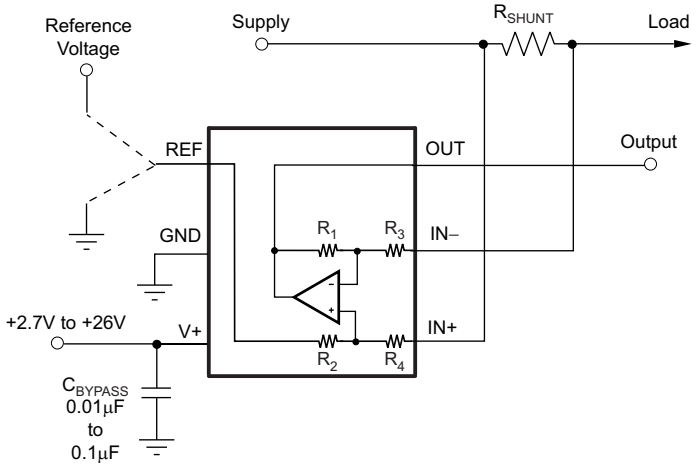
These devices operate from a single 2.7-V to 26-V power supply, drawing a maximum of 100 µA of supply current. All versions are specified from –40°C to 105°C, and offered in both SC70-6 and thin UQFN-10 packages.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA199	SC70 (6)	2.00 mm × 1.25 mm
	UQFN (10)	1.80 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2012) to Revision E — **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (August 2012) to Revision D — **Page**

- Changed Frequency Response, *Bandwidth* parameter in Electrical Characteristics table ... 6
- Updated Figure 21 ... 14
- Updated Figure 22 ... 15

Changes from Revision B (February 2010) to Revision C — **Page**

- Added INA199Bx gains to fourth Features bullet ... 1
- Added INA199Bx data to Product Family Table ... 4
- Added INA199Bx data to Package Information table ... 4
- Added QFN package information to *Temperature Range* section of *Electrical Characteristics* table ... 6
- Added silicon version B data to Input, *Common-Mode Input Range* parameter of Electrical Characteristics table ... 7
- Updated Figure 3 ... 8
- Updated Figure 9 ... 9
- Updated Figure 12 ... 9
- Changed last paragraph of the *Selecting* R_S section to cover both INA199Ax and INA199Bx versions ... 13
- Changed *Input Filtering* section ... 14
- Added *Improving Transient Robustness* section ... 18

Changes from Revision A (June 2009) to Revision B **Page**

- Deleted ordering information content from Package/Ordering table 4
- Updated DCK pinout drawing 4

Changes from Original (April 2009) to Revision A **Page**

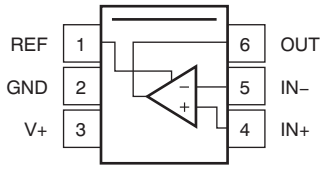
- Added *ordering number* and *transport media, quantity* columns to *Package/Ordering Information* table 4

5 Device Comparison Table

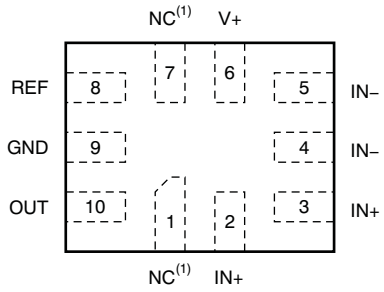
PRODUCT	GAIN	R_3 AND R_4	R_1 AND R_2
INA199x1	50	20 kΩ	1 MΩ
INA199x2	100	10 kΩ	1 MΩ
INA199x3	200	5 kΩ	1 MΩ

6 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



RSW Package
10-Pin UQFN
Top View



(1) NC denotes no internal connection. These pins can be left floating or connected to any voltage between GND and V+.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SC70	UQFN		
GND	2	9	Analog	Ground
IN–	5	4, 5	Analog input	Connect to load side of shunt resistor.
IN+	4	2, 3	Analog input	Connect to supply side of shunt resistor.
NC	—	1, 7	—	Not internally connected. Leave floating or connect to ground.
OUT	6	10	Analog output	Output voltage
REF	1	8	Analog input	Reference voltage, 0 V to V+
V+	3	6	Analog	Power supply, 2.7 V to 26 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage			26	V
Analog inputs, V_{IN+}, V_{IN-} (2)	Differential (V_{IN+}) – (V_{IN-})	–26	26	V
	Common-mode (3)	GND – 0.3	26	V
REF input		GND – 0.3	(V+) + 0.3	V
Output (3)		GND – 0.3	(V+) + 0.3	V
Input current Into all pins (3)			5	mA
Operating temperature		–40	125	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5 mA.

7.2 ESD Ratings

			VALUE	UNIT
INA199A1, INA199A2, and INA199A3 in DCK and RSW Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine Model (MM)	±200	
INA199B1, INA199B2, and INA199B3 in DCK and RSW Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine Model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage (applied to V+)		5		V
T_A	Operating free-air temperature	–40		105	°C

7.4 Thermal Information

THERMAL METRIC[1]		INA199		UNIT
		DCK (SC70)	RSW (UQFN)	
		6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.3	107.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.1	18.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.4	18.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, T_A = 25°C

At T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, $V_{SENSE} = V_{IN+} - V_{IN-}$, and $V_{REF} = V_S / 2$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage, RTI[1]		V_{SENSE} = 0 mV		±5	±150	µV
PSR	Power supply rejection		V_S = 2.7 V to 18 V, V_{IN+} = 18 V, V_{SENSE} = 0 mV		±0.1		µV/V
I_B	Input bias current		V_{SENSE} = 0 mV		28		µA
I_{OS}	Input offset current		V_{SENSE} = 0 mV		±0.02		µA
OUTPUT							
G	Gain	INA199x1			50		V/V
		INA199x2			100		V/V
		INA199x3			200		V/V
	Nonlinearity error		V_{SENSE} = –5 mV to 5 mV		±0.01%		
	Maximum capacitive load		No Sustained Oscillation		1		nF
FREQUENCY RESPONSE							
GBW	Bandwidth		C_{LOAD} = 10 pF, INA199A1 and INA199B1		80		kHz
			C_{LOAD} = 10 pF, INA199A2 and INA199B2		30		kHz
			C_{LOAD} = 10 pF, INA199A3 and INA199B3		14		kHz
SR	Slew rate				0.4		V/µs
NOISE, RTI[1]							
Voltage Noise Density					25		nV/√Hz
POWER SUPPLY							
V_S	Operating voltage range		–20°C to 85°C			26	V
I_Q	Quiescent current		V_{SENSE} = 0 mV		65	100	µA
TEMPERATURE RANGE							
	Specified range			–40		105	°C
	Operating range			–40		125	°C

(1) RTI = Referred-to-input.

7.6 Electrical Characteristics, T_A = –40°C to 105°C

At T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, $V_{SENSE} = V_{IN+} - V_{IN–}$, and $V_{REF} = V_S / 2$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{CM}	Common-mode input range		Version A	–0.3		26	V
			Version B	–0.1		26	V
CMR	Common-mode rejection		V_{IN+} = 0 V to 26 V, V_{SENSE} = 0 mV	100	120		dB
dV_{OS}/dT	Offset voltage, RTI(1) vs temperature				0.1	0.5	µV/°C
OUTPUT							
	Gain error		V_{SENSE} = –5 mV to 5 m V		±0.03%	±1.5%	
		vs temperature			3	10	ppm/°C
	Swing to V+ power-supply rail		R_L = 10 kΩ to GND		(V+) – 0.05	(V+) – 0.2	V
	Swing to GND		R_L = 10 kΩ to GND		(V_{GND}) + 0.005	(V_{GND}) + 0.05	V
POWER SUPPLY							
V_S	Operating voltage range			2.7		26	V
			–20°C to 85°C	2.5			V
I_Q	Quiescent current	over temperature				115	µA

(1) RTI = Referred-to-input.

7.7 Typical Characteristics

Performance measured with the INA199A3 at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

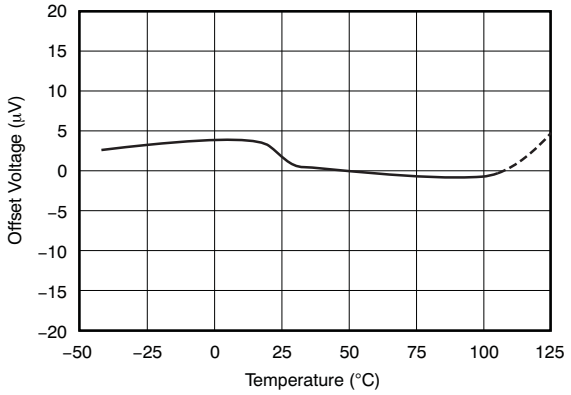


Figure 1. Offset Voltage vs Temperature

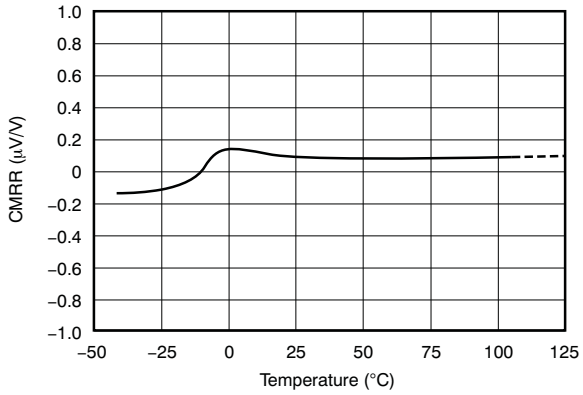


Figure 2. Common-Mode Rejection Ratio vs Temperature

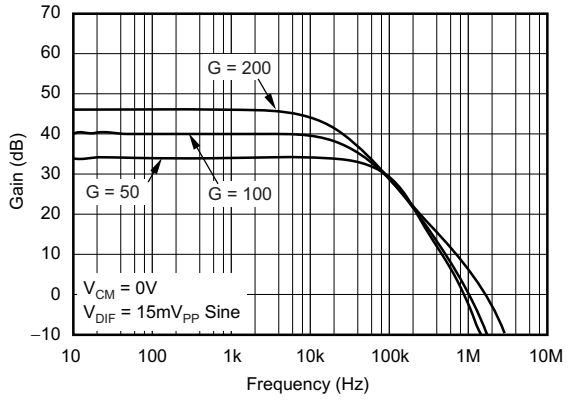


Figure 3. Gain vs Frequency

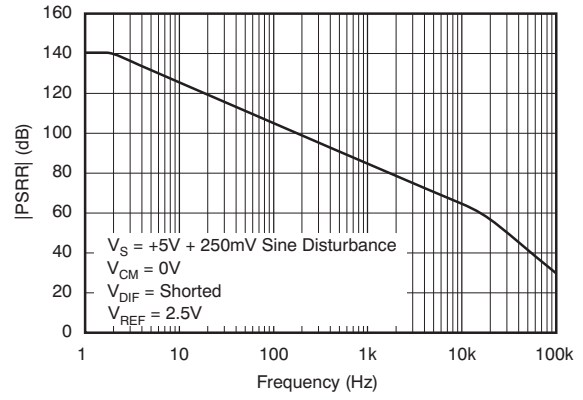


Figure 4. Power-Supply Rejection Ratio vs Frequency

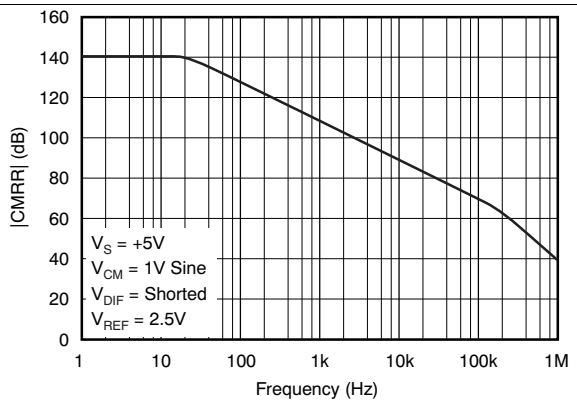


Figure 5. Common-Mode Rejection Ratio vs Frequency

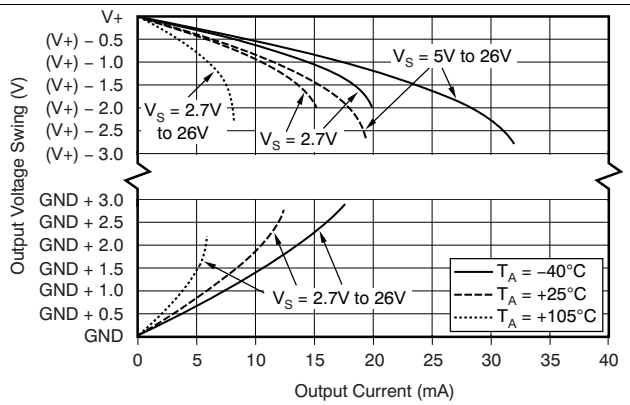
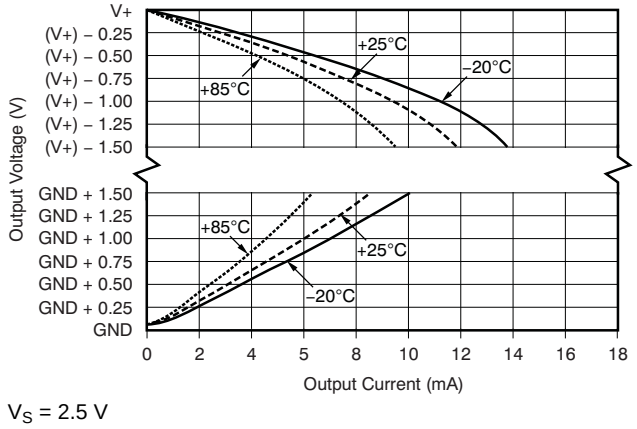


Figure 6. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

Performance measured with the INA199A3 at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.



V_S = 2.5 V

Figure 7. Output Voltage Swing vs Output Current

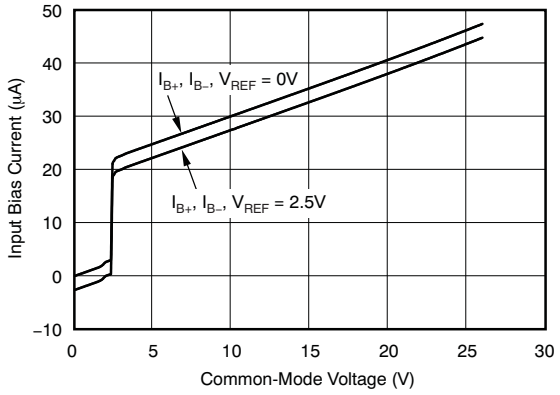


Figure 8. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 5 V

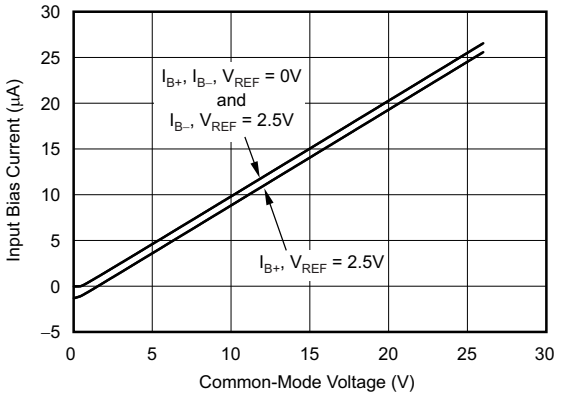


Figure 9. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 0 V (Shutdown)

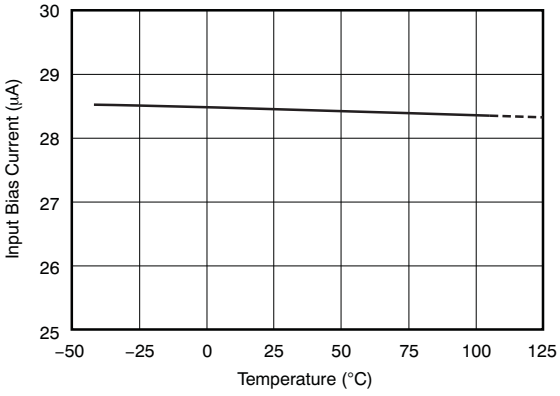


Figure 10. Input Bias Current vs Temperature

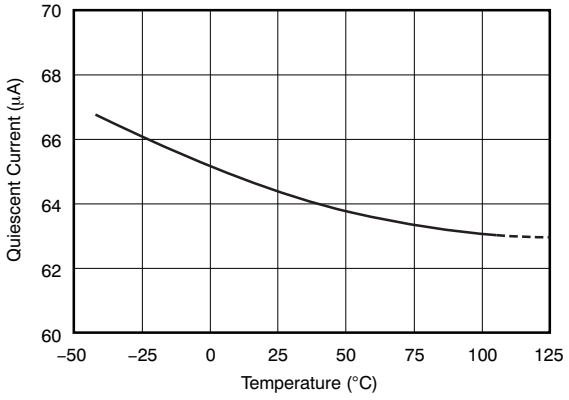


Figure 11. Quiescent Current vs Temperature

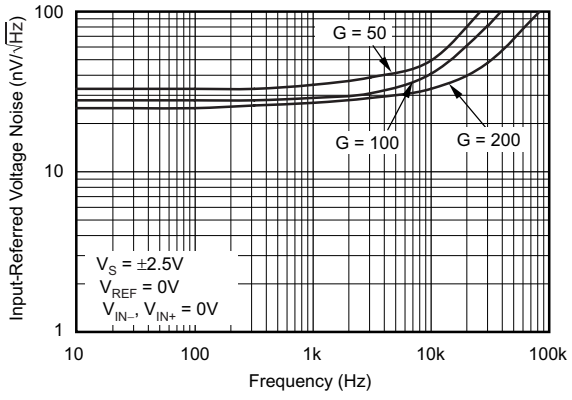


Figure 12. Input-Referred Voltage Noise vs Frequency

Typical Characteristics (continued)

Performance measured with the INA199A3 at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

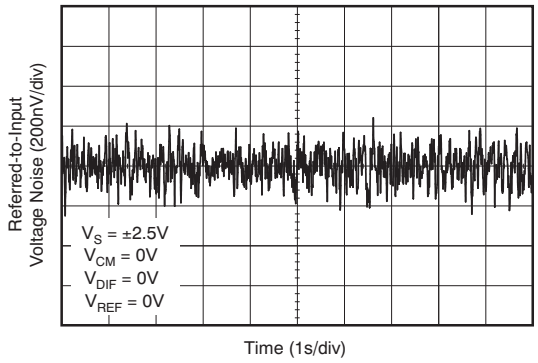


Figure 13. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

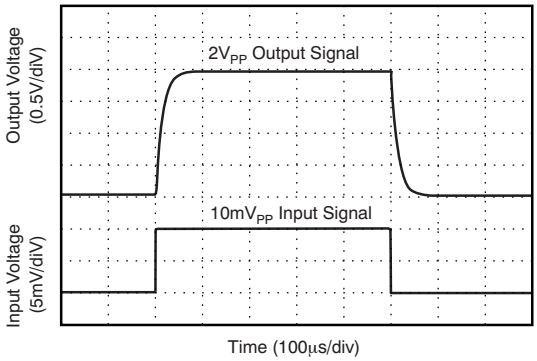


Figure 14. Step Response (10-mV_{PP} Input Step)

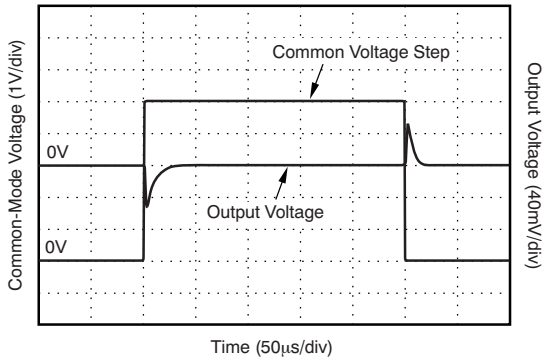


Figure 15. Common-Mode Voltage Transient Response

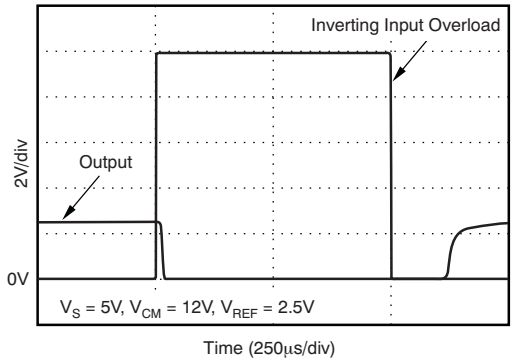


Figure 16. Inverting Differential Input Overload

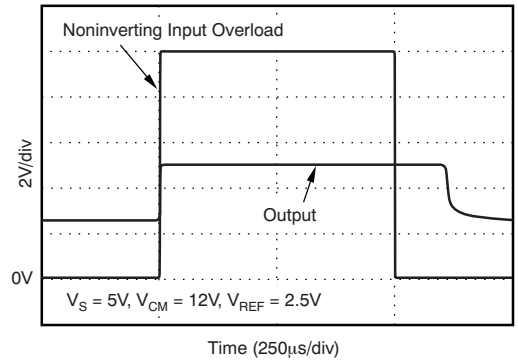


Figure 17. Noninverting Differential Input Overload

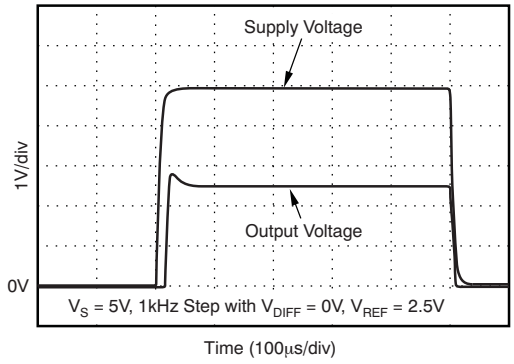


Figure 18. Start-Up Response

Typical Characteristics (continued)

Performance measured with the INA199A3 at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

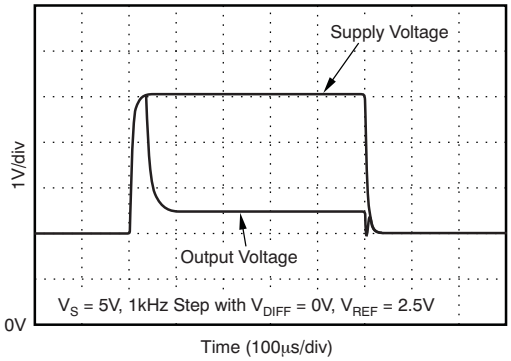


Figure 19. Brownout Recovery

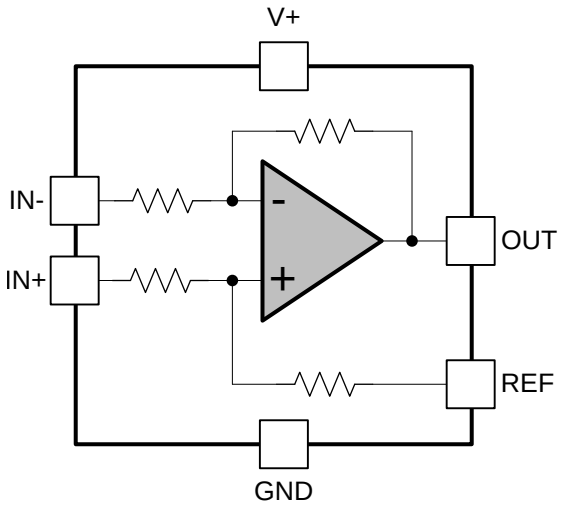
8 Detailed Description

8.1 Overview

The INA199 is a 26-V common mode, zero-drift topology, current-sensing amplifier that can be used in both low-side and high-side configurations. It is a specially-designed, current-sensing amplifier that is able to accurately measure voltages developed across a current-sensing resistor on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V while the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 150 µV with a maximum temperature contribution of 0.5 µV/°C over the full temperature range of –40°C to +105°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Basic Connections

Figure 20 shows the basic connections for the INA199. The input pins, IN+ and IN–, must be connected as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

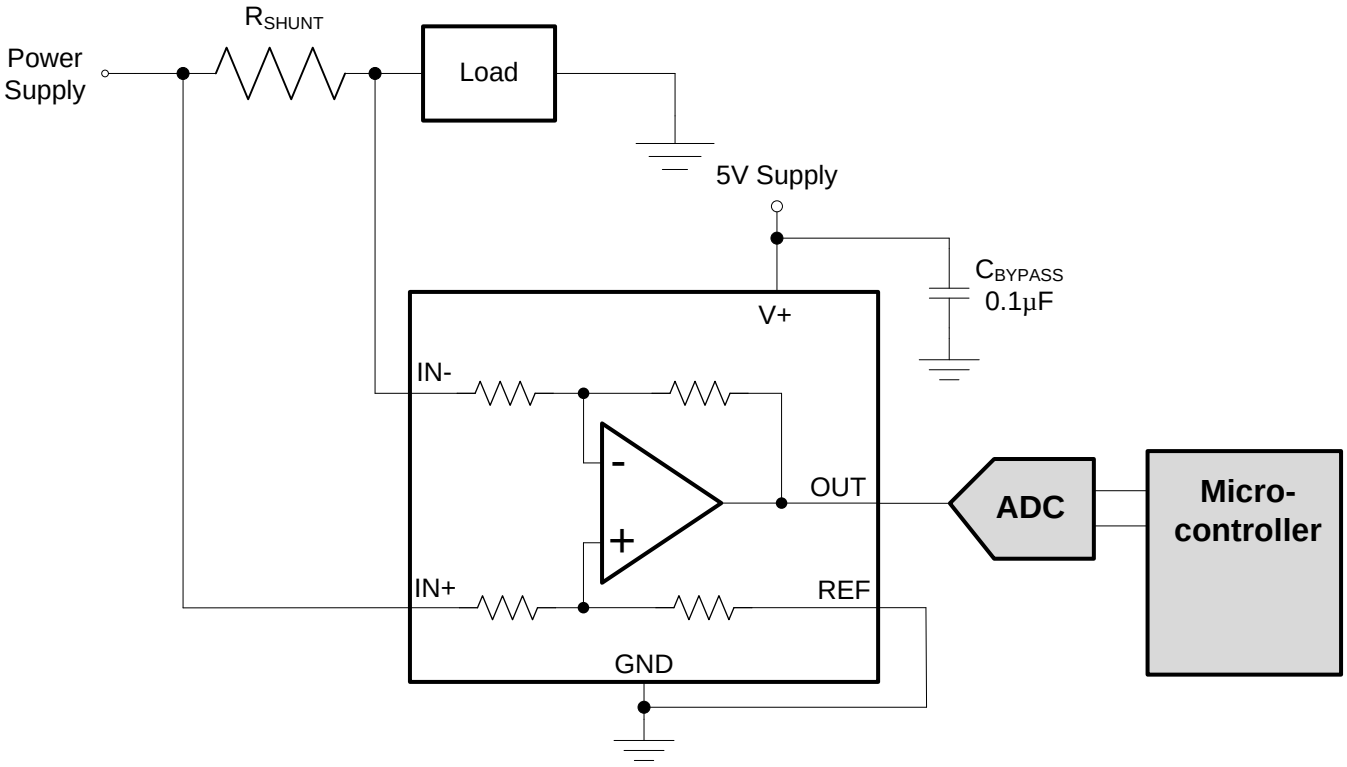


Figure 20. Typical Application

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

On the RSW package, two pins are provided for each input. These pins must be tied together (that is, tie IN+ to IN+ and tie IN– to IN–).

8.3.2 Selecting R_S

The zero-drift offset performance of the INA199 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current shunt monitors typically require a full-scale range of 100 mV.

The INA199 series gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gain of 50 or 100 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA199A1 operating on a 3.3-V supply could easily handle a full-scale shunt drop of 60 mV, with only 150 µV of offset.

8.4 Device Functional Modes

8.4.1 Input Filtering

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the ±30% tolerance of the internal resistances. Figure 21 shows a filter placed at the inputs pins.

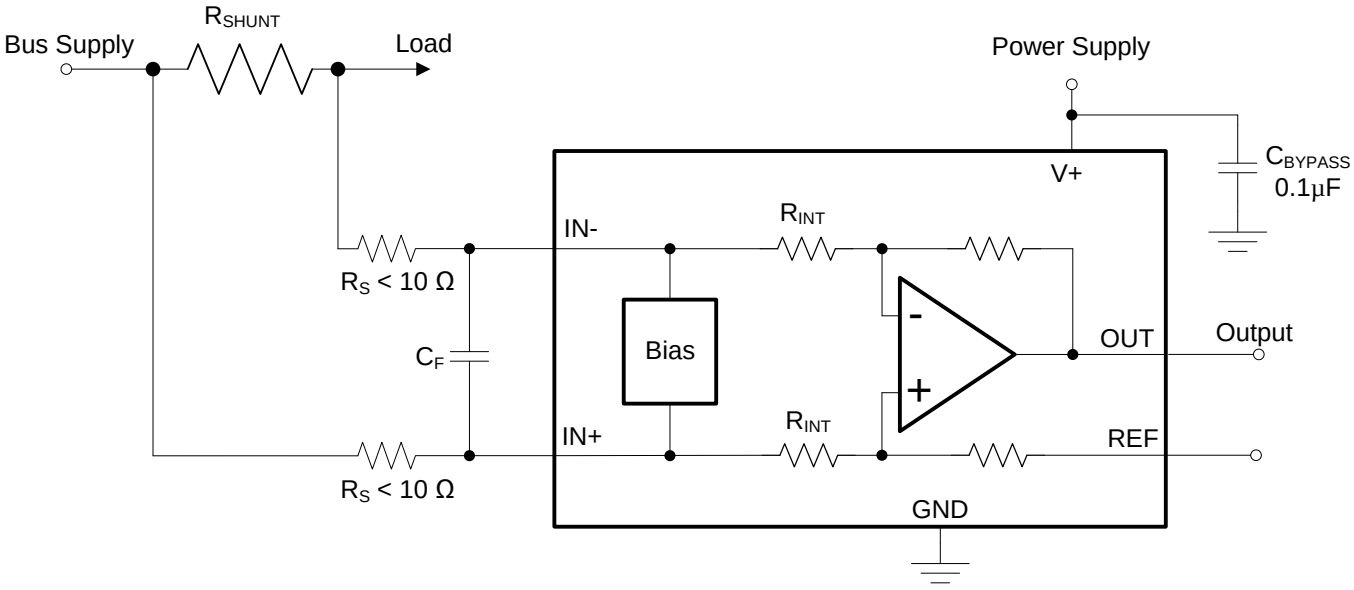


Figure 21. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors must be kept to 10 Ω (or less if possible) to reduce impact to accuracy. The internal bias network shown in Figure 21 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistor add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as shown in Figure 21). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in Equation 1:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (1)$$

where:

- R_{INT} is the internal input resistor (R3 and R4).
- R_S is the external series resistance.

Device Functional Modes (continued)

With the adjustment factor equation including the device internal input resistance, this factor varies with each gain version, as listed in Table 1. Each individual device gain error factor is listed in Table 2.

Table 1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INA199x1	50	20
INA199x2	100	10
INA199x3	200	5

Table 2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA199x1	$\frac{20{,}000}{(17 \times R_S) + 20{,}000}$
INA199x2	$\frac{10{,}000}{(9 \times R_S) + 10{,}000}$
INA199x3	$\frac{1000}{R_S + 1000}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

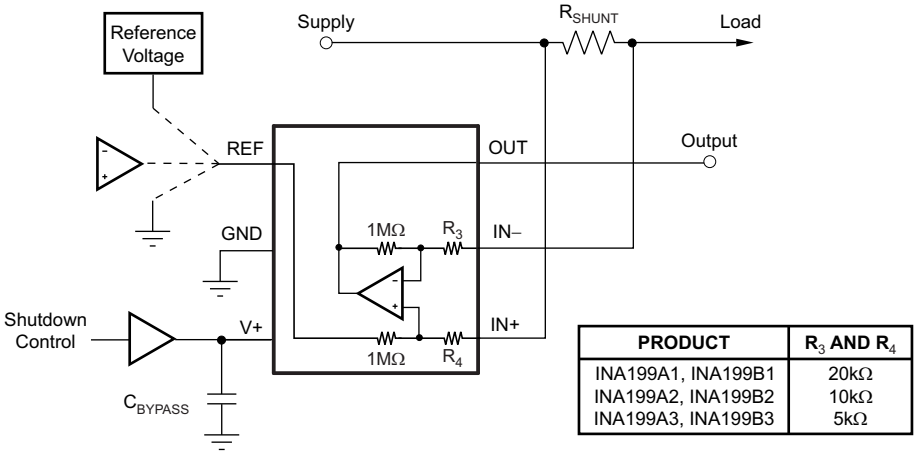
$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (2)$$

For example, using an INA199A2 or INA199B2 and the corresponding gain error equation from Table 2, a series resistance of 10-Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 0.89% solely because of the external 10-Ω series resistors. Using an INA199A1 or INA199B1 with the same 10-Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

8.4.2 Shutting Down the INA199 Series

Although the INA199 series does not have a shutdown pin, the low power consumption of the device allows the output of a logic gate or transistor switch to power the INA199. This gate or switch turns on and turns off the INA199 power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INA199 in shutdown mode shown in Figure 22.



NOTE: 1-MΩ paths from shunt inputs to reference and INA199 outputs.

Figure 22. Basic Circuit for Shutting Down INA199 With Grounded Reference

The is typically slightly more than 1-MΩ impedance (from the combination of 1-MΩ feedback and 5-kΩ input resistors) from each input of the INA199 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or operational amplifier is powered while the INA199 is shut down, the calculation is direct; instead of assuming 1-MΩ to ground, however, assume 1-MΩ to the reference voltage. If the reference or operational amplifier is also shut down, some knowledge of the reference or operational amplifier output impedance under shutdown conditions is required. For instance, if the reference source behaves as an open circuit when not powered, little or no current flows through the 1-MΩ path.

Regarding the 1-MΩ path to the output pin, the output stage of a disabled INA199 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage impressed across a 1-MΩ resistor.

NOTE

When the device is powered up, there is an additional, nearly constant, and well-matched 25 µA that flows in each of the inputs as long as the shunt common-mode voltage is 3 V or higher. Below 2-V common-mode, the only current effects are the result of the 1-MΩ resistors.

8.4.3 REF Input Impedance Effects

As with any difference amplifier, the INA199 series common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin must be buffered by an operational amplifier.

In systems where the INA199 output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 23 depicts a method of taking the output from the INA199 by using the REF pin as a reference.

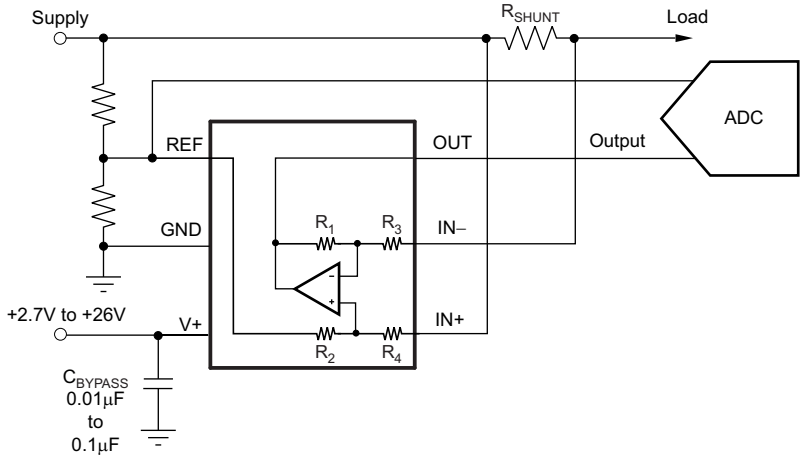


Figure 23. Sensing INA199 to Cancel Effects of Impedance on the REF Input

8.4.4 Using the INA199 With Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the INA199 series can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only Zener diode or Zener-type transient absorbers (sometimes referred to as *Transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as shown in Figure 24 as a working impedance for the Zener. It is desirable to keep these resistors as small as possible, most often around 10 Ω. Larger values can be used with an effect on gain that is

discussed in the section on input filtering. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523. Refer to *TIDA-00302 Transient Robustness for Current Shunt Monitor Design Guide*, TIDU473 for more information on transient robustness and current shunt monitor input protection.

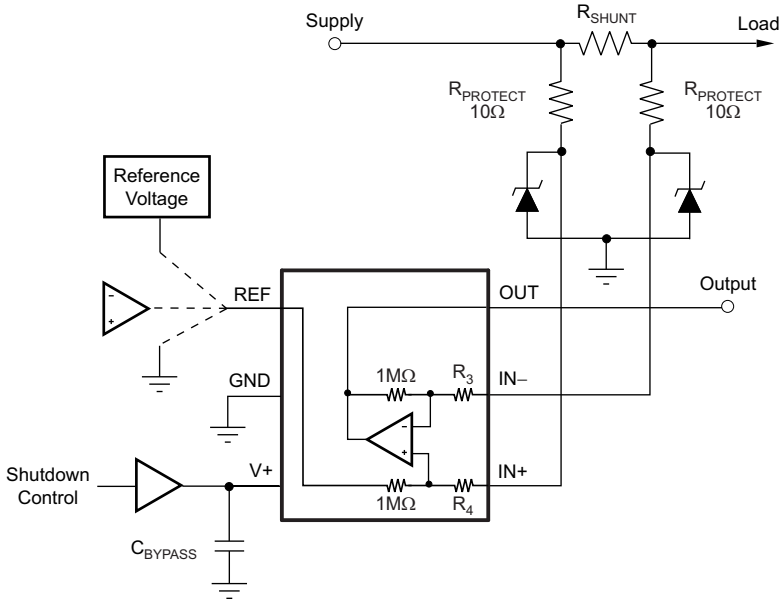


Figure 24. INA199 Transient Protection Using Dual Zener Diodes

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. This method is shown in Figure 25. In either of these examples, the total board area required by the INA199 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

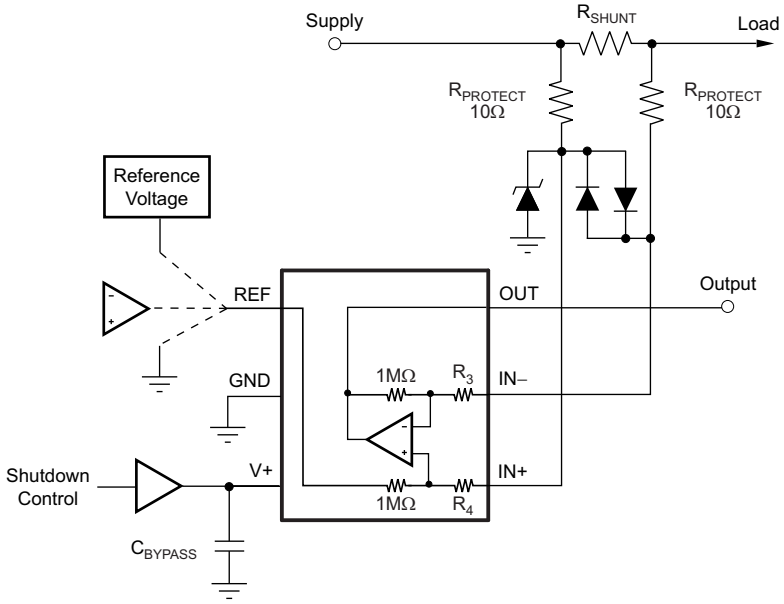


Figure 25. INA199 Transient Protection Using a Single Transzorb and Input Clamps

8.4.5 Improving Transient Robustness

Applications involving large input transients with excessive dV/dt above 2 kV per microsecond present at the device input pins may cause damage to the internal ESD structures on version A devices. This potential damage is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Take care to ensure that external series input resistance does not significantly impact gain error accuracy. For accuracy purposes, keep the resistance under 10 Ω if possible. Ferrite beads are recommended for this filter because of their inherently low DC ohmic value. Ferrite beads with less than 10 Ω of resistance at DC and over 600 Ω of resistance at 100 MHz to 200 MHz are recommended. The recommended capacitor values for this filter are between 0.01 µF and 0.1 µF to ensure adequate attenuation in the high-frequency region. This protection scheme is shown in Figure 26. Again, refer to *TIDA-00302 Transient Robustness for Current Shunt Monitor Design Guide*, TIDU473 for more information on transient robustness and current shunt monitor input protection.

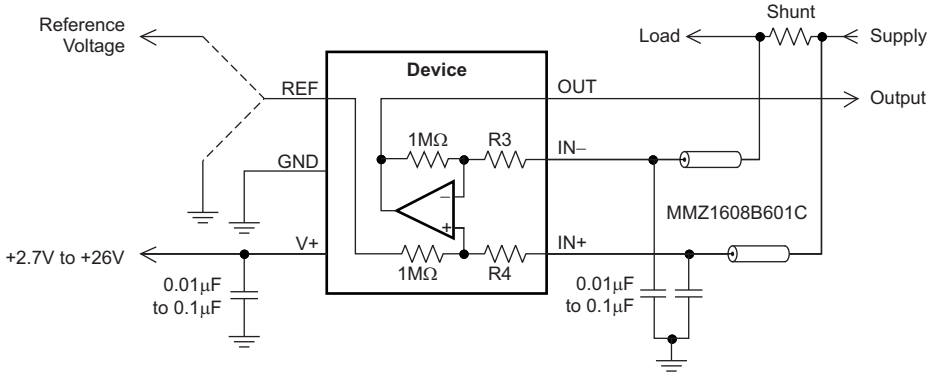


Figure 26. Transient Protection

To minimize the cost of adding these external components to protect the device in applications where large transient signals may be present, version B devices are now available with new ESD structures that are not susceptible to this latching condition. Version B devices are incapable of sustaining these damage-causing latched conditions so they do not have the same sensitivity to the transients that the version A devices have, thus making the version B devices a better fit for these applications.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA199 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

9.2 Typical Applications

9.2.1 Unidirectional Operation

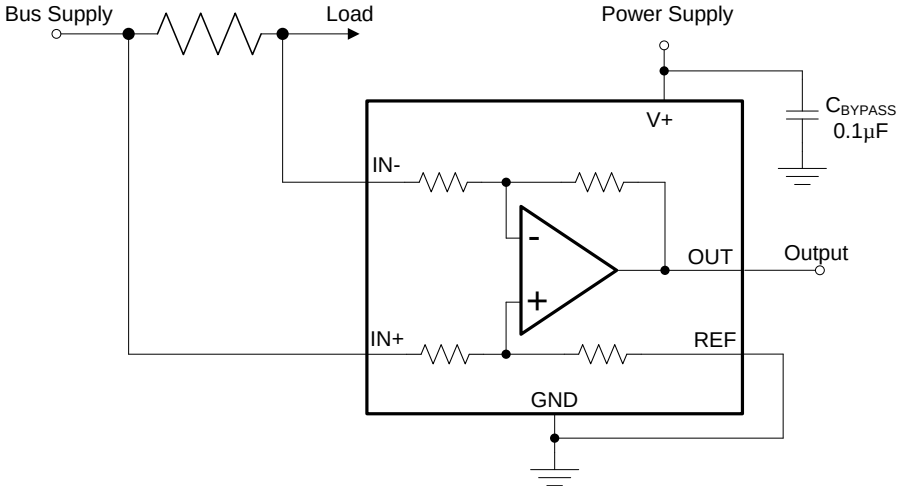


Figure 27. Unidirectional Application Schematic

9.2.1.1 Design Requirements

The device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 27. When the input signal increases, the output voltage at the OUT pin increases.

9.2.1.2 Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, TI recommends buffering the reference voltage connected to the REF pin.

A less frequently-used output biasing method is to connect the REF pin to the supply voltage, V+. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed the device supply voltage.

Typical Applications (continued)

9.2.1.3 Application Curve

An example output response of a unidirectional configuration is shown in Figure 28. With the REF pin connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

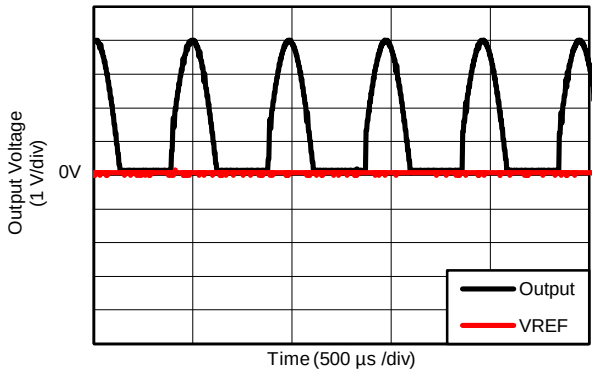


Figure 28. Unidirectional Application Output Response

9.2.2 Bidirectional Operation

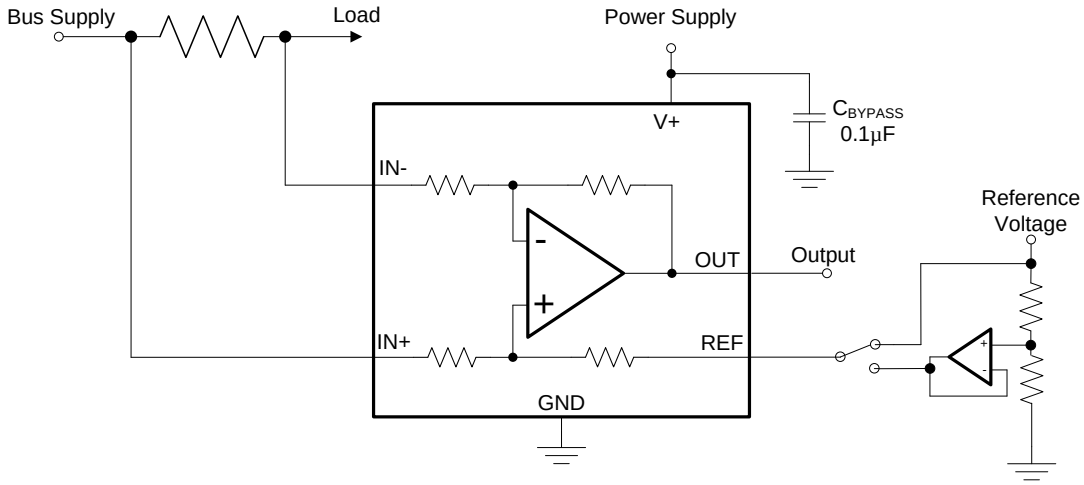


Figure 29. Bidirectional Application Schematic

9.2.2.1 Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

9.2.2.2 Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin, as shown in Figure 29. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V+. For bidirectional applications, V_{REF} is typically set at mid-scale for equal signal range in both current directions. In some cases, however, V_{REF} is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

Typical Applications (continued)

9.2.2.3 Application Curve

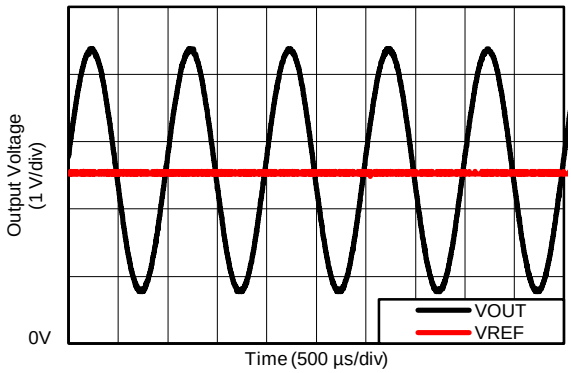


Figure 30. Bidirectional Application Output Response

10 Power Supply Recommendations

The input circuitry of the INA199 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Also, the INA199 can withstand the full input signal range up to 26-V range in the input pins, regardless of whether the device has power applied or not.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. TI recommends using a bypass capacitor with a value of 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.2 Layout Example

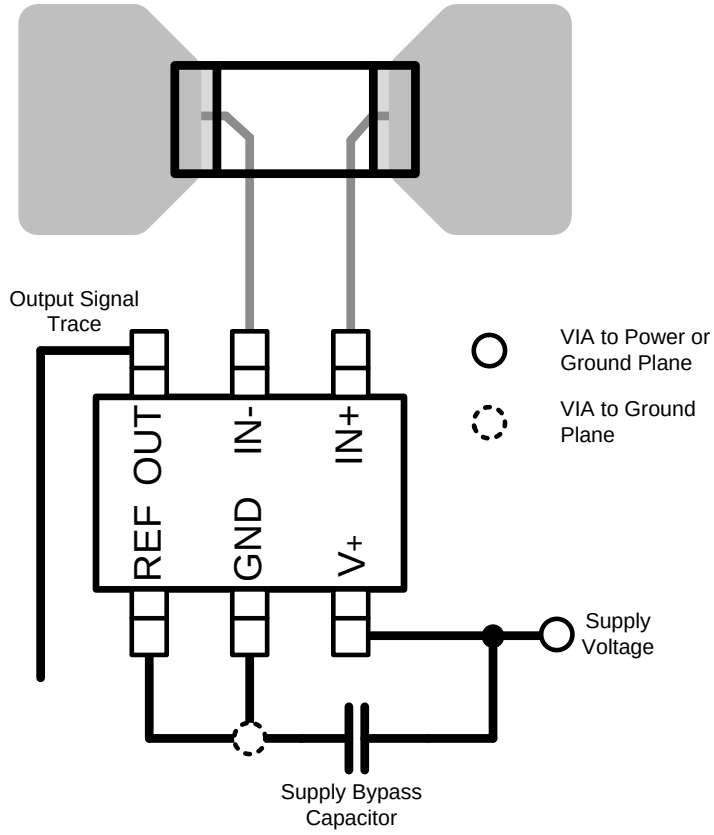


Figure 31. Recommended Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *INA199A1-A3EVM User's Guide*, SBOU085
- *TIDA-00302 Transient Robustness for Current Shunt Monitor*, TIDU473

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA199A1DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBG	Samples
INA199A1DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBG	Samples
INA199A1RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NSJ	Samples
INA199A1RSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NSJ	Samples
INA199A2DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBH	Samples
INA199A2DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBH	Samples
INA199A2RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NTJ	Samples
INA199A2RSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NTJ	Samples
INA199A3DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBI	Samples
INA199A3DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBI	Samples
INA199A3RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NUJ	Samples
INA199A3RSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NUJ	Samples
INA199B1DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEB	Samples
INA199B1DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEB	Samples
INA199B1RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHV	Samples
INA199B1RSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHV	Samples
INA199B2DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEG	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA199B2DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEG	Samples
INA199B2RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHW	Samples
INA199B2RSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHW	Samples
INA199B3DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHE	Samples
INA199B3DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHE	Samples
INA199B3RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHX	Samples
INA199B3RSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

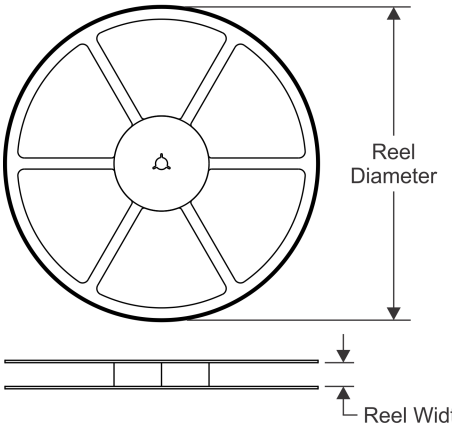
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

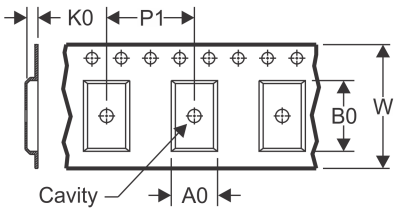
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

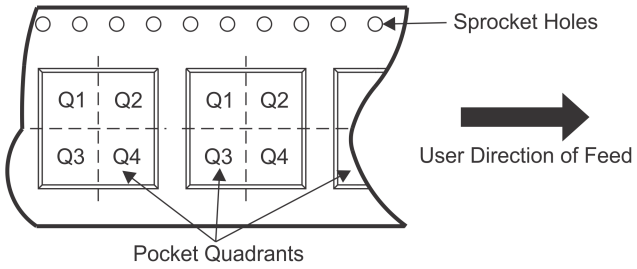


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

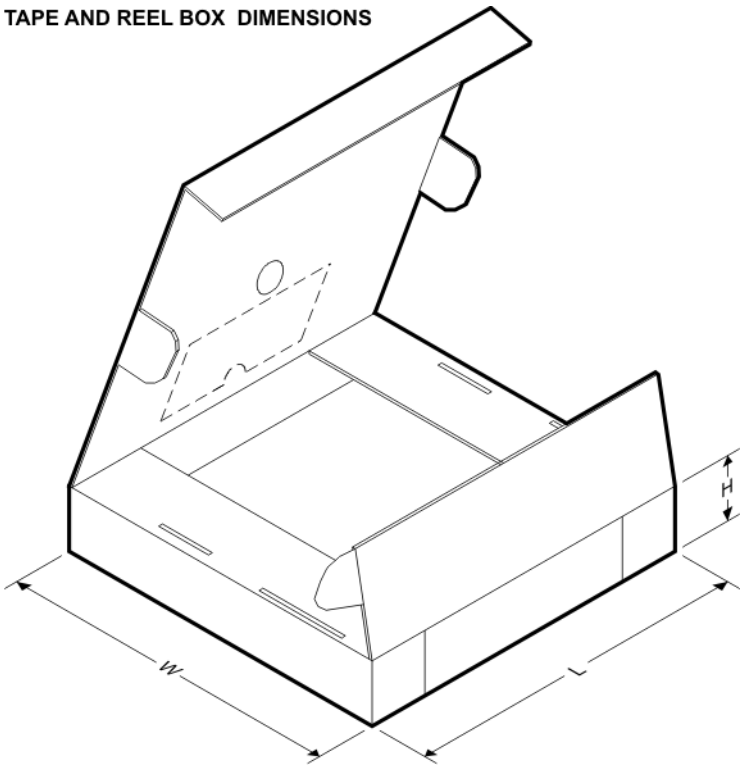


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA199A1DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A1DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
INA199A1DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A1DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A1DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A1RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A1RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A2DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A2DCKR	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA199A2DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A2DCKT	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA199A2DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A2DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A2RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A2RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A3DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A3DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199A3DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA199A3DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA199A3RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199A3RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B1DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B1DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B1RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B1RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B2DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B2DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B2RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B2RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B3DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B3DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA199B3RSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA199B3RSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

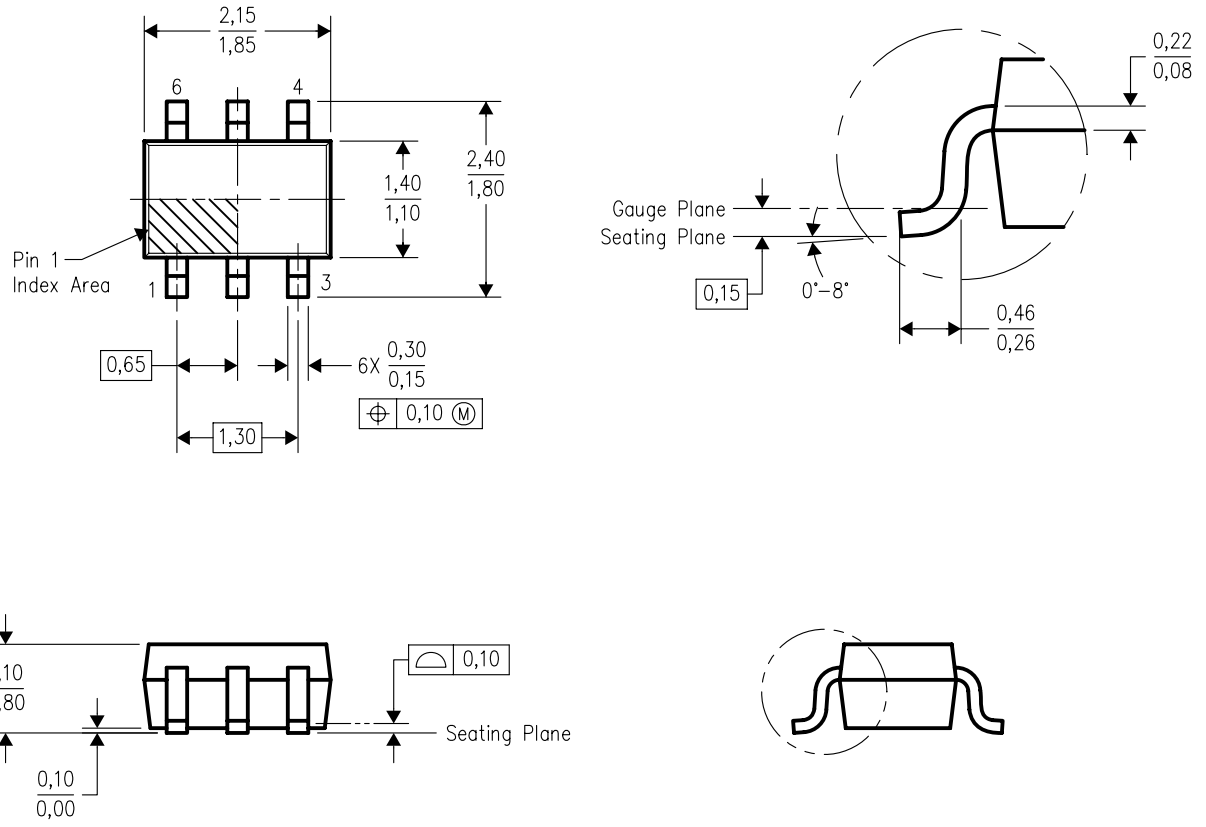


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA199A1DCKR	SC70	DCK	6	3000	195.0	200.0	45.0
INA199A1DCKR	SC70	DCK	6	3000	202.0	201.0	28.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA199A1DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199A1DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199A1DCKT	SC70	DCK	6	250	195.0	200.0	45.0
INA199A1RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA199A1RSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA199A2DCKR	SC70	DCK	6	3000	195.0	200.0	45.0
INA199A2DCKR	SC70	DCK	6	3000	223.0	270.0	35.0
INA199A2DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199A2DCKT	SC70	DCK	6	250	223.0	270.0	35.0
INA199A2DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199A2DCKT	SC70	DCK	6	250	195.0	200.0	45.0
INA199A2RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA199A2RSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA199A3DCKR	SC70	DCK	6	3000	195.0	200.0	45.0
INA199A3DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199A3DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199A3DCKT	SC70	DCK	6	250	195.0	200.0	45.0
INA199A3RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA199A3RSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA199B1DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199B1DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199B1RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA199B1RSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA199B2DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199B2DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199B2RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA199B2RSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA199B3DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA199B3DCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA199B3RSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA199B3RSWT	UQFN	RSW	10	250	203.0	203.0	35.0

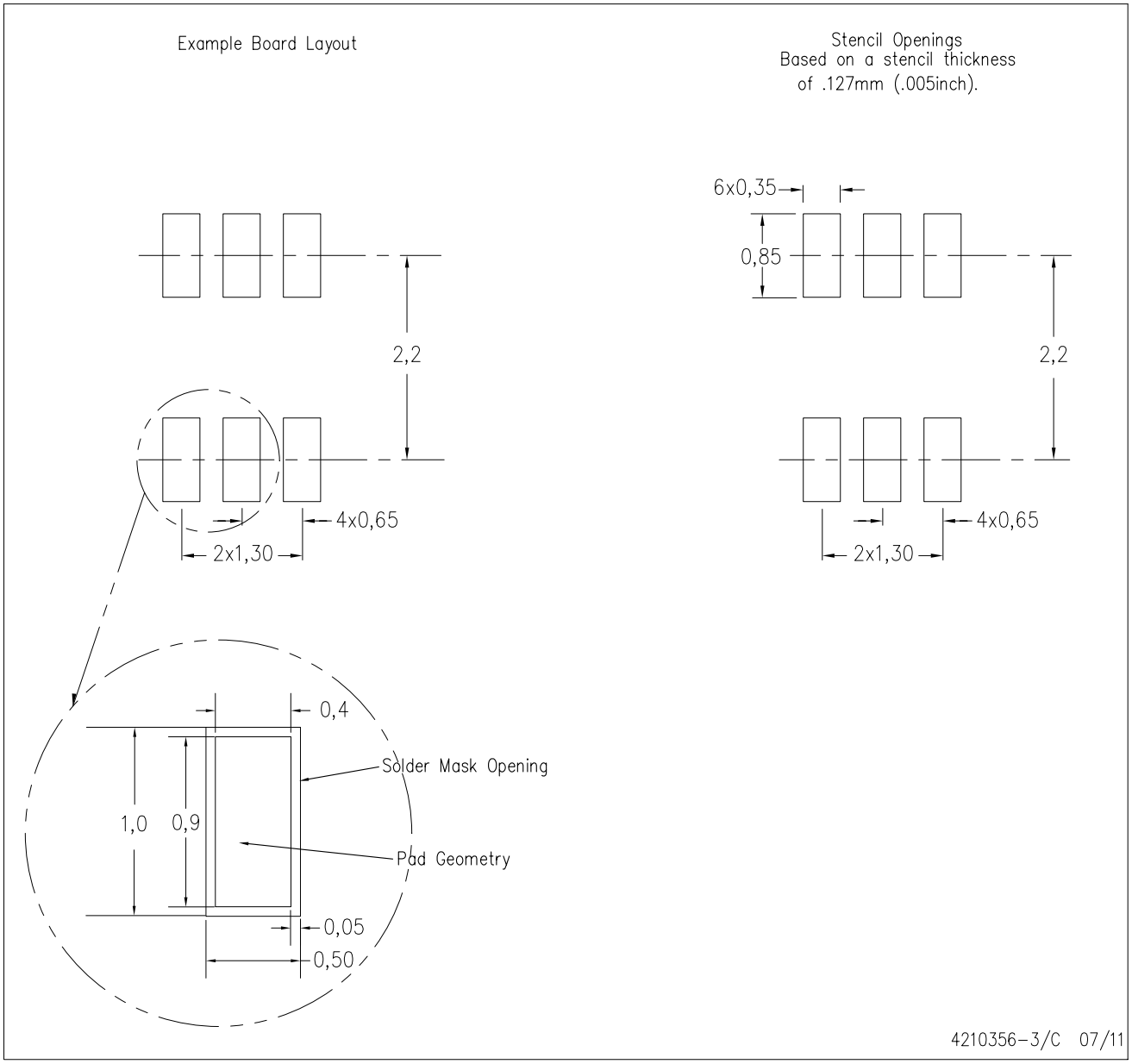
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

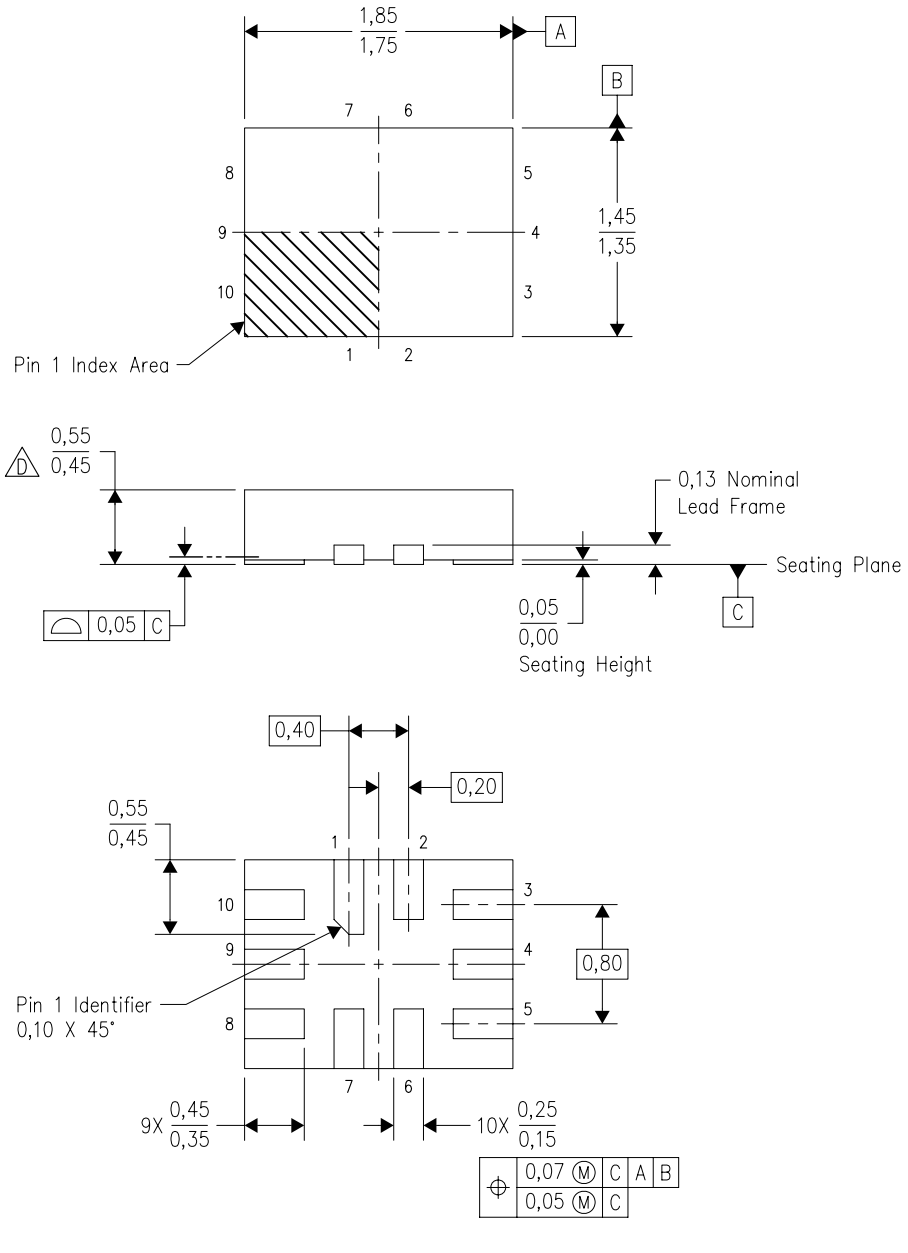
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

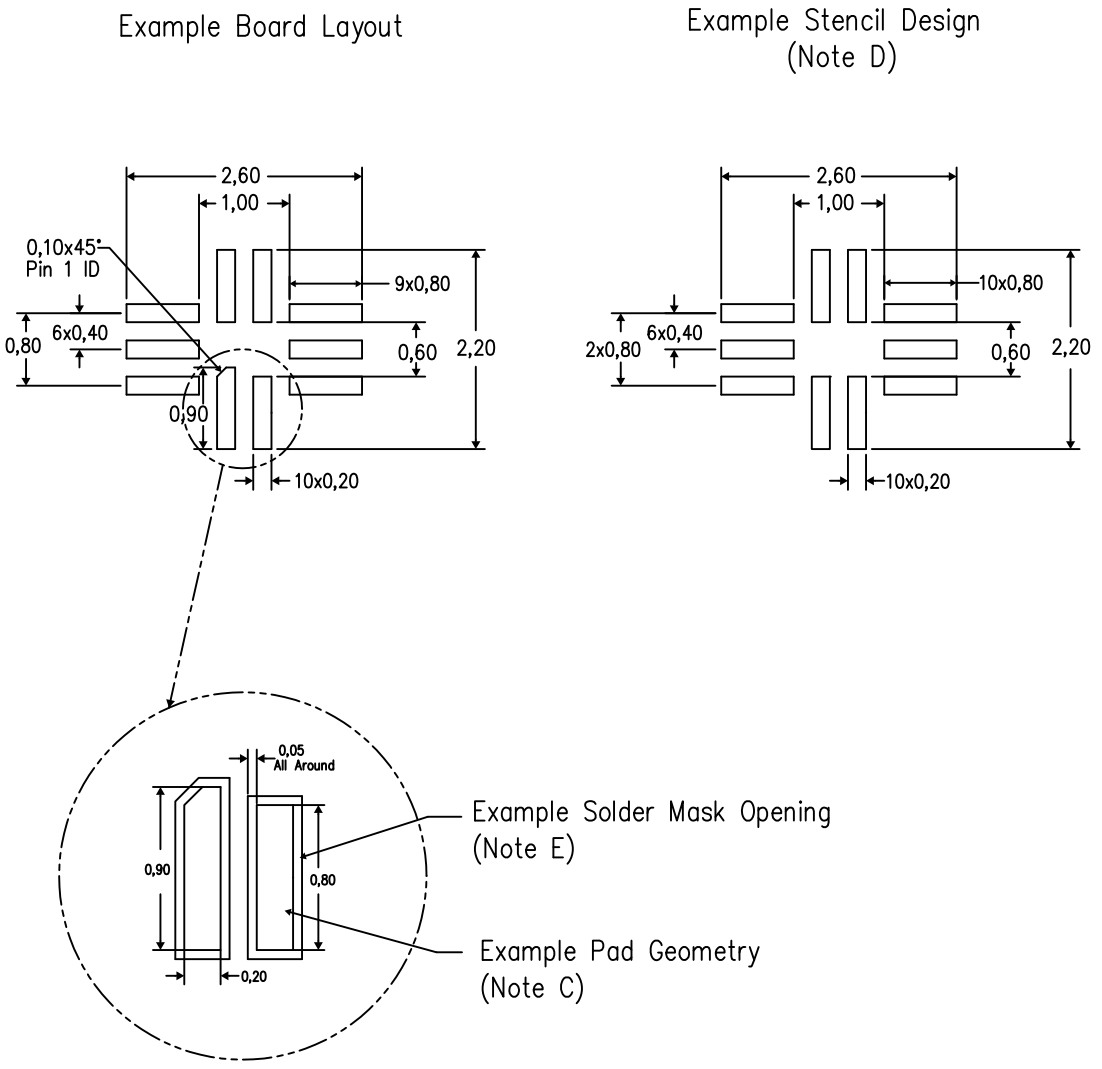
RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4208097/C 07/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation UDEE, except minimum package height.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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