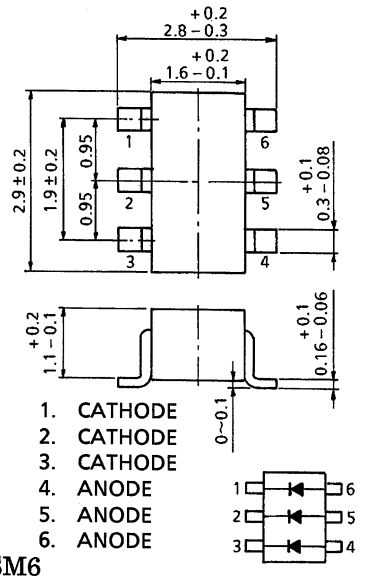
TOSHIBA Diode Silicon Epitaxial Planar Type

HN2D01F

Ultra High Speed Switching Application

Unit in mm



JEDEC	—
EIAJ	SC-74
TOSHIBA	1-3K1C

Weight: 0.015g

- HN2D01F is composed of 3 independent diodes.
- Low forward voltage : $V_{F\ (3)}$ = 0.98V (typ.)
- Fast reverse recovery time : t_{rr} = 1.6ns (typ.)
- Small total capacitance : C_T = 0.5μF (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse Voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current	I_{FM}	240 (*)	mA
Average forward current	I_O	80 (*)	mA
Surge current (10ms)	I_{FSM}	1 (*)	A
Power dissipation	P	300	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55~125	°C

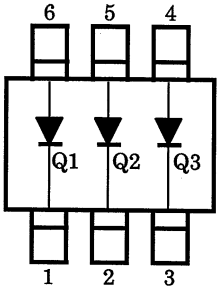
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(*) This is absolute maximum rating of single diode (Q1 or Q2 or Q3).
In the case of using 2 ro 3 diodes, the absolute maximum ratings per diodes is 75 %f the single diode one.

Electrical Characteristics (Q1, Q2, Q3 Common Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_{F\ (1)}$	—	I_F = 1mA	—	0.62	—	V
	$V_{F\ (2)}$	—	I_F = 10mA	—	0.75	—	
	$V_{F\ (3)}$	—	I_F = 100mA	—	0.98	1.20	
Reverse current	$I_{R\ (1)}$	—	V_R = 30V	—	—	0.1	μA
	$I_{R\ (2)}$	—	V_R = 80V	—	—	0.5	
Total capacitance	C_T	—	V_R = 0, f = 1MHz	—	0.5	3.0	pF
Reverse recovery time	t_{rr}	—	I_F = 10mA (Fig.1)	—	1.6	4.0	ns

Pin Assignment (Top View)



Marking

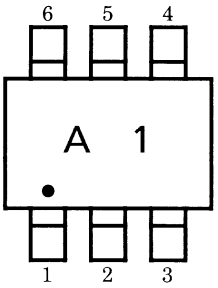
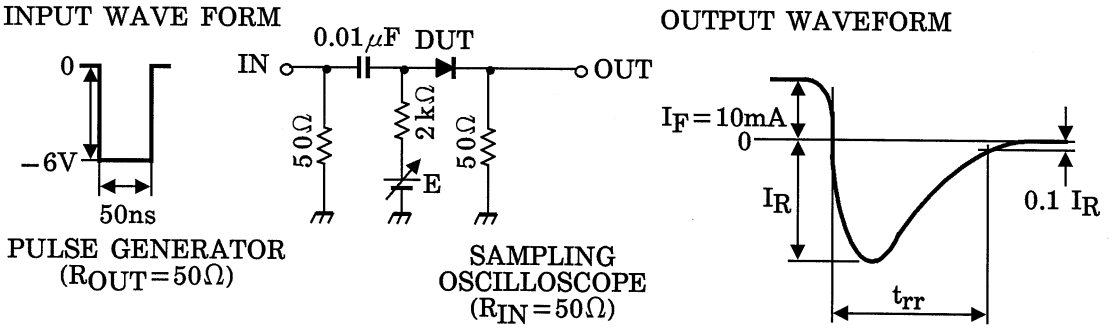
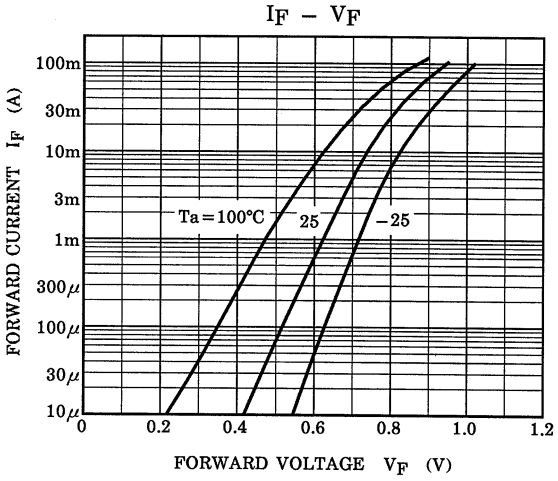
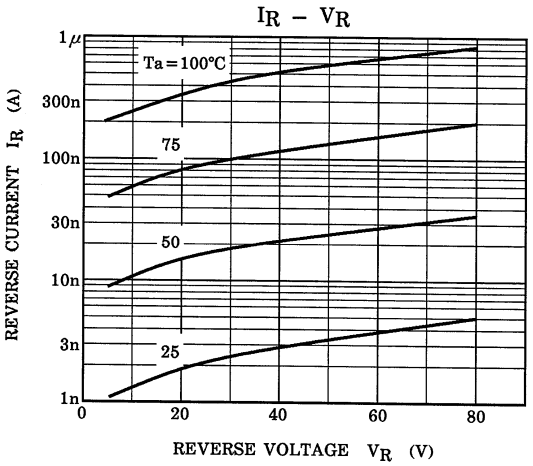
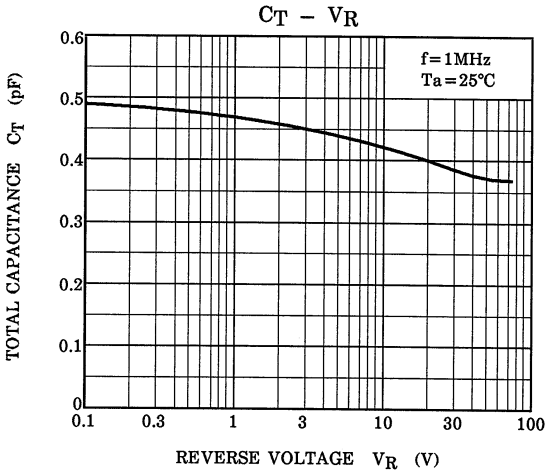


Fig.1 Reverse Recovery Time (t_{rr}) Test Circuit









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20070701-EN GENERAL

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