HMC1061LC5

v01.0613

DC - 18 GHz, ULTRA-WIDEBAND, DUAL RANK 4 GS/s TRACK-AND-HOLD AMPLIFIER

Typical Applications

The HMC1061LC5 is ideal for:

- RF ATE Applications
- Digital Sampling Oscilloscopes
- RF Demodulation Systems
- Digital Receiver Systems
- High Speed Peak Detectors
- Software Defined Radio
- Radar, ECM & ELINT Systems
- High Speed DAC De-Glitching

Features

18 GHz Input bandwidth (1 Vp-p Full Scale)

4 GS/s Maximum Sampling Rate

68 dB SFDR (4 GHz / 0.5 Vp-p Input, CLK = 1 GS/s)

56 dB SFDR (4 GHz / 1 Vp-p Input, CLK = 1 GS/s)

Direct-Coupled I/O

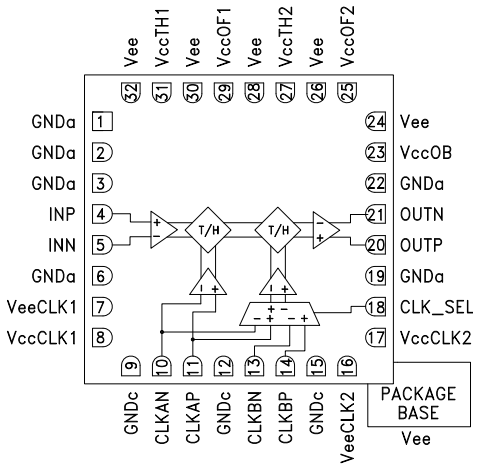
Ultra-Clean Output Waveforms, Minimal Glitching

>60 dB Hold Mode Feedthrough Rejection

1.5 mV RMS Hold Mode Output Noise

RoHS Compliant 5x5 mm SMT Package

Functional Diagram



General Description

The HMC1061LC5 is a SiGe monolithic, fully differential, dual rank, track-and-hold (T/H) that provides unprecedented bandwidth and dynamic-range performance to wideband sampled signal systems. The T/H offers precision signal sampling over 18 GHz bandwidth, with 9 - 10-bit linearity from DC to beyond 5 GHz input frequency, 1.5 mV noise, and <70 fs random aperture jitter. The device can be clocked to 4 GS/s with minimal dynamic range loss. The T/H can be used to expand the bandwidth and/or high-frequency linearity of high-speed A/D conversion and signal acquisition systems.

Electrical Specifications T_A = +25 °C, See Test Conditions on following page herein.

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Units
Analog Inputs (INP, INN)						
Differential Full Scale Range	Full-scale input for linearity test	1		1		Vpp
Input Resistance	Each lead to ground	3		50		Ω
Return Loss	0 to 12 GHz	3		-23		dB
Return Loss	12 to 18 GHz	3		-8		dB
Input Common Mode Voltage		3	-0.1	0	0.1	V
Clock Inputs (CLKAp, CLKAn, CLKBp, CLKBn)						
DC Differential Clock High Voltage		3	20	40	2000	mV
DC Differential Clock Low Voltage		3	-2000	-40	-20	mV
Amplitude (Sinusoidal Input)	Per Port	2	-6	0	10	dBm
Input Common Mode Voltage		3	-0.5	0	0.5	V
Clock Slew Rate	Recommended for best linearity	3		2 - 4		V/ns
Return Loss	0 to 3 GHz	3		24		dB
Return Loss	3 to 6 GHz	3		18		dB
Input Resistance	Each Lead to Ground	3		50		Ω

Electrical Specifications (continued)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Units
Analog Outputs (OUTP, OUTN)						
Differential Full Scale Range		4		1		Vp-p
Common Mode Output Voltage		4		0		V
Output Impedance	Per Port	3		50		Ω
Return Loss	0 to 5 GHz	3		14		dB
Track Mode Dynamics						
Baseband Gain		1	-2.5	0	1	dB
Track Mode Bandwidth	@ 1 Vp-p Input	4		TBD		GHz
Integrated Noise [2]		3		TBD		mV RMS
Hold Mode Dynamics						
Sampling Bandwidth	@ -3 dB Gain, 1 Vp-p Input Level	3		18		GHz
Differential Droop Rate (Linear Component)		1		-1.4		%/ns
Differential Droop Rate Magnitude (Fixed Component)		1		4		mV/ns
Feedthrough Rejection	@ 3 GHz	3		≥ 60		dB
Integrated Noise [2]	500 MHz Clock Frequency	3		1.45		mV RMS
Maximum Hold Time (1st Rank)		3		2		ns
Maximum Hold Time (2nd Rank)		3		2		ns
Total Maximum Effective Hold Time		3		4		ns
Single Tone THD/SFDR @ 0.995 GHz	Full Scale Input (1 Vp-p) [1]	3		-54 / 54		dB
Single Tone THD/SFDR @ 1.995 GHz	Full Scale Input (1 Vp-p) [1]	3		-55 / 55		dB
Single Tone THD/SFDR @ 2.995 GHz	Full Scale Input (1 Vp-p) [1]	3		-55 / 55		dB
Single Tone THD/SFDR @ 3.995 GHz	Full Scale Input (1 Vp-p) [1]	1		-55 / 56		dB
Single Tone THD/SFDR @ 4.995 GHz	Full Scale Input (1 Vp-p) [1]	3		-55 / 57		dB
Single Tone THD/SFDR @ 5.995 GHz	Full Scale Input (1 Vp-p) [1]	3		-52 / 54		dB
Single Tone THD/SFDR @ 7.995 GHz	Full Scale Input (1 Vp-p) [1]	3		-43 / 46		dB
Single Tone THD/SFDR @ 9.995 GHz	Full Scale Input (1 Vp-p) [1]	3		-34 / 37		dB
Single Tone THD/SFDR @ 11.995 GHz	Full Scale Input (1 Vp-p) [1]	3		-31 / 33		dB
Single Tone THD/SFDR @ 0.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-65 / 65		dB
Single Tone THD/SFDR @ 1.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-66 / 66		dB
Single Tone THD/SFDR @ 2.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-65 / 66		dB
Single Tone THD/SFDR @ 3.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-66 / 68		dB
Single Tone THD/SFDR @ 4.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-62 / 63		dB
Single Tone THD/SFDR @ 5.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-61 / 61		dB
Single Tone THD/SFDR @ 7.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-51 / 52		dB
Single Tone THD/SFDR @ 9.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-43 / 44		dB
Single Tone THD/SFDR @ 11.995 GHz	Half Full Scale Input (0.5 Vp-p) [1]	3		-40 / 42		dB
Track-to-Hold & Hold-and-Track Switching						
Aperture Delay	Simulated Value			-6		ps
Random Aperture Jitter	Full-scale Input @ 1 GHz [1]	3		<70		fs
Differential Pedestal (Linear Component) 1st Rank	1 GHz Clock Frequency, 6 dBm Clock Power	3		-1.0		%
Differential Pedestal (Linear Component) 2nd Rank	1 GHz Clock Frequency, 6 dBm Clock Power	3		0.15		%

[1] 1 GS/s Clock, Clock Power = 6 dBm / input terminal.
[2] Noise bandwidth limited by output amplifier bandwidth of ~7 GHz.

Electrical Specifications (continued)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Units
Differential Pedestal Magnitude (Fixed Component) 1st Rank		3		2.8		mV
Differential Pedestal Magnitude (Fixed Component) 2nd Rank		3		1.6		mV
Clock Frequency	@ 50% Duty Cycle	3	250		4000	MHz
Clock Buffer Pipeline Delay	Simulated Value			35		ps
Acquisition Time to 1 mV	Simulated Value			132		ps
Settling Time to 1 mV	Simulated Value			135		ps
Output buffer delay (from 2nd rank hold-node to output)	Simulated Value			43		ps
Power Supply Requirements						
VccTH Voltage (VccTH1 and VccTH2)			1.9	2	2.1	V
VccTH Current (sum of VccTH1 and VccTH2)		1		140		mA
VccOF Voltage (VccOF1 and Vcc OF2)			1.9	2	2.1	V
VccOF Current (sum of VccOF1 and Vcc OF2)		1		47		mA
VccOB Voltage			1.9	2	2.1	V
VccOB Current		1		74		mA
VccCLK Voltage (VccCLK1 and VccCLK2)			1.9	2	2.1	V
VccCLK Current (sum of VccCLK1 and VccCLK2)		1		64		mA
Vee Voltage (VeeCLK1, VeeCLK2, Vee)			-5	-4.75	-4.5	V
(Vee + VeeCLK) Current		1		-357		mA
Power Consumption		1		2.34		W

Test Levels

1. 100% production tested at T_A = +25 °C
2. Guaranteed by design/characterization testing
3. Characterization Sample Tested
4. Typical value only

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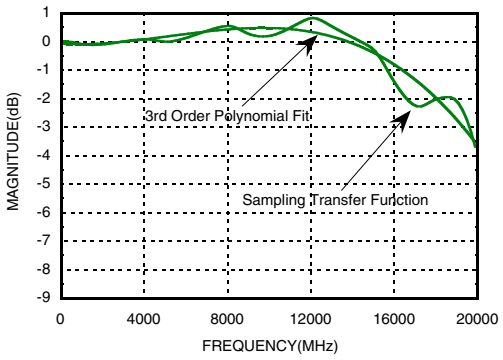
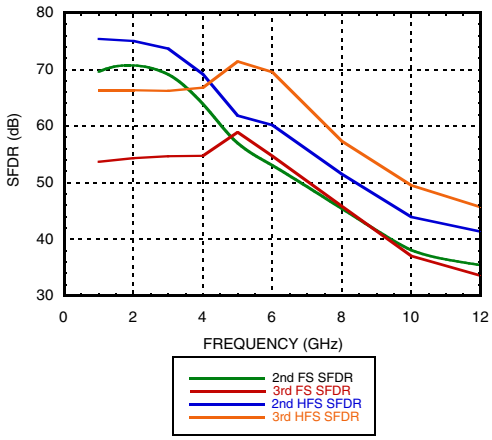
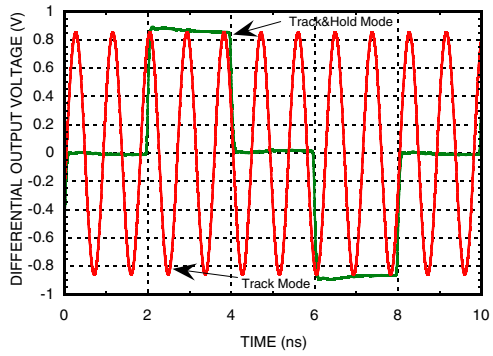
Sampling Transfer Function



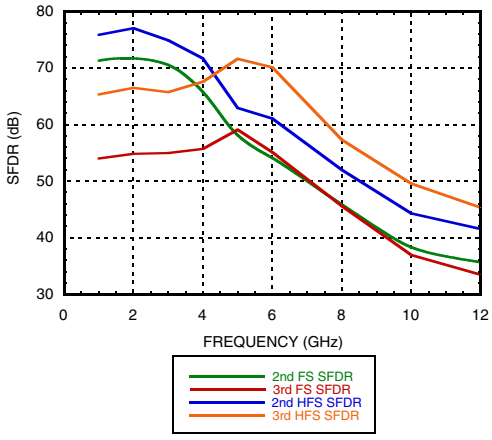
Hold-Mode SFDR vs. Frequency & Input Power @ f_{clk} = 500 MHz @ +10 dBm [1] [2]



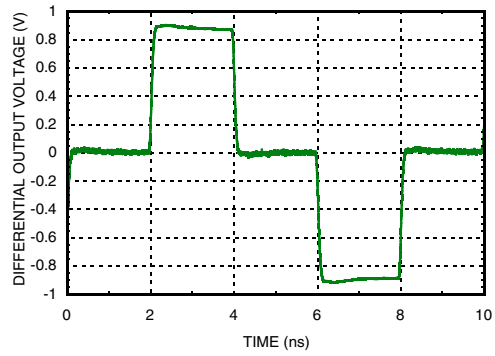
Time Domain Output Waveform @ f_{clk} = 500 MHz, f_{in} = 1.125 GHz



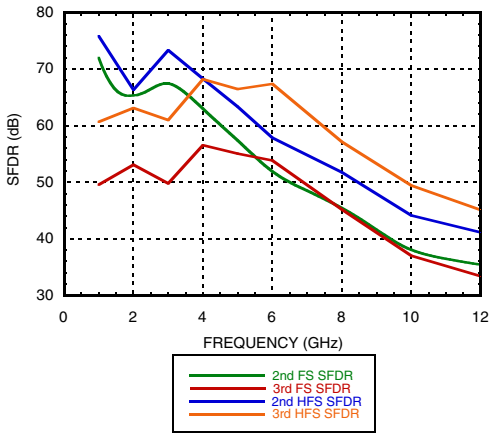
Hold-Mode SFDR vs. Frequency & Input Power @ f_{clk} = 1 GHz @ +6 dBm



Time Domain Output Waveform @ f_{clk} = 500 MHz, f_{in} = 10.125 GHz



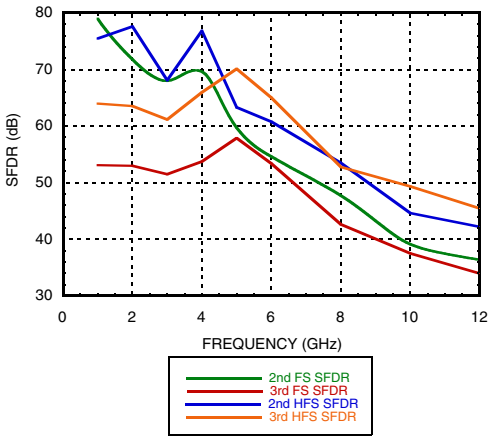
Hold-Mode SFDR vs. Frequency & Input Power @ f_{clk} = 2 GHz @ 0 dBm



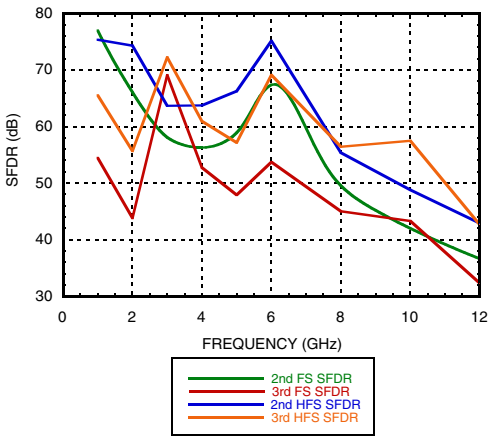
[1] FS = Full-Scale input level, HFS = Half-Full-Scale input level

[2] The measurement dynamic range for half-full-scale and full-scale inputs is about 68 dB and 74 dB, respectively, due to measurement noise floor limitations. Hence the measured spurious products tend to limit at these levels.

Hold-Mode SFDR vs. Frequency & Input Power @ f_{clk} = 3 GHz @ 0 dBm



Hold-Mode SFDR vs. Frequency & Input Power @ f_{clk} = 4 GHz @ 0 dBm



Definition of Specifications

Aperture Delay: The delay of the exact sample time relative to the time that the hold command is applied to the device. It is the difference between the delay of the clock switching transition to the hold node and the input signal group delay to the hold node. If the input signal group delay to the hold node exceeds the clock delay this quantity can be negative.

Aperture Jitter: The standard deviation of the sample instant in time.

Acquisition Time: The interval between the internal hold-to-track transition and the time at which the hold-node signal is tracking the input signal within a specified accuracy. It does not include the pipeline delay of the clock buffer.

Differential Pedestal: A component in the sample value caused by charge redistribution in the T/H switch during the sampling transition. In general, the pedestal can consist of three components: a fixed offset, a component that is linearly related to input signal amplitude, and a component that is nonlinearly related to input signal amplitude. The majority of the pedestal is usually linear. The value of the pedestal can be approximated by

$$P = P_o + P_{lin}\, V_{in}$$

where, P_o is the fixed pedestal component, P_{lin} is the linear pedestal component, and V_{in} is the sampled signal level.

Differential Droop Rate: The slow drift in the differential output voltage of a held sample while the T/H is in hold-mode. It is typically caused by current leakage on the hold capacitors and corresponds to a decay in the held voltage with increasing time. The droop can be approximated as the sum of a fixed component and a component that is linearly related to the held sample voltage. The total droop can be approximated by $D = D_o + D_{lin}$ Vin where D_o is the fixed component, D_{lin} is the linear droop constant and V_{in} is the sampled signal level. The sign of D_o tends to be random so only the magnitude is specified. Since the droop is mostly linear, it causes little nonlinearity.

Feedthrough Rejection: A measure of the off-state (hold-mode) isolation of the T/H's internal switch. It is defined as the ratio of the amplitude of the output signal (for a sinusoidal input) feeding through during the hold mode to the amplitude of the output signal during track mode. Normalization by the track-mode signal gives the true switch isolation without the effects of the output amplifier bandwidth limiting.

Full Scale Range: The voltage range between the minimum and maximum signal levels that can be handled by the T/H while still meeting the specifications.

Sampling Bandwidth: The -3 dB bandwidth of the sampled signal levels represented by the held sample amplitudes. It includes both the bandwidth of the transfer function from the signal input to the hold-node and any band-limiting effects associated with the finite time duration of the sampling aperture.

Settling Time: The interval between the internal track-hold transition and the time at which the held output signal is settled to within a specified accuracy. It does not include the pipeline delay of the clock buffer but does include the group delay of the output amplifier.

Spurious Free Dynamic Range (SFDR): The ratio (usually expressed in dB) between the sinusoidal output signal amplitude and the amplitude of the largest non-linearity product falling within one Nyquist bandwidth. It may be specified for both full scale input and some fraction(s) of full scale input. A SFDR based only on 2nd order nonlinear products is referred to as the 2nd order SFDR (SFDR2). A SFDR based only on 3rd order products is referred to as the 3rd order SFDR (SFDR3).

Total Harmonic Distortion (THD): The ratio of the total power in the non-linearity-generated harmonics and harmonic aliases (measured in one Nyquist band) to the output signal power.

Application Notes

General: The HMC1061LC5 ultra-wideband dual rank T/H amplifier is optimized for use in microwave data conversion applications requiring maximum sampling bandwidth, high linearity over a very wide bandwidth, and low noise. A key application of this device is front end sampling for high speed A/D converters to enhance their input bandwidth and/or high frequency linearity. Although several high speed A/D converters offer enhanced sample rates, few of them offer input bandwidth beyond a few GHz. In addition, maintenance of good sampling linearity at frequencies beyond the UHF band is technologically challenging and most A/D converters suffer rapidly degraded linearity above 1 or 2 GHz signal frequency. The HMC1061LC5 can address these limitations with its 18 GHz input bandwidth and excellent broadband linearity. Once sampling takes place within the T/H, the low bandwidth held output waveform can be processed by an A/D with substantially reduced bandwidth. In addition, A/D converter linearity performance limitations at high input frequencies are also mitigated because the settled waveform is processed with the optimal baseband linearity of the A/D converter.

The dual rank T/H is formed from two cascaded single rank T/Hs which are clocked 180 degrees out of phase such that while the master TH1 is holding, the slave TH2 is tracking and vice versa. The resulting output waveform consists of two time segments. The first segment consists of the TH1 hold mode as seen through TH2 track mode transfer function. At the beginning of the 2nd time segment, TH2 samples the held TH1 waveform and then continues to hold that value while TH1 switches back to track-mode and reacquires/tracks the input waveform. The resulting output waveform provides a held sample value of nearly one complete clock cycle, thus presenting the downstream A/D converter with a constant, settled waveform with minimal high frequency spectral content.

The device can be clocked in one of two ways depending on the voltage applied to the CLKSEL terminal. The device can be configured such that the slave T/H uses an internal clock derived and buffered from the master clock (Clock A). In this case, the CLKSEL terminal should be grounded, the user only needs to provide Clock A, and the internal clock 2 driving the slave always operates at the same frequency as the master Clock A. Alternatively, the CLKSEL terminal can be connected to the Vee supply enabling external Clock B control of the slave. In this mode, users must supply both Clock A and Clock B but they have the option of operating the slave at the same or even a different frequency than the master. This mode can be useful for decimation operations (where Clock B is a submultiple of the master clock) or other more exotic clocking schemes. In all cases, the maximum hold time limits shown in the table must be followed.

ESD: On-chip ESD protection networks are incorporated on the terminals, but the RF/microwave compatible interfaces provide minimal protection and ESD precautions should be used.

Power Supply Sequencing: The recommended power supply startup sequence is VccOB, VccOF, VccTH, VccCLK, Vee / VeeCLK if biased from independent supplies. VccOB, VccOF, VccTH and VccCLK can be connected to one +2 V supply if desired.

Input Signal Drive: For best results, the inputs should be driven differentially. The input can be driven single-ended but the linearity of the device will be degraded somewhat. The unused input should be terminated in 50 Ohms when driving the device single-ended.

Clock Input: The 1st rank device is in track-mode when (CLKAp – CLKAn) is high and it is in hold-mode when (CLKAp – CLKAn) is low. The 2nd rank device has an opposite polarity clock. It is in track-mode when (CLKBp-CLKBn) is low. The clock inputs should be driven differentially if possible. The clock inputs can be driven single-ended if desired but the single-ended amplitude/slew rate should be similar to the full differential amplitude / slew rate recommended for differential drive. The unused input should be terminated in 50 ohms.

The T/H-mode linearity of the device varies somewhat with clock power at lower clock frequencies. This results from a weak dependence of the linearity on clock zero crossing slew rate for slew rates beneath a critical value. For optimal linearity, a clock zero-crossing slew rate of roughly 2 - 4 V/ns (per clock input) or more is recommended. For sinusoidal clock inputs, 4 V/ns corresponds to a sinusoidal clock power per differential half-circuit input of -6 dBm at 4 GHz, 0 dBm at 2 GHz, and 6 dBm at 1 GHz. Regardless of the clock frequency, a minimum clock amplitude of -6 dBm is recommended (per differential half-circuit input).

Outputs: The outputs should be sensed differentially for the cleanest output waveforms. The output impedance is 50 Ohms resistive returned to the VccOB supply. The output stage is designed to drive 50 ohms terminated to ground on each differential half-circuit output. The device offers a true ground-referenced common mode output

Application Notes *(continued)*

that is usually within ±50 mV of ground; however it is possible to adjust the VccOB power supply slightly to fine tune the output common-mode level to precisely 0 V if desired. Additionally, the common-mode output level may be adjusted within the range of approximately ±0.5 V by adjusting the VccOB power supply according to the approximate relation Vocm=(VccOB-2)/2 where Vocm is the output common mode voltage and VccOB can be varied in the range of +1 V < VccOB < +3 V.

The bandwidth of the output amplifier that buffers the T/H signal between the hold-node and the 50 ohm outputs is approximately 7 GHz. The broad output buffer bandwidth is maintained to support the fast settling times required for users operating at high clock rates. However, because of the broad bandwidth, the output amplifier noise contribution to the total output noise is significant. Users operating at lower clock rates (such as < 1 GHz) may optimize their signal-to-noise ratio by filtering the output to a lower bandwidth than the output amplifier bandwidth of 7 GHz. Such an output filter will not reduce the sampled front-end noise (which is frozen into the signal samples and represents the majority of the T/H noise because of the wide front-end bandwidth) but it can reduce the output amplifier noise contribution. The user can filter the output to the lowest bandwidth that still retains the maximum settling time required to support the chosen clock rate. Typically this optimal bandwidth is of the order of 2 to 3 times the clock rate and it can be realized with a simple single pole RC filter if desired (for example a shunt capacitance on the outputs). For example, a user operating at a clock rate of 350 MHz with a 1 GHz noise bandwidth output filter can achieve approximately 1 dB lower noise relative to the unfiltered output condition.

The output will have very sharp transitions at the clock edges due to the broad output amplifier bandwidth. The user should be aware that any significant length of cable between the chip output and the load will cause frequency response roll-off and dispersion that can produce low amplitude tails with relatively long time-constants in the settling of the output waveform into the load. This effect is most noticeable when operating in a lab setting with output cables of a few feet length, even with high quality cable. Output cables between the T/H and the load should be of very high quality and 2 ft or less in length.

Reflections between the load and the device will also degrade the hold mode response. The output cable length can be adjusted to minimize the reflection perturbations to some extent. In general, the round trip transit time of the cable should be an integer number of clock periods to obtain the minimal reflection perturbation in the hold mode portion of the waveform. The optimal performance is obtained when the T/H is within 50 ps or less of the load since this gives a reflection duration equal to the approximate settling time of the device. In A/D converter applications the T/H should be placed as close as possible to the A/D converter to minimize reflection effects on the path between the T/H output and the input of the A/D converter.

Linearity Measurement

When characterizing the linearity of a T/H, the transfer function linearity of the held samples (referred to as T/H-mode linearity) is usually the quantity of most interest to the user. These samples contain the signal information that is ultimately digitized by the downstream A/D converter. A linearity measurement issue unique to the T/H device is the need for output waveform frequency response correction. In the case of a dual rank T/H, the output waveform resembles a square wave with duration equal to the clock period. Mathematically, the output can be viewed as the convolution of an ideal delta-function sample train with a single square pulse of duration equal to one clock period. This weights the output spectral content with a SIN(πf/fs)/(πf/fs) (Sinc) function frequency response envelope which has nulls at harmonics of the clock frequency fs and substantial response reduction beyond half the clock frequency. This spectral content and envelope function are observed during spectrum analyzer measurement because the analyzer simply reproduces the entire spectrum of the incoming waveform. However, the spectral content of the held samples without the envelope weighting is required for proper measurement of the sample's linearity, as would be measured by a downstream A/D converter that samples a time instant in the held waveform. Either the impact of the response envelope must be corrected in the data or a measurement method must be used that heterodynes the relevant nonlinear harmonic products to low frequencies to avoid significant envelope response weighting. This latter method is referred to as the low frequency beat-product technique.

Linearity Measurement (continued)

The low frequency beat-product technique is commonly used for high-speed T/H linearity measurements, although the measurement does impose restrictions on the specific input signal and clock frequencies that can be used. For example, with a clock frequency of 512.5 MHz, a single tone input at 995 MHz beats with the 2nd harmonic of the sampling frequency (through the sampling process) to produce a 1st order beat product at 30 MHz. Likewise, the 2nd and 3rd harmonics of the input signal (generated via distortion in the T/H) beat with the 4th and 6th harmonics of the sampling frequency respectively to produce 2nd and 3rd order beat products at 60 MHz and 90 MHz. In this manner, the T/H nonlinearity in the vicinity of 1 GHz can be measured even though the 995 MHz fundamental and the 1.99 GHz and 2.985 GHz nonlinear harmonics are well beyond the 256 MHz 4 dB bandwidth of the SINx/x response envelope.

The possible input frequency choices are overly limited when the low frequency beat-product technique is used at high clock rates. A related high frequency beat-product measurement utilizing correction for the SINx/x envelope weighting must be employed to measure linearity over a wide range of input frequencies. Hittite uses both low frequency and high frequency beat product methods to measure linearity for a wide range of clock and signal frequencies. Our high frequency beat-product measurement avoids excessive envelope correction error by maintaining all beat products within the 4 dB bandwidth of the Sinc function, where the envelope response is well behaved and easily modeled.

Independent and accurate measurement of linearity in a T/H waveform (without a downstream ADC to sample a single point on the held waveform) is challenging at these low nonlinearity levels. This is due to the waveform transitions/ small glitches that can impact the measured spectrum during direct spectrum analyzer measurements of the output waveform (without sampling). These measurement artifacts are worst case at high clock frequencies where a significant fraction of the waveform duration is consumed by transients. It is believed that these measurement artifacts at high clock frequencies contribute to the linearity ripple seen in the plots at higher clock rates. The true linearity is likely represented by the average through these curve variations.

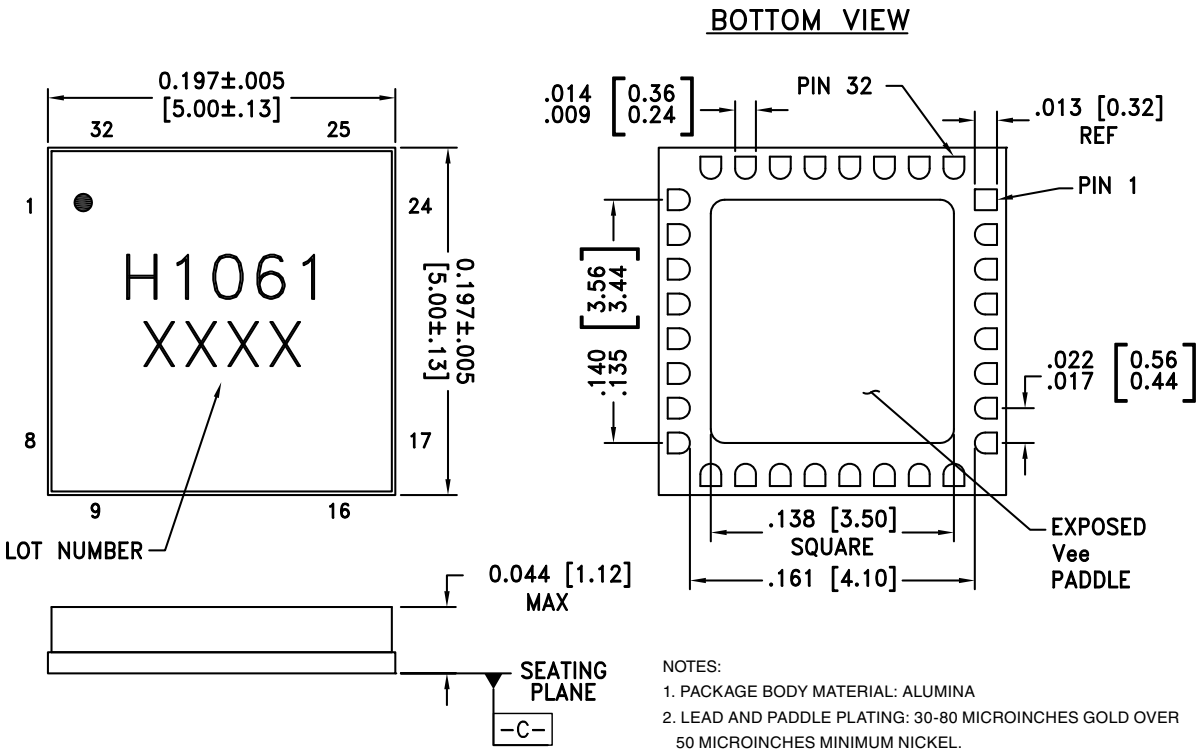
For the same reasons as described above, we find that the linearity characterization of the T/H waveform via direct spectrum analysis tends to represent a worst case scenario relative to the true linearity obtained by sampling one point on the held waveform as would be obtained during T/H-ADC measurements. This is supported by our T/H-ADC combination measurements documented in our application notes that show substantially better linearity, particularly at low signal frequencies. The measured linearity presented here from direct spectrum analysis of the entire T/H waveform is believed to represent a worst case indication of the true T/H linearity.

Absolute Maximum Ratings

VccTHx, VccOFx, VccCLKx	2.1 Vdc
VccOB	3 Vdc
Vee, VeeCLK	-5.25 Vdc
CLKAp, CLKAn, CLKBp, CLKBn Input Power	+10 dBm
INp, INn Input Power	+10 dBm
Junction Temperature	125 °C
Continuous Pdiss (T= 85 °C)	2.5 W
Thermal Resistance (junction to package bottom)	16.0 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

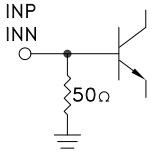
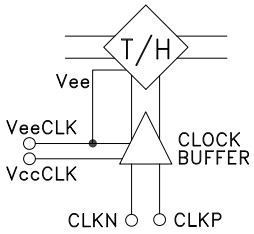
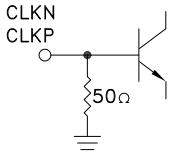
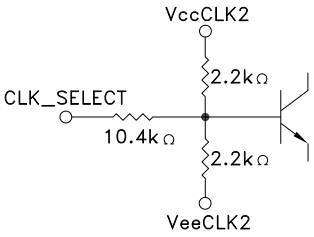
Outline Drawing



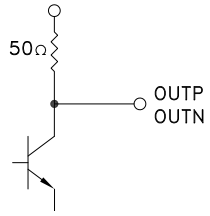
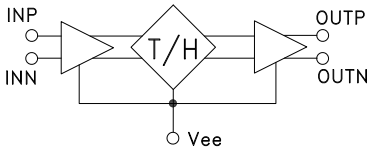
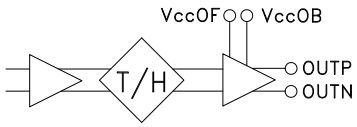
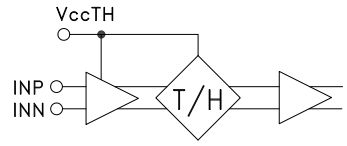
NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND. PACKAGE BASE MUST BE SOLDERED TO Vee PLANE.
7. CLASSIFIED AS MOISTURE SENSITIVITY LEVEL (MSL) 1.
8. DUE TO THE DEVICE'S POWER DISSIPATION OF 2.34 W, THE PADDLE TEMPERTURE SHOULD BE HELD BELOW 85 °C, PREFERABLY USING VERTICAL THERMAL CONDUCTION TO A HEAT SINK.

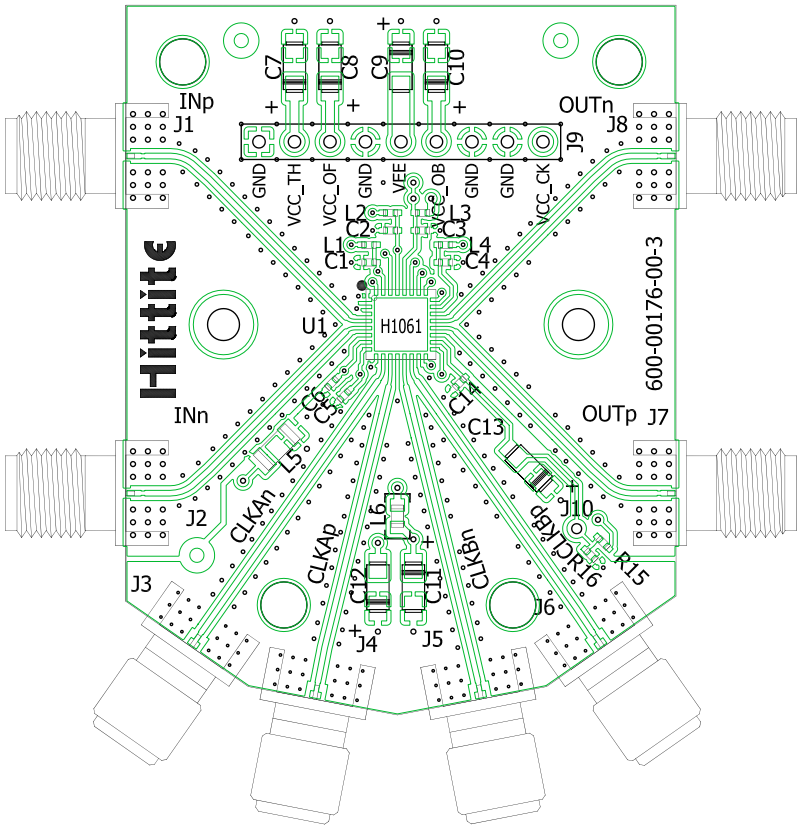
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 3, 6, 19, 22	GNDa	Analog ground. This ground and clock ground must be connected to the same DC potential but they can be RF-isolated from each other if desired.	
4	INP	Differential signal input (positive) DC-coupled, ground referenced input with nominal common mode level = 0 V Input impedance = 50 ohms Full-scale differential voltage = 1 Vpp Maximum input level = +10 dBm	
5	INN	Differential signal input (negative) DC-coupled, ground referenced input with nominal common mode level = 0 V Input impedance = 50 ohms Full-scale differential voltage = 1 Vpp Maximum input level = +10 dBm	
7, 16	VeeCLK1 VeeCLK2	Clock buffer Vee supplies Nominal voltage = -4.75 V (Vee+VeeCLK1+VeeCLK2) Current = -357 mA nominal	
8, 17	VccCLK1 VccCLK2	Clock buffer Vcc supplies Nominal voltage = +2 V (VccCLK1+VccCLK2) Current = 64 mA nominal	
9, 12, 15	GNDc	Clock ground. This ground and analog ground must be connected to the same DC potential but they can be RF-isolated from each other.	
10, 11	CLKAn CLKAp	Differential clock A input (negative and positive) Provides clock to 1st rank device Also provides properly timed clock to 2nd rank device when clk_sel = 0 V DC-coupled, ground referenced input with nominal common mode level = 0 V Input impedance = 50 ohms 1st rank track mode: differential clock positive 1st rank hold mode: differential clock negative Maximum input level = +10 dBm	
13, 14	CLKBn CLKBp	Differential clock B input (negative and positive) Provides clock to 2nd rank device if clk_sel = -4.75 V DC-coupled, ground referenced input with nominal common mode level = 0 V Input impedance = 50 ohms Terminated if unused 2nd rank track mode: differential clock negative 2nd rank hold mode: differential clock positive Maximum input level = +10 dBm	
18	CLK_SELECT	Clock mode select terminal Nominal 0 V for internal clock B mode, current = 230 µA nominal Nominal -4.75 V for external clock B mode, current = -230 µA nominal	

Pin Descriptions *(continued)*

Pin Number	Function	Description	Interface Schematic
20, 21	OUTp, OUTn	Differential output (positive and negative) DC-coupled, ground refernced output with nominal common mode level = 0 V Output impedance = 50 ohms Intended to be DC or AC coupled to 50 ohm load impedance	
24, 26, 28, 30, 32, Package Base	Vee	Vee supply Nominal voltage = -4.75 V (Vee+VeeCLK1+VeeCLK2), current = -357 mA nominal	
23	VccOB	Vcc supply for the 50 ohm output buffer Nominal voltage = +2 V, current = 74 mA nominal Can be biased with +1 <Vcc_ob <+3 V to adjust the output common mode voltage to an exact desired value between -0.5 and 0.5 V. Output common mode voltage adjustment has a sensitivity of apporximately Vocm (V) ~ 0.5 (Vcc_ob - 2)	
25, 29	VccOF2 VccOF1	Vcc supplies for front end of the output buffer circuitry VccOF2 is for the output of the IC, while VccOF1 is for the interstage buffer between the 1st and 2nd rank T/Hs Nominal voltage = +2 V (VccOF1+VccOF2), current = 47 mA nominal	
27, 31	VccTH2 VccTH1	VccTH2 supply for 2nd rank T/H core circuitry and VccTH1 is the supply fo the 1st rank T/H Nominal voltage = + 2 V (VccTH1+VccTH2), current = 140 mA nominal	

Evaluation PCB



List of Materials for Evaluation PCB EVAL01-HMC1061LC5 [1]

Item	Description
J1, J2, J7, J8	SRI K-Connector
J3 - J6	SRI SMA-Connector
J9	Header, 0.9", 9 Pin, Thruhole, TIN
J10	DC Pin
C1 - C6, C14	0.01 µF Capacitor, 0402 Pkg.
C7 - C12	4.7 µF Capacitor, Tantalum
L1 - L4	Ferrite, 0402, Steward LI0402E300R-10
L5	Ferrite, 1206, Steward HF1206J150R-10
L6	Ferrite, 0603, Steward LI0603E470R-10
R16	0 Ohm Resistor, 0402 Pkg.
U1	HMC1061LC5 Track-and-Hold Amplifier
PCB [2]	600-00176-00 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The package base is internally connected to the Vee and VeeCLK supply and should be connected to a Vee supply plane for heat sinking. A sufficient number of via holes should be used to connect the top and bottom ground planes in order to provide good RF grounding. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit for Evaluation PCB