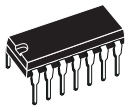
HCF4013

Dual D-type flip-flop

Datasheet - production data



PDIP14

SO14

Features

- Set-reset capability
- Static flip-flop operation - retains state indefinitely with clock level either “high” or “low”
- Medium speed operation 16 MHz (typ.), clock toggle rate at 10 V
- Standardized symmetrical output characteristics
- Quiescent current specified up to 20 V
- 5 V, 10 V, and 15 V parametric ratings
- Input leakage current I_I = 100 nA (max.) at V_{DD} = 18 V, T_A = 25 °C
- 100 % tested for quiescent current
- ESD performance
  - HBM: 2 kV
  - MM: 200 V
  - CDM: 1 kV

Applications

- Automotive
- Industrial
- Computer
- Consumer

Description

The HCF4013 is a monolithic integrated circuit fabricated in metal oxide semiconductor technology available in PDIP14 and SO14 packages.

The HCF4013 consists of two identical, independent data type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs, and Q and $\overline{Q}$ outputs. This device can be used for shift register applications. It can also be used for counter and toggle applications by connecting $\overline{Q}$ output to the data input.

The logic level present at the D input is transferred to the $\overline{Q}$ output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

Table 1. Device summary table

Order code	Temperature range	Package	Packing	Marking
HCF4013M013TR	-55 ° C to +125 ° C	SO14	Tape and reel	HCF4013
HCF4013YM013TR (1)	-40 ° C to +125 ° C	SO14 (automotive grade)(1)		HCF4013Y
HCF4013BEY	-55 ° C to +125 ° C	PDIP14	Tube	HCF4013BE

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

Contents

1 Pin information

Figure 1. Pin connections (top view)

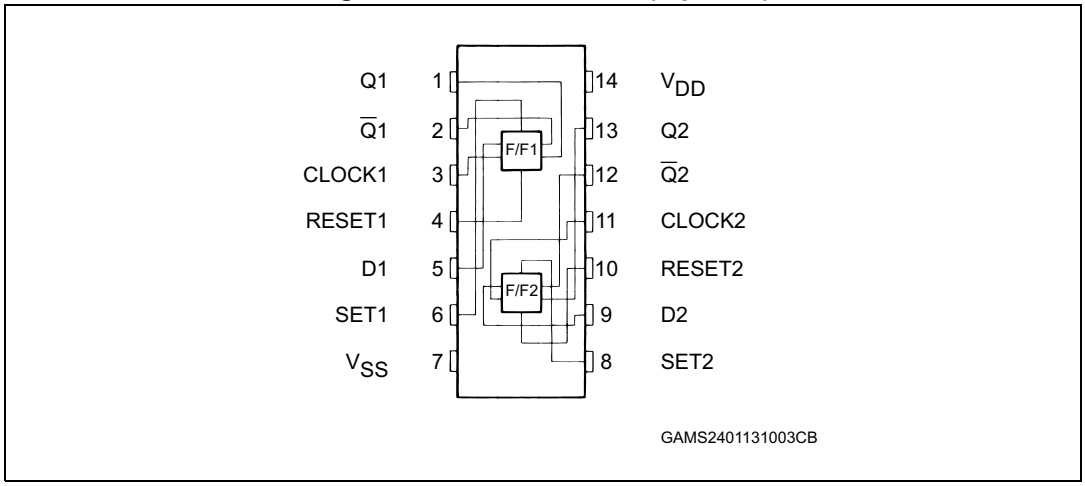
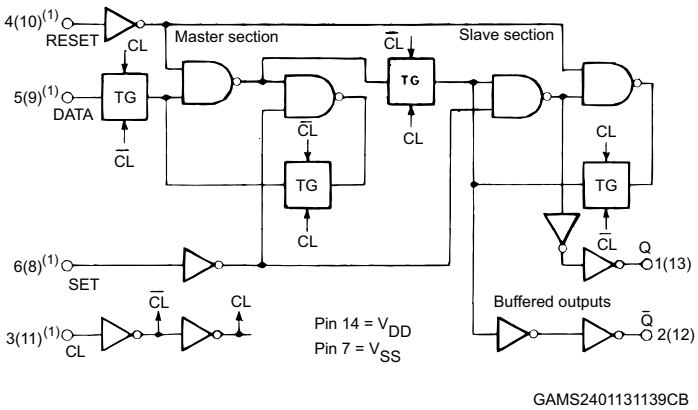


Table 2. Pin description

Pin no	Symbol	Name and function
3, 11	CLOCK1 CLOCK2	Clock inputs
4, 10	RESET1 RESET2	Reset inputs
6, 8	SET1, SET2	Set inputs
5, 9	D1, D2	Data inputs
1, 13	Q1, Q2	Data outputs
2, 12	$\overline{Q}1$, $\overline{Q}2$	Data outputs
7	V_{SS}	Negative supply voltage
14	V_{DD}	Positive supply voltage

2 Functional description

Figure 2. Logic diagram



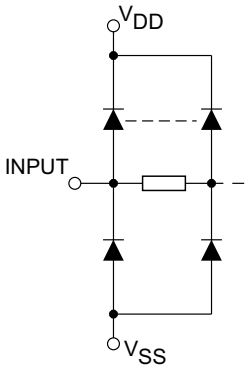
1. All inputs are protected by a COS/MOS protection network.

Table 3. Truth table

CLOCK(1)	D	RESET	SET	Q	$\overline{Q}$
⌐‾|	L	L	L	L	H
⌐‾|	H	L	L	H	L
‾⌐		X(2)	L	L	Q	$\overline{Q}$
X(2)		X(2)	H	L	L	H
X(2)		X(2)	L	H	H	L
X(2)		X(2)	H	H	H	H

1. Low level
2. Don’t care

Figure 3. Input equivalent circuit



3 Electrical characteristics

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to V_{SS} pin voltage.

Table 4. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to +22	V
V_I	DC input voltage	-0.5 to V_{DD} + 0.5	
I_I	DC input current	±10	mA
P_D	Power dissipation per package	200	mW
	Power dissipation per output transistor	100	
T_{op}	Operating temperature	-55 to +125	°C
T_{stg}	Storage temperature	-65 to +150	

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	3 to 20	V
V_I	Input voltage	0 to V_{DD}	
T_{op}	Operating temperature	-55 to 125	°C

Table 6. DC specifications(1)

Sym.	Parameter	Test condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD}(V)	T_A = 25 °C			-40 to 85 °C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent current	0/5			5		0.02	1		30		30	µA
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.04	20		600		600	
V_{OH}	High level output voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low level output voltage	5/0		<1	5		0.05			0.05		0.05	
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High level input voltage		0.5/4.5	<1	5	3.5			3.5		3.5		
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low level input voltage		4.5/0.5	<1	5			1.5		1.5		1.5	
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output drive current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output sink current	0/5	0.4	<1	5	0.44	1		0.36		0.36		
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input leakage current	0/18	Any input		18		$\pm 10^{-5}$	±0.1		±1		±1	µA
C_I	Input capacitance		Any input				5	7.5					pF

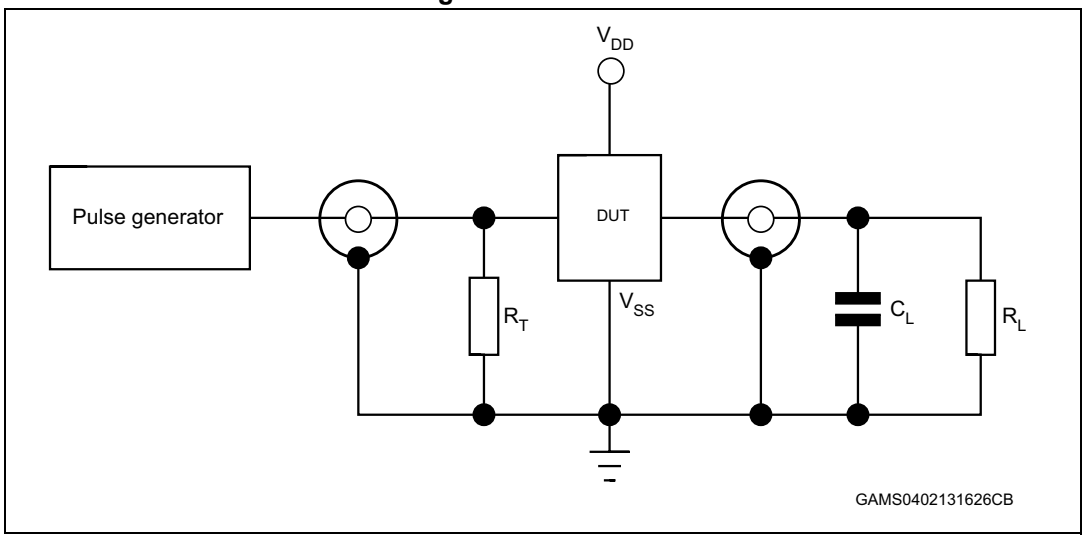
1. The noise margin for both level "1" and "0" is: 1 V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, and 2.5 V min. with V_{DD} = 15 V.

Table 7. Dynamic electrical characteristics
(T_{amb} = 25 °C, C_L = 50 pF, R_L = 200 kΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test condition	Value[1]			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{TLH}, t_{THL}	Propagation delay time (CLOCK to Q or Q outputs)	5		150	300	ns
		10		65	130	
		15		45	90	
t_{PLH}	Propagation delay time (SET to Q or RESET to Q)	5		150	300	
		10		65	130	
		15		45	90	
t_{PHL}	Propagation delay time (SET to Q or RESET to Q)	5		200	400	
		10		85	170	
		15		60	120	
t_{THL}, t_{TLH}	Transition time	5		100	200	
		10		50	100	
		15		40	80	
f_{CL}[2]	Maximum clock input frequency	5	3.5	7		MHz
		10	8	16		
		15	12	24		
t_W	Clock pulse width	5	140	70		ns
		10	60	30		
		15	40	20		
	Set or reset pulse width	5	180	90		
		10	80	40		
		15	50	25		
t_r , t_f [3]	Clock input rise or fall time	5			15	µs
		10			4	
		15			1	
t_s	Data setup time	5	40	20		ns
		10	20	10		
		15	15	7		

1. The typical temperature coefficient for all V_{DD} values is 0.3 %/°C.
2. Input tr, tf = 5 ns
3. If more than one unit is cascaded in a parallel clocked application, tr should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

Figure 4. Test circuit



1. Legend: C_L = 50 pF or equivalent (includes jig and probe capacitance), R_L = 200 KΩ, $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 5. Dn to Qn timings (50 % clock duty cycle)

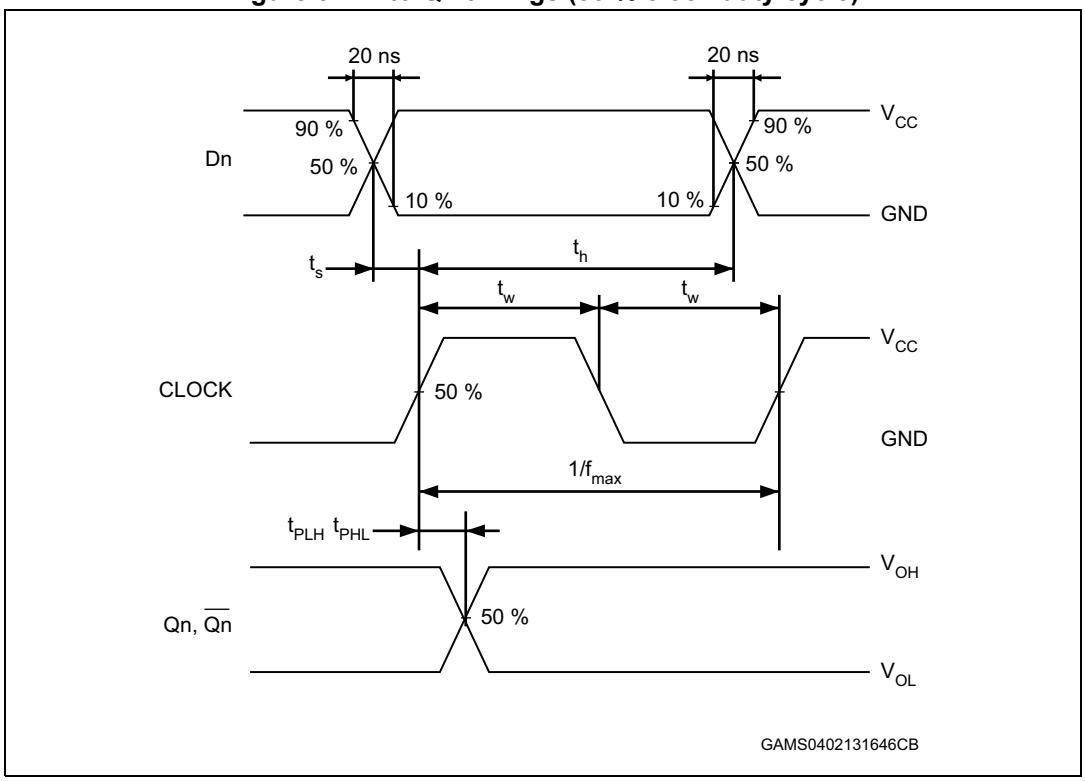
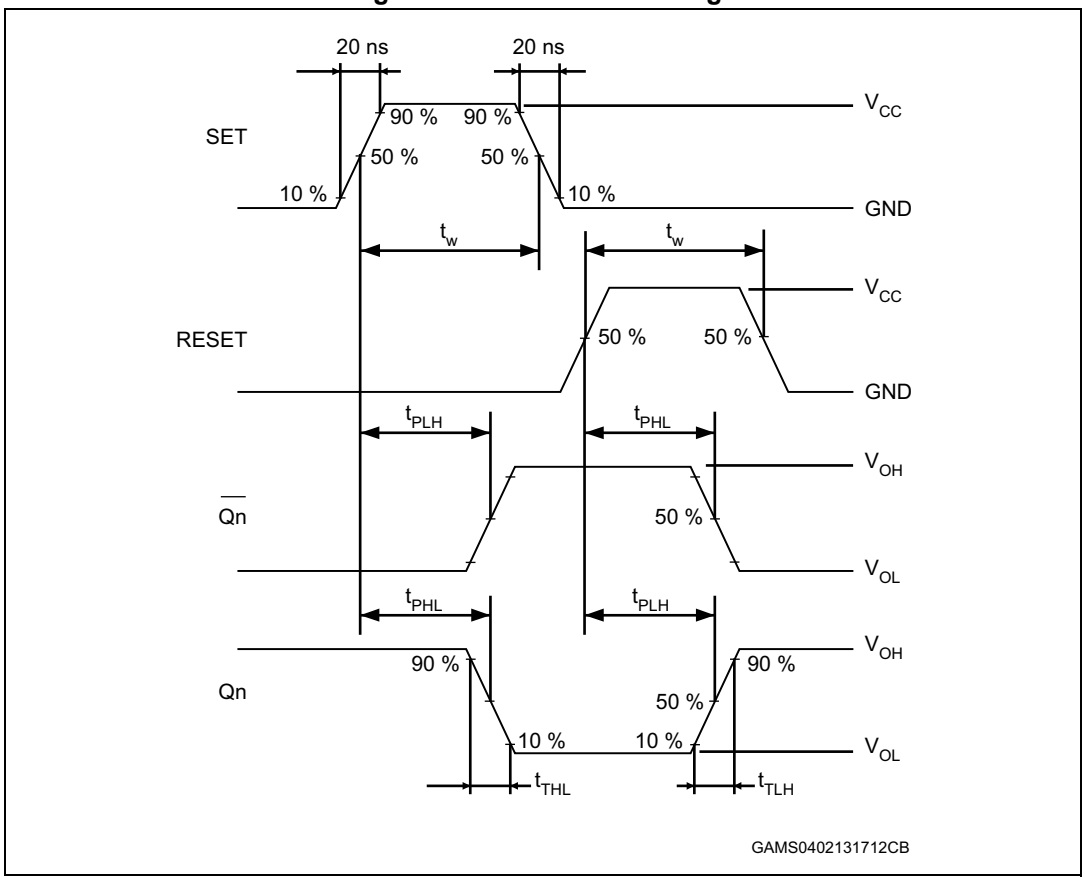


Figure 6. Set and reset timings



4 Package information

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4.1 PDIP14 package information

Figure 7. PDIP14 package mechanical drawing

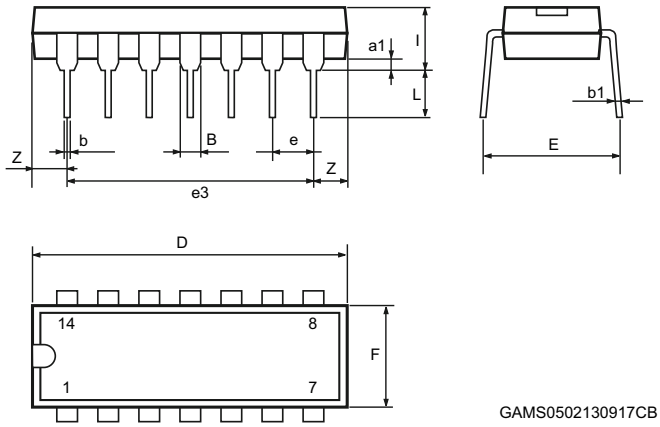

Table 8. PDIP14 package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

4.2 SO14 package information

Figure 8. SO14 package mechanical drawing

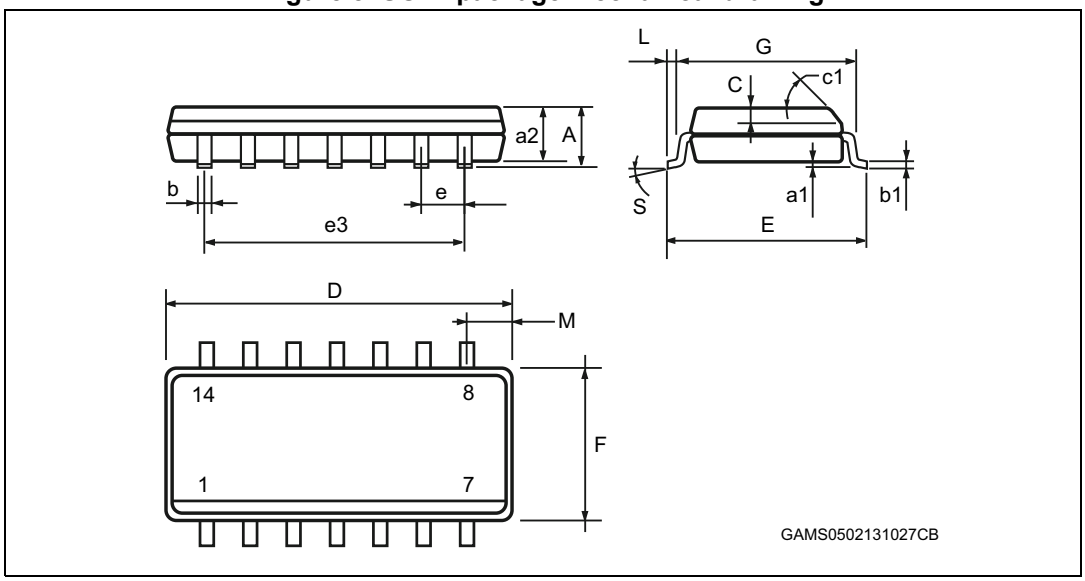

Table 9. SO14 package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1		45 °			45 °	
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S			8 °			8 °

5 Ordering information

Table 10. Order codes

Order code	Temperature range	Package	Packing	Marking
HCF4013M013TR	-55 ° C to +125 ° C	SO14	Tape and reel	HCF4013
HCF4013YM013TR(1)	-40 ° C to +125 ° C	SO14 (automotive grade)(1)		HCF4013Y
HCF4013BEY	-55 ° C to +125 ° C	PDIP14	Tube	HCF4013BE

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
Sep-2001	1	Initial release.
18-Feb-2013	2	Document template and layout updated Removed “B” from part number Added ESD information to *Features* Updated package names (PDIP-14 and SO-14 instead of DIP-14 and SOP-14). Added *Applications* Added *Device summary table* Updated symbol names in *Table 7* Added *Section 5: Ordering information*
30-Apr-2013	3	*Features*: updated ESD information
30-May-2013	4	*Features*: updated ESD information Updated footnote in *Table 1* and *Table 10*

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