ON Semiconductor

FPF2281
Over-Voltage Protection Load Switch

Features

- Surge Protection
  - IEC 61000-4-5: > 100 V
- Over-Voltage Protection (OVP)
- Over-Temperature Protection (OTP)
- ESD Protection
  - Human Body Model (HBM): > 3.5 kV
  - Charged Device Model (CDM): > 2 kV
  - IEC 61000-4-2 Air Discharge: > 15 kV
  - IEC 61000-4-2 Contact Discharge: > 8 kV

Applications

- Mobile Handsets and Tablets
- Portable Media Players
- MP3 Players

Description

The FPF2281 features a low-R_{ON} internal FET and an operating range of 2.5 V_{DC} to 25 V_{DC} (absolute maximum of 29 V_{DC}). An internal clamp is capable of shunting surge voltages >100 V, protecting downstream components and enhancing system robustness. The FPF2281 features over-voltage protection that powers down the internal FET if the input voltage exceeds the OVP threshold. The OVP threshold is adjustable with optional external resistors. Over-temperature protection also powers down the device at 130°C (typical). Exceptionally low off-state current (<1 μA maximum) facilitates compliance with standby power requirements.

The FPF2281 is available in a fully "green" compliant 1.3 mm × 1.8 mm Wafer-Level Chip-Scale Package (WLCSP) with backside laminate.

Related Resources

- http://www.onsemi.com/

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FPF2281BUCX-F130	-40°C – 85°C	HE	12-Ball, 0.4 mm Pitch WLCSP	Tape & Reel

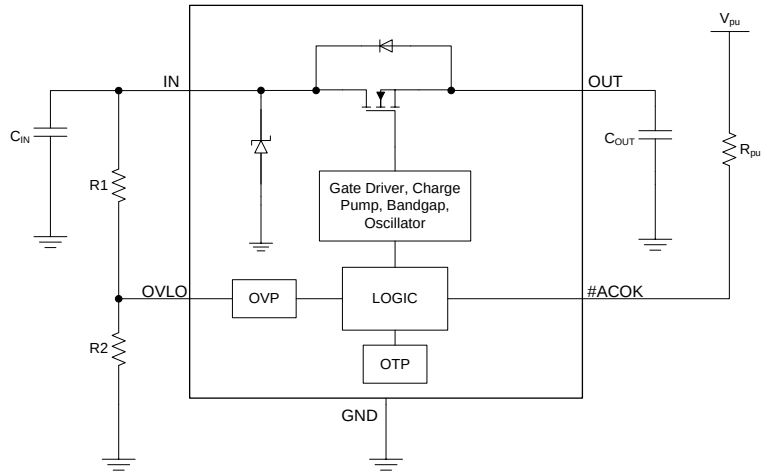
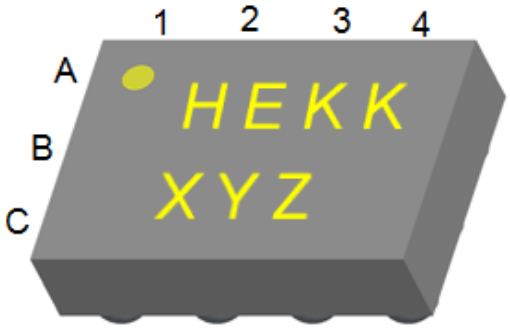


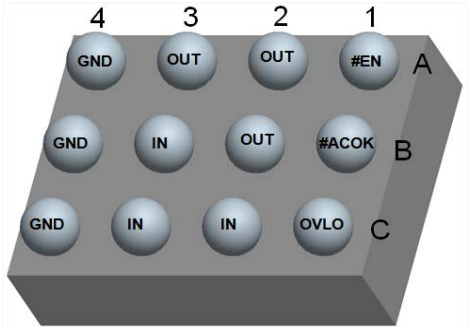
Figure 1. Functional Block Diagram

November-2017,Rev. 2

Publication Order Number:
FPF2281/D

Pin Configuration





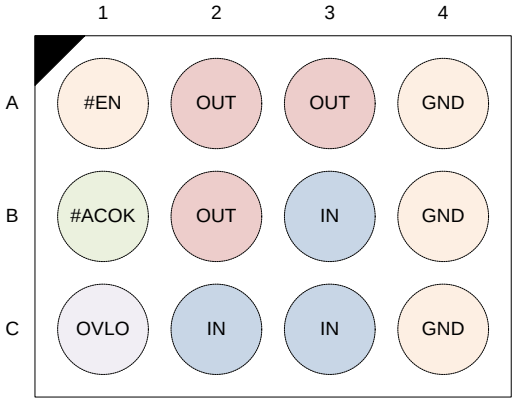


Figure 2. Pin Configuration (Top View)

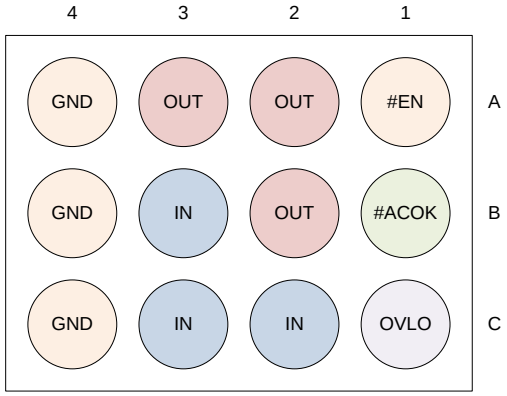


Figure 3. Pin Configuration (Bottom View)

Pin Definitions

Name	Bump	Type	Description		
IN	B3, C2, C3	Input/Supply	Switch Input and Device Supply		
OUT	A2, A3, B2	Output	Switch Output to Load		
#ACOK	B1	Output	Power Good	1	$V_{IN} < V_{IN\_min}$ or $V_{IN} \geq V_{OVLO}$
				0	Voltage Stable
#EN	A1	Input	Device Enable (Active LOW)		
OVLO	C1	Input	Over-Voltage Lockout Adjustment Pin		
GND	A4, B4, C4	Supply	Device Ground		

Over-Voltage Lockout (OVLO) Calculation

OVLO can be set externally and override default OVP. By connecting an external resistor-driver to the OVLO pin. Equation (1) can produce the desired trip voltage and resistor values.

$$V_{IN\_OLVO} = V_{OVLO\_TH} \times [1 + R1/R2] \quad (1)$$

Recommended minimum R1 = 1 MΩ.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_IN to GND & V_IN to V_OUT = GND or Float		-0.3	29.0	V
V_{OUT}	V_OUT to GND		-0.3	V_{IN} + 0.3	V
V_{OVLO}	OVLO to GND		-0.3	25.0	V
$V_{\#EN\_ACOK}$	Maximum DC Voltage Allowed on #EN or ACOK Pin			6	V
I_{IN}	Switch I/O Current (Continuous)			4.5	A
	Peak Switch I/O Current (10 ms)			9	A
tP_D	Total Power Dissipation at T_A = 25°C			1.48	W
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient[1] (1-in.^{2} Pad of 2-oz. Copper)			84.1	°C/W
ESD	IEC 61000-4-2 System ESD	Air Gap	15.0		kV
		Contact	8.0		
	Human Body Model, ANSI / ESDA / JEDEC JS-001-2012	All Pins	3.5		
	Charged Device Model, JEDEC JESD22-C101	All Pins	2.0		
Surge	IEC 61000-4-5, Surge Protection	V_{IN}	100		V

Note:

1. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.5	25.0	V
T_A	Operating Temperature	-40	+85	°C

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise indicated. Typical values are V_{IN} = 5.0 V, I_{IN} ≤ 3 A, C_{IN} = 0.1 µF and T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN_CLAMP}	Input Clamping Voltage	I_{IN} = 10 mA		35		V
I_Q	Input Quiescent Current	V_{IN} = 5 V, #EN = 0 V		58	100	µA
I_{IN_Q}	OVLO Supply Current	V_{OVLO} = 3 V, V_{IN} = 5 V, V_{OUT} = 0 V		52	100	µA
V_{IN_OVLO}	Internal Over-Voltage Trip Level	V_{IN} Rising	13.6	14.0	14.4	V
		V_{IN} Falling	13.0			V
V_{OVLO_TH}	OVLO Set Threshold	V_{IN} = 2.5 V to V_{OVLO}	1.12	1.20	1.24	
V_{OVLO_RNG}	Adjustable OVLO Threshold Range	V_{IN} = 2.5 V to V_{OVLO}	4		25	V
V_{OVLO_SELECT}	External OVLO Select Threshold			0.30	0.28	V
V_{UVLO}	Under-Voltage Trip Level	VIN Rising, T_A= -40 to 85°C		2.25	2.4	V
		VIN Falling, T_A= -40 to 85°C		1.95	2.1	V
R_{ON}	Resistance from V_{IN} to V_{OUT}	V_{IN} = 5 V, I_{OUT} = 1 A, T_A = 25°C		30	39	mΩ
C_{OUT}	OUT Load Capacitance(2)	V_{IN} = 5 V			1000	µF
I_{OLVO}	OVLO Input Leakage Current	V_{OVLO} = V_{OVLO_TH}	-100		100	nA
T_{SDN}	Thermal Shutdown(2)			130		°C
T_{SDN_HYS}	Thermal Shutdown Hysteresis(2)			20		°C
Digital Signals						
V_{OL}	#ACOK Output Low Voltage	I_{SINK} = 1 mA			0.4	V
VIH_#EN	Enable HIGH Voltage	V_{IN} = 2.5 V to V_{OVLO}	1.2			V
VIL_#EN	Enable LOW Voltage	V_{IN} = 2.5 V to V_{OVLO}			0.5	V
I_{ACOK_LEAK}	#ACOK Leakage Current	V_{ACOK} = 3 V, #ACOK Deasserted	-0.5		0.5	µA
#EN_Leak	#EN Leakage Current	V_{IN} = 5.0 V, V_{OUT} = Float	-1.0		1.0	µA
Timing Characteristics						
t_{DEB}	Debounce Time	Time from 2.5 V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 0.1 × V_{IN}		15		ms
t_{START}	Soft-Start Time	Time from V_{IN} = V_{IN_min} to 0.2 × #ACOK, V_{IO} = 1.8 V with 10 kΩ Pull-up Resistor		30		ms
t_{ON}	Switch Turn-On Time	R_L = 100 Ω, C_L = 22 µF, V_{OUT} from 0.1 × V_{IN} to 0.9 × V_{IN},		2		ms
t_{OFF}	Switch Turn-Off Time(2)	R_L = 100 Ω, C_L = 0 µF, V_{IN} > V_{OVLO} to V_{OUT} = 0.8 × V_{IN}		125		ns

Note:

2. Guaranteed by characterization and design.

Timing Diagrams

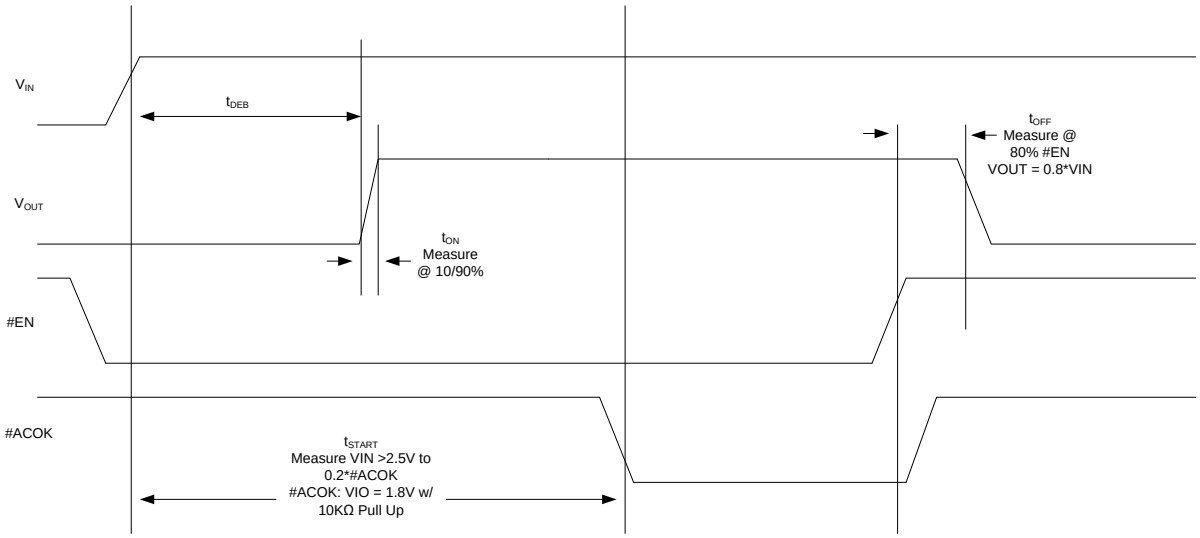


Figure 4. Timing for Power Up and Normal Operation

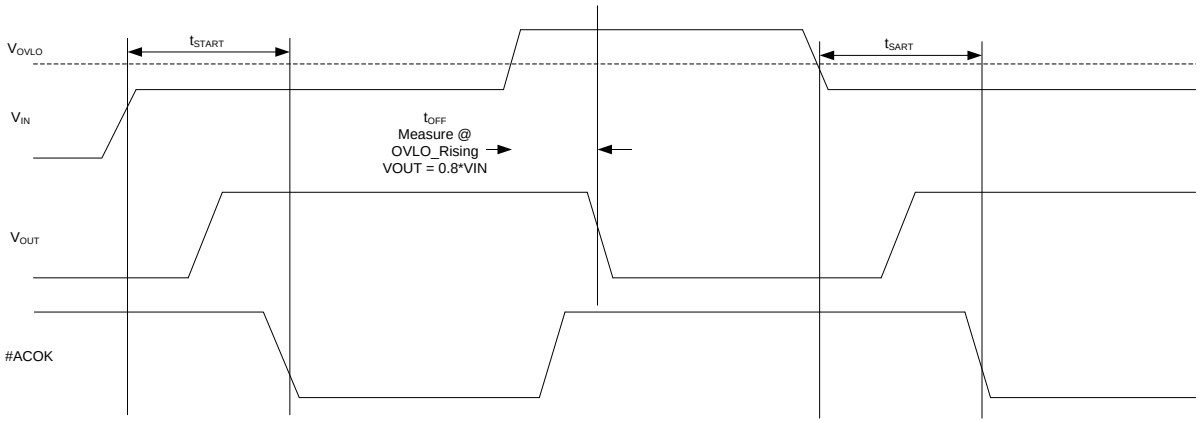


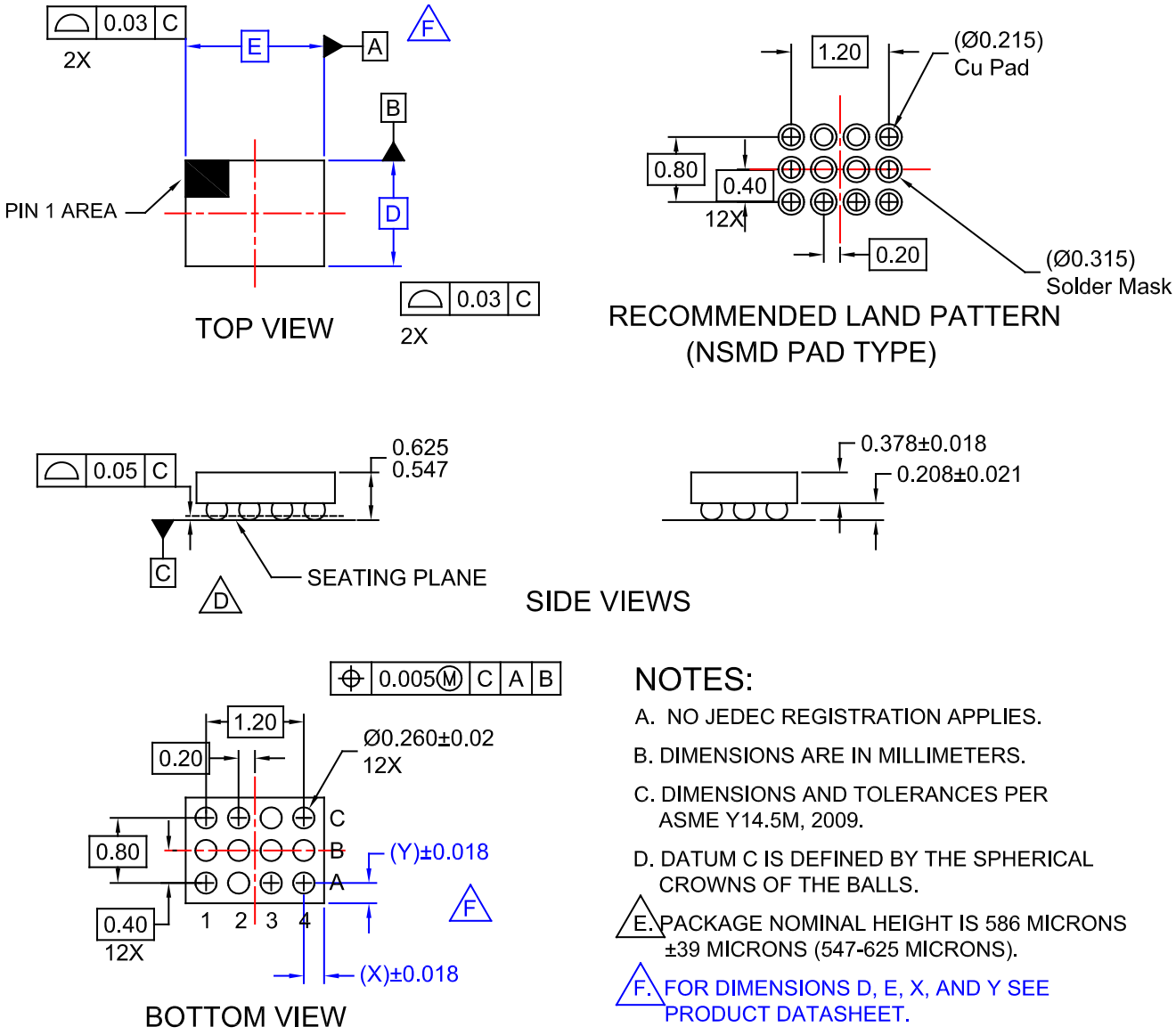
Figure 5. Timing for OVLO Trip

Product-Specific Dimensions

The table below provides information regarding the WLCSP package on the following page.

D	E	X	Y
1288 µm ±30 µm	1828 µm ±30 µm	314 µm ±18 µm	244 µm ±18 µm

Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

Figure 6. 12-Ball, 3×4 Array, 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
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