FDMS8D8N15C

N-Channel Shielded Gate POWERTRENCH® MOSFET

150 V, 85 A, 8.8 mΩ

General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench process that incorporates Shielded Gate technology. This process has been optimized to minimize on−state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 8.8 mΩ at V_{GS} = 10 V, I_D = 45 A
- Max $r_{DS(on)}$ = 9.4 mΩ at V_{GS} = 8 V, I_D = 22.5 A
- Low Qrr, Soft Recovery Body Diode
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Primary DC−DC MOSFET
- Synchronous Rectifier in DC−DC and AC−DC
- Motor Drive
- Solar

ON Semiconductor®

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
150 V	8.8 mΩ @ 10 V	85 A
	9.4 mΩ @ 8 V	

S (1, 2, 3)

G (4)

D (5, 6, 7, 8)

N-CHANNEL MOSFET

Pin 1

Top   Bottom

**Power 56
(PQFN8)
CASE 483AF**

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

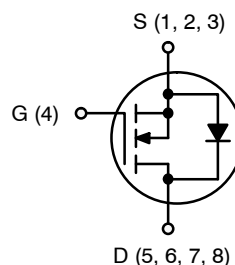| Symbol	Parameter	Value	Unit
V_{DS}	Drain−to−Source Voltage	150	V
V_{GS}	Gate−to−Source Voltage	±20	V
I_D	Drain Current: Continuous, T_C = 25°C (Note 5) Continuous, T_C = 100°C (Note 5) Continuous, T_A = 25°C (Note 1a) Pulsed (Note 4)	85 54 12.2 340	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	102	mJ
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	132 2.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
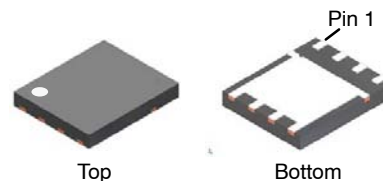
THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case	0.95	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 1a)	46	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–to–Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	150			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		86		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate–to–Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate–to–Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	3.5	4.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate–to–Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		–7.9		mV/°C
$r_{DS(on)}$	Static Drain–to–Source On Resistance	V_{GS} = 10 V, I_D = 45 A		7.0	8.8	mΩ
		V_{GS} = 8 V, I_D = 22.5 A		7.6	9.4	
		V_{GS} = 10 V, I_D = 45 A, T_J = 125°C		12.8	16.1	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 45 A		120	216	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 75 V, V_{GS} = 0 V, f = 1 MHz		3132	3600	pF
C_{oss}	Output Capacitance			927	1160	pF
C_{rss}	Reverse Transfer Capacitance			5.3	9.3	pF
R_g	Gate Resistance			0.73	1.2	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 75 V, I_D = 45 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		23	40	ns
t_r	Rise Time			19	38	ns
$t_{d(off)}$	Turn-Off Delay Time			30	49	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 75 V, I_D = 45 A		38	50	nC
Q_{gs}	Gate–to–Source Charge	V_{DD} = 75 V, I_D = 45 A		16.4		nC
Q_{gd}	Gate–to–Drain "Miller" Charge	V_{DD} = 75 V, I_D = 45 A		5.7		nC
Q_{oss}	Output Charge	V_{DD} = 75 V, V_{GS} = 0 V		101		nC

## ELECTRICAL CHARACTERISTICS $(T_J = 25°C$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source–to–Drain Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 2.2$ A (Note 2)		0.73	0.98	V
		$V_{GS} = 0$ V, $I_S = 45$ A (Note 2)		0.88	1.0	
t_{rr}	Reverse Recovery Time	$I_F = 45$ A, di/dt = 100 A/μs		68	86	ns
Q_{rr}	Reverse Recovery Charge			108	172	nC
t_{rr}	Reverse Recovery Time	$I_F = 45$ A, di/dt = 1000 A/μs		39	50	ns
Q_{rr}	Reverse Recovery Charge			495	748	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:
1. $R_{θJA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5×1.5 in. board of FR–4 material. $R_{θCA}$ is determined by the user's board design.
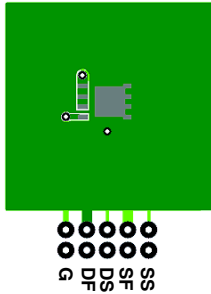
a) 46°C/W when mounted on a 1 in² pad of 2 oz copper.
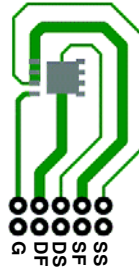
b) 115°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 102 mJ is based on starting $T_J = 25°C$; N-ch: L = 0.1 mH, $I_{AS} = 45$ A, $V_{DD} = 150$ V, $V_{GS} = 10$ V. 100% tested at L = 0.1 mH, $I_{AS} = 45$ A.
4. Pulsed Id please refer to Figure 11 SOA graph for more details. (Note: the final number may change pending results on device characterization).
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Quantity
FDMS8D8N15C	FDMS8D8N15C	Power 56 (PQFN8) (Pb-Free / Halogen Free)	13″	12 mm	3000 units

FDMS8D8N15C

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)
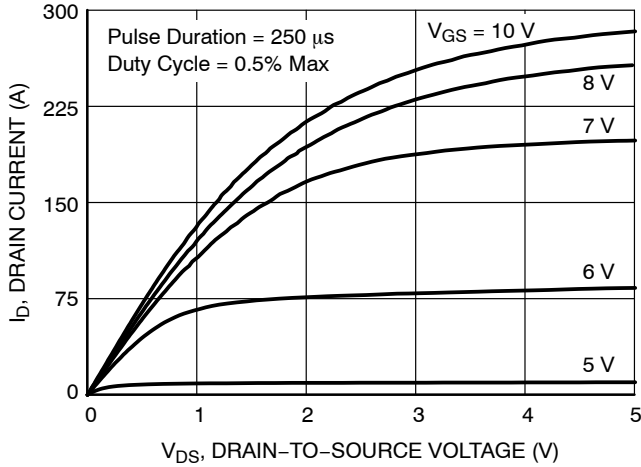
Figure 1. On−Region Characteristics
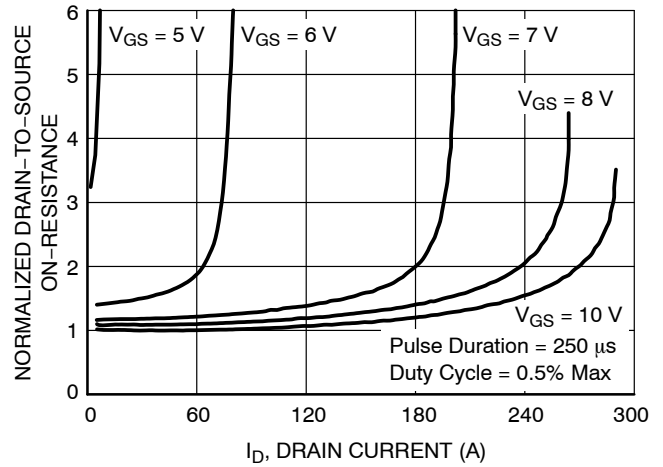
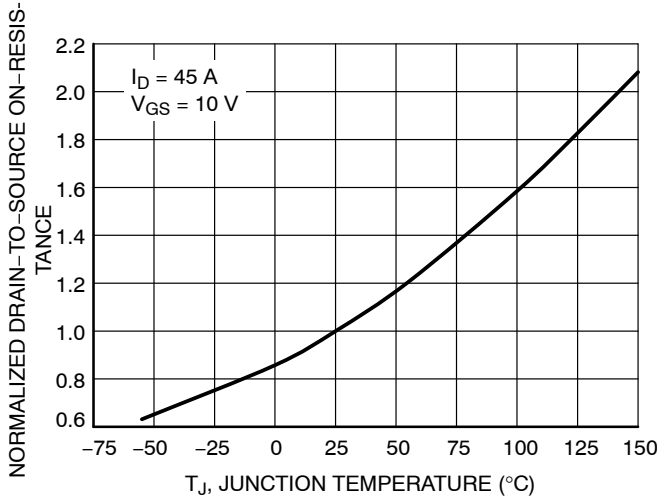**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

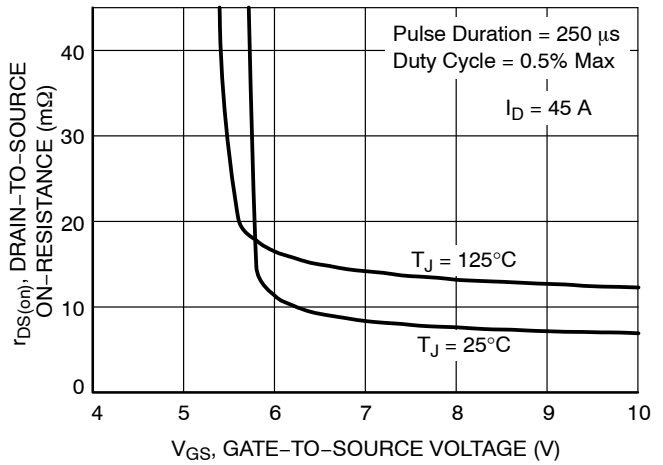**Figure 3. Normalized On−Resistance vs. Junction Temperature**
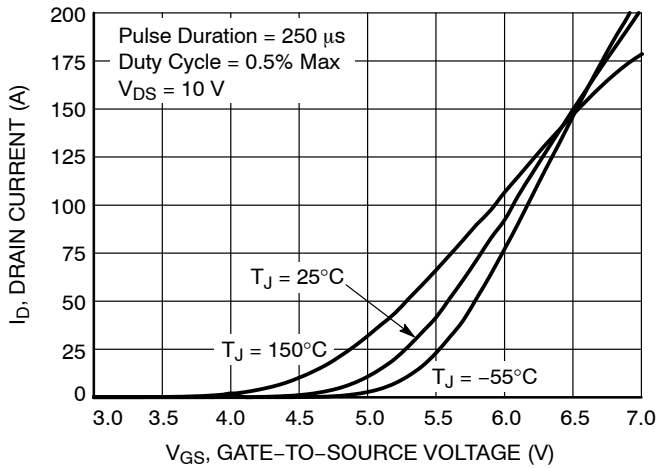
Figure 4. On−Resistance vs. Gate−to−Source Voltage
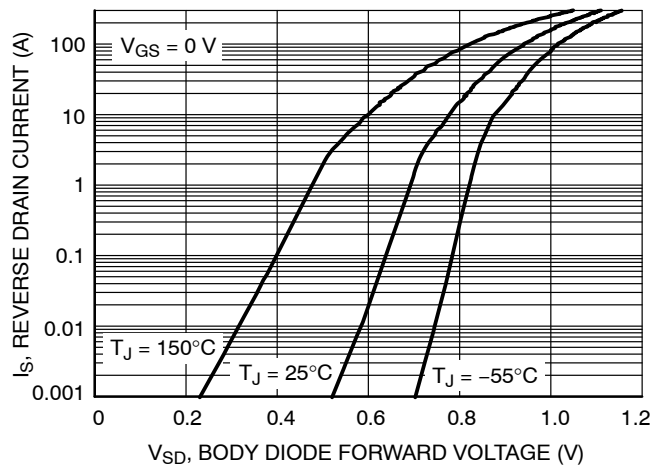
Figure 5. Transfer Characteristics

Figure 6. Source−to−Drain Diode Forward Voltage vs. Source Current

FDMS8D8N15C

TYPICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted.)
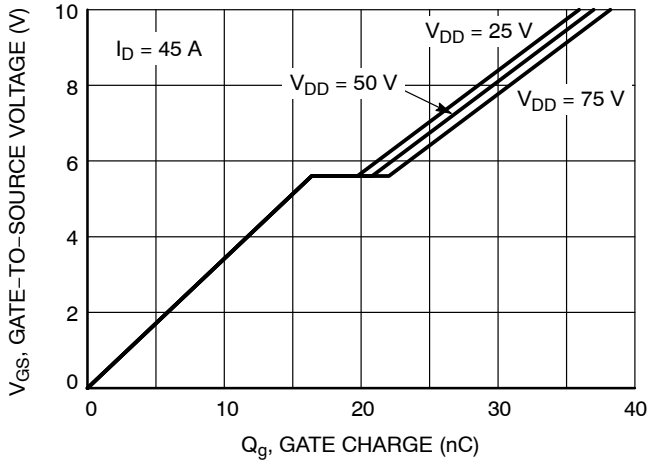
Figure 7. Gate Charge Characteristics
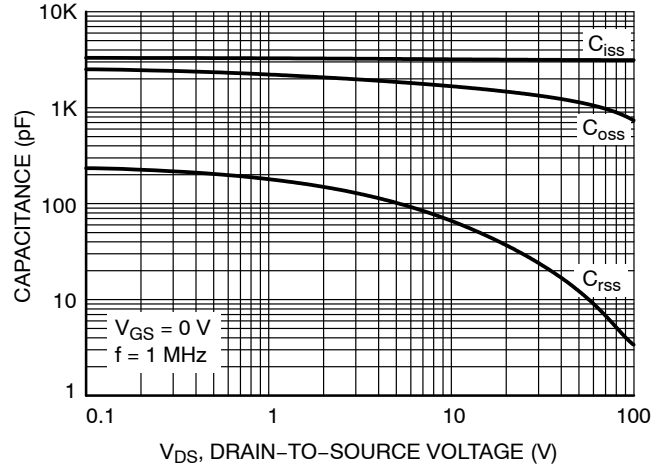
Figure 8. Capacitance vs. Drain−to−Source Voltage
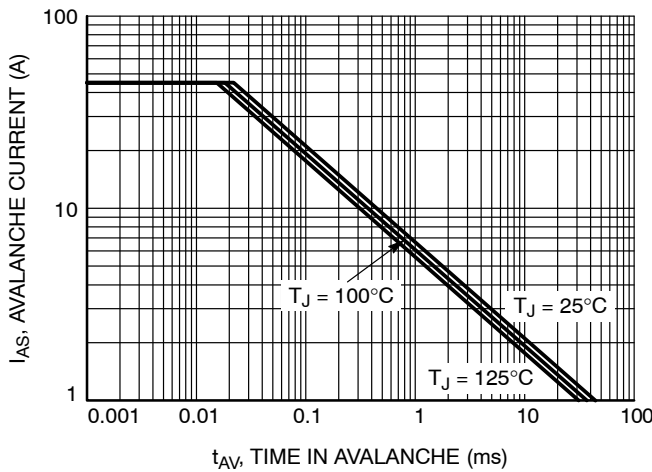
Figure 9. Unclamped Inductive Switching Capability
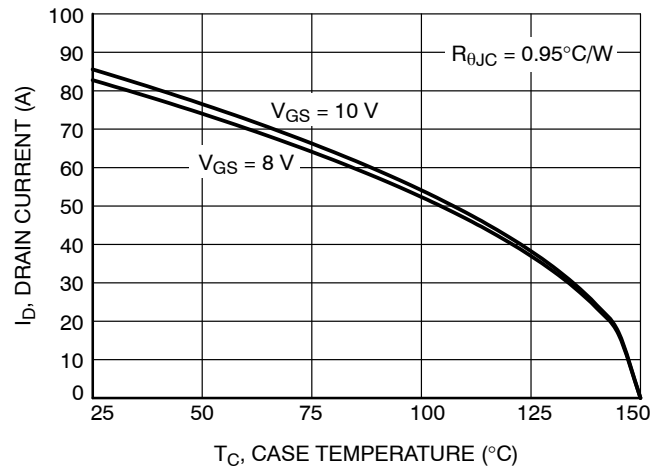
Figure 10. Maximum Continuous Drain Current vs. Case Temperature
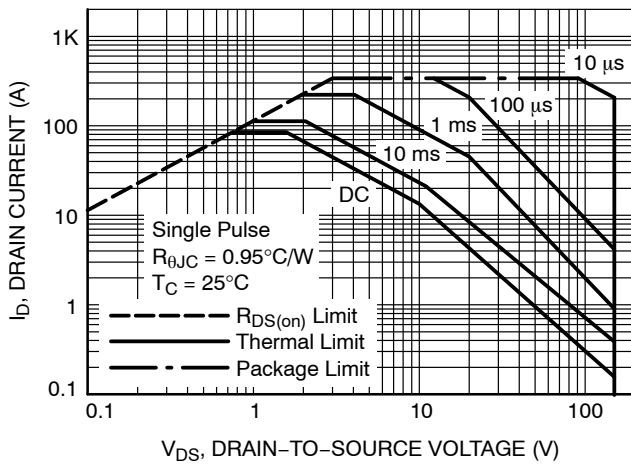
Figure 11. Forward Bias Safe Operating Area
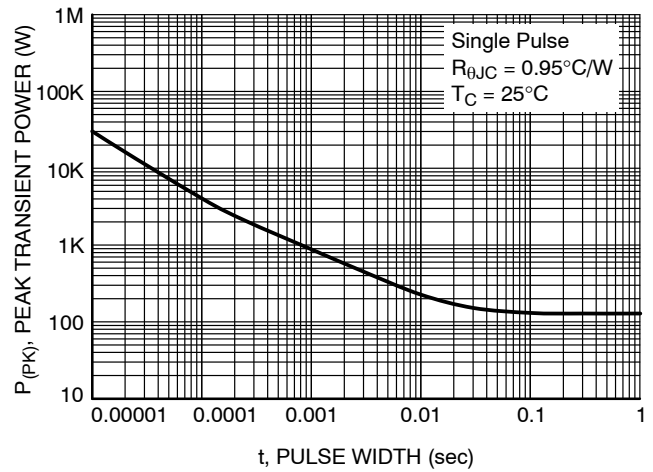
Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)
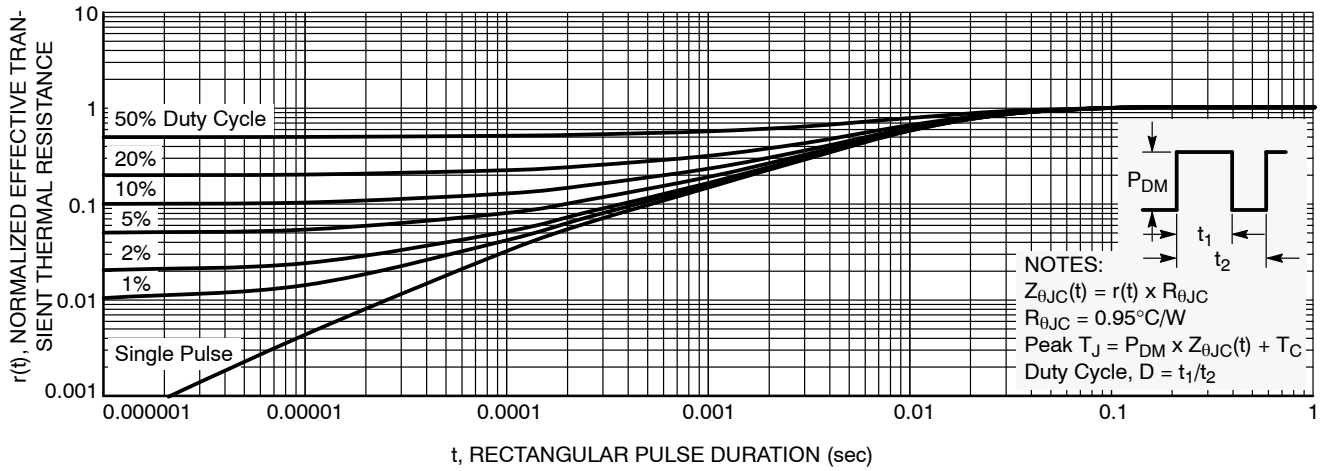
Figure 13. Junction−to−Case Transient Thermal Response Curve
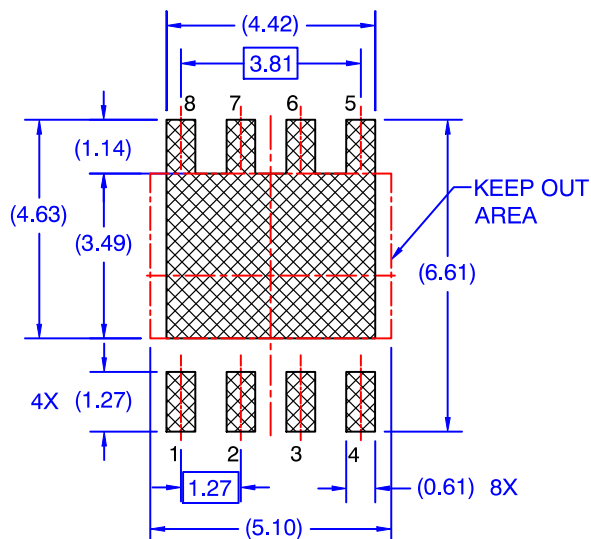
PQFN8 5X6, 1.27P
CASE 483AF
ISSUE O

DATE 30 SEP 2016

TOP VIEW

PIN #1 INDICATOR

SIDE VIEW

SEE DETAIL A

LAND PATTERN RECOMMENDATION

KEEP OUT AREA

DETAIL A
SCALE: 2:1

SEATING PLANE

BOTTOM VIEW
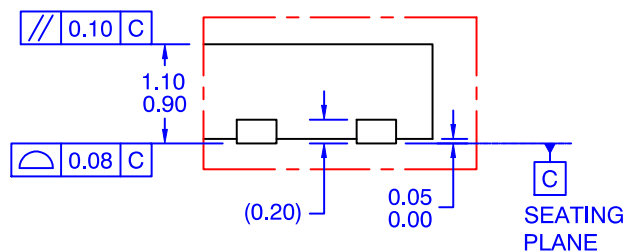
NOTES: UNLESS OTHERWISE SPECIFIED
A) PACKAGE STANDARD REFERENCE:
   JEDEC MO-240, ISSUE A, VAR. AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS
   OR MOLD FLASH. MOLD FLASH OR
   BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER
   ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES
   OR VIAS WITHIN THE KEEP OUT AREA.
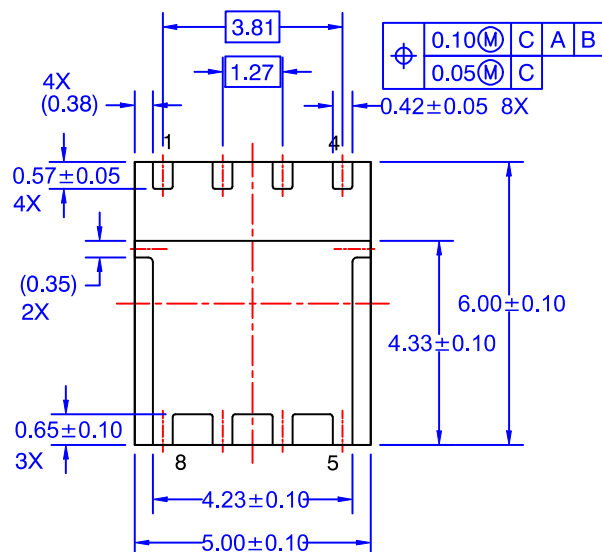
DOCUMENT NUMBER:	98AON13656G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	PQFN8 5X6, 1.27P		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊