

ESDALC6V1-5P6

ESD protection for high speed interface

Features

- Diode array topology
- Low capacitance (12 pF typical)
- Lead-free package

Benefits

- Low capacitance uni-directional ESD protection.
- Low PCB space consuming, 2.5 mm² max. footprint
- Low leakage current
- High reliability offered by monolithic integration

Complies with the following standards

- IEC 61000-4-2 level 4:
 - 8 kV (contact discharge)
 - 15 kV (air discharge)
- MIL STD 883G-Method 3015-7: class3B
 - Human body model

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Description

The ESDALC6V1-5P6 is a monolithic array designed to protect up to 5 lines against ESD transients.

The device is ideal for high speed interface applications where both reduced printed circuit board space and power absorption capability are required.







1/8

1 Characteristics

Symbol	Parameter			Value	Unit
V _{PP} ⁽¹⁾	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge		± 8 ± 15	kV
P _{PP} ⁽¹⁾	Peak pulse power dissipation (8/20 μ s) T_j initial = T_{amb}			30	W
I _{PP}	Peak pulse current (8/20 μs)			2.5	Α
Тj	Junction temperature			125	°C
T _{stg}	Storage temperature range			-55 to +150	°C
TL	Maximum lead temperature for soldering during 10 s			260	°C
T _{OP}	Operating temperature range			- 40 + 125	°C

Table 1. Absolute ratings ($T_{amb} = 25 \ ^{\circ}C$)

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Electrical characteristics ($T_{amb} = 25 \text{ °C}$)

Table 2.	Electrical characteristics $(1_{amb} = 25 C)$						
Symbol	Parameter			▲ 1			
V _{RM}	Stand-off voltage			F			
V _{BR}	Breakdown voltage	V _{CL} V _{BR} V _{RM}					
V _{CL}	Clamping voltage						
I _{RM}	Leakage current						
I _{PP}	Peak pulse current			>V			
αΤ	Voltage temperature coefficient						
V _F	Forward voltage drop						
С	Capacitance	Slope: 1/R _d					
R _d	Dynamic resistance	↓					
Parameter	Test condition		Min	Тур	Max	Unit	
V _{RRM}	Reverse stand-off voltage				5	V	
V_{BR}	I _R = 1 mA		6.1		7.2	V	
I _{RM}	V _{RM} = 3 V				70	nA	
V	Non repetitive peak pulse voltage	I _{PP} = 1 A			10	V	
V _{CL}	(8/20 μs)	I _{PP} = 2.5 A			14	v	
V _F	I _F = 10 mA				1	V	
R _d				2	3	Ω	
αT ⁽¹⁾	I _R = 1 mA				5	10 ⁻⁴ /°C	
С	$V_{R} = 0 V DC, F = 1 MHz,$ $V_{osc} = 30 mV rms$			12	15	pF	

1. $\Delta V_{BR} = \alpha T x (T_{amb} - 25 \text{ °C}) x V_{BR} (25 \text{ °C})$







Figure 4. Clamping voltage versus peak pulse current (typical values)



Breakdown voltage versus initial Figure 6. junction temperature

Figure 5. **Relative variation of leakage** current versus junction temperature (typical values)

t_p(μs)

10



Figure 7. Junction capacitance versus reverse voltage applied (typical values)



Figure 3. (T_i initial = 25 °C)

P_{PP}(W)

1000

100

10

1

100



ESD response to IEC 61000-4-2 (air discharge -15 kV surge)

Figure 8. ESD response to IEC 61000-4-2 (air discharge +15 kV surge)



Figure 9.

Figure 10. Frequency response curves - all lines together

Figure 11. Crosstalk response curves - 1/2 and 1/3



2 Application information





3 Ordering information scheme







4 Package information

• Epoxy meets UL 94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 3. SOT666 dimensions



Figure 14. SOT666 footprint (dimensions in mm)









5 Ordering information

Table 4. Ordering informatic

	<u> </u>				
Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1-5P6	J ⁽¹⁾	SOT666	2.9 mg	3000	Tape and reel

1. The marking can be rotated by 90° to diferentiate assembly location

6 Revision history

Date	Revision	Description of changes
29-May-2007	1	First issue.
30-Jul-2007	2	Upgrade V_{CL} from 8 V to 10 V and from 9.5 V to 14 V.
15-Nov-2007	3	Reformatted to current standards. Marking changed to J in <i>Table 4</i> . Notes on marking rotation added to <i>Table 4</i> and <i>Figure 15</i> .



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