Protection Device

TVS (Transient Voltage Suppressor)

ESD202-B1-CSP01005

Bi-directional, 5.5 V, 6.5 pF, 01005, RoHS and Halogen Free compliant

ESD202-B1-CSP01005

Data Sheet

Revision 1.2, 2014-12-23
Final

Power Management & Multimarket

Edition 2014-12-23

Published by
Infineon Technologies AG
81726 Munich, Germany

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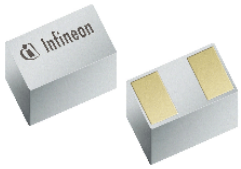
1 Product Overview

1.1 Features



- ESD / Transient protection of data lines according to:
  - **IEC61000-4-2 (ESD): ±17 kV (air discharge), ±15 kV (contact discharge)**
  - **IEC61000-4-4 (EFT):± 2 kV / ±40 A (5/50 ns)**
  - **IEC61000-4-5 (surge): ±3 A (8/20 µs)**
- Bi-directional, working voltage up to V_{RWM} **= ±5.5 V**
- Line capacitance: C_L **= 6.5 pF (typical) at** f **= 1 MHz**
- Low clamping voltage V_{CL} **= 13 V (typical) at** I_{TLP} **= 16 A**
- Low dynamic resistance: R_{DYN} **= 0.2 Ω (typical)**
- Minimized overshoot due to extremely low parasitic inductance of chip scale package
- Miniature form factor (XY) = 01005 (0.43 mm x 0.23 mm)
- Thin 0.15 mm package thickness to allow direct integration into modules
- Optimized assembly: its bidirectional and symmetric I/V characteristics allow placement on the PCB with no danger of polarity orientation issues
- Pb-free (RoHS compliant) and halogen free package

RoHS

1.2 Application Examples

- ESD Protection of highly susceptible IC/ASICs in audio, headset, human digital interfaces
- Dedicated solution to boost space saving and high performance in miniaturized modern electronics

1.3 Product Description

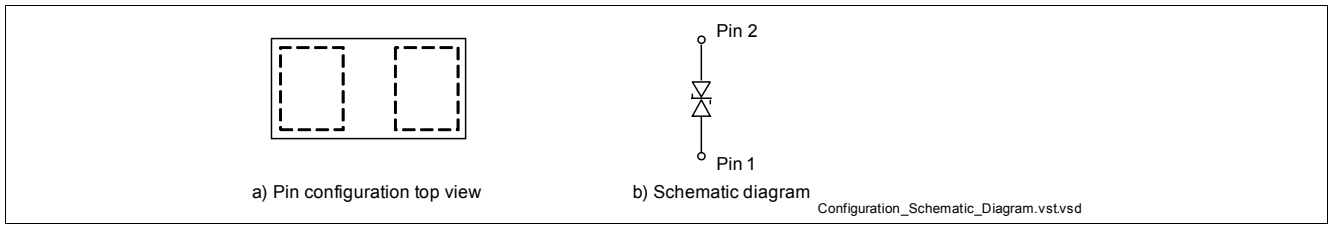


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD202-B1-CSP01005	WLL-2-2	1 line, bi-directional	A[1)]

1) The device does not have any marking or date code on the device backside. The marking code is on pad side.

2 Maximum Ratings

Table 2-1 Maximum Ratings at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values	Unit
ESD discharge[2)] contact air	V_{ESD}	 ±15 ±17	kV
Peak pulse current[3)]	I_{PP}	±3	A
Operating temperature range	T_{OP}	-40 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

1) Device is electrically symmetrical

2) V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)

3) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics

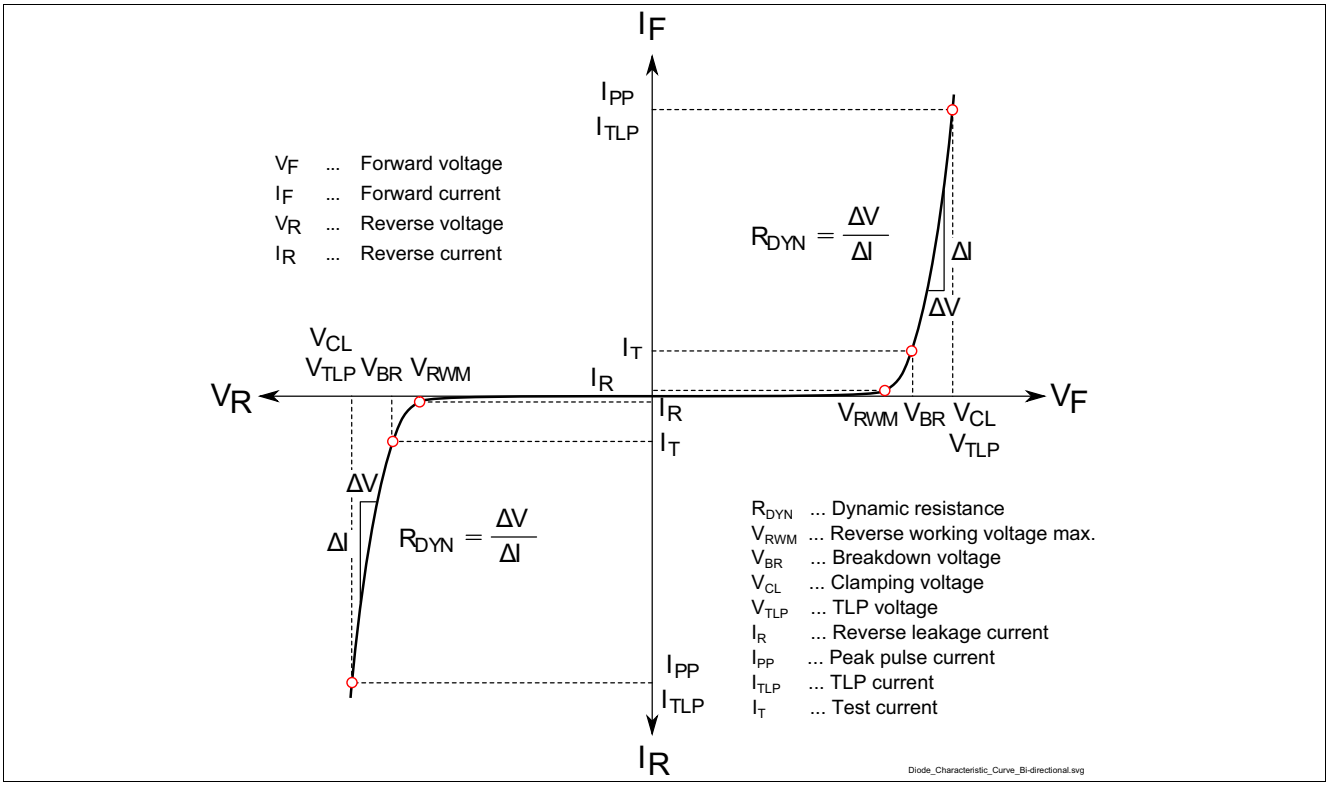


Figure 3-1 Definitions of electrical characteristics

Table 3-1 DC Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-5.5	-	5.5	V	
Breakdown voltage	V_{BR}	6	-	10	V	I_{BR} = 1 mA
Reverse current	I_R	-	-	100	nA	V_R = 5.5 V

1) Device is electrically symmetrical

Table 3-2 AC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	6.5	–	pF	V_R = 0 V, f = 1 MHz
		–	6.5	–		V_R = 0 V, f = 1 GHz

Table 3-3 ESD and Surge Characteristics at T_A = 25 °C, unless otherwise specified[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[2)]	V_{CL}	–	13	–	V	I_{TLP} = 16 A, t_p = 100 ns
		–	17	–		I_{TLP} = 30 A, t_p = 100 ns
Clamping voltage[3)]		–	9.5	–		I_{PP} = 1 A, t_p = 8/20 µs
		–	12	–		I_{PP} = 3 A, t_p = 8/20 µs
Dynamic resistance[2)]	R_{DYN}	–	0.2	–	Ω	t_p = 100 ns

1) Device is electrically symmetrical

2) Please refer to Application Note AN210[1]. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps.

3) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at T_A = 25°C, unless otherwise specified

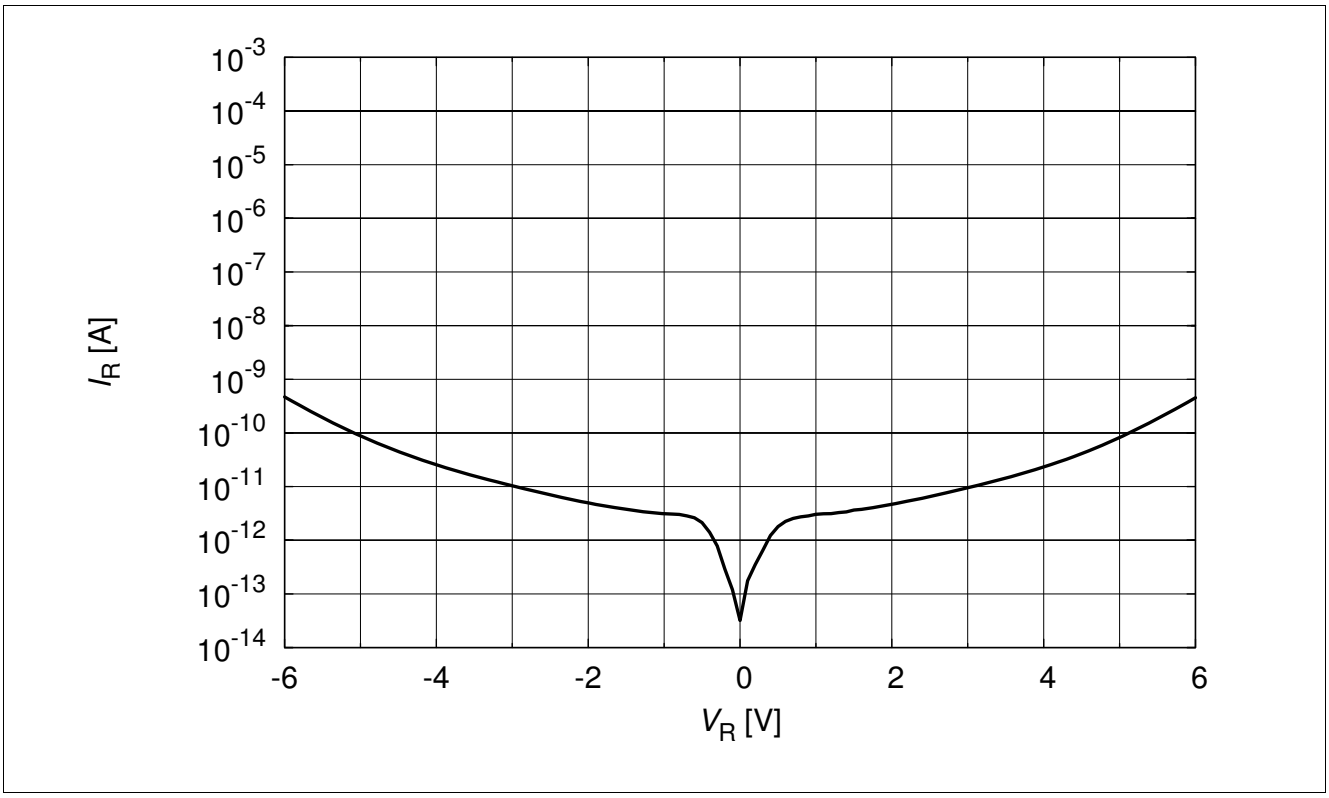


Figure 4-1 Reverse leakage current: $I_R = f(V_R)$

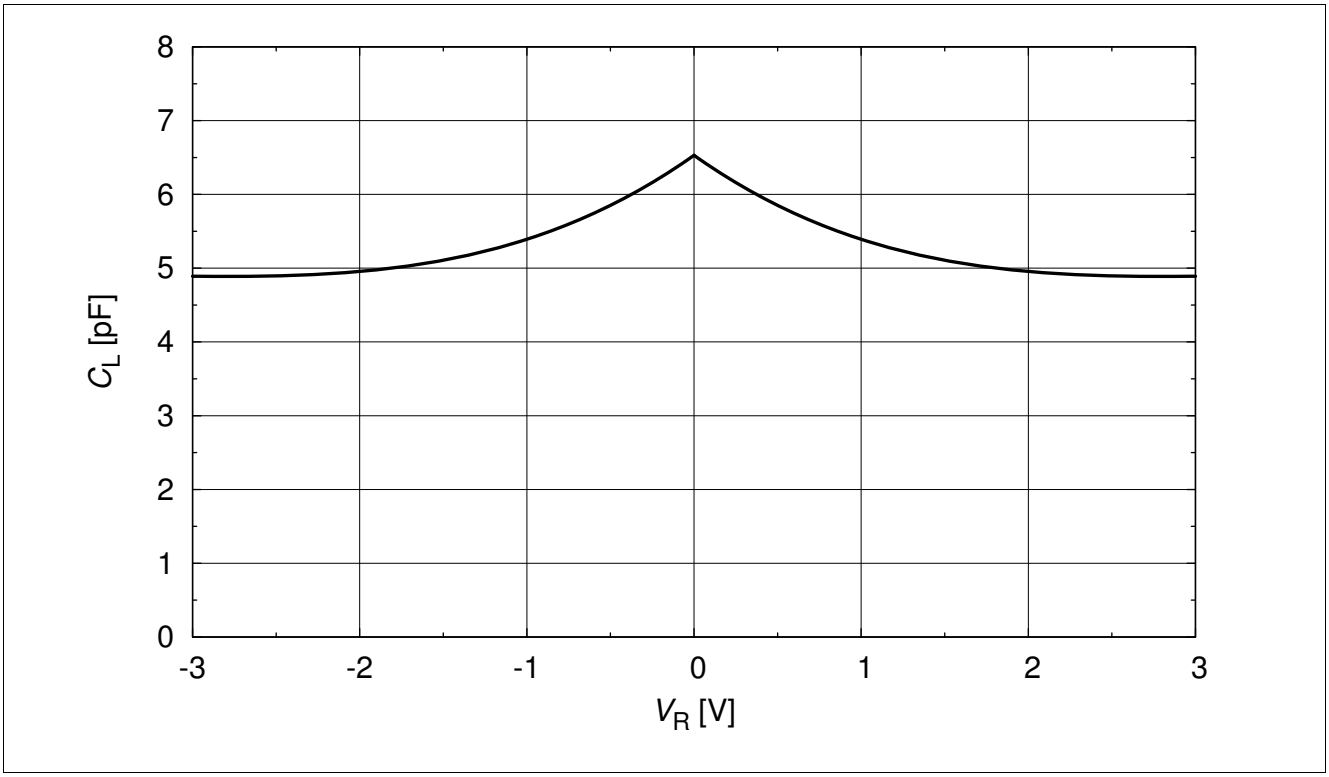


Figure 4-2 Line capacitance: $C_L = f(V_R)$, f = 1 MHz

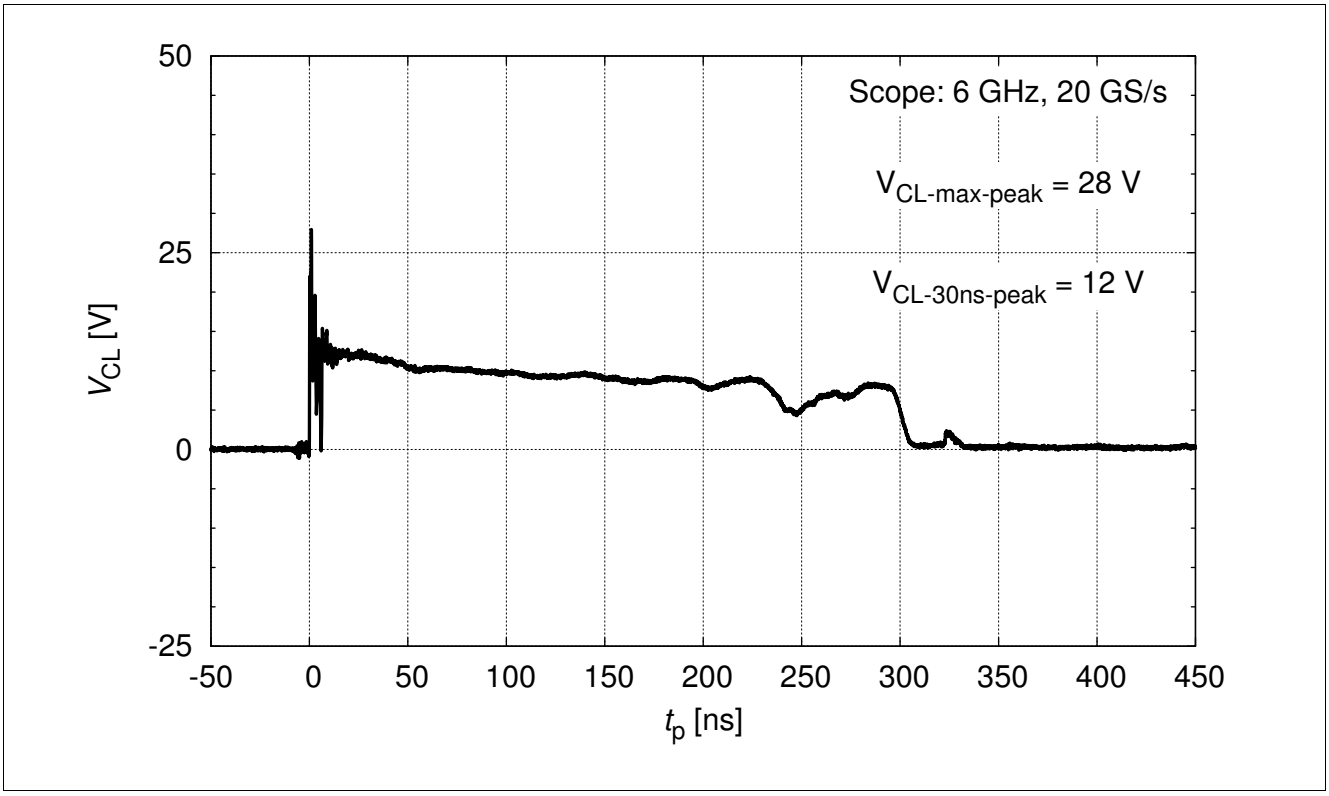


Figure 4-3 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

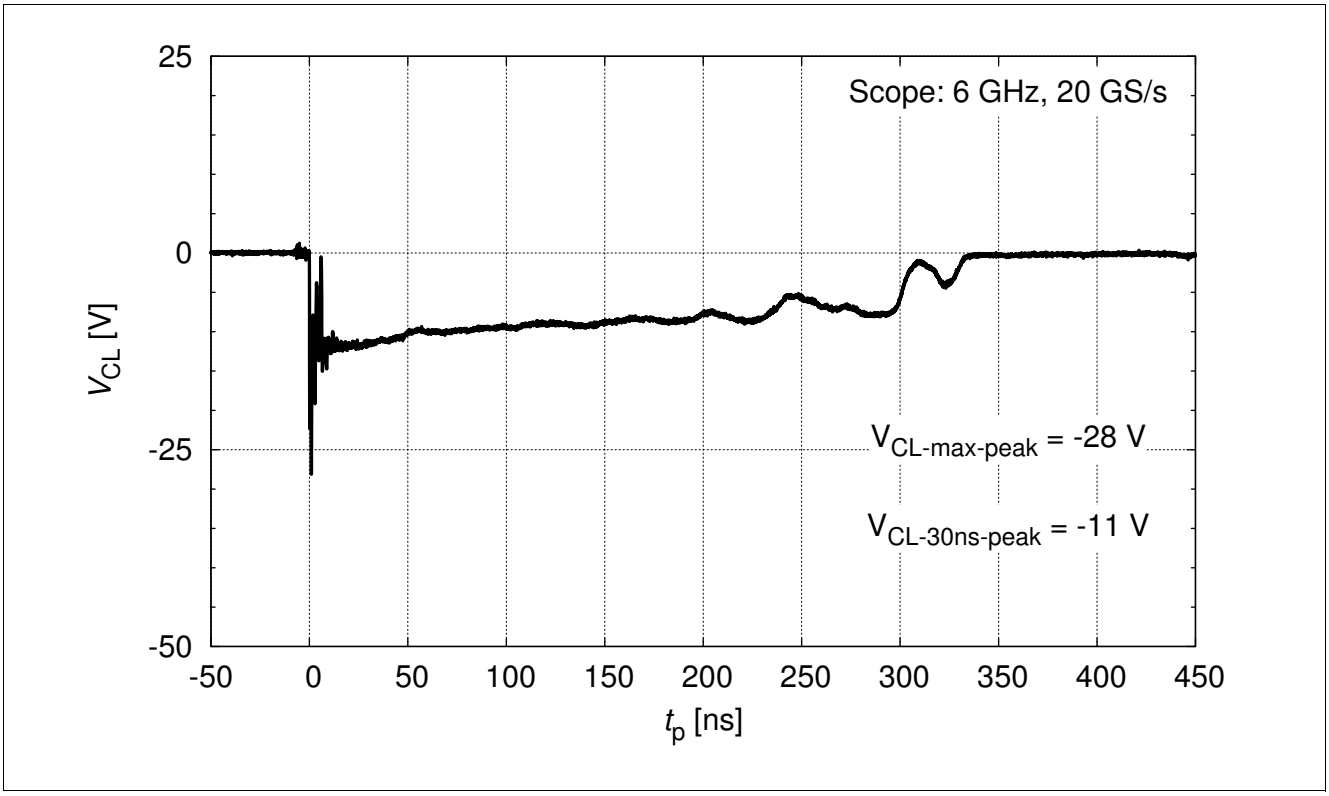


Figure 4-4 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

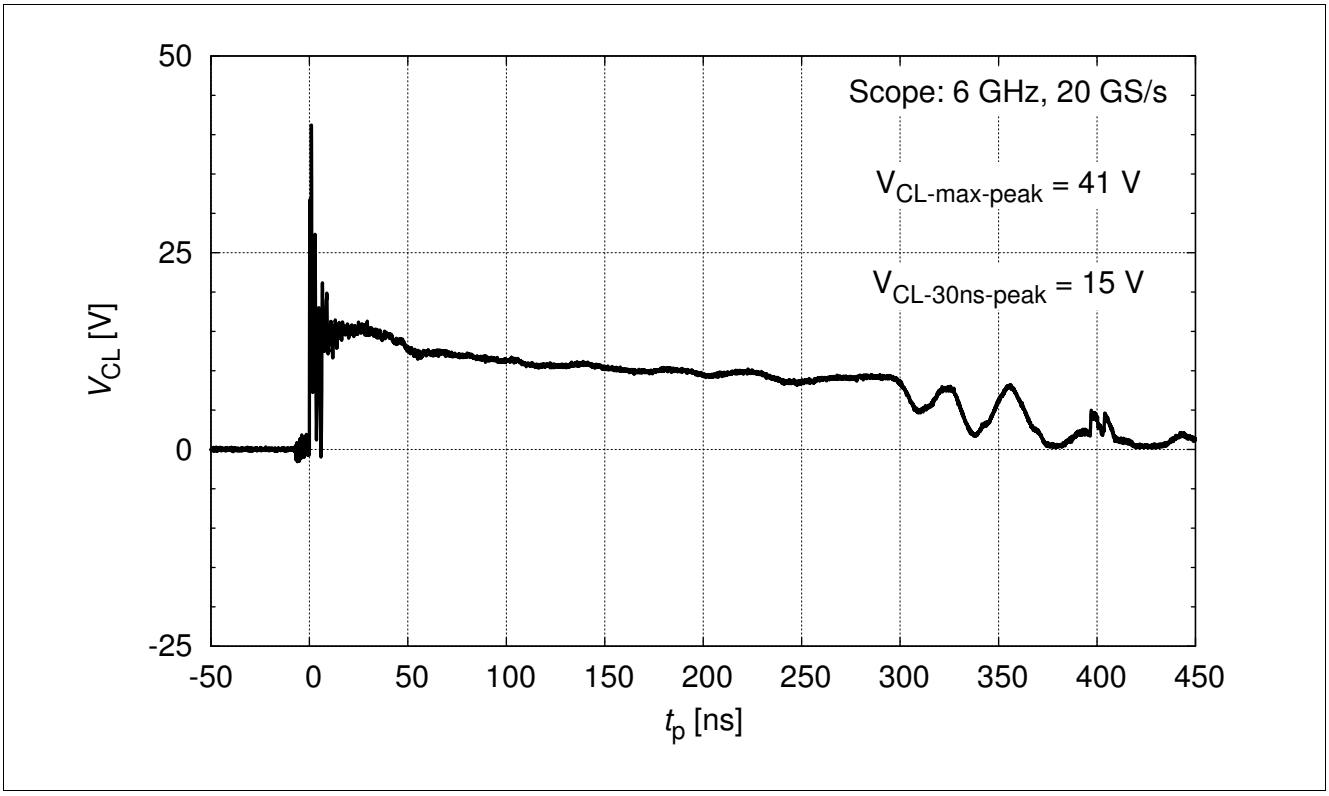


Figure 4-5 Clamping voltage (ESD): V_{CL} = *f*(*t*), 15 kV positive pulse from pin 1 to pin 2

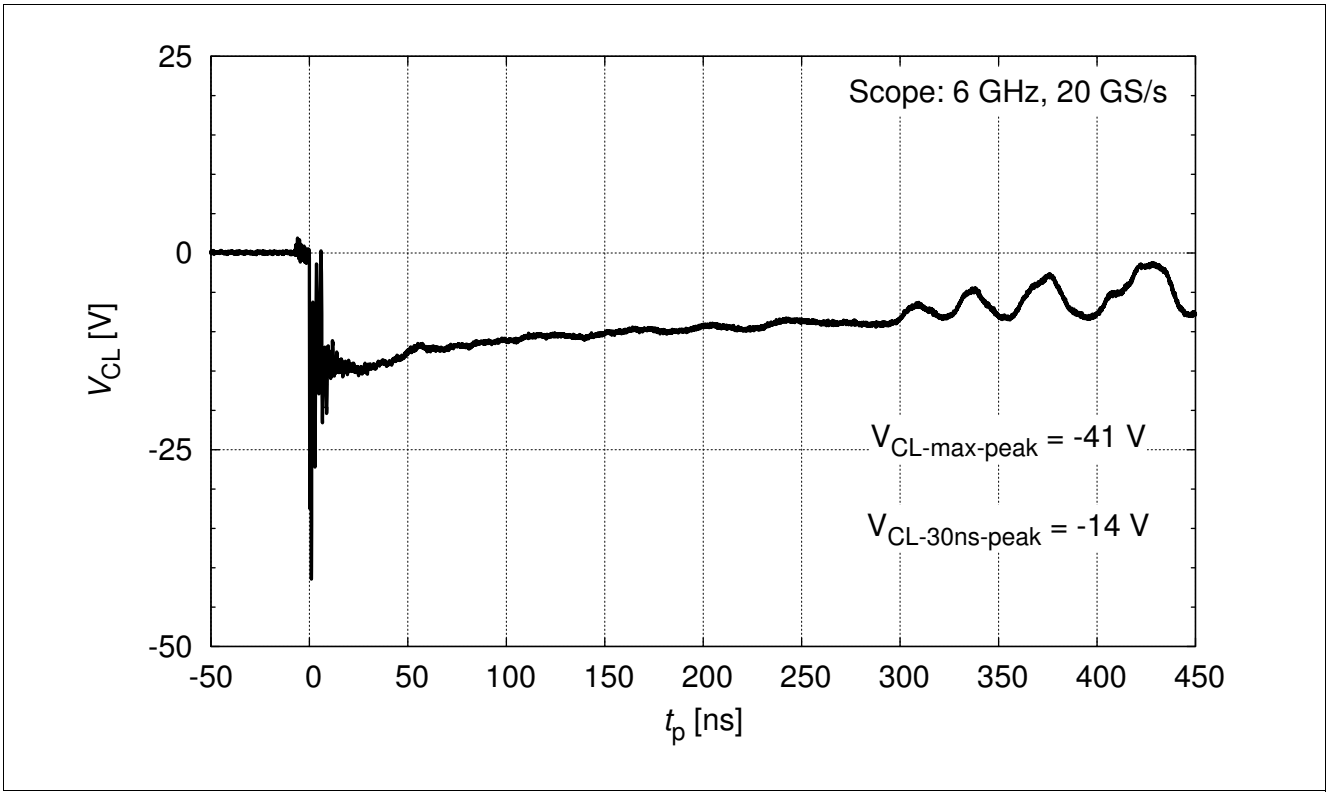


Figure 4-6 Clamping voltage (ESD): V_{CL} = *f*(*t*), 15 kV negative pulse from pin 1 to pin 2

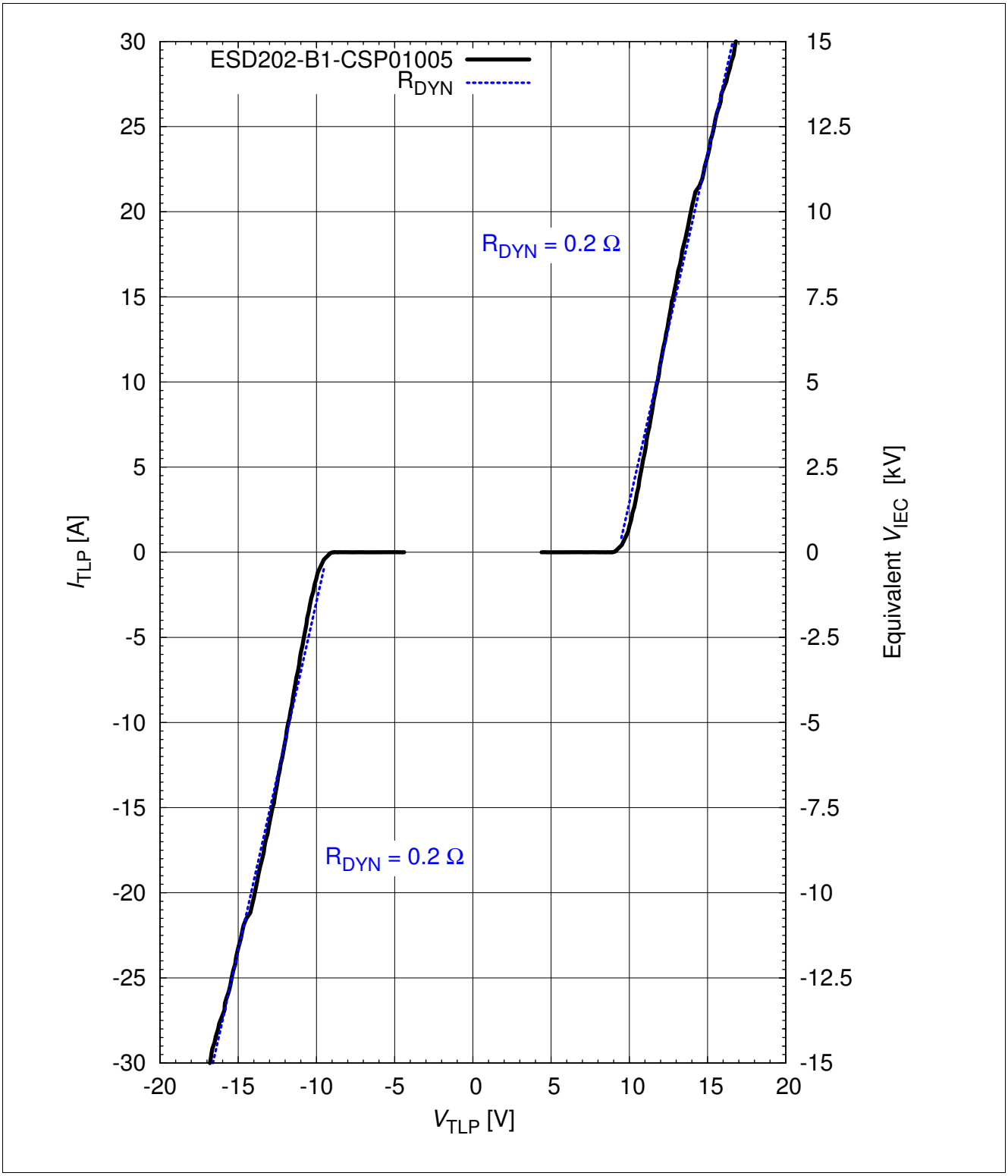


Figure 4-7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2

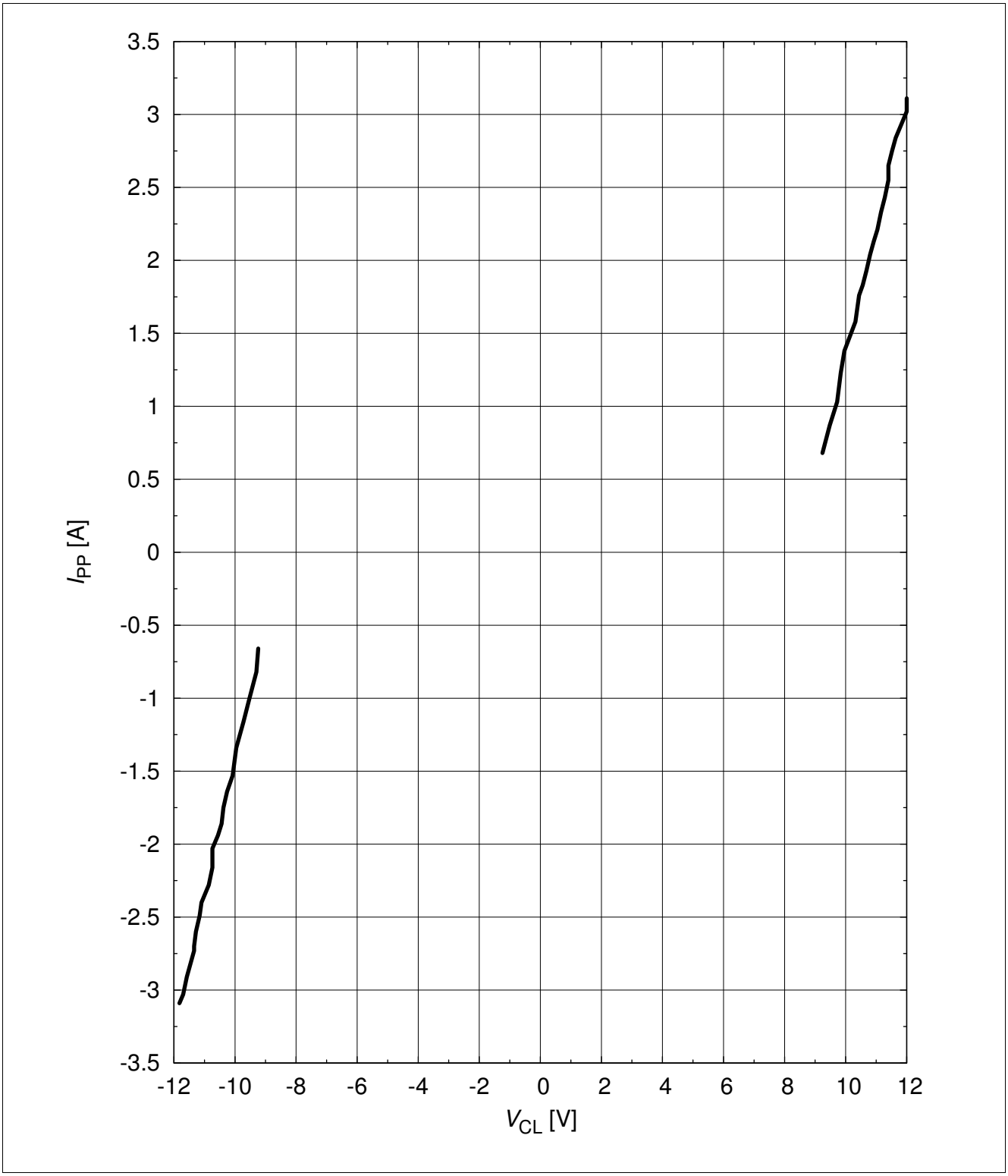


Figure 4-8 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$[1], pin 1 to pin 2

5 Package Information

5.1 WLL-2-2

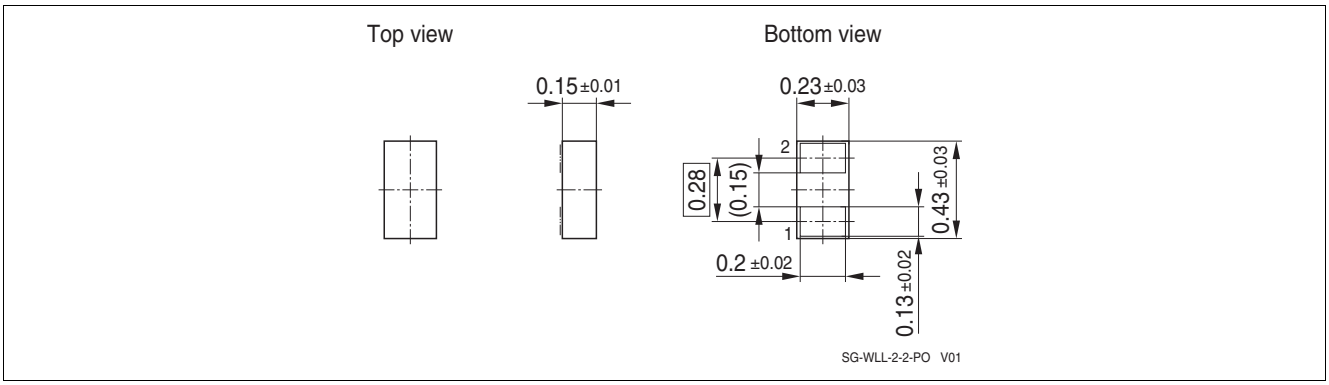


Figure 5-1 WLL-2-2: Package

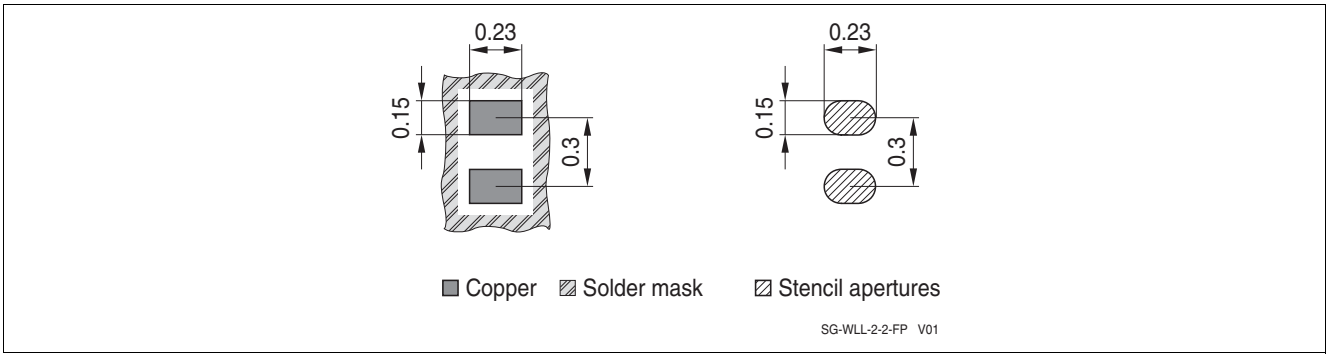


Figure 5-2 WLL-2-2: Footprint (see: Infineon AG - Recommendations for Board Assembly (WLL))

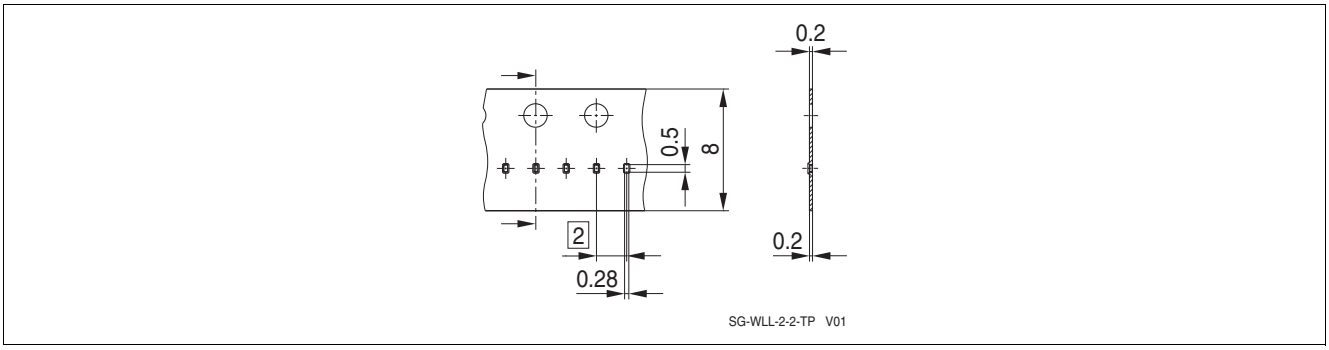


Figure 5-3 WLL-2-2: Packing

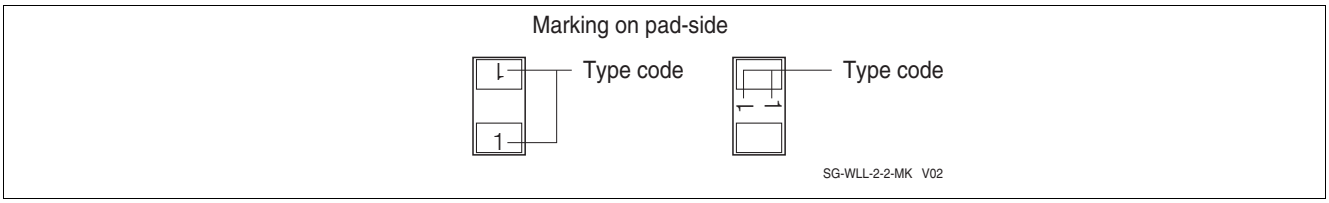


Figure 5-4 WLL-2-2: Marking example Table 1-1 “Part Information” on Page 3

References

[1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendations for Board Assembly (WLL)

Revision History: Rev.1.1, 2014-05-14	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.2, 2014-12-23	
All	Update new format

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