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EFC2J004NUZ

Power MOSFET
for 1-Cell Lithium-ion Battery Protection
12 V, 7.1 mΩ, 14 A, Dual N-Channel

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This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-cell lithium-ion battery applications.

V_{SSS}	R_{SS}(on) Max	I_S Max
12 V	7.1 mΩ @ 4.5 V	14 A
	7.7 mΩ @ 3.8 V	
	9.5 mΩ @ 3.1 V	
	12.4mΩ @ 2.5 V	

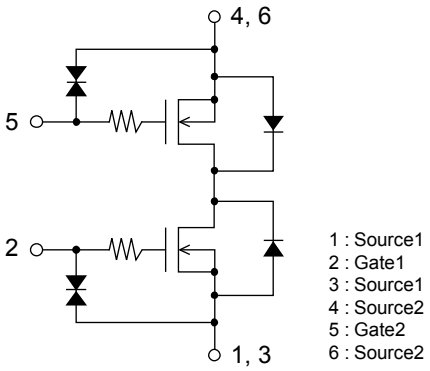
Features

- 2.5 V Drive
- 2 kV ESD HBM
- Common-Drain Type
- ESD Diode-Protected Gate
- Pb-Free, Halogen Free and RoHS compliance

Applications

- 1-Cell Lithium-ion Battery Charging and Discharging Switch

ELECTRICAL CONNECTION
N-Channel



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS at Ta = 25°C (Notes 1, 2)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	±8	V
Source Current (DC)	I_S	14	A
Source Current (Pulse) PW ≤ 10μs, duty cycle ≤ 1%	I_{SP}	60	A
Total Dissipation (Note 2)	P_T	1.5	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55 to +150	°C

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

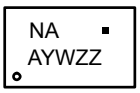
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 2)	$R_{\theta JA}$	83	°C/W

Note 2 : Surface mounted on ceramic substrate (5000 $mm^2 \times 0.8$ mm).

WLCSP6, 2.11x1.18x0.10

GENERIC MARKING DIAGRAM



NA = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot
▪ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS at Ta = 25°C (Notes 3, 4)

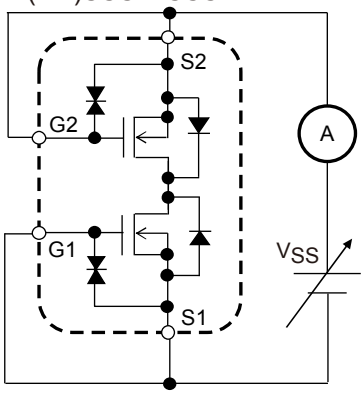
Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V Test Circuit 1	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS} = 10 V, V_{GS} = 0 V Test Circuit 1			1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{SS} = 0 V Test Circuit 2			±1	μA
Gate Threshold Voltage	$V_{GS}(th)$	V_{SS} = 6 V, I_S = 1 mA Test Circuit 3	0.4		1.3	V
Static Source to Source On-State Resistance (Note 4)	$R_{SS}(on)$	I_S = 5 A, V_{GS} = 4.5 V Test Circuit 4	3.7	5.4	7.1	mΩ
		I_S = 5 A, V_{GS} = 3.8 V Test Circuit 4	4.1	5.9	7.7	mΩ
		I_S = 5 A, V_{GS} = 3.1 V Test Circuit 4	4.6	6.7	9.5	mΩ
		I_S = 5 A, V_{GS} = 2.5 V Test Circuit 4	5.8	8.4	12.4	mΩ
Turn-ON Delay Time	$t_d(on)$	V_{SS} = 5 V, V_{GS} = 3.8 V, I_S = 5 A Rg = 10 kΩ Test Circuit 5		15		μs
Rise Time	t_r			35		μs
Turn-OFF Delay Time	$t_d(off)$			100		μs
Fall Time	t_f			75		μs
Total Gate Charge	Qg	V_{SS} = 6 V, V_{GS} = 4.5 V, I_S = 14 A Test Circuit 6		36		nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S = 3 A, V_{GS} = 0 V Test Circuit 7		0.76		V

Note 3 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

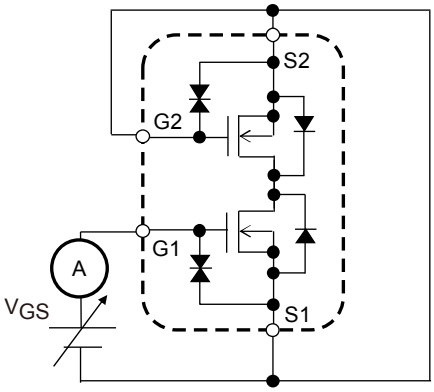
Note 4 : Mounted on ON Semiconductor board.

Test circuits are example of measuring FET1 side

Test Circuit 1
$V_{(BR)SSS}$ / I_{SSS}

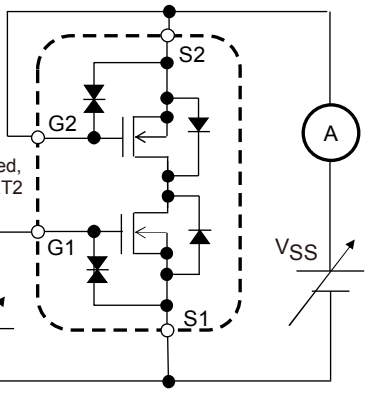


Test Circuit 2
I_{GSS}



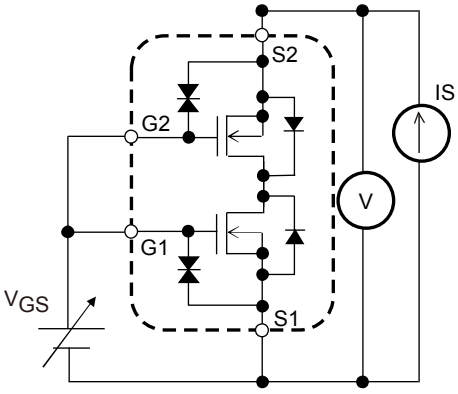
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
$V_{GS(th)}$

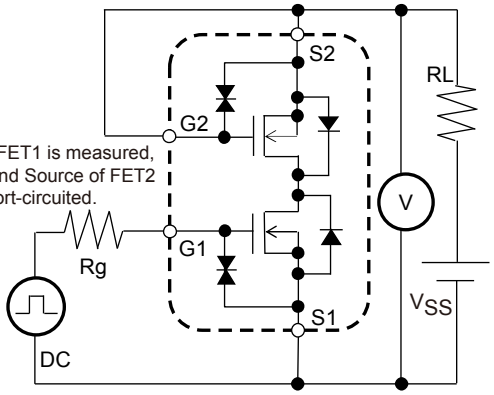


When FET1 is measured, Gate and Source of FET2 are short-circuited.

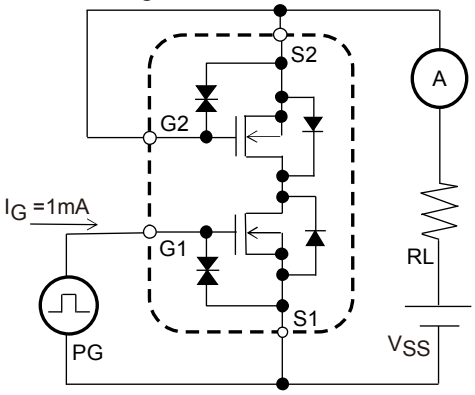
Test Circuit 4
$R_{SS(on)}$



Test Circuit 5
$t_{d(on)}$, t_r, $t_{d(off)}$, t_f

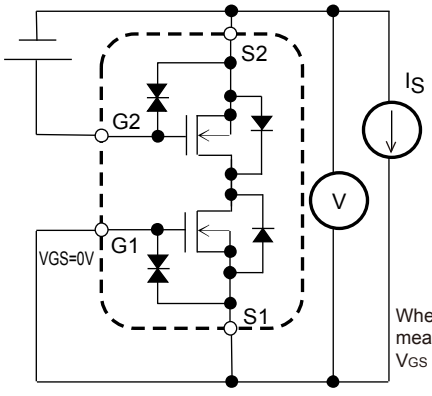


Test Circuit 6
Qg



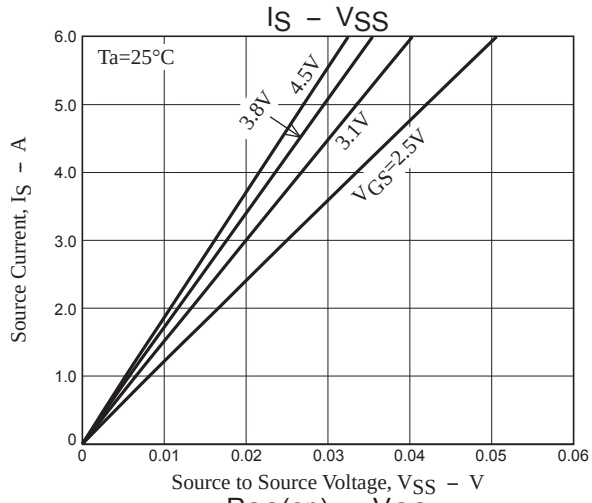
When FET1 is measured, Gate and Source of FET2 are short-circuited.

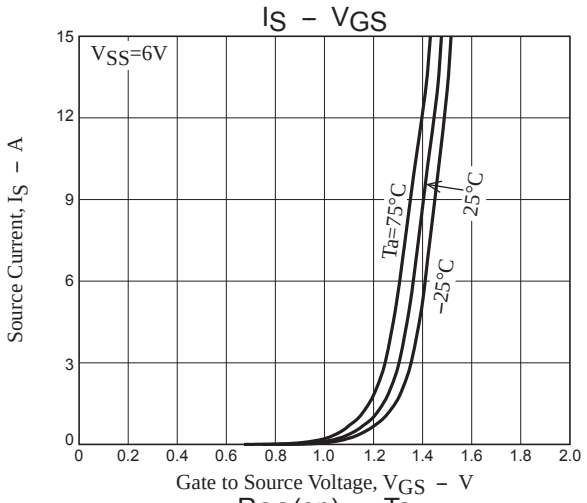
Test Circuit 7
$V_{F(S-S)}$

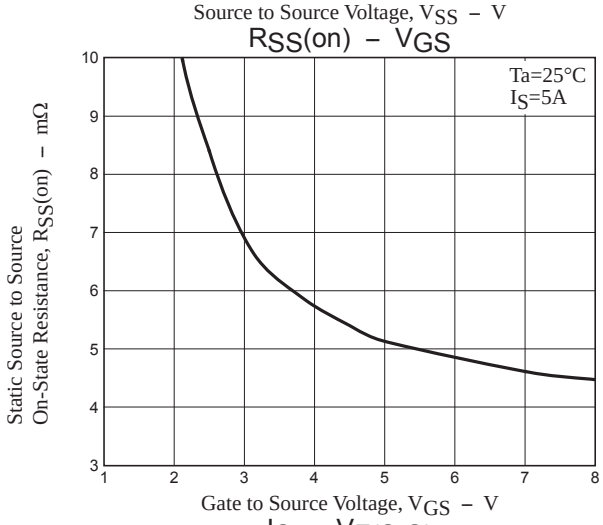


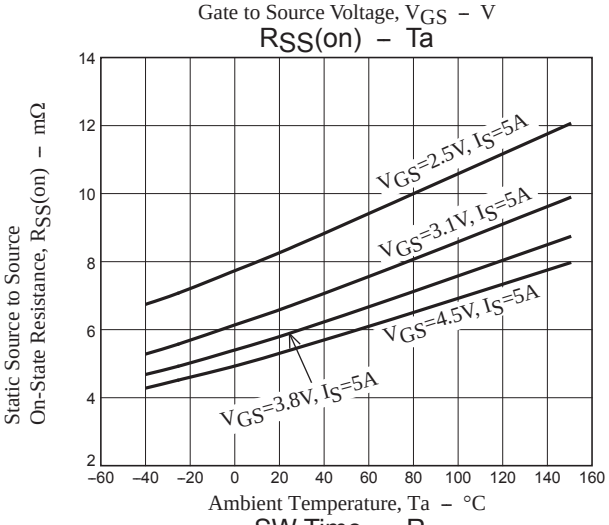
When FET1 is measured,+4.5V is added to V_{GS} of FET2.

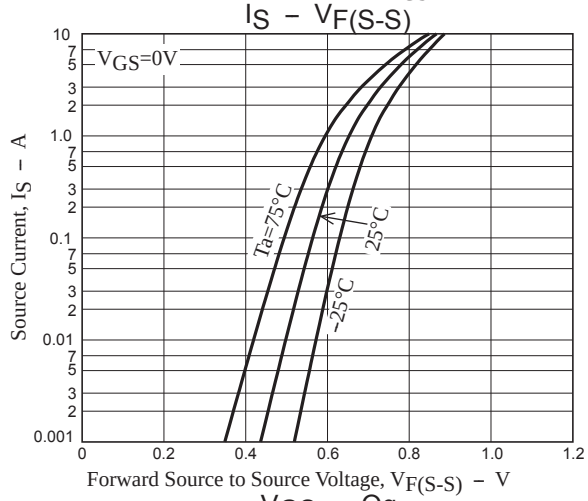
When FET2 is measured, the position of FET1 and FET2 is switched.

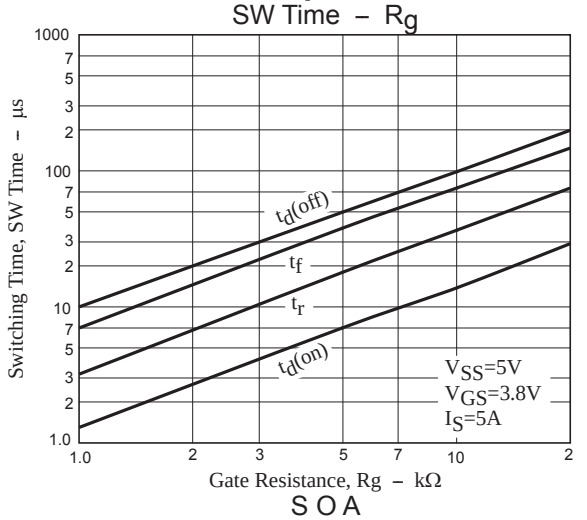

IS – VSS
Ta=25°C
3.8V
4.5V
3.1V
VGS=2.5V
Source Current, IS – A
Source to Source Voltage, VSS – V

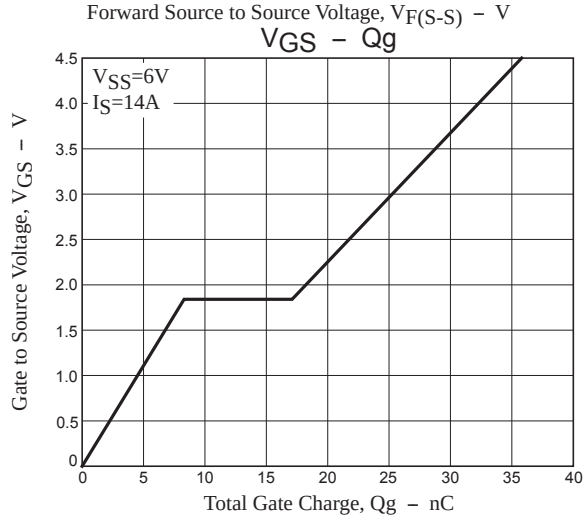

IS – VGS
VSS=6V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Gate to Source Voltage, VGS – V

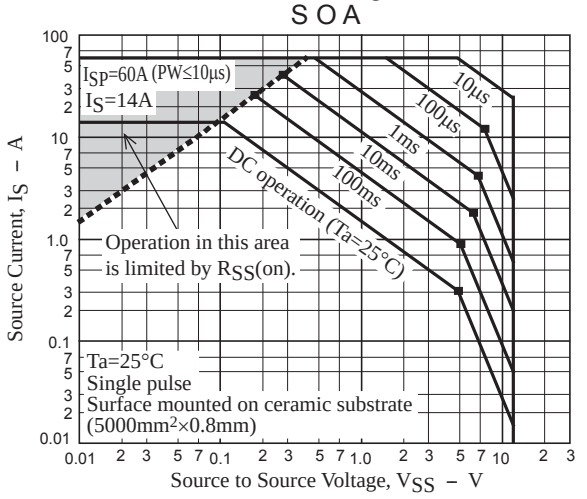

RSS(on) – VGS
Ta=25°C
IS=5A
Static Source to Source
On-State Resistance, RSS(on) – mΩ
Gate to Source Voltage, VGS – V

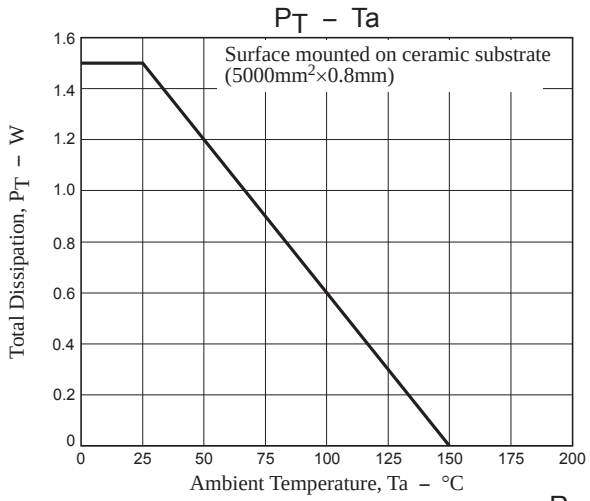

RSS(on) – Ta
VGS=2.5V, IS=5A
VGS=3.1V, IS=5A
VGS=4.5V, IS=5A
VGS=3.8V, IS=5A
Static Source to Source
On-State Resistance, RSS(on) – mΩ
Ambient Temperature, Ta – °C

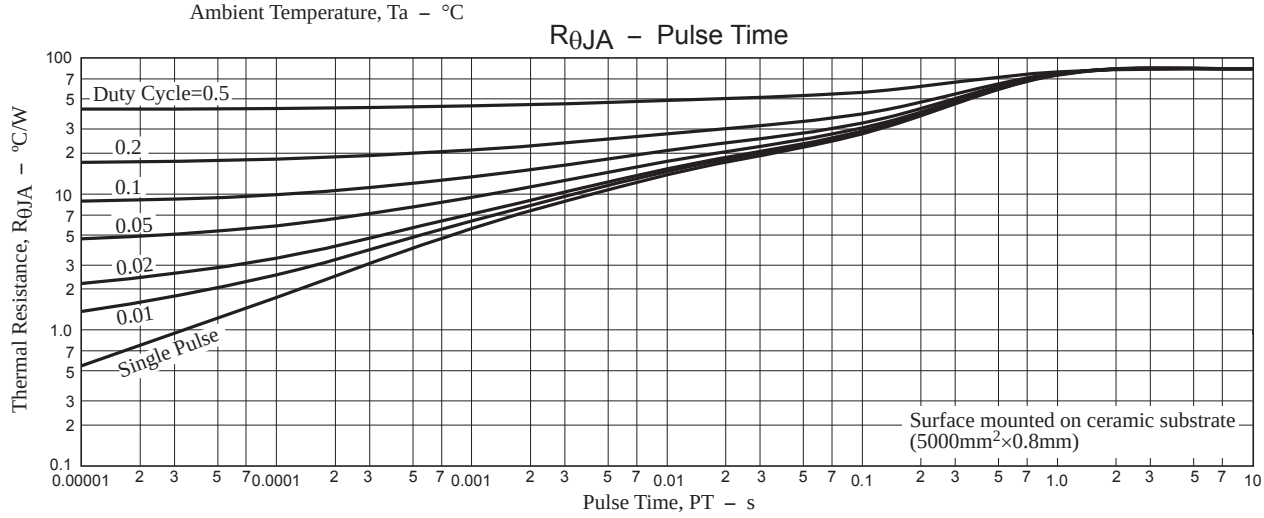

IS – VF(S-S)
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Forward Source to Source Voltage, VF(S-S) – V


SW Time – Rg
td(off)
tf
tr
td(on)
VSS=5V
VGS=3.8V
IS=5A
Switching Time, SW Time – µs
Gate Resistance, Rg – kΩ


VGS – Qg
VSS=6V
IS=14A
Gate to Source Voltage, VGS – V
Total Gate Charge, Qg – nC


S O A
ISP=60A (PW≤10µs)
IS=14A
10µs
100µs
1ms
10ms
100ms
DC operation (Ta=25°C)
Operation in this area
is limited by RSS(on).
Ta=25°C
Single pulse
Surface mounted on ceramic substrate
(5000mm²×0.8mm)
Source Current, IS – A
Source to Source Voltage, VSS – V

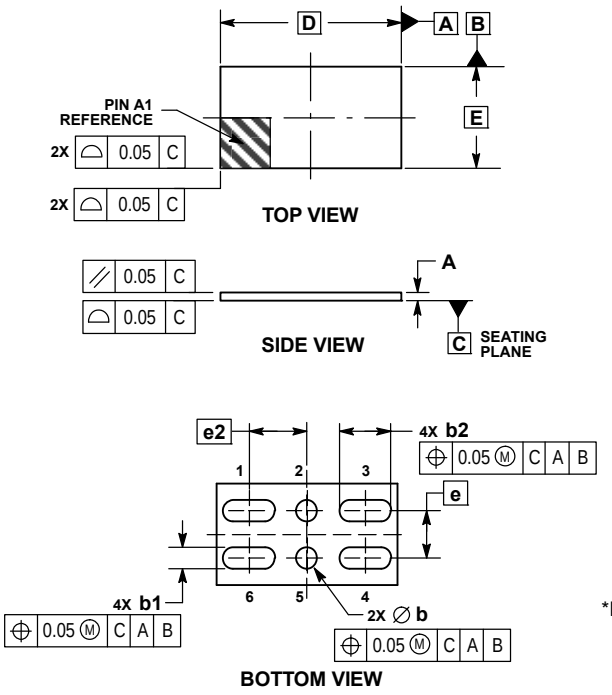

PT – Ta
Surface mounted on ceramic substrate
(5000mm2×0.8mm)
Total Dissipation, PT – W
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
0
25
50
75
100
125
150
175
200
Ambient Temperature, Ta – °C


RθJA – Pulse Time
Duty Cycle=0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Surface mounted on ceramic substrate
(5000mm2×0.8mm)
Thermal Resistance, RθJA – °C/W
100
7
5
3
2
10
7
5
3
2
1.0
7
5
3
2
0.1
0.00001
2
3
5
7
0.0001
2
3
5
7
0.001
2
3
5
7
0.01
2
3
5
7
0.1
2
3
5
7
1.0
2
3
5
7
10
Pulse Time, PT – s

PACKAGE DIMENSIONS

unit : mm

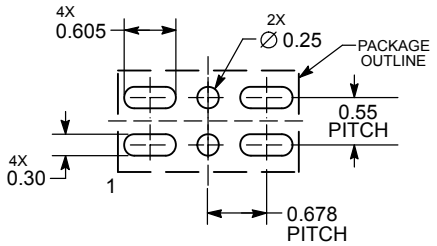
WLCSP6, 2.11x1.18x0.10
CASE 567NP
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.08	0.10	0.12
b	0.22	0.25	0.28
b1	0.27	0.30	0.33
b2	0.575	0.605	0.635
D	2.11 BSC		
E	1.18 BSC		
e	0.55 BSC		
e2	0.6775 BSC		

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

1 : Source1
2 : Gate1
3 : Source1
4 : Source2
5 : Gate2
6 : Source2

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)
EFC2J004NUZTDG	NA	WLCSP6, 2.11x1.18x0.10 (Pb-Free / Halogen Free)	5,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Note on usage : Since the EFC2J004NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.