DS90UB954-Q1 Dual FPD-Link III Deserializer with MIPI CSI-2 outputs for 2MP/60fps Cameras and RADAR

1 Features

- AEC-Q100 Qualified for Automotive Applications:
  - Device Temperature Grade 2: –40℃ to +105℃ Ambient Operating Temperature Range
  - Device HBM ESD Classification Level ±4 kV
  - Device CDM ESD Classification Level C6
- Connects One or Two Active Cameras Over FPD-Link III Interface
- Supports up to 2-Megapixel Sensors With Full HD (1080p) Resolution at 60-Hz Frame Rate
- Multi-Camera Synchronization
- MIPI DPHY Version 1.2 / CSI-2 Version 1.3 Compliant
  - CSI-2 Output Ports
  - Supports 1, 2, 3, 4 Data Lanes
  - CSI-2 Data Rate Scalable for 400 Mbps / 800 Mbps / 1.5 Gbps / 1.6 Gbps each Data Lane
  - Programmable Data Types
  - Four Virtual Channels
  - ECC and CRC Generation
- Ultra-low Data and Control Path Latency
- Supports Single-Ended Coaxial or Shielded Twisted-Pair (STP) Cable
- Adaptive Receive Equalization
- I2C With Fast-Mode Plus up to 1 Mbps
- Flexible GPIOs for Camera Synchronization and Diagnostics
- Compatible with DS90UB953-Q1, DS90UB933-Q1 and DS90UB913A-Q1 Serializers
- CRC Data Protection for Internal and External Data Paths
- ISO 10605 and IEC 61000-4-2 ESD Compliant

2 Applications

- Automotive ADAS
  - Rear View Cameras (RVC)
  - Surround View Systems (SVS)
  - Camera Monitor Systems (CMS)
  - Forward Vision Cameras (FC)
  - Driver Monitoring Systems (DMS)
  - Satellite RADAR Modules
- Security and Surveillance

3 Description

The DS90UB954-Q1 is a versatile deserializer capable of receiving serialized camera data from 1 or 2 independent video datastreams via an FPD-Link III interface. When paired with a DS90UB953-Q1 serializer, the DS90UB954-Q1 receives data from imagers supporting 2MP/60fps and 4MP/30fps cameras as well as satellite RADAR. Data is received and aggregated into a MIPI CSI-2 compliant output for interconnect to a downstream processor. For cameras with DS90UB933-Q1/DS90UB913A-Q1 serializers, the DS90UB954-Q1 receives and aggregates data from imagers supporting 1MP/60fps and 2MP/30fps as well. When configuring the CSI-2 interface for 2-Lane operation a second MIPI CSI-2 output port is available to provide a second replicated output. Replication mode creates 2 copies of the aggregated video stream for datalogging and parallel processing.

The DS90UB953/954-Q1 chipset is fully AEC-Q100 qualified and designed to receive data across either 50-Ω single-ended coaxial or 100-Ω differential STP cables. The receive equalizer automatically adapts to compensate for cable loss characteristics, including degradation over time with no additional programming required.

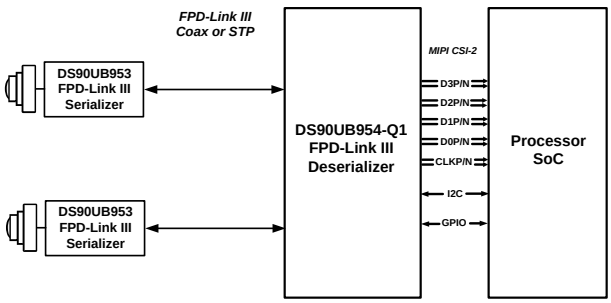
Each of the FPD-Link III interfaces also includes a separate low latency bi-directional control channel that continuously conveys I2C, GPIO, and other control information. General purpose I/O signals such as those required for camera synchronization and diagnostic features also make use of this bi-directional control channel.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UB954-Q1	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



PRODUCT PREVIEW

4 Device and Documentation Support

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

4.3 Trademarks

E2E is a trademark of Texas Instruments.

4.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB954TRGZRQ1	PREVIEW	VQFN	RGZ	48	2500	TBD	Call TI	Call TI	-40 to 105		
DS90UB954TRGZTQ1	PREVIEW	VQFN	RGZ	48	250	TBD	Call TI	Call TI	-40 to 105		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

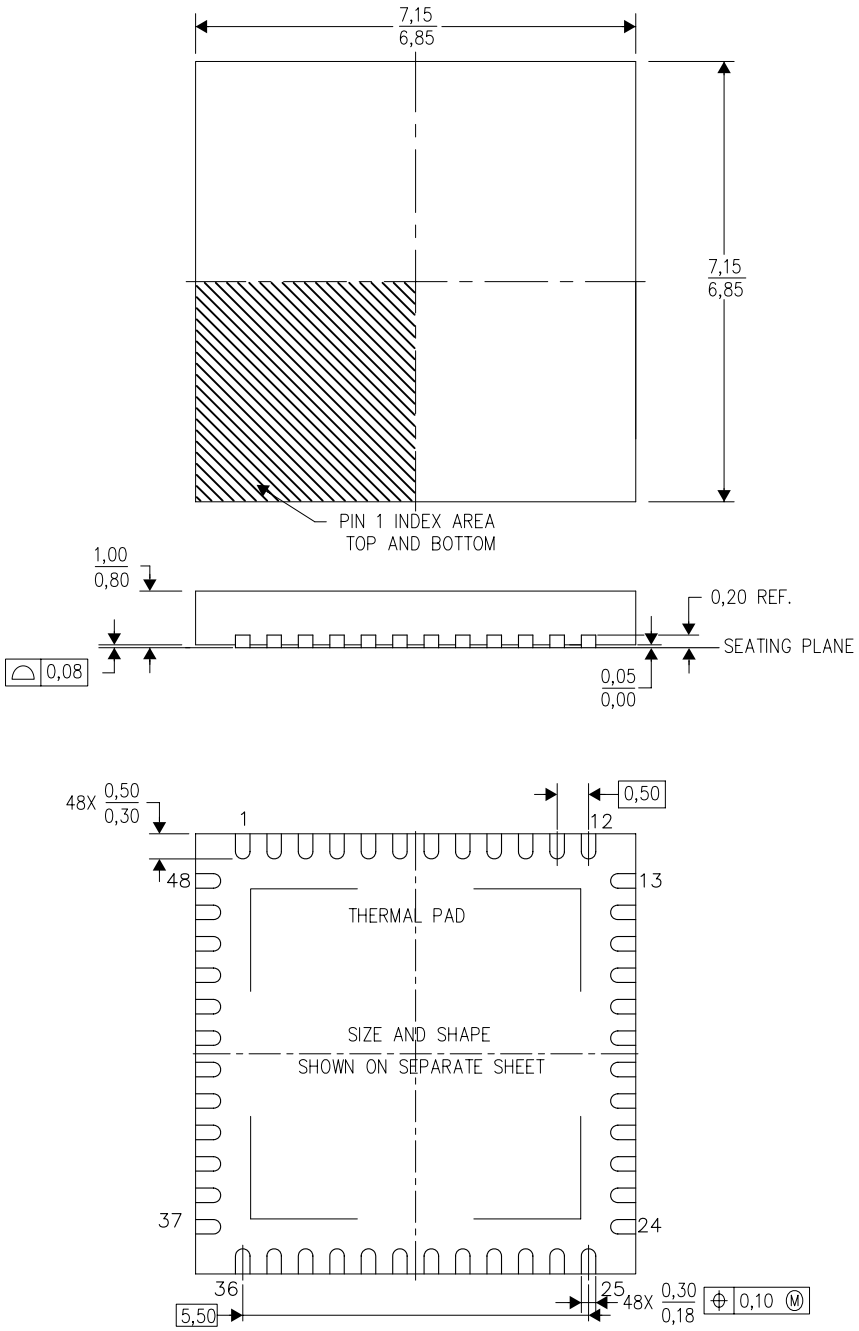
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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