TEXAS INSTRUMENTS

5 - 85 MHz 24-bit Color FPD-Link III Deserializer with Bidirectional Control Channel

General Description

The DS90UB926Q deserializer, in conjunction with the DS90UB925Q serializer, provides a complete digital interface for concurrent transmission of high-speed video, audio, and control data for automotive display and image sensing applications.

This chipset translates a parallel RGB Video Interface into a single pair high-speed serialized interface. The serial bus scheme, FPD-Link III, supports full duplex of high speed forward data transmission and low speed backchannel communication over a single differential link. Consolidation of video data and control over a single differential pair reduces the interconnect size and weight, while also eliminating skew issues and simplifying system design.

The DS90UB926Q deserializer recovers the RGB data, three video control signals and four synchronized I2S audio signals. It extracts the clock from a high speed serial stream. An output LOCK pin provides the link status if the incoming data stream is locked, without the use of a training sequence or special SYNC patterns, as well as a reference clock.

The DS90UB926Q deserializer has a 31-bit parallel LVCMOS output interface to accommodate the RGB, video control, and audio data.

An adaptive equalizer optimizes the maximum cable reach. EMI is minimized by output SSC generation (SSCG) and enhanced progressive turn-on (EPTO) features.

Features

- Bidirectional control interface channel interface with I2C compatible serial control bus
- Supports high definition (720p) digital video format
- RGB888 + VS, HS, DE and synchronized I2S audio supported
- 5 to 85 MHz PCLK supported
- Single 3.3V Operation with 1.8V or 3.3V compatible LVCMOS I/O interface
- AC-coupled STP Interconnect up to 10 meters
- Parallel LVCMOS video outputs
- I2C compatible serial control bus for configuration
- DC-balanced & scrambled Data w/ Embedded Clock
- Adaptive cable equalization
- Supports repeater application
- @ SPEED Link BIST Mode and LOCK status pin
- Image Enhancement (White Balance and Dithering) and Internal pattern generation
- EMI Minimization (SSCG and EPTO)
- Low power modes minimize power dissipation
- Automotive grade product: AEC-Q100 Grade 2 qualified
- >8kV HBM and ISO 10605 ESD rating
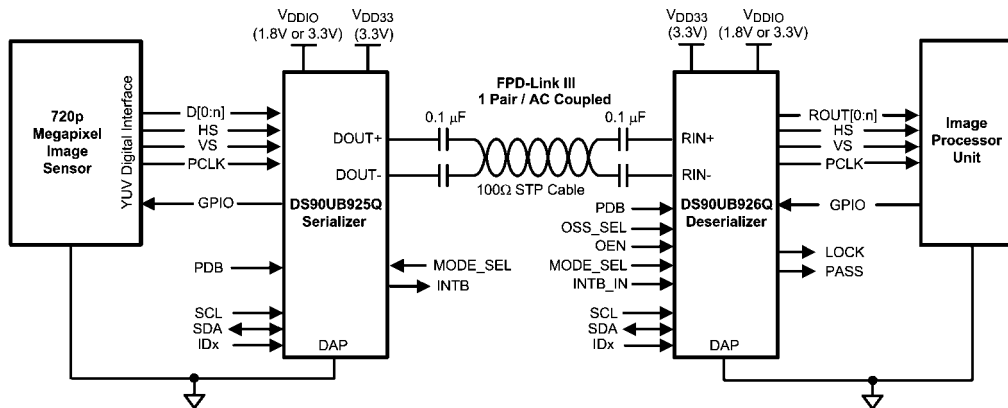- Backward compatible to FPD-Link II

Applications

- Automotive Display for Navigation
- Rear Seat Entertainment Systems
- Automotive Drive Assistance
- Automotive Megapixel Camera Systems

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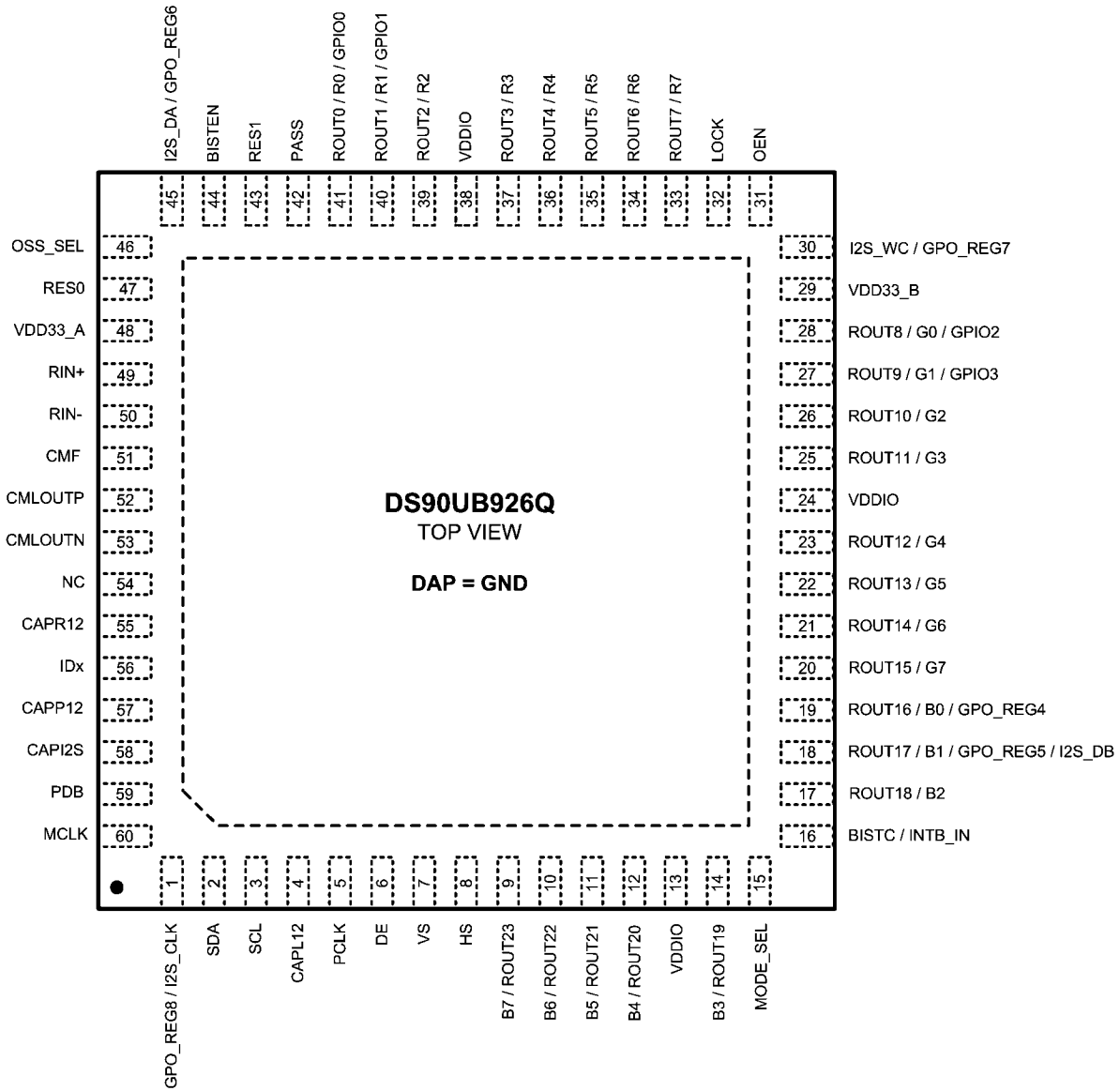
Typical Displays Applications Diagram
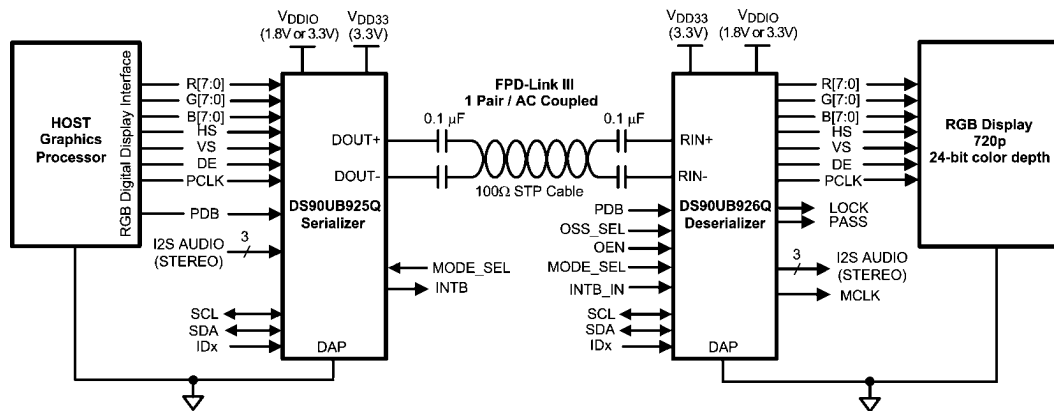
Typical Display Applications Diagram

DS90UB926Q Pin Diagram


DS90UB926Q — Top View

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Pin Descriptions

Pin Name	Pin #	I/O, Type	Description
LVCMOS Parallel Interface			
ROUT[23:0] / R[7:0], G [7:0], B[7:0]	41, 40, 39, 37, 36, 35, 34, 33, 28, 27, 26, 25, 23, 22, 21, 20, 19, 18, 17, 14, 12, 11, 10, 9	O, LVCMOS w/ pull down	Parallel Interface Data Output Pins. Leave open if unused. ROUT0 / R0 can optionally be used as GPIO0 and ROUT1 / R1 can optionally be used as GPIO1. ROUT8 / G0 can optionally be used as GPIO2 and ROUT9 / G1 can optionally be used as GPIO3. ROUT16 / B0 can optionally be used as GPO_REG4 and ROUT17/ B1 can optionally be used as I2S_DB / GPO_REG5.
HS	8	O, LVCMOS w/ pull down	Horizontal Sync Output Pin Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled. There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled. The signal is limited to 2 transitions per 130 PCLKs. See *Table 9*
VS	7	O, LVCMOS w/ pull down	Vertical Sync Output Pin Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
DE	6	O, LVCMOS w/ pull down	Data Enable Output Pin Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled. There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled. The signal is limited to 2 transitions per 130 PCLKs. See *Table 9*
PCLK	5	O, LVCMOS w/ pull down	Pixel Clock Output Pin. Strobe edge set by RFB configuration register. See *Table 9*
I2S_CLK, I2S_WC, I2S_DA	1, 30, 45	O, LVCMOS w/ pull down	Digital Audio Interface Data Output Pins Leave open if unused I2S_CLK can optionally be used as GPO_REG8, I2S_WC can optionally be used as GPO_REG7, and I2S_DA can optionally be used as GPO_REG6.
MCLK	60	O, LVCMOS w/ pull down	I2S Master Clock Output. x1, x2, or x4 of I2S_CLK Frequency.
Optional Parallel Interface			
I2S_DB	18	O, LVCMOS w/ pull down	Second Channel Digital Audio Interface Data Output pin at 18–bit color mode and set by MODE_SEL or configuration register Leave open if unused I2S_B can optionally be used as BI or GPO_REG5.
GPIO[3:0]	27, 28, 40, 41	I/O, LVCMOS w/ pull down	Standard General Purpose IOs. Available only in 18-bit color mode, and set by MODE_SEL or configuration register. See *Table 9* Leave open if unused Shared with G1, G0, R1 and R0.
GPO_REG [8:4]	1, 30, 45, 18, 19	O, LVCMOS w/ pull down	General Purpose Outputs and set by configuration register. See *Table 9* Shared with I2S_CLK, I2S_WC, I2S_DA, I2S_DB or B1, B0.
INTB_IN	16	Input, LVCMOS w/ pull-down	Interrupt Input Shared with BISTC

Pin Name	Pin #	I/O, Type	Description
Optional Parallel Interface			
PDB	59	I, LVCMOS w/ pull-down	Power-down Mode Input Pin PDB = H, device is enabled (normal operation) Refer to "Power Up Requirements and PDB Pin" in the Applications Information Section. PDB = L, device is powered down. When the device is in the POWER DOWN state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. .
OEN	31	Input, LVCMOS w/ pull-down	Output Enable Pin. See *Table 3*
OSS_SEL	46	Input, LVCMOS w/ pull-down	Output Sleep State Select Pin. See *Table 3*
MODE_SEL	15	I, Analog	Device Configuration Select. See *Table 4*
IDx	56	I, Analog	I2C Serial Control Bus Device ID Address Select External pull-up to V_{DD33} is required under all conditions, DO NOT FLOAT. Connect to external pull-up and pull-down resistor to create a voltage divider. See *Figure 19*
SCL	3	I/O, LVCMOS Open Drain	I2C Clock Input / Output Interface Must have an external pull-up to V_{DD33}, DO NOT FLOAT. Recommended pull-up: 4.7kΩ.
SDA	2	I/O, LVCMOS Open Drain	I2C Data Input / Output Interface Must have an external pull-up to V_{DD33}, DO NOT FLOAT. Recommended pull-up: 4.7kΩ.
BISTEN	44	I, LVCMOS w/ pull-down	BIST Enable Pin. 0: BIST Mode is disabled. 1: BIST Mode is enabled.
BISTC	16	I, LVCMOS w/ pull-down	BIST Clock Select. Shared with INTB_IN 0: PCLK; 1: 33 MHz
Status			
LOCK	32	O, LVCMOS w/ pull down	LOCK Status Output Pin 0: PLL is unlocked, ROUT[23:0]/RGB[7:0], I2S[2:0], HS, VS, DE and PCLK output states are controlled by OEN. May be used as Link Status or Display Enable 1: PLL is Locked, outputs are active
PASS	42	O, LVCMOS w/ pull down	PASS Output Pin 0: One or more errors were detected in the received payload 1: ERROR FREE Transmission Leave Open if unused. Route to test point (pad) recommended
FPD-Link III Serial Interface			
RIN+	49	I, LVDS	True Input. The interconnection should be AC Coupled to this pin with a 0.1 µF capacitor.
RIN-	50	I, LVDS	Inverting Input. The interconnection should be AC Coupled to this pin with a 0.1 µF capacitor.
CMLOUTP	52	O, LVDS	True CML Output Monitor point for equalized differential signal
CMLOUTN	53	O, LVDS	Inverting CML Output Monitor point for equalized differential signal
CMF	51	Analog	Common Mode Filter. Connect 0.1 µF capacitor to GND

Pin Name	Pin #	I/O, Type	Description
Power and Ground			
VDD33_A, VDD33_B	48, 29	Power	Power to on-chip regulator **3.0 V – 3.6 V**. Requires 4.7 uF to GND at each VDD pin.
V$_{DDIO}$	13, 24, 38	Power	LVCMOS I/O Power **1.8 V ±5% OR 3.0 V – 3.6 V**. Requires 4.7 uF to GND at each VDDIO pin.
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the LLP package. **Connect to the ground plane** (GND) with at least 9 vias.
Regulator Capacitor			
CAPR12, CAPP12, CAPI2S	55, 57, 58	CAP	Decoupling capacitor connection for on-chip regulator. Requires a 4.7uF to GND at each CAP pin.
CAPL12	4	CAP	Decoupling capacitor connection for on-chip regulator. Requires two 4.7uF to GND at this CAP pin.
Others			
NC	54	NC	No connect. This pin may be left open or tied to any level.
RES[1:0]	43.47	GND	Reserved. Tie to Ground.

The VDD (V$_{DD33}$ and V$_{DDIO}$) supply ramp should be faster than 1.5 ms with a monotonic rise.

Block Diagram

DS90UB926Q Deserializer
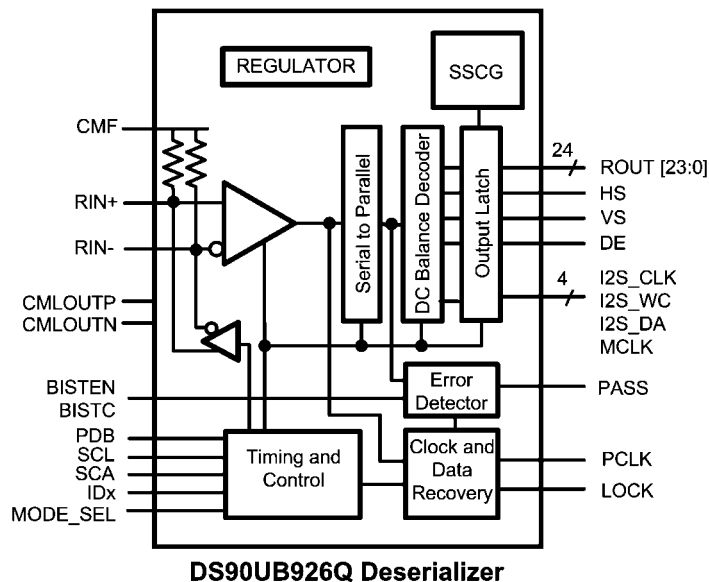
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Ordering Information

PART NUMBER	PACKAGE DESCRIPTION	QUANTITY	SPEC	PACKAGE ID
DS90UB926QSQE	60-pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	250	NOPB	SQA60B
DS90UB926QSQ	60-pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	1000	NOPB	SQA60B
DS90UB926QSQX	60-pin LLP, 9.0 X 9.0 X 0.8 mm, 0.5 mm pitch	2500	NOPB	SQA60B
Note: Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard. Automotive Grade products are identified with the letter Q. For more information go to http://www.ti.com/automotive.				

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Supply Voltage – V_{DD33}	−0.3V to +4.0V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS I/O Voltage	−0.3V to (V_{DDIO} + 0.3V)
Deserializer Input Voltage	−0.3V to +2.75V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
60 LLP Package Maximum Power Dissipation Capacity at 25°C	
Derate above 25°C	1/ θ_{JA}°C/W
θ_{JA}	31 °C/W
θ_{JC}	2.4 °C/W
ESD Rating (IEC, powered-up only), R_D = 330Ω, C_S = 150pF	
Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
Contact Discharge (R_{IN+}, R_{IN-})	≥±8 kV
ESD Rating (ISO10605), R_D = 330Ω, C_S = 150pF	
Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
Contact Discharge(R_{IN+}, R_{IN-})	≥±8 kV
ESD Rating (ISO10605), R_D = 2kΩ, C_S = 150 & 330pF	
Air Discharge (R_{IN+}, R_{IN-})	≥±15 kV
Contact Discharge (R_{IN+}, R_{IN-})	≥±8 kV
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1.25 kV
ESD Rating (MM)	≥±250 V

For soldering specifications:
    see product folder at www.ti.com and
    www.ti.com/lit/an/snoa549c/snoa549c.pdf	

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DD33})	3.0	3.3	3.6	V
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
PCLK Frequency	5		85	MHz
Supply Noise (*Note 7*)			100	mV_{P-P}

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
LVCMOS I/O DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		PDB	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO} = 3.0 to 3.6V			−10	±1	+10	µA
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		OEN, OSS_SEL, BISTEN, BISTC / INTB_IN, GPIO[3:0]	2.0		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89V			0.65* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89V			GND		0.35* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6V		−10	±1	+10	µA
			V_{DDIO} = 1.7 to 1.89V		−10	±1	+10	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4mA	V_{DDIO} = 3.0 to 3.6V	ROUT[23:0], HS, VS, DE, PCLK, LOCK, PASS, MCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB, GPO_REG [8:4]	2.4		V_{DDIO}	V
			V_{DDIO} = 1.7 to 1.89V		V_{DDIO}- 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +4mA	V_{DDIO} = 3.0 to 3.6V		GND		0.4	V
			V_{DDIO} = 1.7 to 1.89V		GND		0.35	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−60		mA
I_{OZ}	TRI-STATE® Output Current	V_{OUT} = 0V or V_{DDIO}, PDB = L			−10		+10	µA

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
FPD-LINK III CML RECEIVER INPUT DC SPECIFICATIONS								
V_{TH}	Differential Threshold High Voltage	V_{CM} = 2.5V (Internal V_{BIAS})		RIN+, RIN-			+50	mV
V_{TL}	Differential Threshold Low Voltage				−50			mV
V_{CM}	Differential Common-mode Voltage					1.8		V
R_T	Internal Termination Resistor - Differential				80	100	120	Ω
CML MONITOR DRIVER OUTPUT DC SPECIFICATIONS								
V_{ODp-p}	Differential Output Voltage	R_L = 100Ω		CMLOUTP, CMLOUTN	360			mVp-p
SUPPLY CURRENT								
I_{DD1}	Supply Current (includes load current) f = 85MHz	C_L = 12pF, Checker Board Pattern *Figure 1*	V_{DD33}= 3.6V	V_{DD33}		125	145	mA
I_{DDIO1}			V_{DDIO}= 3.6V	V_{DDIO}		110	118	mA
			V_{DDIO} = 1.89V			60	75	mA
I_{DD2}	Supply Current (includes load current) f = 85MHz	C_L = 4pF Checker Board Pattern, *Figure 1*	V_{DD33} = 3.6V	V_{DD33}		125	145	mA
I_{DDIO2}			V_{DDIO} = 3.6V	V_{DDIO}		75	85	mA
			V_{DDIO} = 1.89V			50	65	mA
I_{DDS}	Supply Current Sleep Mode	Without Input Serial Stream	V_{DD33} = 3.6V	V_{DD33}		90	115	mA
I_{DDIOS}			V_{DDIO} = 3.6V	V_{DDIO}		3	5	mA
			V_{DDIO} = 1.89V			2	3	mA
I_{DDZ}	Supply Current Power Down	PDB = L, All LVCMOS inputs are floating or tied to GND	V_{DD33} = 3.6V	V_{DD33}		2	10	mA
I_{DDIOZ}			V_{DDIO} = 3.6V	V_{DDIO}		0.05	10	mA
			V_{DDIO} = 1.89V			0.05	10	mA

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
GPIO BIT RATE							
B_R	Forward Channel Bit Rate	(*Note 8*, *Note 9*)	f = 5 – 85MHz, GPIO[3:0]		0.25*f		Mbps
	Back Channel Bit Rate			>50	>75		kbps
CML MONITOR DRIVER OUTPUT AC SPECIFICATIONS							
E_W	Differential Output Eye Opening Width (*Note 6*)	R_L = 100Ω, Jitter Freq >f / 40 *Figure 2* (*Note 8*, *Note 9*)	CMLOUTP, CMLOUTN, f = 85MHz	0.3	0.4		UI
E_H	Differential Output Eye Height			200	300		mV
SWITCHING CHARACTERISTICS							
t_{RCP}	PCLK Output Period	t_{RCP} = t_{TCP}	PCLK	11.76	T	200	ns
t_{RDC}	PCLK Output Duty Cycle			45	50	55	%
t_{CLH}	LVCMOS Low-to-High Transition Time *Figure 3*	V_{DDIO} = 1.71 - 1.89V, C_L = 12pF	ROUT[23:0], HS, VS, DE, PCLK, LOCK, PASS, MCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB		2	3	ns
		V_{DDIO} = 3.0 – 3.6V, C_L = 12pF			2	3	ns
t_{CHL}	LVCMOS High-to-Low Transition Time *Figure 3*	V_{DDIO} = 1.71 - 1.89V, C_L = 12pF			2	3	ns
		V_{DDIO} = 3.0 – 3.6V, C_L = 12pF			2	3	ns
t_{ROS}	Data Valid before PCLK – Setup Time SSCG = OFF *Figure 6*	V_{DDIO} = 1.71 - 1.89V, C_L = 12pF		2.2			ns
		V_{DDIO} = 3.0 – 3.6V, C_L = 12pF		2.2			ns
t_{ROH}	Data Valid after PCLK – Hold Time SSCG = OFF *Figure 6*	V_{DDIO} = 1.71 - 1.89V, C_L = 12pF		3.0			ns
		V_{DDIO} = 3.0 – 3.6V, C_L = 12pF		3.0			ns
t_{XZR}	Active to OFF Delay *Figure 5* (*Note 8*, *Note 9*)	OEN = L, OSS_SEL = H	ROUT[23:0]		10		ns
			HS, VS, DE, PCLK, LOCK, PASS		15		ns
			MCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB		60		ns
t_{DDLT}	Lock Time *Figure 5* (*Note 8*, *Note 9*)	SSCG = OFF	f = 5 – 85MHz		5	40	ms
t_{DD}	Delay – Latency (*Note 8*, *Note 9*)		f = 5 – 85MHz		147*T		ns
t_{DCCJ}	Cycle-to-Cycle Jitter (*Note 8*, *Note 9*)	SSCG = OFF	f = 5 – <15 MHz		0.5		ns
			f = 15 – 85 MHz		0.2		ns
			I2S_CLK = 1 - 12.28MHz		+/-2		ns

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{ONS}	Data Valid After OEN = H SetupTime *Figure 7* (*Note 8*, *Note 9*)	VDDIO = 1.71 - 1.89V, CL = 12pF	ROUT[23:0], HS, VS, DE, PCLK, MCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB		50		ns
		VDDIO = 3.0 – 3.6V, CL = 12pF			50		ns
t_{ONH}	Data Tri-State After OEN = L SetupTime *Figure 7* (*Note 8*, *Note 9*)	VDDIO = 1.71 - 1.89V, CL = 12pF			50		ns
		VDDIO = 3.0 – 3.6V, CL = 12pF			50		ns
t_{SES}	Data Tri-State after OSS_ SEL = H, Setup Time *Figure 7* (*Note 8*, *Note 9*)	VDDIO = 1.71 - 1.89V, CL = 12pF			5		ns
		VDDIO = 3.0 – 3.6V, CL = 12pF			5		ns
t_{SEH}	Data to Low after OSS_SEL = L Setup Time *Figure 7* (*Note 8*, *Note 9*)	VDDIO = 1.71 - 1.89V, CL = 12pF			5		ns
		VDDIO = 3.0 – 3.6V, CL = 12pF			5		ns
BIST Mode							
t_{PASS}	BIST PASS Valid Time BISTEN = H *Figure 8* (*Note 8*, *Note 9*)		PASS		800		ns
SSCG Mode							
f_{DEV}	Spread Spectrum Clocking Deviation Frequency	*Figure 12* Tables 1, 2 (*Note 8*, *Note 9*)	f = 85MHz, SSCG = ON	±0.5		±2.5	%
f_{MOD}	Spread Spectrum Clocking Modulation Frequency			8		100	kHz

Recommended Timing for the Serial Control Bus

Over 3.3V supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_{HIGH}	SCL High Period	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{HD;STA}$	Hold time for a start or a repeated start condition *Figure 9*	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{SU:STA}$	Set Up time for a start or a repeated start condition *Figure 9*	Standard Mode	4.7			us
		Fast Mode	0.6			us
$t_{HD;DAT}$	Data Hold Time *Figure 9*	Standard Mode	0		3.45	us
		Fast Mode	0		0.9	us
$t_{SU;DAT}$	Data Set Up Time *Figure 9*	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition, *Figure 9*	Standard Mode	4.0			us
		Fast Mode	0.6			us
t_{BUF}	Bus Free Time between STOP and START, *Figure 9*	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_r	SCL & SDA Rise Time, *Figure 9*	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, *Figure 9*	Standard Mode			300	ns
		Fast mode			300	ns

DC and AC Serial Control Bus Characteristics

Over 3.3V supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	$0.7* V_{DD33}$		V_{DD33}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		$0.3* V_{DD33}$	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA, IOL = 1.25mA	0		0.36	V
I_{in}		SDA or SCL, Vin = V_{DD33} or GND	-10		+10	µA
t_R	SDA RiseTime – READ	SDA, RPU = 10kΩ, Cb ≤ 400pF, *Figure 9*		430		ns
t_F	SDA Fall Time – READ			20		ns
$t_{SU;DAT}$	Set Up Time — READ	*Figure 9*		560		ns
$t_{HD;DAT}$	Hold Up Time — READ	*Figure 9*		615		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Typical values represent most likely parametric norms at V_{DD} = 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 4: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD and ΔVOD, which are differential voltages.

Note 5: t_{DDLT} is the time required by the device to obtain lock when exiting power-down state with an active serial stream.

Note 6: UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / 35*PCLK). The UI scales with PCLK frequency.

Note 7: Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DD33} and V_{DDIO} supplies with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 50MHz. The Des on the other hand shows no error when the noise frequency is less than 50 MHz.

Note 8: Specification is guaranteed by characterization and is not tested in production.

Note 9: Specification is guaranteed by design and is not tested in production.
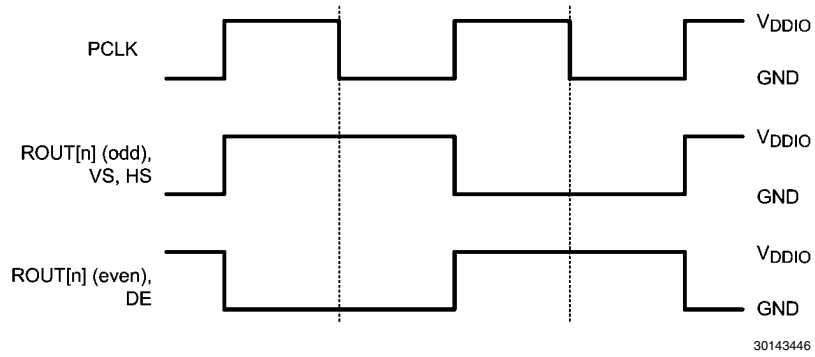
AC Timing Diagrams and Test Circuits
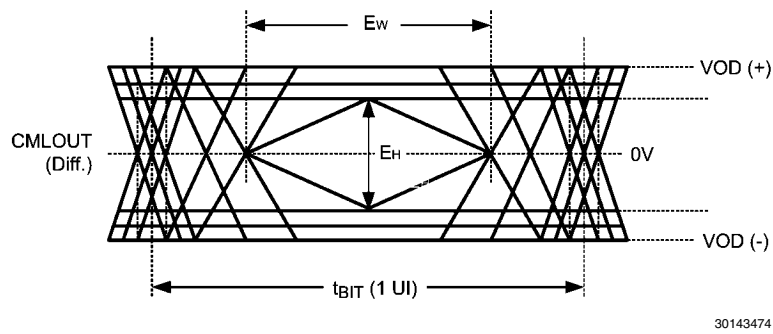

FIGURE 1. Checker Board Data Pattern
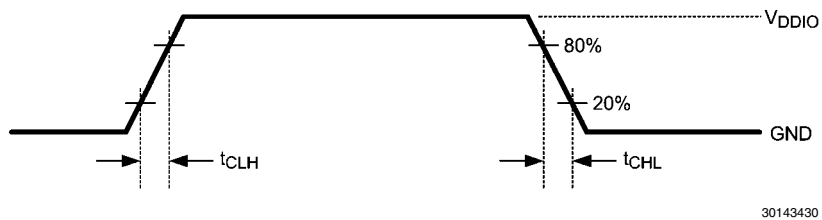

FIGURE 2. CML Output Driver

FIGURE 3. LVCMOS Transition Times

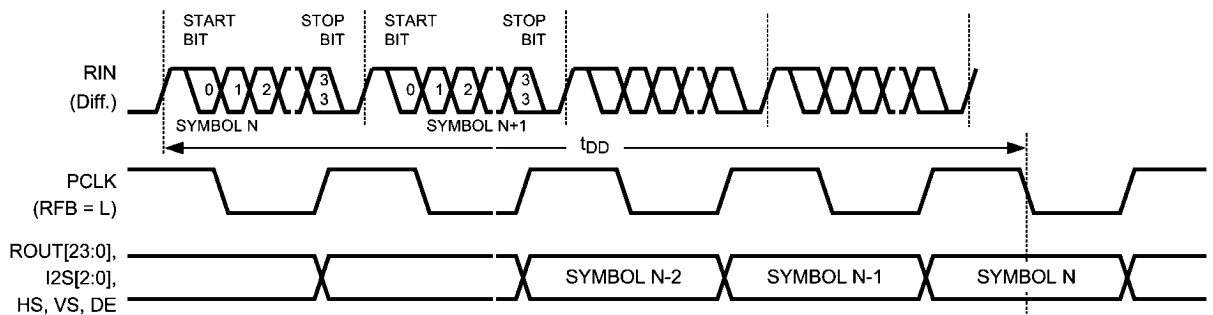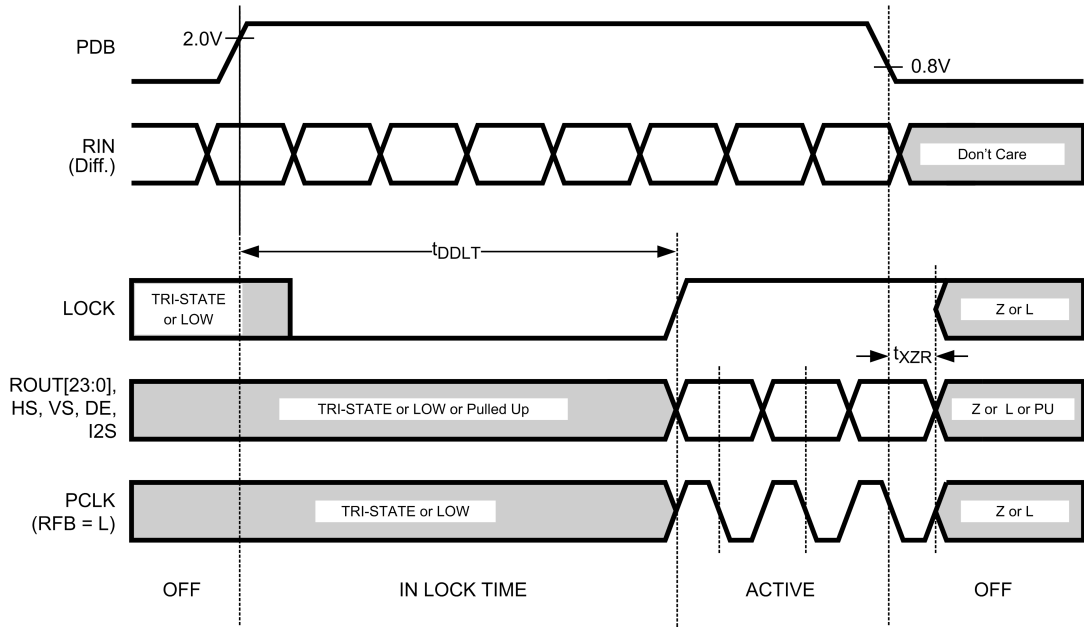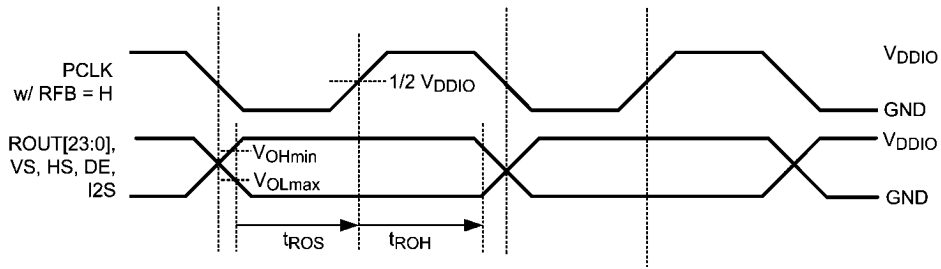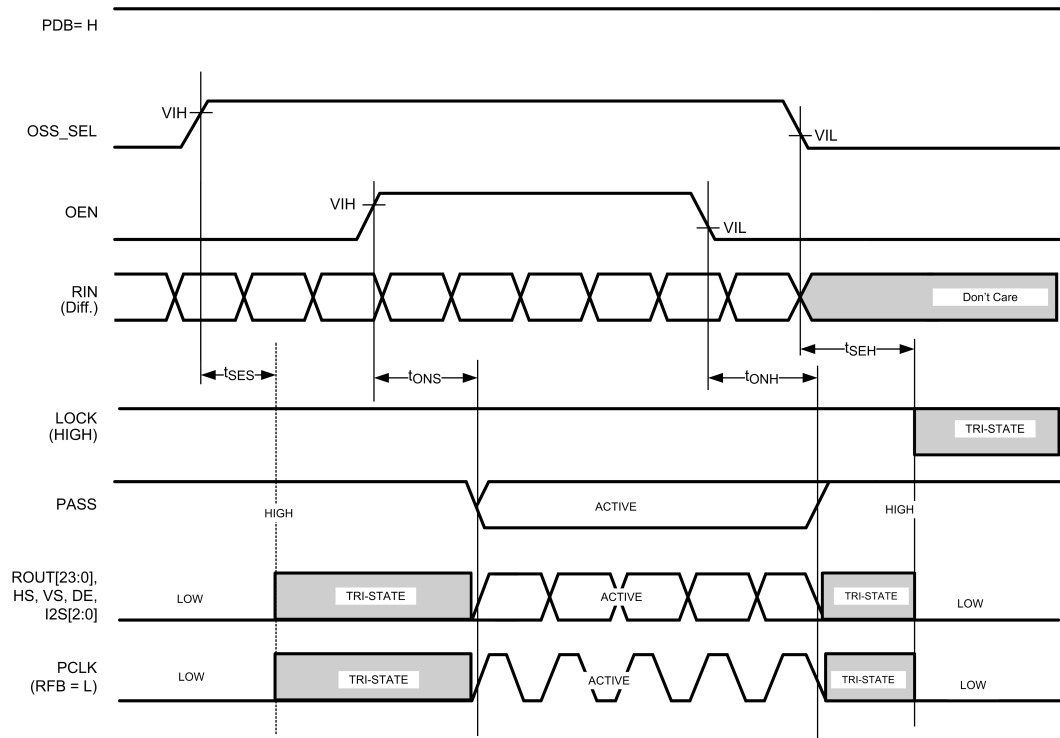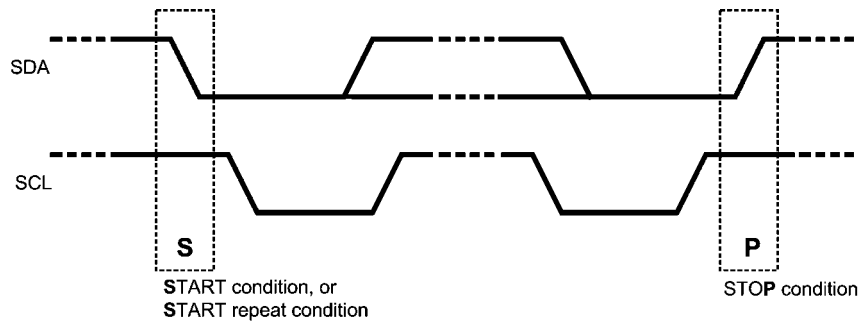**FIGURE 4. Delay - Latency**

FIGURE 5. PLL Lock Times and PDB TRI-STATE Delay

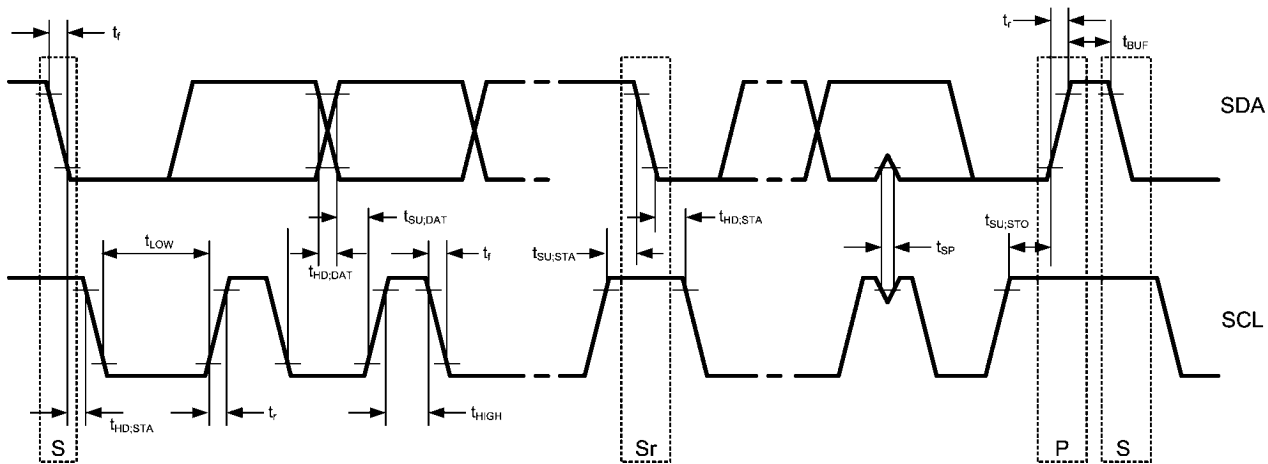**FIGURE 6. Output Data Valid (Setup and Hold) Times with SSCG = Off**

FIGURE 7. Output State (Setup and Hold) Times

FIGURE 8. BIST PASS Waveform

FIGURE 9. Serial Control Bus Timing Diagram

Functional Description

The DS90UB926Q deserializer receives a 35-bits symbol over a single serial FPD-Link III pair operating upto 2.975 Gbps application payload. The serial stream contains an embedded clock, video control signals and the DC-balanced video data and audio data which enhance signal quality to support AC coupling.

The DS90UB926Q deserializer attains lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic "plug and lock" performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating then deserializing the incoming data stream. The recovered parallel LVCMOS video bus is then provided to the display. The deserializer is intended for use with the DS90UB925Q serializer, but is also backward compatible with DS90UR905Q or DS90UR907Q FPD-Link II serializer.

HIGH SPEED FORWARD CHANNEL DATA TRANSFER

The High Speed Forward Channel (HS_FC) is composed of 35 bits of data containing DIN[23:0] or RGB[7:0] or YUV data, sync signals, I2C, and I2S audio transmitted from Serializer to Deserializer. *Figure 10* illustrates the serial stream per PCLK cycle. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.
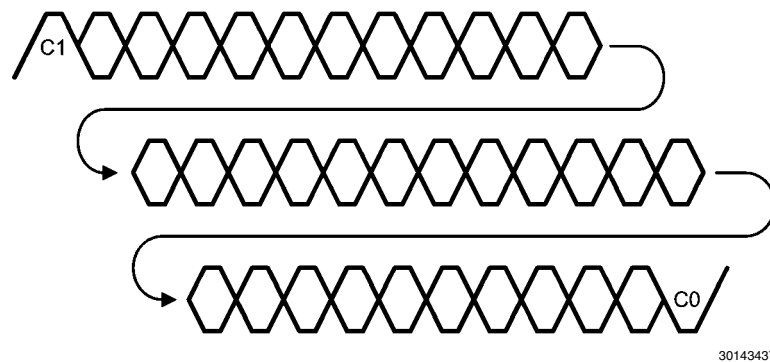

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FIGURE 10. FPD-Link III Serial Stream

The device supports clocks in the range of 5 MHz to 85 MHz. The application payload rate is 2.975 Gbps maximum (175 Mbps minimum) with the actual line rate of 2.975 Gbps maximum and 525 Mbps Minimum.

LOW SPEED BACK CHANNEL DATA TRANSFER

The Low-Speed Backward Channel (LS_BC) of the DS90UB926Q provides bidirectional communication between the display and host processor. The information is carried back from the Deserializer to the Serializer per serial symbol. The back channel control data is transferred over the single serial link along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high speed forward channel. The back channel contains the I2C, CRC and 4 bits of standard GPIO information with 10 Mbps line rate.

BACKWARD COMPATIBLE MODE

The DS90UB926Q is also backward compatible to DS90UR905Q and DS90UR907Q FPD Link II serializers at 15 - 65 MHz pixel clock frequencies. It receives 28-bits of data over a single serial FPD-Link II pair operating at the line rate of 420 Mbps to 1.82 Gbps. This backward compatible mode is provided through the MODE_SEL pin (*Table 4*) or the configuration register (*Table 9*).

Note: In this mode, the minimum PCLK frequency is 15 MHz.

INPUT EQUALIZATION GAIN

FPD-Link III input adaptive equalizer provides compensation for transmission medium losses and reduces the medium-induced deterministic jitter. It equalizes up to 10m STP cables with 3 connection breaks at maximum serialized stream payload rate of 2.975 Gbps.

COMMON MODE FILTER PIN (CMF)

The deserializer provides access to the center tap of the internal termination. A capacitor must be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 0.1 µF capacitor has to be connected to this pin to Ground.

VIDEO CONTROL SIGNAL FILTER

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled: DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled: DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See *Figure 11*.
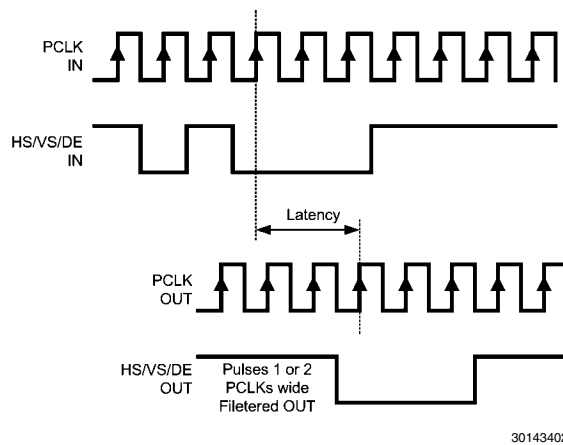

FIGURE 11. Video Control Signal Filter Waveform

EMI REDUCTION FEATURES

Spread Spectrum Clock Generation (SSCG)

The DS90UB926Q provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2.5% (5% total) at up to 100 kHz modulations are available. This feature may be controlled by register. See *Table 1*, *Table 2*, and *Table 9*.
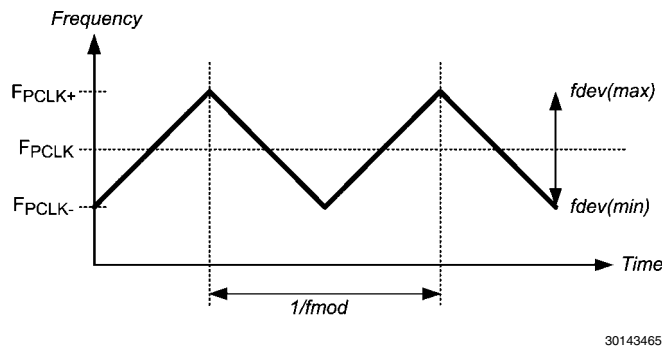

FIGURE 12. SSCG Waveform

TABLE 1. SSCG Configuration
LFMODE = L (15 - 85 MHz)

SSCG Configuration (0x2C) LFMODE = L (15 - 85MHz)			Spread Spectrum Output	
SSC[2]	SSC[1]	SSC[0]	Fdev (%)	Fmod (kHz)
L	L	L	±0.9	PCLK / 2168
L	L	H	±1.2	
L	H	L	±1.9	
L	H	H	±2.5	
H	L	L	±0.7	PCLK / 1300
H	L	H	±1.3	
H	H	L	±2.0	
H	H	H	±2.5	

TABLE 2. SSCG Configuration
LFMODE = H (5 - <15 MHz)

SSCG Configuration (0x2C) LFMODE = H (5 - <15 MHz)			Spread Spectrum Output	
SSC[2]	SSC[1]	SSC[0]	Fdev (%)	Fmod (kHz)
L	L	L	±0.5	PCLK / 628
L	L	H	±1.3	
L	H	L	±1.8	
L	H	H	±2.5	
H	L	L	±0.7	PCLK / 388
H	L	H	±1.2	
H	H	L	±2.0	
H	H	H	±2.5	

Enhanced Progressive Turn-On (EPTO)

The deserializer LVCMOS parallel outputs timing are delayed. Groups of 8-bit R, G and B outputs switch in a different time. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

LVCMOS VDDIO Option

The deserializer parallel bus can operate with 1.8 V or 3.3 V levels (VDDIO) for target (Display) compatibility. The 1.8 V levels will offer a lower noise (EMI) and also a system power savings.

POWER DOWN (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the V_{DDIO}, where V_{DDIO} = 3.0V to 3.6V or V_{DD33}. To save power disable the link when the display is not needed (PDB = LOW). When the pin is driven by the host, make sure to release it after V_{DD33} and V_{DDIO} have reached final levels; no external components are required. In the case of driven by the V_{DDIO} = 3.0V to 3.6V or V_{DD33} directly, a 10 kohm resistor to the V_{DDIO} = 3.0V to 3.6V or V_{DD33} , and a >10uF capacitor to the ground are required (See *Figure 22* Typical Connection Diagram).

STOP STREAM SLEEP

The deserializer enters a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the deserializer will then lock to the incoming signal and recover the data. Note – in STOP STREAM SLEEP, the Serial Control Bus Registers values are retained.

SERIAL LINK FAULT DETECT

The serial link fault detection is able to detect any of following seven (7) conditions

1) cable open

2) "+" to "-" short

3) "+" short to GND

4) "-" short to GND

5) "+" short to battery

6) "-" short to battery

7) Cable is linked incorrectly

If any one of the fault conditions occurs, The Link Detect Status is 0 (cable is not detected) on the Serial Control Bus Register bit 0 of address 0x1C *Table 9*. The link errors can be monitored though Link Error Count of the Serial Control Bus Register bit [4:0] of address 0x41 *Table 9*.

OSCILLATOR OUTPUT

The deserializer provides an optional PCLK output when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature is controlled by register Address 0x02, bit 5 (OSC Clock Enable). See *Table 9*.

PIXEL CLOCK EDGE SELECT (RFB)

The RFB determines the edge that the data is strobed on. If RFB is High ('1'), output data is strobed on the Rising edge of the PCLK. If RFB is Low ('0'), data is strobed on the Falling edge of the PCLK. This allows for inter-operability with downstream devices. The deserializer output does not need to use the same edge as the Ser input. This feature may be controlled by register. See *Table 9*.

CLOCK-DATA RECOVERY STATUS FLAG (LOCK), OUTPUT ENABLE (OEN) AND OUTPUT STATE SELECT (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK is TRI-STATE or LOW (depending on the value of the OEN setting). After the DS90UB926Q completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and PCLK outputs. The State of the outputs are based on the OEN and OSS_SEL setting (*Table 3*) or register bit (*Table 9*). See *Figure 7*.

TABLE 3. Output States

Inputs				Outputs			
Serial input	PDB	OEN	OSS_SEL	Lock	Pass	Data, GPIO, I2S	CLK
X	0	X	X	Z	Z	Z	Z
X	1	0	0	L or H	L	L	L
X	1	0	1	L or H	Z	Z	Z
Static	1	1	0	L	L	L	L/OSC (Register bit enable)
Static	1	1	1	L	Previous Status	L	L
Active	1	1	0	H	L	L	L
Active	1	1	1	H	Valid	Valid	Valid

LOW FREQUENCY OPTIMIZATION (LFMODE)

The LFMODE is set via register (*Table 9*) or MODE_SEL Pin 24 (*Table 4*). It controls the operating frequency of the deserializer. If LFMODE is Low (default), the PCLK frequency is between 15 MHz and 85 MHz. If LFMODE is High, the PCLK frequency is between 5 MHz and <15 MHz. Please note when the device LFMODE is changed, a PDB reset is required.

INTERRUPT PIN — FUNCTIONAL DESCRIPTION AND USAGE (INTB)

1. On DS90UB925, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. DS90UB926Q deserializer INTB_IN (pin 16) is set LOW by some downstream device.
3. DS90UB925Q serializer pulls INTB (pin 31) LOW. The signal is active low, so a LOW indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read ISR register .
5. A read to ISR will clear the interrupt at the DS90UB925, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving INTB_IN. This would be when the downstream device releases the INTB_IN (pin 16) on the DS90UB926Q. The system is now ready to return to step (1) at next falling edge of INTB_IN.

CONFIGURATION SELECT (MODE_SEL)

Configuration of the device may be done via the MODE_SEL input pin, or via the configuration register bit. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL input (V_{R4}) and V_{DD33} to select one of the other 10 possible selected modes. See *Figure 13* and *Table 4*.
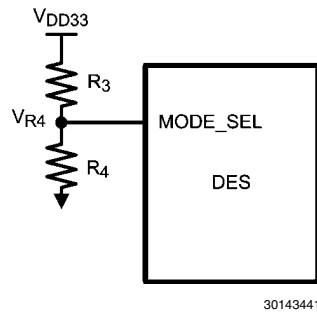

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FIGURE 13. MODE_SEL Connection Diagram

TABLE 4. Configuration Select (MODE_SEL)

#	Ideal Ratio V_{R4}/V_{DD33}	Ideal V_{R4} (V)	Suggested Resistor R3 kΩ (1% tol)	Suggested Resistor R4 kΩ (1% tol)	LFMODE	Repeater	Backward Compatible	I2S Channel B (18–bit Mode)
1	0	0	Open	40.2 or Any	L	L	L	L
2	0.121	0.399	294	40.2	L	L	L	H
3	0.152	0.502	280	49.9	L	H	L	L
4	0.242	0.799	240	76.8	L	H	L	H
5	0.311	1.026	226	102	H	L	L	L
6	0.402	1.327	196	130	H	L	L	H
7	0.492	1.624	169	165	H	H	L	L
8	0.583	1.924	137	191	H	H	L	H
9	0.629	2.076	124	210	L	L	H	L

LFMODE: L = 15 – 85 MHz (Default); H = 5 – <15 MHz

Repeater: L = Repeater Off (Default); H = Repeater On

Backward Compatible: L = Backward Compatible Off (Default); H = Backward Compatible On to 905/907 (15 - 65MHz)

I2S Channel B: L = I2S Channel B Off, Normal 24-bit RGB Mode (Default); H = I2S Channel B On, 18-bit RGB Mode with I2S_DB Enabled.

I2S RECEIVING

In normal 24-bit RGB operation mode, the DS90UB926Q provides up to 3-bit of I2S. They are I2S_CLK, I2S_WC and I2S_DA, as well as the Master I2S Clock (MCLK). The audio is received through the forward video frame, or can be configured to receive during video blanking periods. A jitter cleaning feature reduces I2S_CLK output jitter to +/- 2ns.

I2S Jitter Cleaning

The DS90UB926Q features a standalone PLL to clean the I2S data jitter supporting high end car audio systems. If I2S CLK frequency is less than 1MHz, this feature has to be disabled through the register bit I2S Control (0x2B) in *Table 9*.

Secondary I2S Channel

In 18-bit RGB operation mode, the secondary I2S data (I2S_DB) can be used as the additional I2S audio channel in additional to the 3–bit of I2S. The I2S_DB is synchronized to the I2S_CLK. To enable this synchronization feature on this bit, set the MODE_SEL (*Table 4*) or program through the register bit (*Table 9*).

MCLK

The deserializer has an I2S Master Clock Output. It supports x1, x2, or x4 of I2S CLK Frequency. When the I2S PLL is disabled, the MCLK output is off. below covers the range of I2S sample rates and MCLK frequencies.

By default, all the MCLK output frequencies are x2 of the I2S CLK frequencies. The MCLK frequencies can also be enabled through the register bit [7:4] (*I2S MCLK Output*) of 0x3A shown in *Table 9*. To select desired MCLK frequency, write bit 7 (0x3A) = 1, then write to bit [6:4] accordingly.

TABLE 5. Audio Interface Frequencies

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S CLK (MHz)	MCLK Output (MHz)	Bit [6:4] (Address 0x3A)
32	16	1.024	x1 of I2S CLK	000
			x2 of I2S CLK	001
			x4 of I2S CLK	010
44.1	16	1.411	x1 of I2S CLK	000
			x2 of I2S CLK	001
			x4 of I2S CLK	010
48	16	1.536	x1 of I2S CLK	000
			x2 of I2S CLK	001
			x4 of I2S CLK	010
96	16	3.072	x1 of I2S CLK	001
			x2 of I2S CLK	010
			x4 of I2S CLK	011
192	16	6.144	x1 of I2S CLK	010
			x2 of I2S CLK	011
			x4 of I2S CLK	100
32	24	1.536	x1 of I2S CLK	000
			x2 of I2S CLK	001
			x4 of I2S CLK	010
44.1	24	2.117	x1 of I2S CLK	001
			x2 of I2S CLK	010
			x4 of I2S CLK	011
48	24	2.304	x1 of I2S CLK	001
			x2 of I2S CLK	010
			x4 of I2S CLK	011
96	24	4.608	x1 of I2S CLK	010
			x2 of I2S CLK	011
			x4 of I2S CLK	100
192	24	9.216	x1 of I2S CLK	011
			x2 of I2S CLK	100
			x4 of I2S CLK	101
32	32	2.048	x1 of I2S CLK	001
			x2 of I2S CLK	010
			x4 of I2S CLK	011
44.1	32	2.822	x1 of I2S CLK	001
			x2 of I2S CLK	010
			x4 of I2S CLK	011
48	32	3.072	x1 of I2S CLK	001
			x2 of I2S CLK	010
			x4 of I2S CLK	011
96	32	6.144	x1 of I2S CLK	010
			x2 of I2S CLK	011
			x4 of I2S CLK	100
192	32	12.288	x1 of I2S CLK	011
			x2 of I2S CLK	100
			x4 of I2S CLK	110

GPIO[3:0] and GPO_REG[8:4]

In 18-bit RGB operation mode, the optional R[1:0] and G[1:0] of the DS90UB926Q can be used as the general purpose IOs GPIO [3:0] in either forward channel (Outputs) or back channel (Inputs) application.

GPIO[3:0] Enable Sequence

See *Table 6* for the GPIO enable sequencing.

Step 1: Enable the 18-bit mode either through the configuration register bit *Table 9* on DS90UB925Q only. DS90UB926Q is automatically configured as in the 18-bit mode.

Step 2: To enable GPIO3 forward channel, write 0x03 to address 0x0F on DS90UB925Q, then write 0x05 to address 0x1F on DS90UB926Q.

TABLE 6. GPIO Enable Sequencing Table

#	Description	Device	Forward Channel	Back Channel
1	Enable 18-bit mode	DS90UB925Q	0x12 = 0x04	0x12 = 0x04
		DS90UB926Q	Auto Load from DS90UB925Q	Auto Load from DS90UB925Q
2	GPIO3	DS90UB925Q	0x0F = 0x03	0x0F = 0x05
		DS90UB926Q	0x1F = 0x05	0x1F = 0x03
3	GPIO2	DS90UB925Q	0x0E = 0x30	0x0E = 0x50
		DS90UB926Q	0x1E = 0x50	0x1E = 0x30
4	GPIO1	DS90UB925Q	0x0E = 0x03	0x0E = 0x05
		DS90UB926Q	0x1E = 0x05	0x0E = 0x05
5	GPIO0	DS90UB925Q	0x0D = 0x93	0x0D = 0x95
		DS90UB926Q	0x1D = 0x95	0x1D = 0x93

GPO_REG[8:4] Enable Sequence

GPO_REG[8:4] are the outputs only pins. They must be programmed through the local register bits. See *Table 7* for the GPO_REG enable sequencing.

Step 1: Enable the 18-bit mode either through the configuration register bit on DS90UB925Q only. DS90UB926Q is automatically configured as in the 18-bit mode.

Step 2: To enable GPO_REG8 outputs an "1" , write 0x90 to address 0x21 on DS90UB926Q..

TABLE 7. GPO_REG Enable Sequencing Table

#	Description	Device	Local Access	Local Output Value
1	Enable 18-bit mode	DS90UB926Q	0x12 = 0x04 (on DS90UB925Q)	
2	GPO_REG8	DS90UB926Q	0x21 = 0x90	"1"
			0x21 = 0x10	"0"
3	GPO_REG7	DS90UB926Q	0x21 = 0x09	"1"
			0x21 = 0x01	"0"
4	GPO_REG6	DS90UB926Q	0x20 = 0x90	"1"
			0x20 = 0x10	"0"
5	GPO_REG5	DS90UB926Q	0x20 = 0x09	"1"
			0x20 = 0x01	"0"
6	GPO_REG4	DS90UB926Q	0x1F = 0x90	"1"
			0x1F = 0x10	"0"

REPEATER APPLICATION

The DS90UB925Q and DS90UB926Q can be configured to extend data transmission over multiple links to multiple display devices. Setting the devices into repeater mode provides a mechanism for transmitting to all receivers in the system.

Repeater Configuration

In a repeater application, In this document, the DS90UB925Q is referred to as the Transmitter or transmit port (TX), and the DS90UB926Q is referred to as the Receiver (RX). Figure 14 shows the maximum configuration supported for Repeater implementations using the DS90UB925Q (TX) and DS90UB926Q (RX). Two levels of Repeaters are supported with a maximum of three Transmitters per Receiver.
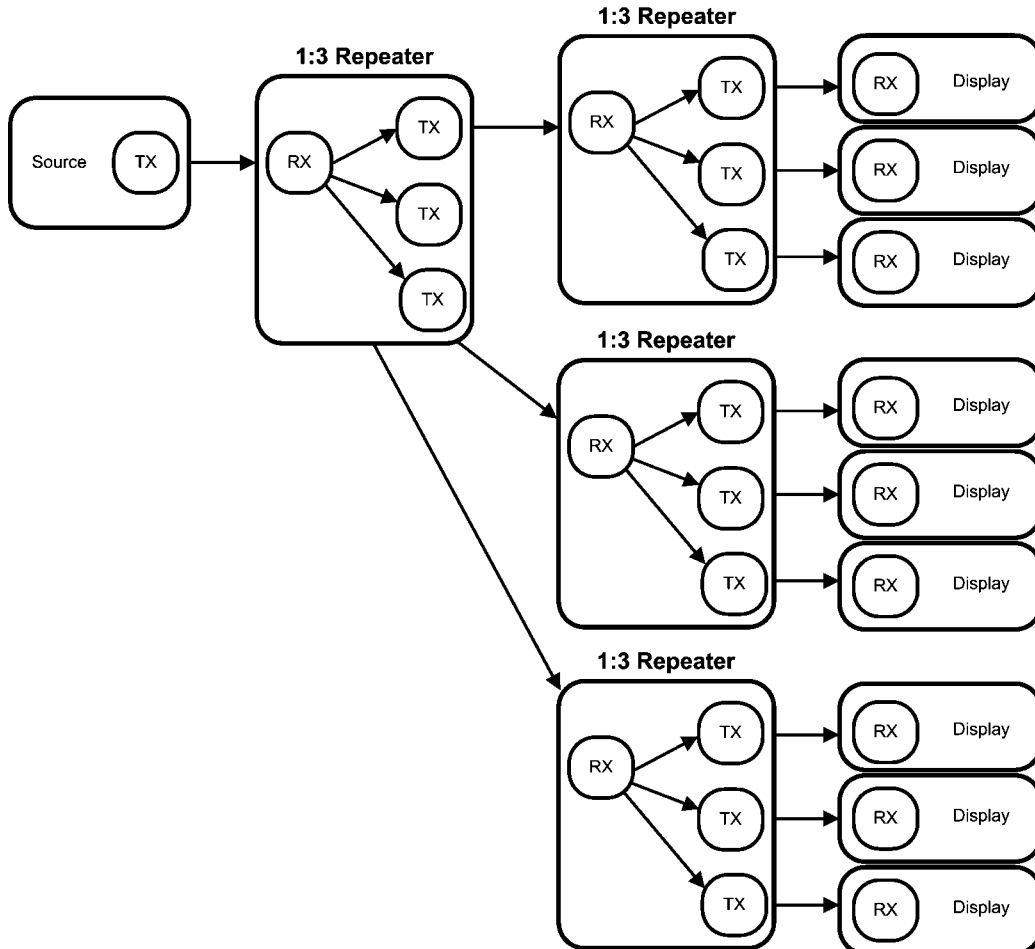
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FIGURE 14. Maximum Repeater Application

In a repeater application, the I2C interface at each TX and RX may be configured to transparently pass I2C communications upstream or downstream to any I2C device within the system. This includes a mechanism for assigning alternate IDs (Slave Aliases) to downstream devices in the case of duplicate addresses.

At each repeater node, the parallel LVCMOS interface fans out to up to three serializer devices, providing parallel RGB video data, HS/VS/DE control signals and, optionally, packetized audio data (transported during video blanking intervals). Alternatively, the I2S audio interface may be used to transport digital audio data between receiver and transmitters in place of packetized audio. All audio and video data is transmitted at the output of the Receiver and is received by the Transmitter..

Figure 15 provides more detailed block diagram of a 1:2 repeater configuration.
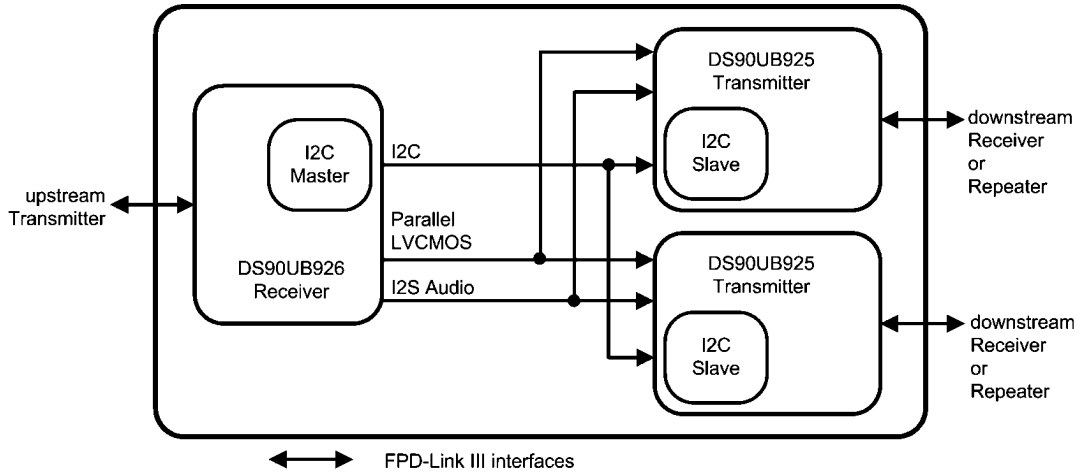
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FIGURE 15. 1:2 Repeater Configuration

Repeater Connections

The Repeater requires the following connections between the Receiver and each Transmitter *Figure 16*.

1) Video Data – Connect PCLK, RGB and control signals (DE, VS, HS).

2) I2C – Connect SCL and SDA signals. Both signals should be pulled up to V_{DD33} with 4.7 kΩ resistors.

3) Audio – Connect I2S_CLK, I2S_WC, and I2S_DA signals.

4) IDx pin – Each Transmitter and Receiver must have an unique I2C address.

5) MODE_SEL pin – All Transmitter and Receiver must be set into the Repeater Mode.

6) Interrupt pin– Connect DS90UB926Q INTB_IN pin to DS90UB925Q INTB pin. The signal must be pulled up to V_{DDIO}.
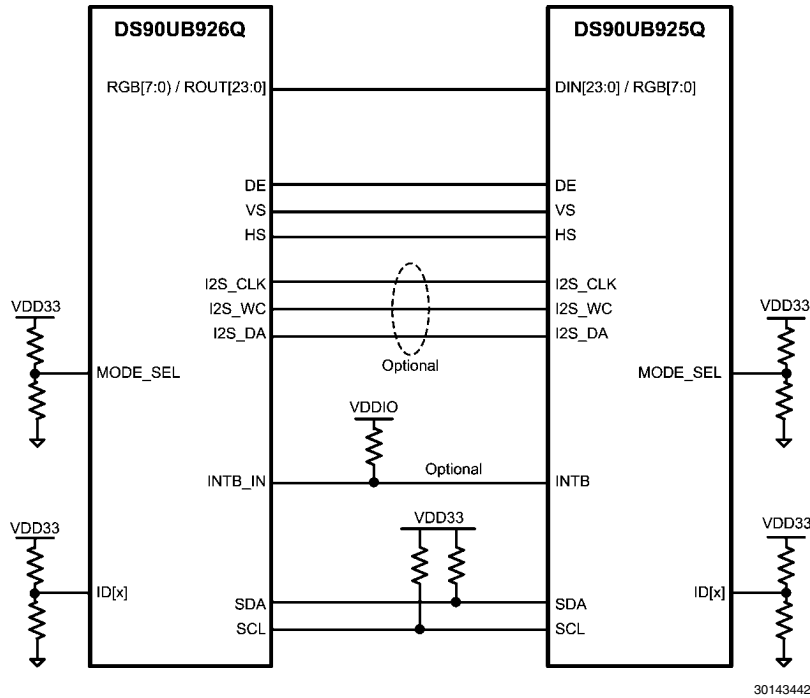
FIGURE 16. Repeater Connection Diagram

BUILT IN SELF TEST (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high speed serial link and the low- speed back channel. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. Note: BIST is not available in backwards compatible mode.

BIST Configuration and Status

The BIST mode is enabled at the deseralizer by the Pin select (Pin 44 BISTEN and Pin 16 BISTC) or configuration register(*Table 9*) through the deserializer. When LFMODE = 0, the pin based configuration defaults to external PCLK or 33 MHz internal Oscillator clock (OSC) frequency. In the absence of PCLK, the user can select the desired OSC frequency (default 33 MHz or 25MHz) through the register bit. When LFMODE = 1, the pin based configuration defaults to external PCLK or 12.5MHz MHz internal Oscillator clock (OSC) frequency.

When BISTEN of the deserializer is high, the BIST mode enable information is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The PASS output pin toggles to flag any payloads that are received with 1 to 35 bit errors.

The BIST status is monitored real time on PASS pin. The result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. This BIST feature also contains a Link Error Count and a Lock Status. If the connection of the serial link is broken, then the link error count is shown in the register. When the PLL of the deserializer is locked or unlocked, the lock status can be read in the register. See *Table 9*.

Sample BIST Sequence

See *Figure 17* for the BIST mode flow diagram.

Step 1: For the DS90UB925Q and DS90UB926Q FPD-Link III chipset, BIST Mode is enabled via the BISTEN pin of DS90UB926Q FPD-Link III deserializer. The desired clock source is selected through BISTC pin.

Step 2: The DS90UB925Q serializer is woken up through the back channel if it is not already on. The all zero pattern on the data pins is sent through the FPD-Link III to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: The Link returns to normal operation after the deserializer BISTEN pin is low. *Figure 18* shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (Rx Equalization).
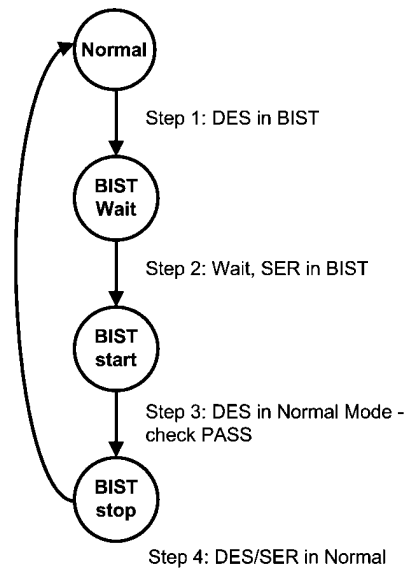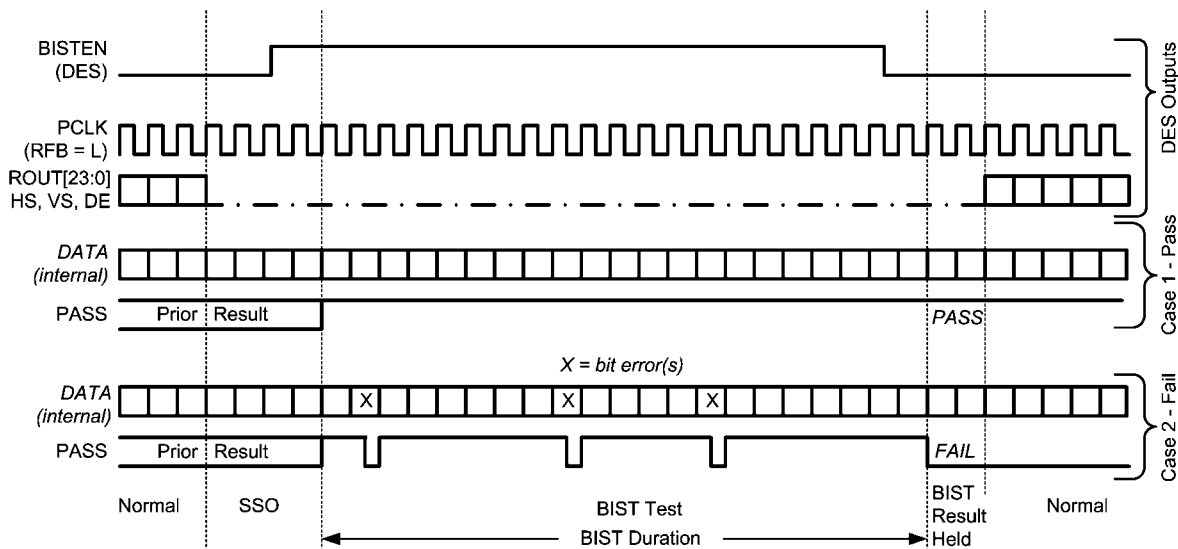

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FIGURE 17. BIST Mode Flow Diagram

Forward Channel and Back Channel Error Checking

While in BIST mode, the serializer stops sampling RGB input pins and switches over to an internal test pattern. The internal all-zeroes pattern goes through scrambler, dc-balancing etc. and goes over the serial link to the deserializer. The deserializer on locking to the serial stream compares the recovered serial stream with all-zeroes and records any errors in status registers and dynamically indicates the status on PASS pin.

The back-channel data is checked for CRC errors once the serializer locks onto back-channel serial stream as indicated by link detect status (register bit 0x0C[0]). The CRC errors are recorded in an 8-bit register. The register is cleared when the serializer enters the BIST mode. As soon as the serializer exits BIST mode, the functional mode CRC register starts recording the CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of last BIST run until cleared or enters BIST mode again.


FIGURE 18. BIST Waveforms

Serial Control Bus

The DS90UB926Q is configured by the use of a serial control bus that is I2C protocol compatible. . Multiple deserializer devices may share the serial control bus since 16 device addresses are supported. Device address is set via R_1 and R_2 values on IDx pin. See *Figure 19* below.

The serial control bus consists of two signals and a configuration pin. The SCL is a Serial Bus Clock Input / Output. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V_{DD33}. For most applications a 4.7 k pull-up resistor to V_{DD33} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.
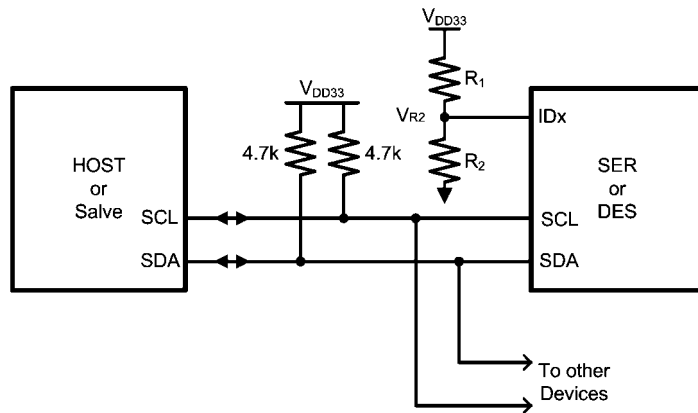
FIGURE 19. Serial Control Bus Connection

The configuration pin is the IDx pin. This pin sets one of 16 possible device addresses. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the IDx input (V_{R2}) and V_{DD33} to select one of the other 16 possible addresses. See *Table 8*.

TABLE 8. Serial Control Bus Addresses for IDx

#	Ideal Ratio V_{R2} / V_{DD33}	Ideal V_{R2} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	Address 7'b	Address 8'b Appended
1	0	0	Open	40.2 or Any	0x2C	0x58
2	0.121	0.399	294	40.2	0x2D	0x5A
3	0.152	0.502	280	49.9	0x2E	0x5C
4	0.182	0.601	270	60.4	0x2F	0x5E
5	0.212	0.700	267	71.5	0x30	0x60
6	0.242	0.799	240	76.8	0x31	0x62
7	0.273	0.901	243	90.9	0x32	0x64
8	0.310	1.023	226	102	0x33	0x66
9	0.356	1.175	210	115	0x34	0x68
10	0.402	1.327	196	130	0x35	0x6A
11	0.447	1.475	182	147	0x36	0x6C
12	0.492	1.624	169	165	0x37	0x6E
13	0.538	1.775	154	180	0x38	0x70
14	0.583	1.924	137	191	0x39	0x72
15	0.629	2.076	124	210	0x3A	0x74
16	0.727	2.399	90.9	243	0x3B	0x76

TABLE 9. Serial Control Bus Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
0	0x00	I2C Device ID	7:1	RW		Device ID	7–bit address of Deserializer See *Table 4*
			0	RW		ID Setting	I2C ID Setting 1: Register I2C Device ID (Overrides IDx pin) 0: Device ID is from IDx pin
1	0x01	Reset	7	RW	0x04	Remote Auto Power Down	Remote Auto Power Down 1: Power down when no forward channel link is detected 0: Do not power down when no forward channel link is detected
			6:3				***Reserved***
			2	RW		BC Enable	Back channel enable 1: Enable 0: Disable
			1	RW		Digital RESET1	Reset the entire digital block including registers This bit is self-clearing. 1: Reset 0: Normal operation
			0	RW		Digital RESET0	Reset the entire digital block except registers This bit is self-clearing 1: Reset 0: Normal operation
2	0x02	Configuration [0]	7	RW	0x00	Output Enable	LVCMOS Output Enable. 1: Enable 0: Disable. Tri-state Outputs
			6	RW		OEN and OSS_SEL Override	Overrides Output Enable Pin and Output State pin 1: Enable override 0: Disable - no override
			5	RW		OSC Clock Enable	OSC Clock Output Enable If loss of lock OSC clock is output onto PCLK 0: Disable 1: Enable
			4	RW		Output Sleep State Select (OSS_SEL)	OSS Select to Control Output State during Lock Low Period 1: Enable 0: Disable
			3	RW		Backward Compatible Mode Override	Mode_Sel Backward compatible Mode Override Enable. 1: Use register bit "reg_02[2]" to set BC Mode 0: Use MODE_SEL option.
			2	RW		Backward Compatible Mode Select	Backward Compatible Mode Select to DS90UR905Q and DS90UR907Q. If Reg_02[3] = 1 1: Backward Compatible is on 0: Backward Compatible is off
			1	RW		LFMODE Pin Override	LFMODE Pin Override Enable 1: Use register bit "reg_02[0]" to set LFMODE 0: Use LFMODE Pin
			0	RW		LFMODE	Low Frequency Mode Select 1: PCLK = 5 - <15 MHz 0: PCLK = 15 - 85 MHz

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
3	0x03	Configuration [1]	7		0xF0		***Reserved***
			6	RW		CRC Generator Enable	CRC Generator Enable (Back Channel) 1: Enable 0: Disable
			5				***Reserved***
			4	RW		Filter Enable	HS, VS, DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected 1: Filtering enable 0: Filtering disable
			3	RW		I2C Pass-through	I2C Pass-Through Mode 1: Pass-Through Enabled 0: Pass-Through Disabled
			2	RW		Auto ACK	ACK Select 1: Auto ACK enable 0: Self ACK
			1				***Reserved***
			0	RW		RRFB	Pixel Clock Edge Select 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.
4	0x04	BCC Watchdog Control	7:1	RW	0xFE	BCC Watchdog Timer	The watchdog timer allows termination of a control channel transaction, if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0
			0	RW		BCC Watchdog Timer Disable	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation"
5	0x05	I2C Control [1]	7	RW	0x2E	I2C Pass Through All	I2C Pass-Through All Transactions 1: Enabled 0: Disabled
			6:4	RW		I2C SDA Hold Time	Internal I2C SDA Hold Time It configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 ns.
			3:0	RW		I2C Filter Depth	I2C Glitch Filter Depth It configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 ns.

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
6	0x06	I2C Control [2]	7	R	0x00	Forward Channel Sequence Error	Control Channel Sequence Error Detected It indicates a sequence error has been detected in forward control channel. It this bit is set, an error may have occurred in the control channel operation.
			6	RW		Clear Sequence Error	It clears the Sequence Error Detect bit This bit is not self-clearing.
			5				*Reserved*
			4:3	RW		SDA Output Delay	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50 ns. Nominal output delay values for SCL to SDA are: 00 : 250ns 01: 300ns 10: 350ns 11: 400ns
			2	RW		Local Write	Disable Remote Writes to Local Registers through Serializer (Does not affect remote access to I2C slaves at Deserializer) 1: Stop remote write to local device registers 0: remote write to local device registers
			1	RW		I2C Bus Timer Speed	Speed up I2C Bus Watchdog Timer 1: Timer expires after approximately 50 ms 0: Timer expires after approximately 1s
			0	RW		I2C Bus Timer Disable	Disable I2C Bus Timer When the I2C Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 s, the I2C bus is assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL
7	0x07	Remote Device ID	7:1	RW	0x18	Remote ID	Remote ID Configures the I2C Slave ID of the remote Serializer. A value of 0 in this field disables I2C access to remote Serializer. This field is automatically configured via the Serializer Forward Channel. Software may overwrite this value, but should also set the FREEZE DEVICE ID bit to prevent overwriting by the Forward Channel.
			0	RW		Freeze Device ID	Freeze Serializer Device ID 1: Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written. 0: Update
8	0x08	SlaveID[0]	7:1	RW	0x00	Target Slave Device ID0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				*Reserved*

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
9	0x09	SlaveID[1]	7:1	RW	0x00	Target Slave Device ID1	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				*Reserved*
10	0x0A	SlaveID[2]	7:1	RW	0x00	Target Slave Device ID2	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				*Reserved*
11	0x0B	SlaveID[3]	7:1	RW	0x00	Target Slave Device ID3	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				*Reserved*
12	0x0C	SlaveID[4]	7:1	RW	0x00	Target Slave Device ID4	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				*Reserved*
13	0x0D	SlaveID[5]	7:1	RW	0x00	Target Slave Device ID5	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				*Reserved*
14	0x0E	SlaveID[6]	7:1	RW	0x00	Target Slave Device ID6	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				*Reserved*

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
15	0x0F	SlaveID[7]	7:1	RW	0x00	Target Slave Device ID7	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				*Reserved*
16	0x10	SlaveAlias[0]	7:1	RW	0x00	ID[0] Match	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				*Reserved*

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
17	0x11	SlaveAlias[1]	7:1	RW	0x00	ID[1] Match	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				*Reserved*
18	0x12	SlaveAlias[2]	7:1	RW	0x00	ID[2] Match	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				*Reserved*
19	0x13	SlaveAlias[3]	7:1	RW	0x10	ID[3] Match	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				*Reserved*
20	0x14	SlaveAlias[4]	7:1	RW	0x00	ID[4] Match	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				*Reserved*
21	0x15	SlaveAlias[5]	7:1	RW	0x00	ID[5] Match	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				*Reserved*
22	0x16	SlaveAlias[6]	7:1	RW	0x00	ID[6] Match	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	RW			*Reserved*

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
23	0x17	SlaveAlias[7]	7:1	RW	0x00	ID[7] Match	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				*Reserved*
28	0x1C	General Status	7:4	RW	0x00		*Reserved*
			3	R		I2S Locked	I2S Lock Status 0: I2S PLL controller not locked 1: I2S PLL controller locked to input I2S clock
			2				*Reserved*
			1				*Reserved*
			0	R		Lock	Deserializer CDR, PLL's clock to recovered clock frequency 1: Deserializer locked to recovered clock 0: Deserializer not locked
29	0x1D	GPIO0 Config	7:4	R	0xA0	Rev-ID	Revision ID: 1010: Production Device
			3	RW		GPIO0 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO0 Remote Enable	Remote GPIO0 Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Serializer
			1	RW		GPIO0 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO0 Enable	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
30	0x1E	GPIO2 and GPIO1 Config	7	RW	0x00	GPIO2 Output Value	Local GPIO Output Value This value is output on the GPIO when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			6	RW		GPIO2 Remote Enable	Remote GPIO2 Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Serializer.
			5	RW		GPIO2 Direction	Local GPIO Direction 1: Input 0: Output
			4	RW		GPIO2 Enable	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
			3	RW		GPIO1 Output Value	Local GPIO Output Value This value is output on the GPIO when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO1 Remote Enable	Remote GPIO1 Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Serializer.
			1	RW		GPIO1 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO1 Enable	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
31	0x1F	GPO_REG4 and GPO3 Config	7	RW	0x00	GPO_REG4 Output Value	Local GPO_REG4 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			6:5				*Reserved*
			4	RW		GPO_REG4 Enable	GPO_REG4 Function Enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPIO3 Output Value	Local GPIO Output Value This value is output on the GPIO when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO3 Remote Enable	Remote GPIO3 Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Serializer.
			1	RW		GPIO3 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO3 Enable	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
32	0x20	GPO_REG6 and GPO_REG5 Config	7	RW	0x00	GPO_REG6 Output Value	Local GPO_REG6 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			6:5				*Reserved*
			4	RW		GPO_REG6 Enable	GPO_REG6 Function Enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPO_REG5 Output Value	Local GPO_REG5 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			2:1				*Reserved*
			0	RW		GPO_REG5 Enable	GPO_REG5 Function Enable 1: Enable GPO operation 0: Enable normal operation
33	0x21	GPO8 and GPO7 Config	7	RW	0x00	GPO_REG8 Output Value	Local GPO_REG8 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			6:5				*Reserved*
			4	RW		GPO_REG8 Enable	GPO_REG8 Function Enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPO_REG7 Output Value	Local GPO_REG7 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			2:1				*Reserved*
			0	RW		GPO_REG7 Enable	GPO_REG7 Function Enable 1: Enable GPO operation 0: Enable normal operation

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
34	0x22	Data Path Control	7	RW	0x00	Override FC Config	1: Disable loading of this register from the forward channel, keeping locally written values intact 0: Allow forward channel loading of this register
			6	RW		Pass RGB	Setting this bit causes RGB data to be sent independent of DE. This allows operation in systems which may not use DE to frame video data or send other data when DE is deasserted. Note that setting this bit blocks packetized audio. This bit does not need to be set in DS90UB925 or in Backward Compatibility mode. 1: Pass RGB independent of DE 0: Normal operation Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			5	RW		DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low) Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			4	RW		I2S_Gen	This bit controls whether the Receiver outputs packetized Auxiliary/Audio data on the RGB video output pins. 1: Don't output packetized audio data on RGB video output pins 0: Output packetized audio on RGB video output pins. Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			3	RW		I2S Channel B Enable Override	1: Set I2S Channel B Enable from reg_22[0] 0: Set I2S Channel B Enable from MODE_SEL pin Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			2	RW		18-bit Video Select	1: Select 18-bit video mode 0: Select 24-bit video mode Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			1	RW		I2S Transport Select	1: Enable I2S Data Forward Channel Frame Transport 0: Enable I2S Data Island Transport Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			0	RW		I2S Channel B Enable	I2S Channel B Enable 1: Enable I2S Channel B on B1 output 0: I2S Channel B disabled Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
35	0x23	General Purpose Control	7	RW	0x10	Rx RGB Checksum	RX RGB Checksum Enable Setting this bit enables the Receiver to validate a one-byte checksum following each video line. Checksum failures are reported in the STS register
			6:5				*Reserved*
			4	R		Mode_Sel	Mode Select is Done
			3	R		LFMODE	Low Frequency Mode Status
			2	R		Repeater	Repeater Mode Status
			1	R		Backward	Backward Compatible Mode Status
			0	R		I2S Channel B	I2S Channel B Status
36	0x24	BIST Control	7:4		0x08		*Reserved*
			3	RW		BIST Pin Config	BIST Configured through Pin 1: BIST configured through pin 0: BIST configured through register bit
			2:1	RW		BIST Clock Source	BIST Clock Source 00: External Pixel Clock 01: 33 MHz Oscillator 10: Reserved 11: 25 MHz Oscillator
			0	RW		BIST Enable	BIST Control 1: Enabled 0: Disabled
37	0x25	BIST Error	7:0	R	0x00	BIST Error Count	BIST Error Count
38	0x26	SCL High Time	7:0	RW	0x83	SCL High Time	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Deserializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.
39	0x27	SCL Low Time	7:0	RW	0x84	SCL Low Time	I2C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26MHz rather than the nominal 20MHz.

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
41	0x29	FRC Control	7	RW	0x00	Timing Mode Select	Select display timing mode 0: DE only Mode 1: Sync Mode (VS,HS)
			6	RW		VS Polarity	0: Active High 1: Active Low
			5	RW		HS Polarity	0: Active High 1: Active Low
			4	RW		DE Polarity	0: Active High 1: Active Low
			3	RW		FRC2 Enable	0: FRC2 Disable 1: FRC2 Enable
			2	RW		FRC1 Enable	0: FRC1 Disable 1: FRC1 Enable
			1	RW		Hi-FRC 2 Disable	0: Hi-FRC2 Enable 1: Hi-FRC2 Disable
			0	RW		Hi-FRC 1 Disable	0: Hi-FRC1 Enable 1: Hi-FRC1 Disable
42	0x2A	White Balance Control	7:6	RW	0x00	Page Setting	00: Configuration Registers 01: Red LUT 10: Green LUT 11: Blue LUT
			5	RW		White Balance Enable	0: White Balance Disable 1: White Balance Enable
			4	RW		LUT Reload Enable	0: Reload Disable 1: Reload Enable
			3:0				*Reserved*
43	0x2B	I2S Control	7	RW	0x00	I2S PLL	I2S PLL Control 0: I2S PLL is on for I2S data jitter cleaning 1: I2S PLL is off. No jitter cleaning
			6:1				*Reserved*
			0	RW		I2S Clock Edge	I2S Clock Edge Select 0: I2S Data is strobed on the Rising Clock Edge 1: I2S Data is strobed on the Falling Clock Edge

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
44	0x2C	SSCG Control	7:4		0x00		*Reserved*
			3	RW		SSCG Enable	Enable Spread Spectrum Clock Generator 0: Disable 1: Enable
			2:0	RW		SSCG Selection	SSCG Frequency Deviation: When LFMODE = H fdev fmod 000: +/- 0.7 CLK/628 001: +/- 1.3 010: +/- 1.8 011: +/- 2.5 100: +/- 0.7 CLK/388 101: +/- 1.2 110: +/- 2.0 111: +/- 2.5 When LFMODE = L fdev fmod 000: +/- 0.9 CLK/2168 001: +/- 1.2 010: +/- 1.9 011: +/- 2.5 100: +/- 0.7 CLK/1300 101: +/- 1.3 110: +/- 2.0 111: +/- 2.5
58	0x3A	I2S MCLK Output	7	RW	0x00	MCLK Override	1: Override divider select for MCLK 0: No override for MCLK divider
			6:4	RW		MCLK Frequency Slect	See *Table 5*
			3:0				*Reserved*
65	0x41	Link Error Count	7:5		0x03		*Reserved*
			4	RW		Link Error Count Enable	Enable serial link data integrity error count 1: Enable error count 0: Disable
			3:0	RW		Link Error Count	Link error count threshold. Counter is pixel clock based. clk0, clk1 and DCA are monitored for link errors, if error count is enabled, deserilizer loose lock once error count reaches threshold. If disabled deserilizer loose lock with one error.

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
68	0x44	Equalization	7:5	RW	0x60	EQ Stage 1 Select	EQ select value. Used if adaptive EQ is bypassed. 000 Min EQ 1st Stage 001 010 011 100 101 110 111 Max EQ 1st Stage
			4				*Reserved*
			3:1	RW		EQ Stage 2 Select	EQ select value. Used if adaptive EQ is bypassed. 000 Min EQ 2nd Stage 001 010 011 100 101 110 111 Max EQ 2nd Stage
			0	RW		Adaptive EQ	1: Disable adaptive EQ (to write EQ select values) 0: Enable adaptive EQ
86	0x56	CML Output	7:4		0x08		*Reserved*
			3	RW		CMLOUT +/- Enable	1: Disabled (Default) 0: Enabled
			2:0				*Reserved*

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode 0000: Reserved 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/Cyan to White 1000: Horizontally Scaled Black to Green/Magenta to White 1001: Horizontally Scaled Black to Blue/Yellow to White 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/Cyan to White 1100: Vertically Scaled Black to Green/Magenta to White 1101: Vertically Scaled Black to Blue/Yellow to White 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: Reserved
			3:1				***Reserved***
			0	RW		Pattern Generator Enable	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
101	0x65	Pattern Generator Configuration	7:5		0x00		***Reserved***
			4	RW		Pattern Generator 18 Bits	18-bit Mode Select 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness.
			3	RW		Pattern Generator External Clock	Select External Clock Source 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Pattern Generator Timing Select	Timing Select Control 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
			1	RW		Pattern Generator Color Invert	Enable Inverted Color Patterns 1: Invert the color output. 0: Do not invert the color output.
			0	RW		Pattern Generator Auto-Scroll Enable	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.
102	0x66	Pattern Generator Indirect Address	7:0	RW	0x00	Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See *AN-2198*
103	0x67	Pattern Generator Indirect Data	7:0	RW	0x00	Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See *AN-2198*
240	0xF0	RX ID	7:0	R	0x5F	ID0	First byte ID code: '_'
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code: 'U'
242	0xF2		7:0	R	0x48	ID2	Third byte of ID code, Value will be either 'B'.
243	0xF3		7:0	R	0x39	ID3	Fourth byte of ID code: '9'
244	0xF4		7:0	R	0x32	ID4	Fifth byte of ID code: '2'
245	0xF5		7:0	R	0x36	ID5	Sixth byte of ID code: '6'

Image Enhancement Features

Several image enhancement features are provided. White balance LUTs allow the user to define and target the color temperature of the display. Adaptive Hi-FRC dithering enables the presentation of "true-color" images on an 18–bit color display.

WHITE BALANCE

The White Balance feature enables similar display appearance when using LCD's from different vendors. It compensates for native color temperature of the display, and adjusts relative intensities of R, G, B to maintain specified color temperature. Programmable control registers are used to define the contents of three LUTs (8-bit color value for Red, Green and Blue) for the White Balance Feature. The LUTs map input RGB values to new output RGB values. There are three LUTs, one LUT for each color. Each LUT contains 256 entries, 8-bits per entry with a total size of 6144 bits (3 x 256 x 8). All entries are readable and writable. Calibrated values are loaded into registers through the I2C interface (deserializer is a slave device). This feature may also be applied to lower color depth applications such as 18–bit (666) and 16–bit (565). White balance is enabled and configured via serial control bus register.

LUT contents

The user must define and load the contents of the LUT for each color (R,G,B). Regardless of the color depth being driven (888, 666, 656), the user must always provide contents for 3 complete LUTs - 256 colors x 8 bits x 3 tables. Unused bits - LSBs -shall be set to "0" by the user.

When 24-bit (888) input data is being driven to a 24-bit display, each LUT (R, G and B) must contain 256 unique 8-bit entries. The 8-bit white balanced data is then available at the output of the DS90UB926Q deserializer, and driven to the display.

When 18-bit (666) input data is being driven to an 18-bit display, the white balance feature may be used in one of two ways. First, simply load each LUT with 256, 8-bit entries. Each 8-bit entry is a 6-bit value (6 MSBs) with the 2 LSBs set to "00". Thus as total of 64 unique 6-bit white balance output values are available for each color (R, G and B). The 6-bit white balanced data is available at the output of the DS90UB926Q deserializer, and driven directly to the display.

Alternatively, with 6-bit input data the user may choose to load complete 8-bit values into each LUT. This mode of operation provides the user with finer resolution at the LUT output to more closely achieve the desired white point of the calibrated display. Although 8-bit data is loaded, only 64 unique 8-bit white balance output values are available for each color (R, G and B). The result is 8-bit white balanced data. Before driving to the output of the deserializer, the 8-bit data must be reduced to 6-bit with an FRC dithering function. To operate in this mode, the user must configure the DS90UB926Q to enable the FRC2 function.

Examples of the three types of LUT configurations described are shown in *Figure 20*

Enabling white balance

The user must load all 3 LUTs prior to enabling the white balance feature. The following sequence must be followed by the user.

To initialize white balance after power-on (*Table 10*):

1) Load contents of all 3 LUTs . This requires a sequential loading of LUTs - first RED, second GREEN, third BLUE. 256, 8-bit entries must be loaded to each LUT. Page registers must be set to select each LUT.

2) Enable white balance

By default, the LUT data may not be reloaded after initialization at power-on.

An option does exist to allow LUT reloading after power-on and initial LUT loading (as described above). This option may only be used after enabling the white balance reload feature via the associated serial control bus register. In this mode the LUTs may be reloaded by the master controller via I2C. This provides the user with the flexibility to refresh LUTs periodically , or upon system requirements to change to a new set of LUT values. The host controller loads the updated LUT values via the serial bus interface. There is no need to disable the white balance feature while reloading the LUT data. Refreshing the white balance to the new set of LUT data will be seamless - no interruption of displayed data.

It is important to note that initial loading of LUT values requires that all 3 LUTs be loaded sequentially. When reloading, partial LUT updates may be made.

8-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000000b
1	00000001b
2	00000011b
3	00000011b
4	00000110b
5	00000110b
6	00000111b
7	00000111b
8	00001000b
9	00001010b
10	00001001b
11	00001011b
⋮	⋮
248	11111010b
249	11111010b
250	11111011b
251	11111011b
252	11111110b
253	11111101b
254	11111101b
255	11111111b

6-bit in / 6 bit out

Gray level Entry	Data Out (8-bits)
0	00000000b
1	N/A
2	N/A
3	N/A
4	00000100b
5	N/A
6	N/A
7	N/A
8	00001000b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11111000b
249	N/A
250	N/A
251	N/A
252	11111100b
253	N/A
254	N/A
255	N/A

6-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000001b
1	N/A
2	N/A
3	N/A
4	00000110b
5	N/A
6	N/A
7	N/A
8	00001011b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11111010b
249	N/A
250	N/A
251	N/A
252	11111111b
253	N/A
254	N/A
255	N/A

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FIGURE 20. White Balance LUT Configurations

TABLE 10. White Balance Register Table

PAGE	ADD (dec)	ADD (hex)	Register Name	Bit(s)	Access	Default (hex)	Function	Description
0	42	0x2A	White Balance Control	7:6	RW	0x00	Page Setting	00: Configuration Registers 01: Red LUT 10: Green LUT 11: Blue LUT
				5	RW		White Balance Enable	0: White Balance Disable 1: White Balance Enable
				4	RW			0: Reload Disable 1: Reload Enable
				3:0				*Reserved*
1	0 – 255	00 – FF	White Balance Red LUT	FF:0	RW	N/A	Red LUT	256 8–bit entries to be applied to the Red subpixel data
2	0 – 255	00 – FF	White Balance Green LUT	FF:0	RW	N/A	Green LUT	256 8–bit entries to be applied to the Green subpixel data
3	0 – 255	00 – FF	White Balance Blue LUT	FF:0	RW	N/A	Blue LUT	256 8–bit entries to be applied to the Blue subpixel data

ADAPTIVE HI-FRC DITHERING

The Adaptive FRC Dithering Feature delivers product-differentiating image quality. It reduces 24-bit RGB (8 bits per subpixel) to 18-bit RGB (6 bits per sub-pixel), smoothing color gradients, and allowing the flexibility to use lower cost 18-bit displays. FRC (Frame Rate Control) dithering is a method to emulate "missing" colors on a lower color depth LCD display by changing the pixel color slightly with every frame. FRC is achieved by controlling on and off pixels over multiple frames (Temporal). Static dithering regulates the number of on and off pixels in a small defined pixel group (Spatial). The FRC module includes both Temporal and Spatial methods and also Hi-FRC. Conventional FRC can display only 16,194,277 colors with 6-bit RGB source. "Hi-FRC" enables full (16,777,216) color on an 18-bit LCD panel. The "adaptive" FRC module also includes input pixel detection to apply specific Spatial dithering methods for smoother gray level transitions. When enabled, the lower LSBs of each RGB output are not active; only 18 bit data (6 bits per R,G and B) are driven to the display. This feature is enabled via serial control bus register.

Two FRC functional blocks are available, and may be independently enabled. FRC1 precedes the white balance LUT, and is intended to be used when 24-bit data is being driven to an 18-bit display with a white balance LUT that is calibrated for an 18-bit

data source. The second FRC block, FRC2, follows the white balance block and is intended to be used when fine adjustment of color temperature is required on an 18-bit color display, or when a 24-bit source drives an 18-bit display with a white balance LUT calibrated for 24-bit source data.

For proper operation of the FRC dithering feature, the user must provide a description of the display timing control signals. The timing mode, "sync mode" (HS, VS) or "DE only" must be specified, along with the active polarity of the timing control signals. All this information is entered to DS90UB926Q control registers via the serial bus interface.

Adaptive Hi-FRC dithering consists of several components. Initially, the incoming 8-bit data is expanded to 9-bit data. This allows the effective dithered result to support a total of 16.7 million colors. The incoming 9-bit data is evaluated, and one of four possible algorithms is selected. The majority of incoming data sequences are supported by the default dithering algorithm. Certain incoming data patterns (black/white pixel, full on/off sub-pixel) require special algorithms designed to eliminate visual artifacts associated with these specific gray level transitions. Three algorithms are defined to support these critical transitions.

An example of the default dithering algorithm is illustrated in *Figure 21*. The "1" or "0" value shown in the table describes whether the 6-bit value is increased by 1 ("1") or left unchanged ("0"). In this case, the 3 truncated LSBs are "001".

F0L0	Frame = 0, Line = 0
PD1	Pixel Data one
Cell Value 010	R[7:2]+0, G[7:2]+1, B[7:2]+0
LSB=001	three lsb of 9 bit data (8 to 9 for Hi-Frc)

Pixel Index	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	
LSB = 001									
F0L0	010	000	000	000	000	000	010	000	R = 4/32
F0L1	101	000	000	000	101	000	000	000	
F0L2	000	000	010	000	010	000	000	000	G = 4/32
F0L3	000	000	101	000	000	000	101	000	B = 4/32
F1L0	000	000	000	000	000	000	000	000	R = 4/32
F1L1	000	111	000	000	000	111	000	000	
F1L2	000	000	000	000	000	000	000	000	G = 4/32
F1L3	000	000	000	111	000	000	000	111	B = 4/32
F2L0	000	000	010	000	010	000	000	000	R = 4/32
F2L1	000	000	101	000	000	000	101	000	
F2L2	010	000	000	000	000	000	010	000	G = 4/32
F2L3	101	000	000	000	101	000	000	000	B = 4/32
F3L0	000	000	000	000	000	000	000	000	R = 4/32
F3L1	000	000	000	111	000	000	000	111	
F3L2	000	000	000	000	000	000	000	000	G = 4/32
F3L3	000	111	000	000	000	111	000	000	B = 4/32

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FIGURE 21. Default FRC Algorithm

See *Table 11* for recommended FRC settings dependant on 18/24–bit source, 18/24–bit white balance LUT, and 18/24–bit display.

TABLE 11. Recommended FRC settings

Source	White Balance LUT	Display	FRC1	FRC2
24–bit	24–bit	24–bit	Disabled	Disabled
24–bit	24–bit	18–bit	Disabled	Enabled
24–bit	18–bit	18–bit	Enabled	Disabled
18–bit	24–bit	24–bit	Disabled	Disabled
18–bit	24–bit	18–bit	Disabled	Enabled
18–bit	18–bit	18–bit	Disabled	Disabled

Internal Pattern Generation

The DS90UB926Q serializer supports the internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no parallel input is applied. If no PCLK is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to Application Note *AN-2198*.

Applications Information

DISPLAY APPLICATION

The DS90UB926Q, in conjunction with the DS90UB925Q, is intended for interface between a host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888) and high definition (720p) digital video format. It allows to receive a three 8-bit RGB stream with a pixel rate up to 85 MHz together with three control bits (VS, HS and DE) and three I2S-bus audio stream with an audio sampling rate up to 192 kHz.

The deserializer is expected to be located close to its target device. The interconnect between the deserializer and the target device is typically in the 1 to 3 inch separation range. The input capacitance of the target device is expected to be in the 5 to 10 pF range. Care should be taken on the PCLK output trace as this signal is edge sensitive and strobes the data. It is also assumed that the fanout of the deserializer is up to three in the repeater mode. If additional loads need to be driven, a logic buffer or mux device is recommended.

TYPICAL APPLICATION CONNECTION

Figure 22 shows a typical application of the DS90UB926Q deserializer for an 85 MHz 24-bit Color Display Application. inputs utilize 0.1 µF coupling capacitors to the line and the deserializer provides internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, seven 0.1 µF capacitors and two 4.7 µF capacitors should be used for local device bypassing. Ferrite beads are placed on the power lines for effective noise suppression. Since the device in the Pin/STRAP mode, two 10 kΩ pull-up resistors are used on the parallel output bus to select the desired device features.

The interface to the target display is with 3.3V LVCMOS levels, thus the V_{DDIO} pins are connected to the 3.3 V rail. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.
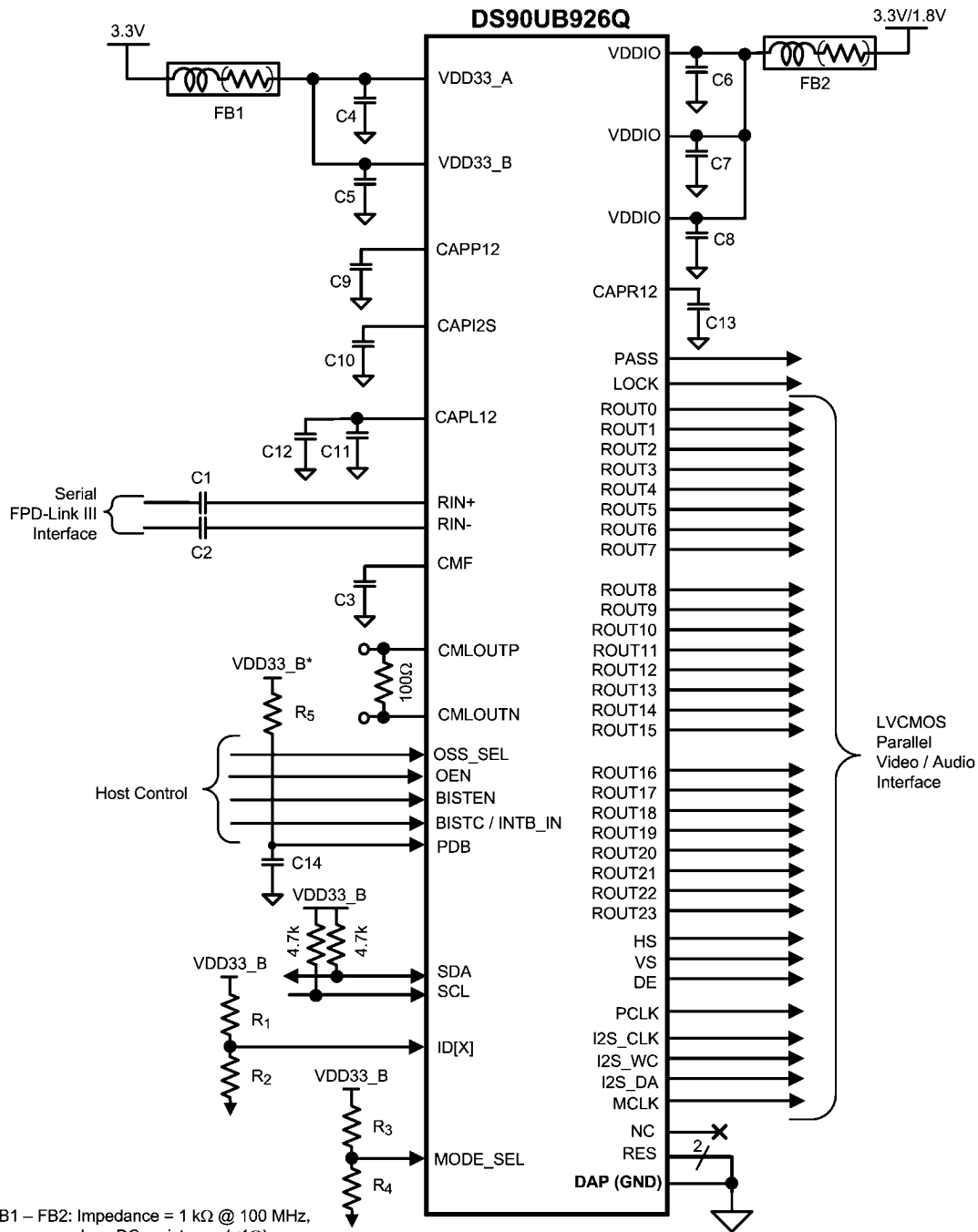
FIGURE 22. Typical Connection Diagram

POWER UP REQUIREMENTS AND PDB PIN

The VDDs (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the VDDs have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO} = 3.0V to 3.6V or V_{DD33}, it is recommended to use a 10 kΩ pull-up and a >10 uF cap to GND to delay the PDB input signal. All inputs must not be driven until V_{DD33} and V_{DDIO} has reached its steady state value.

TRANSMISSION MEDIA

The DS90UB925Q and DS90UB926Q chipset is intended to be used in a point-to-point configuration through a shielded twisted pair cable. The serializer and deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connector) between the serializer and deserializer should have a differential impedance of 100 Ohms. The maximum length of cable that can be used is dependant on the quality of the cable (gauge, impedance), connector, board (discontinuities, power plane), the electrical environment (e.g. power stability, ground noise, input clock jitter, PCLK frequency, etc.) and the application environment.

The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. The Receiver CML Monitor Driver Output Specifications define the acceptable data eye opening width and eye opening height. A differential probe should be used to measure across the termination resistor at the CMLOUT+/- pin *Figure 2* .

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the FPD-Link III devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the CML lines to prevent coupling from the LVCMOS lines to the CML lines. Closely-coupled differential lines of 100 Ohms are typically recommended for CML interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in TI Application Note: AN-1187.

CML INTERCONNECT GUIDELINES
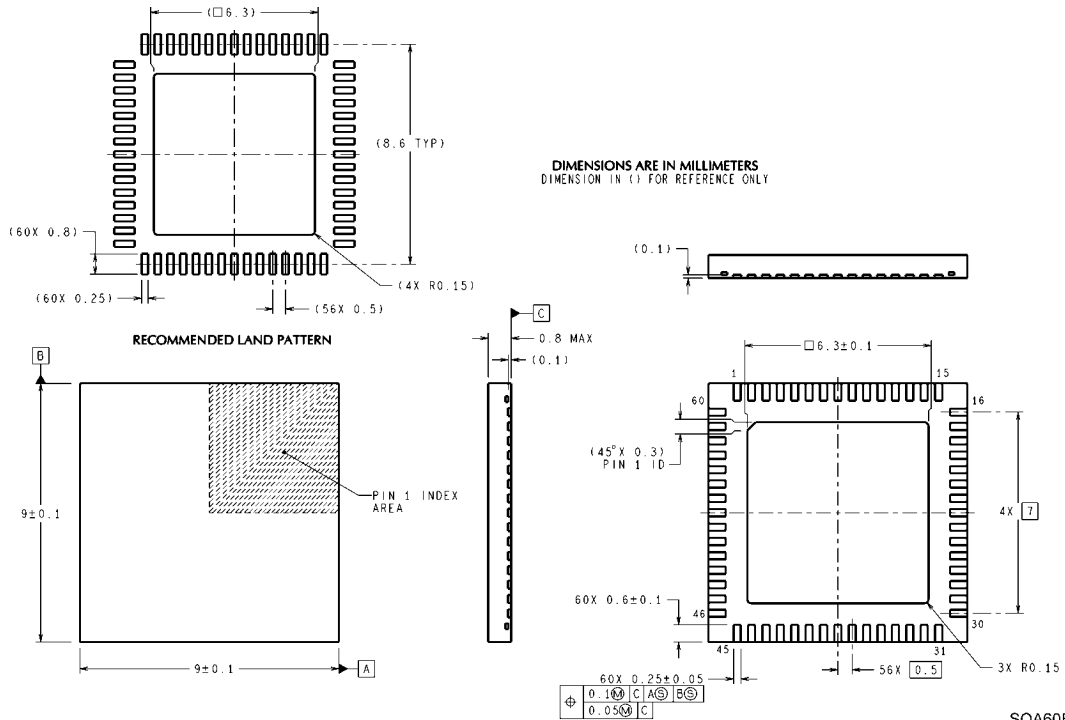
See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
    - S = space between the pair
    - 2S = space between pairs
    - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: **www.ti.com/lvds**

Revision

- **March 30, 2012**
  — Web release
- **July 19, 2012**
  — Converted to hybrid TI format
  — Corrected typo in table "DC and AC Serial Control Bus Characteristics" from VDDIO to VDD33
  — Added "Note: BIST is not available in backwards compatible mode."
  — Added Recommended FRC settings table

Physical Dimensions inches (millimeters) unless otherwise noted

60–pin LLP Package (9.0 mm X 9.0 mm X 0.8 mm, 0.5 mm pitch)
NS Package Number SQA60B

Notes

Notes

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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