DS90LV011AH High Temperature 3V LVDS Differential Driver

Check for Samples: DS90LV011AH

FEATURES

- **-40°C to 125°C Operating Temperature Range**
- **Conforms to TIA/EIA-644-A Standard**
- **>400Mbps (200MHz) Switching Rates**
- **700 ps (100 ps Typical) Maximum Differential Skew**
- **1.5 ns Maximum Propagation Delay**
- **Single 3.3V Power Supply**
- **±350 mV Differential Signaling**
- **Power Off Protection (Outputs in TRI-STATE)**
- **Pinout Simplifies PCB Layout**
- **Low Power Dissipation (23 mW @ 3.3V Typical)**
- **SOT-23 5-Lead Package**
- **Pin Compatible with SN65LVDS1**

DESCRIPTION

The DS90LV011AH is an LVDS driver optimized for high data rate and low power applications. The DS90LV011AH is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is designed to support data rates in excess of 400Mbps (200MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The device is offered in a 5-lead SOT-23 package. The LVDS outputs have been arranged for easy PCB layout. The differential driver outputs provide low EMI with its typical low output swing of 350 mV. The DS90LV011AH can be paired with its companion single line receiver, the DS90LT012AH, or with any of TI's LVDS receivers, to provide a high-speed LVDS interface.

Connection Diagram

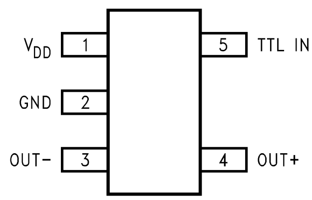
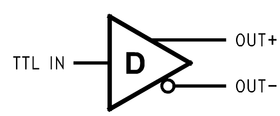


Figure 1. Top View
See Package Number DBV (R-PDSO-G5)

Functional Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)]

Supply Voltage (V_{DD})	−0.3V to +4V
LVCMOS input voltage (TTL IN)	−0.3V to +3.6V
LVDS output voltage (OUT±)	−0.3V to +3.9V
LVDS output short circuit current	24mA
Maximum Package Power Dissipation @ +25°C	
DBV Package	902 mW
Derate DBV Package	7.22 mW/°C above +25°C
Thermal resistance (θ_{JA})	138.5°C/Watt
Storage Temperature	−65°C to +150°C
Lead Temperature Range Soldering	
(4 sec.)	+260°C
Maximum Junction Temperature	+150°C
ESD Ratings	
HBM (1.5 kΩ, 100 pF)	≥ 9kV
EIAJ (0 Ω, 200 pF)	≥ 900V
CDM (0 Ω, 0 pF)	≥ 2000V
IEC direct (330 Ω, 150 pF)	≥ 4kV

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{DD})	3.0	3.3	3.6	V
Temperature (T_A)	−40	+25	+125	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.[(1)(2)(3)]

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
$\|V_{OD}\|$	Output Differential Voltage	$R_L = 100\Omega$ (Figure 2 and Figure 3)		OUT+, OUT−	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change					3	35	mV
V_{OS}	Offset Voltage	$R_L = 100\Omega$ (Figure 2)			1.125	1.22	1.375	V
ΔV_{OS}	Offset Magnitude Change				0	1	25	mV
I_{OFF}	Power-off Leakage	V_{OUT} = 3.6V or GND, V_{DD} = 0V				±1	±10	μA
I_{OS}	Output Short Circuit Current[(4)]	V_{OUT+} and V_{OUT-} = 0V				−6	−24	mA
I_{OSD}	Differential Output Short Circuit Current[(4)]	V_{OD} = 0V				−5	−12	mA
C_{OUT}	Output Capacitance					3		pF
V_{IH}	Input High Voltage			TTL IN	2.0		V_{DD}	V
V_{IL}	Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = 3.3V or 2.4V				±2	±10	μA
I_{IL}	Input Low Current	V_{IN} = GND or 0.5V				±1	±10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.6		V
C_{IN}	Input Capacitance					3		pF
I_{DD}	Power Supply Current	No Load	$V_{IN} = V_{DD}$ or GND	V_{DD}		5	8	mA
		$R_L = 100\Omega$				7	10	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.
(2) All typicals are given for: V_{DD} = +3.3V and T_A = +25°C.
(3) The DS90LV011AH is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified.[(1)(2)(3)(4)]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, C_L = 15 pF (Figure 4 and Figure 5)	0.3	1.0	1.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.3	1.1	1.5	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$[(5)]		0	0.1	0.7	ns
t_{SKD3}	Differential Part to Part Skew[(6)]		0	0.2	1.0	ns
t_{SKD4}	Differential Part to Part Skew[(7)]		0	0.4	1.2	ns
t_{TLH}	Transition Low to High Time		0.2	0.5	1.0	ns
t_{THL}	Transition High to Low Time		0.2	0.5	1.0	ns
f_{MAX}	Maximum Operating Frequency[(8)]		200	250		MHz

(1) All typicals are given for: V_{DD} = +3.3V and T_A = +25°C.
(2) These parameters are specified by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
(3) C_L includes probe and fixture capacitance.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_O = 50\Omega$, $t_r \le 1$ ns, $t_f \le 1$ ns (10%-90%).
(5) t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(6) t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
(7) t_{SKD4}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(8) f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%, V_{OD} > 250mV. The parameter is specified by design. The limit is based on the statistical analysis of the device over the PVT range by the transitions times (t_{TLH} and t_{THL}).

PARAMETER MEASUREMENT INFORMATION

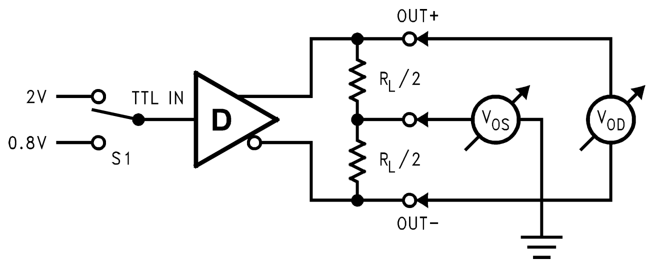


Figure 2. Differential Driver DC Test Circuit

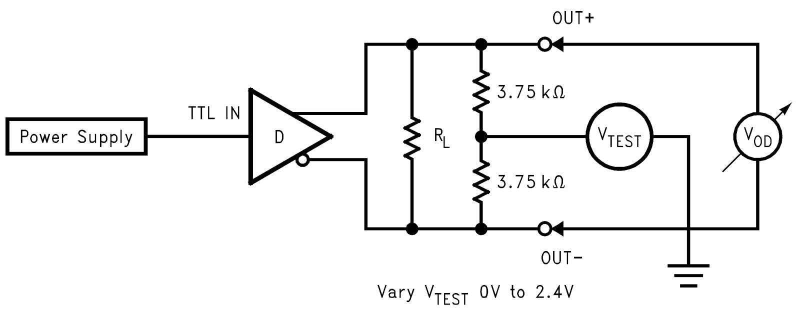


Figure 3. Differential Driver Full Load DC Test Circuit

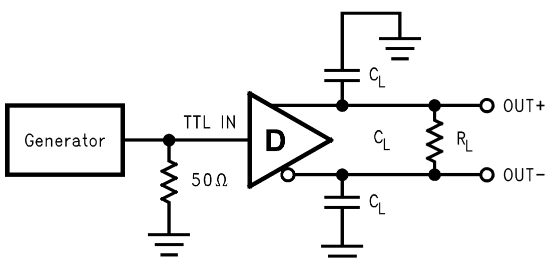


Figure 4. Differential Driver Propagation Delay and Transition Time Test Circuit

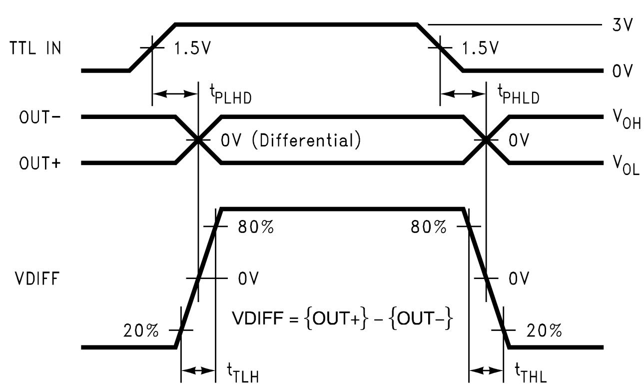


Figure 5. Differential Driver Propagation Delay and Transition Time Waveforms

APPLICATION INFORMATION

Table 1. Device Pin Descriptions

Package Pin Number	Pin Name	Description
SOT-23		
5	TTL IN	LVTTL/LVCMOS driver input pins
4	OUT+	Non-inverting driver output pin
3	OUT−	Inverting driver output pin
2	GND	Ground pin
1	V_{DD}	Power supply pin, +3.3V ± 0.3V
	NC	No connect

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV011AHMF/NOPB	NRND	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		N04	
DS90LV011AHMFX/NOPB	NRND	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		N04	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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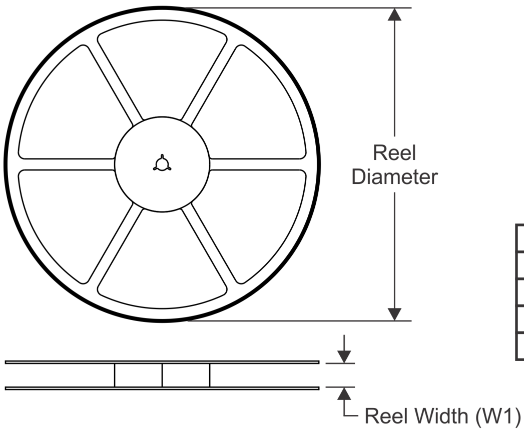
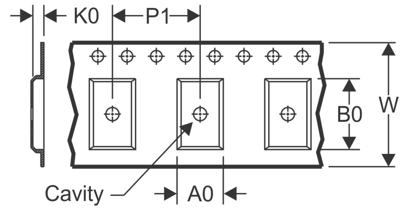
TAPE AND REEL INFORMATION

REEL DIMENSIONS

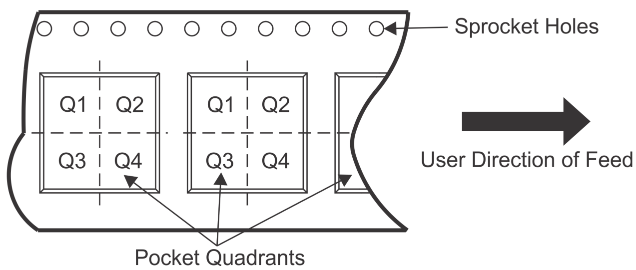


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

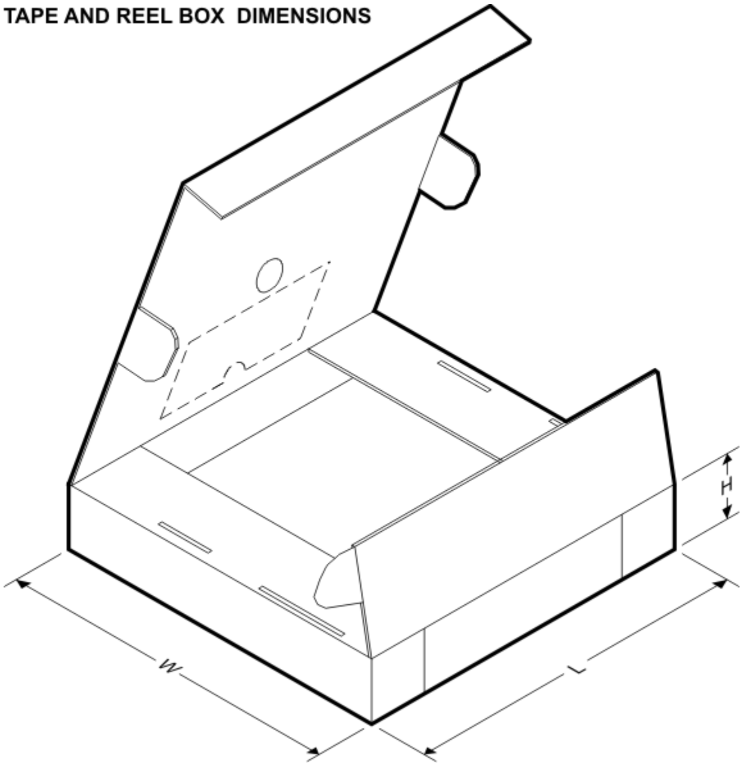
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV011AHMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DS90LV011AHMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

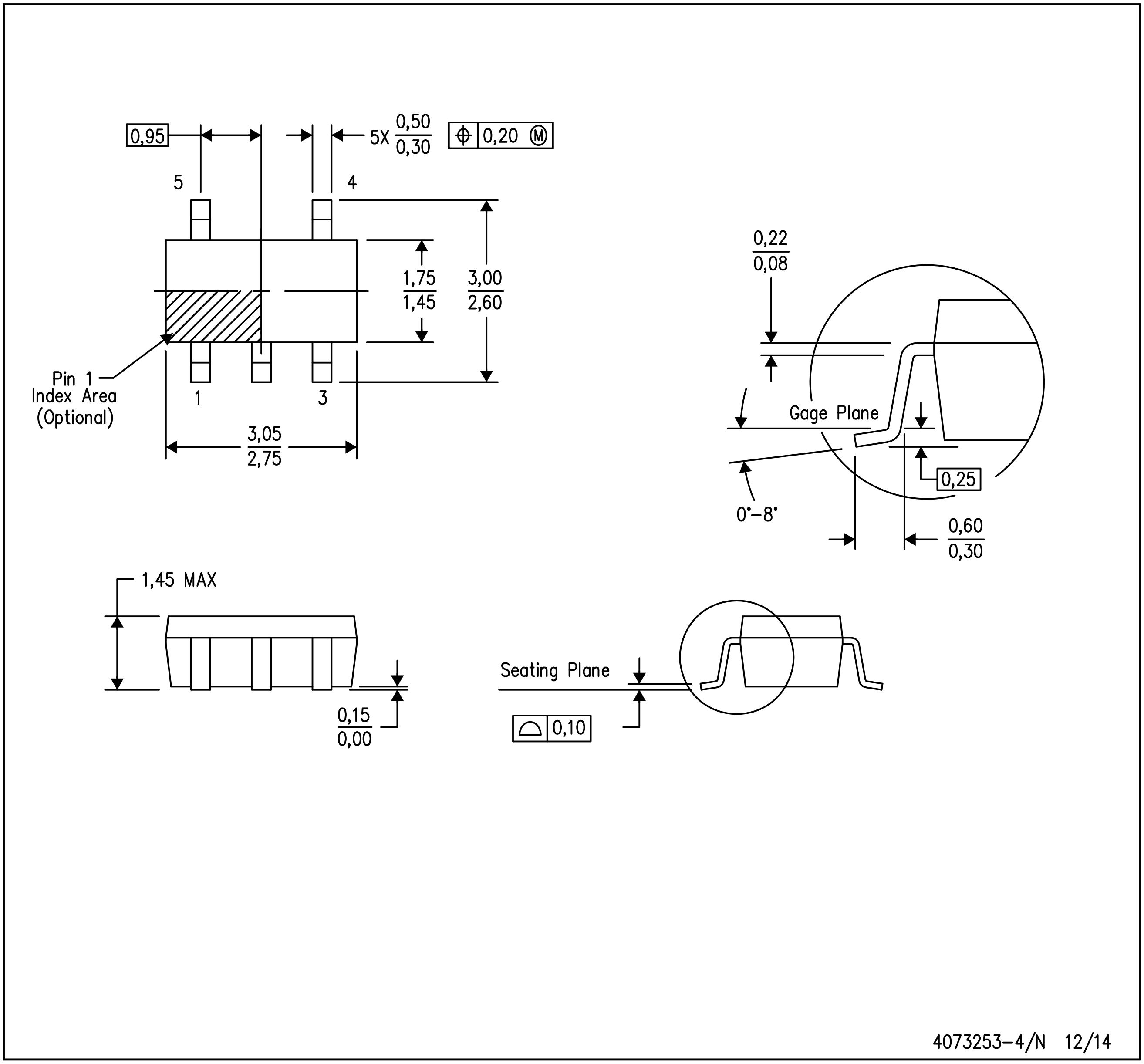
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

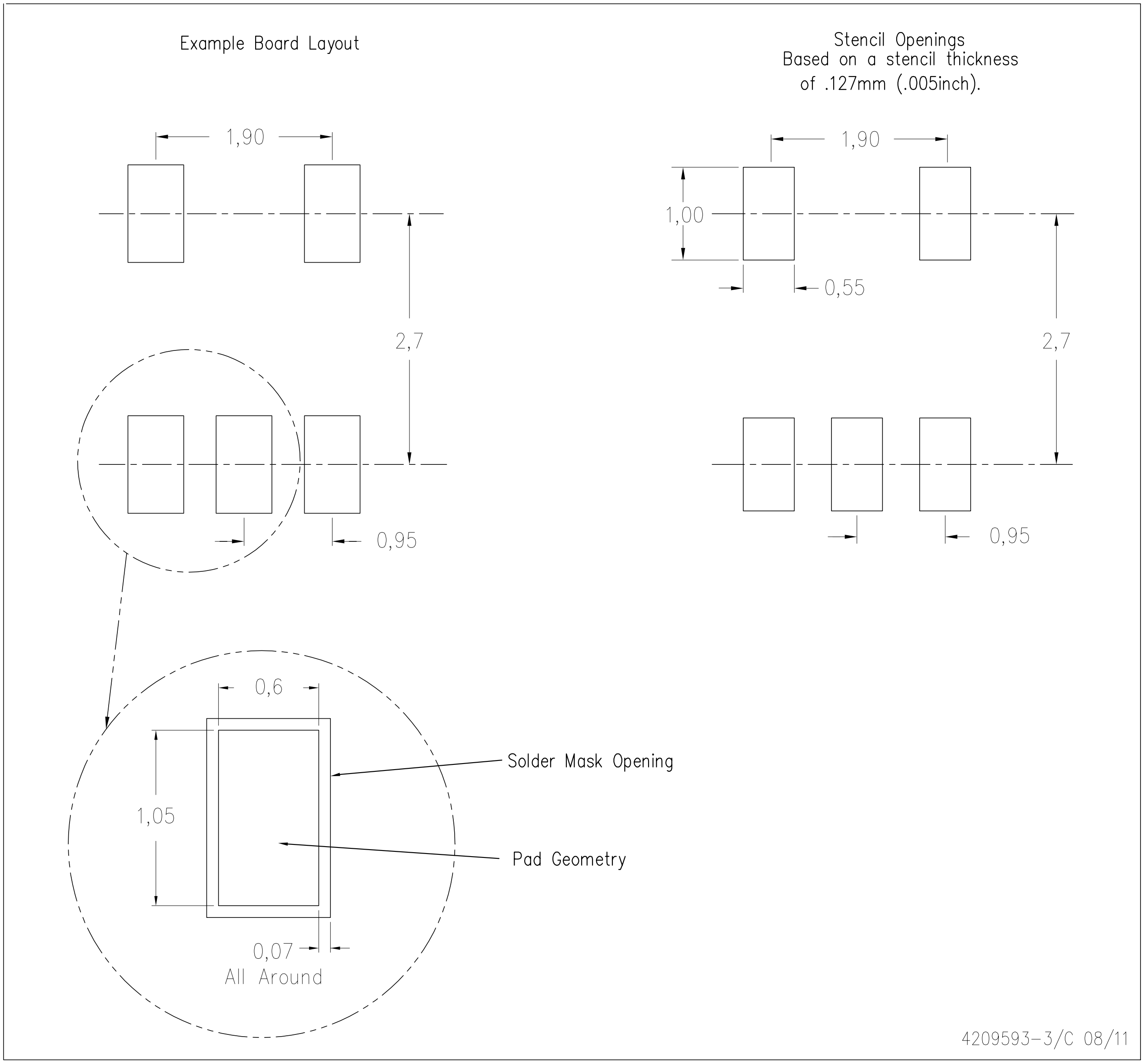
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV011AHMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
DS90LV011AHMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.