19-4835; Rev 6; 8/09

DS34T101/DS34T102/DS34T104/DS34T108
Single/Dual/Quad/Octal TDM-over-Packet Chip

General Description

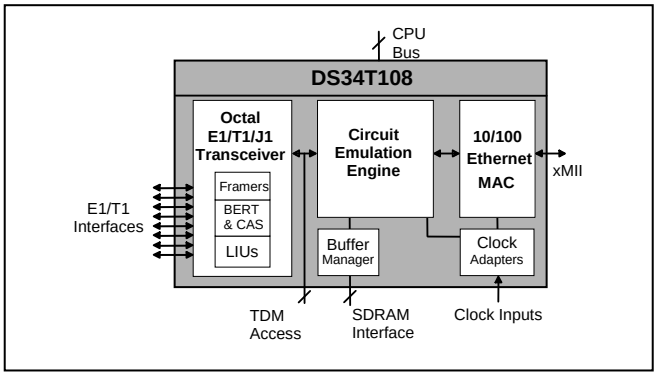
These IETF PWE3 SAToP/CESoPSN/TDMoIP/HDLC compliant devices allow up to eight E1, T1 or serial streams or one high-speed E3, T3, STS-1 or serial stream to be transported transparently over IP, MPLS or Ethernet networks. Jitter and wander of recovered clocks conform to G.823/G.824, G.8261, and TDM specifications. TDM data is transported in up to 64 individually configurable bundles. All standards-based TDM-over-packet mapping methods are supported except AAL2. Frame-based serial HDLC data flows are also supported. With built-in full-featured E1/T1 framers and LIUs. These ICs encapsulate the TDM-over-packet solution from analog E1/T1 signal to Ethernet MII while preserving options to make use of TDM streams at key intermediate points. The high level of integration available with the DS34T10x devices minimizes cost, board space, and time to market.

Applications

TDM Circuit Extension Over PSN
- o Leased-Line Services Over PSN
- o TDM Over GPON/EPON
- o TDM Over Cable
- o TDM Over Wireless

Cellular Backhaul Over PSN
Multiservice Over Unified PSN
HDLC-Based Traffic Transport Over PSN

Functional Diagram



Features

- ♦ **Full-Featured IC Includes E1/T1 LIUs and Framers, TDMoP Engine, and 10/100 MAC**
- ♦ **Transport of E1, T1, E3, T3 or STS-1 TDM or CBR Serial Signals Over Packet Networks**
- ♦ **Full Support for These Mapping Methods: SAToP, CESoPSN, TDMoIP (AAL1), HDLC, Unstructured, Structured, Structured with CAS**
- ♦ **Adaptive Clock Recovery, Common Clock, External Clock and Loopback Timing Modes**
- ♦ **On-Chip TDM Clock Recovery Machines, One Per Port, Independently Configurable**
- ♦ **Clock Recovery Algorithm Handles Network PDV, Packet Loss, Constant Delay Changes, Frequency Changes and Other Impairments**
- ♦ **64 Independent Bundles/Connections**
- ♦ **Multiprotocol Encapsulation Supports IPv4, IPv6, UDP, RTP, L2TPv3, MPLS, Metro Ethernet**
- ♦ **VLAN Support According to 802.1p and 802.1Q**
- ♦ **10/100 Ethernet MAC Supports MII/RMII/SSMII**
- ♦ **Selectable 32-Bit, 16-Bit or SPI Processor Bus**
- ♦ **Operates from Only Two Clock Signals, One for Clock Recovery and One for Packet Processing**
- ♦ **Glueless SDRAM Buffer Management**
- ♦ **Low-Power 1.8V Core, 3.3V I/O**

See detailed feature list in Section 5.

Ordering Information

PART	PORTS	TEMP RANGE	PIN-PACKAGE
DS34T101GN	1	-40°C to +85°C	484 TEBGA
DS34T101GN+	1	-40°C to +85°C	484 TEBGA
DS34T102GN	2	-40°C to +85°C	484 TEBGA
DS34T102GN+	2	-40°C to +85°C	484 TEBGA
DS34T104GN	4	-40°C to +85°C	484 TEBGA
DS34T104GN+	4	-40°C to +85°C	484 TEBGA
DS34T108GN	8	-40°C to +85°C	484 HSBGA
DS34T108GN+	8	-40°C to +85°C	484 HSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package (explanation).

1 Applicable Standards

Table 1-1. Applicable Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102	*Digital Hierarchy—Electrical Interfaces*, 1993
T1.107	*Digital Hierarchy—Formats Specification*, 1995
T1.231.02	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*, 2003
T1.403	*Network and Customer Installation Interfaces—DS1 Electrical Interface*, 1999
AT&T	
TR54016	*Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Superframe Format* (9/1989)
TR62411	*ACCUNET® T1.5 Service Description and Interface Specification* (12/1990)
ETSI	
ETS 300 011	*Integrated Services Digital Network (ISDN); Primary rate User Network Interface (UNI); Part 1: Layer 1 Specification* V1.2.2 (2000-05)
ETS 300 166	*Transmission and Multiplexing (TM); Physical and Electrical Characteristics of Hierarchical Digital Interfaces for Equipment Using the 2 048 kbit/s - Based Plesiochronous or Synchronous Digital Hierarchies* V1.2.1 (2001-09)
ETS 300 233	*Integrated Services Digital Network (ISDN);Access Digital Section for ISDN Primary Rate, ed.1* (1994-05)
IEEE	
IEEE 802.3	*Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications* (2005)
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
IETF	
RFC 4553	*Structure-Agnostic Time Division Multiplexing (TDM) over Packet (SAToP)* (06/2006)
RFC 4618	*Encapsulation Methods for Transport of PPP/High-Level Data Link Control (HDLC) over MPLS Networks* (09/2006)
RFC 5086	*Structure-Aware Time Division Multiplexed (TDM) Circuit Emulation Service over Packet Switched Network (CESoPSN)* (12/2007)
RFC 5087	*Time Division Multiplexing over IP (TDMoIP)* (12/2007)
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces* (11/2001)
G.704	*Synchronous Frame Structures Used at 1544, 6312, 2048, 8448 and 44736 kbit/s Hierarchical Levels* (10/1998)
G.706	*Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704* (1991)
G.732	*Characteristics of primary PCM Multiplex Equipment Operating at 2048Kbit/s* (11/1988)
G.736	*Characteristics of Synchronous Digital Multiplex Equipment Operating at 2048Kbit/s (03/1993)*
G.775	*Loss of Signal (LOS) and Alarm Indication Signal (AIS) and Remote Defect Indication (RD) Defect Detection and Clearance Criteria for PDH Signals* (10/1998)
G.823	*The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy* (03/2000)
G.824	*The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy* (03/2000)
G.8261/Y.1361	*Timing and Synchronization Aspects in Packet Networks* (05/2006)
I.363.1	*B-ISDN ATM Adaptation Layer Specification: Type 1 AAL* (08/1996)
I.363.2	*B-ISDN ATM Adaptation Layer Specification: Type 2 AAL* (11/2000)
I.366.2	*AAL Type 2 Service Specific Convergence Sublayer for Narrow-Band Services* (11/2000)
I.431	*Primary rate user-network interface - Layer 1 specification* (03/1993)
I.432	*B-ISDN User-Network Interface – Physical Layer Specification (03/1993)*
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above* (1992)

SPECIFICATION	SPECIFICATION TITLE
O.161	*In-Service Code Violation Monitors for Digital Systems* (1993)
Y.1413	*TDM-MPLS Network Interworking – User Plane Interworking* (03/2004)
Y.1414	*Voice Services–MPLS Network Interworking* (07/2004)
Y.1452	*Voice Trunking over IP Networks* (03/2006)
Y.1453	*TDM-IP Interworking – User Plane Networking* (03/2006)
MEF	
MEF 8	*Implementation Agreement for the Emulation of PDH Circuits over Metro Ethernet Networks* (10/2004)
MFA	
MFA 4.0	*TDM Transport over MPLS Using AAL1* (06/2003)
MFA 5.0.0	*I.366.2 Voice Trunking Format over MPLS Implementation Agreement (08/2003)*
MFA 8.0.0	*Emulation of TDM Circuits over MPLS Using Raw Encapsulation – Implementation Agreement* (11/2004)

2 Detailed Description

The DS34T108 is an 8-port device integrating a sophisticated multiport TDM-over-Packet (TDMoP) core and eight full-featured, independent, software-configurable E1/T1 transceivers. The DS34T104, DS34T102 and DS34T101 have the same functionality as the DS34T108, except they have only 4, 2 or 1 ports and transceivers, respectively. Each E1/T1 transceiver is composed of a line interface unit (LIU), a framer, an elastic store, an HDLC controller and a bit error rate tester (BERT) block. These transceivers connect seamlessly to the TDMoP block to form a complete solution for mapping and demapping E1/T1 to and from IP, MPLS or Ethernet networks. A MAC built into the TDMoP block supports connectivity to a single 10/100 Mbps PHY over an MII, RMII or SSMII interface. The DS34T10x devices are controlled through a 16 or 32-bit parallel bus interface or a high-speed SPI serial interface.

TDM-over-Packet Core

The TDM-over-Packet (TDMoP) core is the enabling block for circuit emulation and other network applications. It performs transparent transport of legacy TDM traffic over Packet Switched-Networks (PSN). The TDMoP core implements payload mapping methods such as AAL1 for circuit emulation, HDLC method, structure-agnostic SAToP method, and the structure-aware CESoPSN method.

The AAL1 payload-type machine maps and demaps E1, T1, E3, T3, STS-1 and other serial data flows into and out of IP, MPLS or Ethernet packets, according to the methods described in ITU-T Y.1413, Y.1453, MEF 8, MFA 4.1 and IETF RFC 5087 (TDMoIP). It supports E1/T1 structured mode with or without CAS, using a timeslot size of 8 bits, or unstructured mode (carrying serial interfaces, unframed E1/T1 or E3/T3/STS-1 traffic).

The HDLC payload-type machine maps and demaps HDLC dataflows into and out of IP/MPLS packets according to IETF RFC 4618 (excluding clause 5.3 – PPP) and IETF RFC 5087 (TDMoIP). It supports 2-, 7- and 8-bit timeslot resolution (i.e. 16, 56, and 64 kbps respectively), as well as N × 64 kbps bundles (n=1 to 32). Supported applications of this machine include trunking of HDLC-based traffic (such as Frame Relay) implementing Dynamic Bandwidth Allocation over IP/MPLS networks and HDLC-based signaling interpretation (such as ISDN D-channel signaling termination – BRI or PRI, V5.1/2, or GR-303).

The SAToP payload-type machine maps and demaps unframed E1, T1, E3 or T3 data flows into and out of IP, MPLS or Ethernet packets according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 4553. It supports E1/T1/E3/T3 with no regard for the TDM structure. If TDM structure exists it is ignored, allowing this to be the simplest mapping/demapping method. The size of the payload is programmable for different services. This emulation suits applications where the provider edges have no need to interpret TDM data or to participate in the TDM signaling. The PSN network must have almost no packet loss and very low packet delay variation (PDV) for this method.

The CESoPSN payload-type machine maps and demaps structured E1, T1, E3 or T3 data flows into and out of IP, MPLS or Ethernet packets with static assignment of timeslots inside a bundle according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and the IETF RFC 5086 (CESoPSN). It supports E1/T1/E3/T3 while taking into account the TDM structure. The level of structure must be chosen for proper payload conversion such as the framing type (i.e. frame or multiframe). This method is less sensitive to PSN impairments but lost packets could still cause service interruption.

E1/T1 Transceivers

The LIU in each transceiver is composed of a transmitter, a receiver and a jitter attenuator. Internal software configurable impedance matching is provided for both transmit and receive paths, reducing external component count. The transmit interface is responsible for generating the necessary waveshapes for driving the E1/T1 twisted pair or coax cable and providing the correct source impedance depending on the type of cable used. T1 waveform generation includes DSX–1 line build-outs as well as CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides the correct line termination and recovers clock and data from the incoming line. The receive sensitivity adjusts automatically to the incoming signal level and can be programmed for 0dB to -43dB or 0dB to -12dB for E1 applications and 0dB to -15dB or 0dB to -36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator can be placed in either the transmit or receive path and requires only a T1- or E1-rate reference clock, which is typically synthesized by the CLAD1 block from a common reference frequency of 10MHz, 19.44MHz, 38.88MHz or 77.76MHz.

In the framer block, the transmit formatter takes data from the TDMoP core, inserts the appropriate framing patterns and alarm information, calculates and inserts CRC codes, and provides the HDB3 or B8ZS encoding (zero code suppression) and AMI line coding. The receive framer decodes AMI, HDB3 and B8ZS line coding, finds frame and multiframe alignment in the incoming data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock, data, and frame-sync signals to the TDMoP core.

Both transmit and receive paths have built-in HDLC controller and BERT blocks. The HDLC blocks can be assigned to any timeslot, a portion of a timeslot or to the FDL (T1) or Sa bits (E1). Each controller has 64-byte FIFOs, reducing the amount of processor overhead required to manage the flow of data. The BERT blocks can generate and synchronize with pseudo-random and repetitive patterns, insert errors (singly or at a constant error rate) and detect and count errors to calculate bit error rates.

3 Application Examples

In Figure 3-1, a DS34T10x device is used in each TDMoP gateway to map TDM services into a packet-switched metropolitan network. TDMoP data is carried over various media: fiber, wireless, G/EPON, coax, etc.

Figure 3-1. TDMoP in a Metropolitan Packet Switched Network

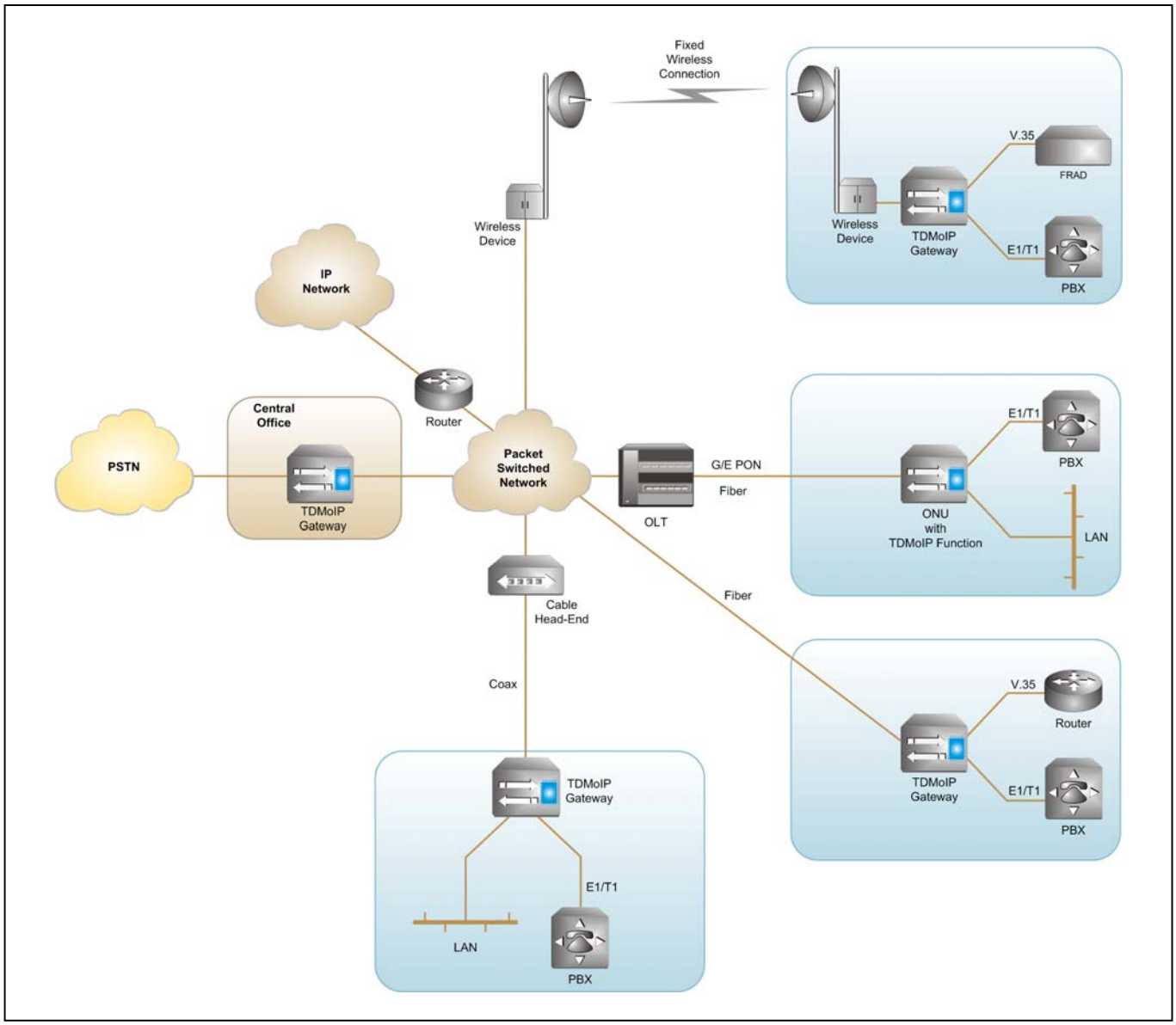
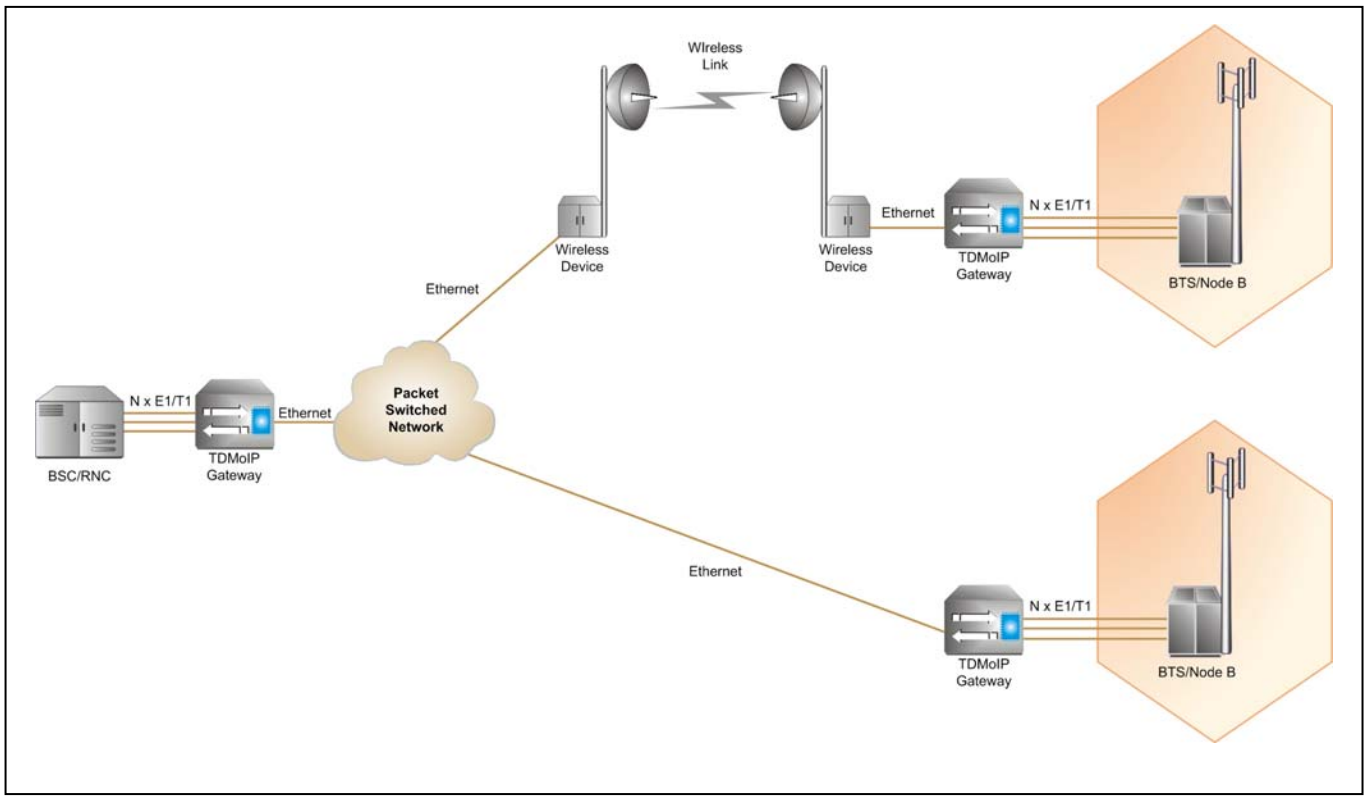


Figure 3-2. TDMoP in Cellular Backhaul



Other Possible Applications

Point-to-Multipoint TDM Connectivity over IP/Ethernet

The DS34T10x devices support NxDS0 TDMoP connections (known as bundles) with or without CAS (Channel Associated Signaling). There is no need for an external TDM cross-connect, since the packet domain can be used as a virtual cross-connect. Any bundle of timeslots can be directed to another remote location on the packet domain.

HDLC Transport over IP/MPLS

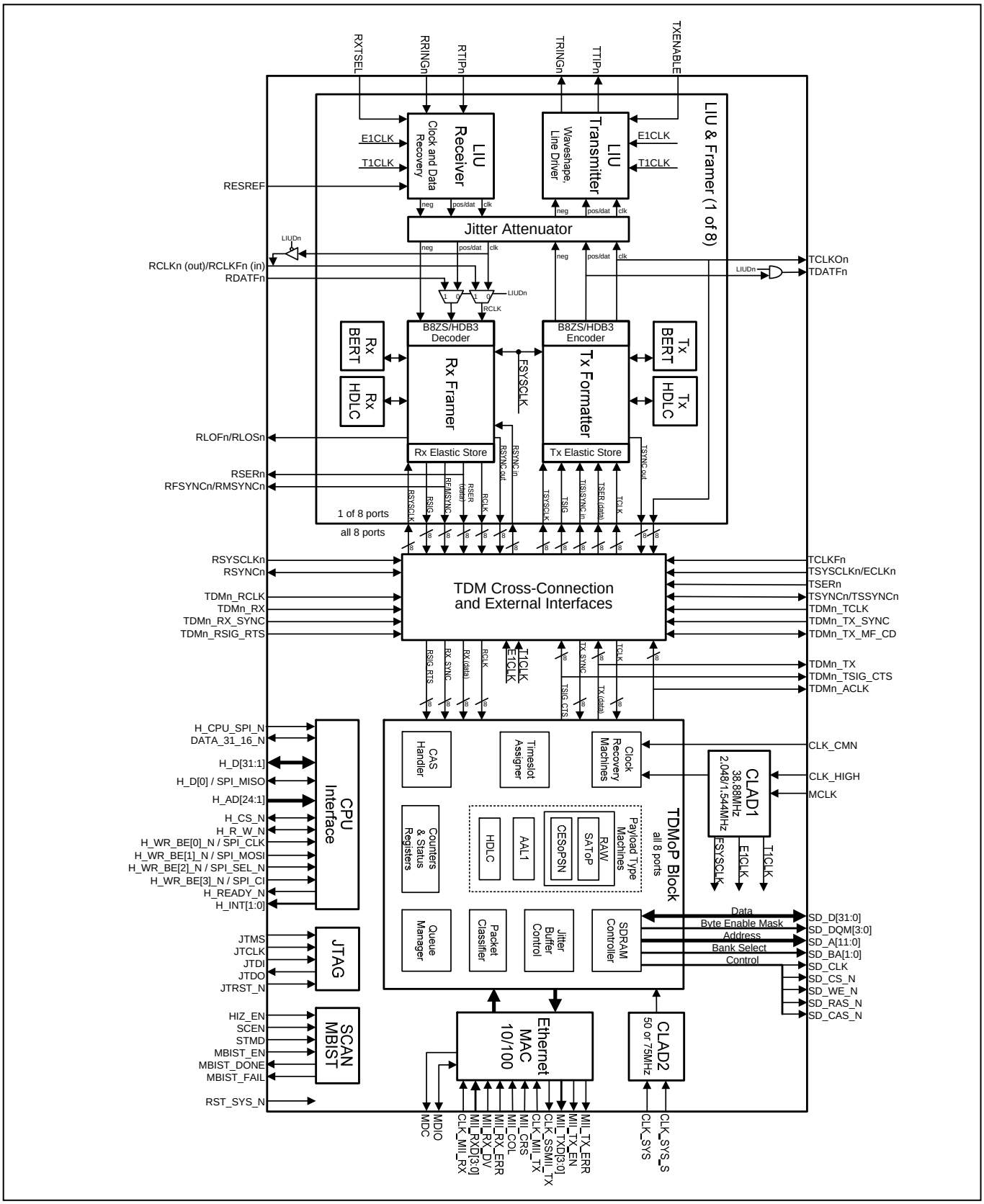
TDM traffic streams often contain HDLC-based control channels and data traffic. These data streams, when transported over a packet domain, should be treated differently than the time-sensitive TDM payload. DS34T10x devices can terminate HDLC channels in the TDM streams and optionally map them into IP/MPLS/Ethernet for transport. All HDLC-based control protocols (ISDN BRI and PRI, SS7 etc.) and all HDLC data traffic can be managed and transported.

Using a Packet Backplane for Multiservice Concentrators

A communications device with all the above-mentioned capabilities can use a packet-based backplane instead of the more expensive TDM bus option. This enables a cost-effective and future-proof design of communication platforms with full support for both legacy and next-generation services.

4 Block Diagram

Figure 4-1. Top-Level Block Diagram



5 Features

Global Features

- TDMoP Interfaces
  - DS34T101: 1 E1/T1 LIU/Framer/TDMoP interface
  - DS34T102: 2 E1/T1 LIUs/Framers/TDMoP interfaces
  - DS34T104: 4 E1/T1 LIUs/Framers/TDMoP interfaces
  - DS34T108: 8 E1/T1 LIUs/Framers/TDMoP interfaces
  - All four devices: optionally 1 high-speed E3/DS3/STS-1 TDMoP interface
  - All four devices: each interface optionally configurable for serial operation for V.35 and RS530
- Ethernet Interface
  - One 10/100 Mbps port configurable for MII, RMII or SSMII interface format
  - Half or full duplex operation
  - VLAN support according to 802.1p and 802.1Q including stacked tags
  - Fully compatible with IEEE 802.3 standard
- End-to-end TDM synchronization through the IP/MPLS domain by on-chip, per-port TDM clock recovery
- 64 independent bundles/connections, each with its own:
  - Transmit and receive queues
  - Configurable jitter-buffer depth
  - Connection-level redundancy, with traffic duplication option
- Flexible on-chip cross-connection capability
  - Internal bundle cross-connect capability, with DS0 resolution
  - Any framer receiver port to any TDMoP block receive interface to maintain bundle connectivity
  - Any TDMoP block transmit interface to any framer transmit port to maintain bundle connectivity
- Packet loss compensation and handling of misordered packets
- Glueless SDRAM interface
- Complies with MPLS-Frame Relay Alliance Implementation Agreements 4.1, 5.1 and 8.0
- Complies with ITU-T standards Y.1413 and Y.1414.
- Complies with Metro Ethernet Forum 3 and 8
- Complies with IETF RFC 4553 (SAToP), RFC 5086 (CESoPSN) and RFC 5087 (TDMoIP)
- IEEE 1146.1 JTAG boundary scan
- 1.8V and 3.3V Operation with 5.0V tolerant I/O

Clock Synthesizers

- Clocks to operate LIUs, jitter attenuators, framers, BERTs and HDLC controllers can be synthesized from a single clock input for both E1 and T1 operation (10MHz, 19.44MHz, 38.88MHz or 77.76MHz on the CLK_HIGH pin or 1.544MHz or 2.048MHz on the MCLK pin)
- Clocks to operate the TDMoP clock recovery machines can synthesized from a single clock input (10MHz, 19.44MHz, 38.88MHz or 77.76MHz on the CLK_HIGH pin)
- Clock to operate TDMoP logic and SDRAM interface (50MHz or 75MHz) can be synthesized from a single 25MHz clock on the CLK_SYS pin

Line Interface Units (LIUs)

- Receives E1, T1 and G.703 2048kHz synchronization signal
- Fully software configurable including software-selectable internal Tx and Rx termination
- Suitable for both short-haul and long-haul applications
- Receive sensitivity options from (0dB to -12dB) to (0dB to -43dB) for E1 and to (0dB to -36dB) for T1
- Receive signal level indication: 0dB to -37.5dB
- Internal receive termination options for 75Ω, 100Ω, 110Ω, and 120Ω lines
- Receive monitor-mode gain settings of 14dB, 20dB, 26dB, and 32dB
- Flexible transmit waveform generation

- T1 DSX-1 line build-outs
- T1 CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted-pair cables
- Several local and remote loopback options including simultaneous local and remote
- Analog loss of signal detection
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Receiver power-down
- Transmitter power-down
- Transmitter short-circuit limiter with current limit exceeded indication
- Transmit open-circuit-detected indication

Jitter Attenuator

- Crystal-less jitter attenuator with programmable buffer depth (16, 32, 64 or 128 bits)
- Can be placed in either the receive path or the transmit path or disabled
- Limit trip indication

Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 SF and ESF framing formats per T1.403, and expanded SLC-96 support (TR-TSY-008).
- E1 FAS framing, CRC-4 multiframe per G.704/G.706, and G.732 CAS multiframe
- Transmit-side synchronizer
- Transmit midpath CRC recalculate (E1)
- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters
  - T1: BPV, CV, CRC-6 and framing bit errors
  - E1: BPV, CV, CRC-4, E-bit and frame alignment errors
  - Timed or manual counter update modes
- T1 Idle Code Generation on a per-channel basis in both transmit and receive paths
  - User defined code generation
  - Digital Milliwatt code generation
- ANSI T1.403-1999 support
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors for loop-up and loop-down codes
- Bit Oriented Code (BOC) support
- Software and hardware signaling support
- Interrupt generation on change of signaling data
- Optional receive signaling freeze on loss-of-frame, loss-of-signal, or frame slip
- Hardware pins provided to indicate loss-of-frame (LOF) or loss-of-signal (LOS)
- Automatic RAI generation to ETS 300 011 specifications
- RAI-CI and AIS-CI support
- Expanded access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support

- Ability to calculate and check CRC-6 according to the Japanese standard
- Ability to generate RAI (yellow alarm) according to the Japanese standard
- T1 to E1 conversion

Framer/Formatter TDM Interface

- Independent two-frame receive and transmit elastic stores
- Independent control and clocking
- Controlled slip capability with status
- Support for T1-to-E1 conversion
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz TDM mode
- Hardware signaling capability
- Receive signaling reinsertion
- Availability of signaling in a separate signal pin
- BERT testing to the system interface

TDM-over-Packet Block

- Enables transport of TDM services (E1, T1, E3, T3, STS-1) or serial data over packet-switched networks
- SAToP payload-type machine maps/demaps unframed E1/T1/E3/T3/STS-1 or serial data flows to/from IP, MPLS or Ethernet packets according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 4553.
- CESoPSN payload-type machine maps/demaps structured E1/T1 data flows to/from IP, MPLS or Ethernet packets with static assignment of timeslots inside a bundle according to ITU-T Y.1413, Y.1453, MEF 8, MFA 8.0.0 and IETF RFC 5086.
- AAL1 payload-type machine maps/demaps E1/T1/E3/T3/STS-1 or serial data flows to/from IP, MPLS or Ethernet packets according to ITU-T Y.1413, MEF 8, MFA 4.1 and IETF RFC 5087. For E1/T1 it supports structured mode with/without CAS using 8-bit timeslot resolution, while implementing static timeslot allocation. For E1/T1, E3/T3/STS-1 or serial interface it supports unstructured mode.
- HDLC payload-type machine maps/demaps HDLC-based E1/T1/serial flow to/from IP, MPLS or Ethernet packets. It supports 2-, 7- and 8-bit timeslot resolution (i.e. 16, 56, and 64 kbps respectively), as well as N x 64 kbps bundles. This is useful in applications where HDLC-based signaling interpretation is required (such as ISDN D channel signaling termination, V.51/2, or GR-303), or for trunking packet-based applications (such as Frame Relay), according to IETF RFC 4618.

TDMoP TDM Interfaces

- Supports single high-speed E3, T3 or STS-1 interface on port 1 or one (DS34T101), two (DS34T102), four (DS34T104) or eight (DS34T108) E1, T1 or serial interfaces
- For single high-speed E3, T3 or STS-1 interface, AAL1 or SAToP payload type is used
- For E1 or T1 interfaces, the following modes are available:
    - Unframed – E1/T1 pass-through mode (AAL1, SAToP or HDLC payload type)
    - Structured – fractional E1/T1 support (all payloads)
    - Structured with CAS – fractional E1/T1 with CAS support (CESoPSN or AAL1 payload type)
- For serial interfaces, the following modes are available:
    - Arbitrary continuous bit stream (using AAL1 or SAToP payload type)
    - Single-interface high-speed mode on port 1 up to STS-1 rate (51.84 Mbps) using a single bundle/connection.
    - Low-speed mode with each interface operating at N x 64 kbps (N = 1 to 63) with an aggregate rate of 18.6Mbps
    - HDLC-based traffic (such as Frame Relay) at N x 64 kbps (N = 1 to 63) with an aggregate rate of 18.6Mbps).
- All serial interface modes are capable of working with a gapped clock.

TDMoP Bundles

- 64 independent bundles, each can be assigned to any TDM interface
- Each bundle carries a data stream from one TDM interface over IP/MPLS/Ethernet PSN from TDMoP source device to TDMoP destination device
- Each bundle may be for N x 64kbps, an entire E1, T1, E3, T3 or STS-1, or an arbitrary serial data stream
- Each bundle is uni-directional (but frequently coupled with opposite-direction bundle for bidirectional communication)
- Multiple bundles can be transported between TDMoP devices
- Multiple bundles can be assigned to the same TDM interface
- Each bundle is independently configured with its own:
    - Transmit and receive queues
    - Configurable receive-buffer depth
    - Optional connection-level redundancy (SAToP, AAL1, CESoPSN only).
- Each bundle can be assigned to one of the payload-type machines or to the CPU
- For E1/T1 the device provides internal bundle cross-connect functionality, with DS0 resolution

TDMoP Clock Recovery

- Sophisticated TDM clock recovery machines, one for each TDM interface, allow end-to-end TDM clock synchronization, despite the packet delay variation of the IP/MPLS/Ethernet network
- The following clock recovery modes are supported:
    - Adaptive clock recovery
    - Common clock (using RTP)
    - External clock
    - Loopback clock
- The clock recovery machines provide both fast frequency acquisition and highly accurate phase tracking:
    - Jitter and wander of the recovered clock are maintained at levels that conform to G.823/G.824 traffic or synchronization interfaces. (For adaptive clock recovery, the recovered clock performance depends on packet network characteristics.)
    - Short-term frequency accuracy (1 second) is better than 16 ppb (using OCXO reference), or 100 ppb (using TCXO reference)
    - Capture range is ±90 ppm
    - Internal synthesizer frequency resolution of 0.5 ppb
    - High resilience to packet loss and misordering, up to 2% without degradation of clock recovery performance
    - Robust to sudden significant constant delay changes
    - Automatic transition to holdover when link break is detected

TDMoP Delay Variation Compensation

- Configurable jitter buffers compensate for delay variation introduce by the IP/MPLS/Ethernet network
- Large maximum jitter buffer depths:
    - E1: up to 256 ms
    - T1 unframed: up to 340 ms
    - T1 framed: up to 256 ms
    - T1 framed with CAS: up to 192 ms
    - E3: up to 60 ms
    - T3: up to 45 ms
    - STS-1: up to 40 ms.
- Packet reordering is performed for SAToP and CESoPSN bundles within the range of the jitter buffer
- Packet loss is compensated by inserting either a pre-configured conditioning value or the last received value.

TDMoP CAS Support

- On-chip CAS handler terminates E1/T1 CAS when using AAL1/CESoPSN in structured-with-CAS mode.
- CPU intervention is not required for CAS handling.

Test and Diagnostics

- IEEE 1149.1 JTAG support
- Per-channel programmable on-chip bit error-rate testing (BERT)
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Error insertion single and continuous
- Total-bit and errored-bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 and E1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel loopback)
- MBIST (memory built-in self test)

CPU Interface

- 32 or 16-bit parallel interface or optional SPI serial interface
- Byte write enable pins for single-byte write resolution
- Hardware reset pin
- Software reset supported
- Software access to device ID and silicon revision
- On-chip SDRAM controller provides access to SDRAM for both the chip and the CPU
- CPU can access transmit and receive buffers in SDRAM used for packets to/from the CPU (ARP, SNMP, etc.)

6 Pin Descriptions

Table 6-1. Short Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
Internal E1/T1 LIU Line Interface		
TXENABLE	I	LIU Transmit Enable Input (for all LIUs)
TTIPn, TRINGn	Oa	LIU Transmitter Analog Outputs
RTIPn, RRINGn	Ia	LIU Receiver Analog Inputs
RXTSEL	I	Receive Termination Selection Input (for All LIUs)
RESREF	I	Reference Resistor for LIU Analog Circuits (precision 10kΩ to ARVSS)
External E1/T1 LIU Interface		
TCLKOn	O	Transmit Clock Output
TDATFn	O	Transmit Data Output
RCLKFn / RCLKn	IO	Receive Clock Input to Framer (RCLKFn) or Recovered Clock Output from LIU Receiver (RCLKn)
RDATFn	I	Receive Data Input to Framer
Framer TDM Interface		
TCLKFn	I	Transmit Clock Input to Formatter
TSYSCLKn / ECLKn	I	Transmit System Clock Input (clock for cross-connect side of elastic store) or External Reference Clock Input
TSERn	I	Transmit Serial Data Input
TSYNCn / TSSYNCn	IO	Transmit Frame/Multiframe Sync Input/Output or Transmit System Frame/Multiframe Sync Input (sync for cross-connect side of elastic store)
RSYSCLKn	I	Receive System Clock Input (clock for cross-connect side of elastic store)
RSERn	O	Receive Serial Data Output
RSYNCn	IO	Receive Frame/Multiframe Sync Input/Output
RFSYNCn/ RMSYNCn	O	Receive Frame Sync or Receive Multiframe Sync Output
RLOFn/ RLOSn	O	Receive Loss of Frame Output or Receive Loss of Signal Output
TDM-over-Packet Engine TDM Interface		
TDMn_ACLK	O	TDMoP Recovered Clock Output
TDMn_TCLK	Ipu	TDMoP Transmit Clock Input (here transmit means “toward LIU”)
TDMn_TX	O	TDMoP Transmit Data Output
TDMn_TX_SYNC	Ipd	TDMoP Transmit Frame Sync Input
TDMn_TX_MF_CD	IOpd	TDMoP Transmit Multiframe Sync Input or Carrier Detect Output
TDMn_TSIG_CTS	O	TDMoP Transmit Signaling Output or Clear to Send Output
TDMn_RCLK	Ipu	TDMoP Receive Clock Input (here receive means “toward Ethernet MII”)
TDMn_RX	Ipu	TDMoP Receive Data Input
TDMn_RX_SYNC	Ipd	TDMoP Receive Frame/Multiframe Sync Input
TDMn_RSIG_RTS	Ipu	TDMoP Receive Signaling Input or Request To Send Input
SDRAM Interface		
SD_CLK	O	SDRAM Clock
SD_D[31:0]	IO	SDRAM Data Bus
SD_DQM[3:0]	O	SDRAM Byte Enable Mask
SD_A[11:0]	O	SDRAM Address Bus
SD_BA[1:0]	O	SDRAM Bank Select Outputs
SD_CS_N	O	SDRAM Chip Select (Active Low)
SD_WE_N	O	SDRAM Write Enable (Active Low)
SD_RAS_N	O	SDRAM Row Address Strobe (Active Low)
SD_CAS_N	O	SDRAM Column Address Strobe (Active Low)
Ethernet PHY Interface (MII/RMII/SSMII)		
CLK_MII_TX	I	MII Transmit Clock Input
CLK_SSMII_TX	O	SSMII Transmit Clock Output
MII_TXD[3:0]	O	MII Transmit Data Outputs
MII_TX_EN	O	MII Transmit Enable Output
MII_TX_ERR	O	MII Transmit Error Output
CLK_MII_RX	I	MII Receive Clock Input
MII_RXD[3:0]	I	MII Receive Data Inputs

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
MII_RX_DV	I	MII Receive Data Valid Input
MII_RX_ERR	I	MII Receive Error Input
MII_COL	I	MII Collision Input
MII_CRS	I	MII Carrier Sense Input
MDC	O	PHY Management Clock Output
MDIO	IOpu	PHY Management Data Input/Output
Global Clocks		
CLK_SYS_S	I	System Clock Selection Input
CLK_SYS	I	System Clock Input: 25, 50 or 75MHz
CLK_CMN	I	Common Clock Input (for common clock mode also known as differential mode)
CLK_HIGH	I	Clock High Input (for adaptive clock recovery machines and E1/T1 master clocks)
MCLK	I	Master Clock Input (for E1/T1 master clocks)
CPU Interface		
H_CPU_SPI_N	Ipu	Host Bus Interface (1=Parallel Bus, 0=SPI Bus)
DAT_32_16_N	Ipu	Data Bus Width (1=32-bit , 0=16-bit)
H_D[31:1]	IO	Host Data Bus
H_D[0] / SPI_MISO	IO	Host Data LSb or SPI Data Output
H_AD[24:1]	I	Host Address Bus
H_CS_N	I	Host Chip Select (Active Low)
H_R_W_N / SPI_CP	I	Host Read/Write Control or SPI Clock Phase
H_WR_BE0_N / SPI_CLK	I	Host Write Enable Byte 0 (Active Low) or SPI Clock
H_WR_BE1_N / SPI_MOSI	I	Host Write Enable Byte 1 (Active Low) or SPI Data Input
H_WR_BE2_N / SPI_SEL_N	I	Host Write Enable Byte 2 or SPI Chip Select (Active Low)
H_WR_BE3_N / SPI_CI	I	Host Write Enable Byte 3 (Active Low) or SPI Clock Invert
H_READY_N	Oz	Host Ready Output (Active Low)
H_INT[1:0]	O	Host Interrupt Outputs. H_INT[0] for TDMoP. H_INT[1] for LIU and Framer
JTAG Interface		
JTRST_N	Ipu	JTAG Test Reset
JTCLK	Ipd	JTAG Test Clock
JTMS	Ipu	JTAG Test Mode Select
JTDI	Ipu	JTAG Test Data Input
JTDO	Oz	JTAG Test Data Output
Reset and Factory Test Pins		
RST_SYS_N	Ipu	System Reset (Active Low)
HIZ_N	I	High Impedance Enable (Active Low)
SCEN	Ipd	Used for factory tests.
STMD	Ipd	Used for factory tests.
MBIST_EN	I	Used for factory tests.
MBIST_DONE	O	Used for factory tests.
MBIST_FAIL	O	Used for factory tests
TEST_CLK	O	Used for factory tests.
TST_CLD	I	Used for factory tests. DS34T104 only.
TST_Tm, TST_Rm	O	m = A , B or C. Used for factory tests. DS34T104 only.
Power and Ground		
DVDDC	P	1.8V Core Voltage for Framers and TDM-over-Packet Digital Logic (17 pins)
DVDDIO	P	3.3V for I/O Pins (16 pins)
DVSS	P	Ground for Framers, TDM-over-Packet and I/O Pins (31 pins)
DVDDLIU	P	3.3V for LIU Digital Logic (2 pins)
DVSSLIU	P	Ground for LIU Digital Logic (2 pins)
ATVDDn	P	3.3 V for LIU Transmitter Analog Circuits (8pins)
ATVSSn	P	Ground for LIU Transmitter Analog Circuits (8 pins)
ARVDDn	P	3.3 V for LIU Receiver Analog Circuits (8 pins)
ARVSSn	P	Ground for LIU Receiver Analog Circuits (8 pins)
ACVDD1, ACVDD2	P	1.8V for CLAD Analog Circuits
ACVSS1, ACVSS2	P	Ground for CLAD Analog Circuits

Note 1: In pin names, the suffix "n" stands for port number: n=1 to 8 for DS34S108; n=1 to 4 for DS34S104; n=2 for DS34S102; n=1 for DS34S101. All pin names ending in "_N" are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL unless otherwise specified in the pin description.

PIN TYPES

I = input pin
I_{PD} = input pin with internal 50kΩ pulldown to DVSS
I_{PU} = input pin with internal 50kΩ pullup to DVDDIO
IO = input/output pin
IO_{PD} = input/output pin with internal 50kΩ pulldown to DVSS
IO_{PU} = input/output pin with internal 50kΩ pullup to DVDDIO
O = output pin
O_Z = output pin that can be placed in a high-impedance state
P = power-supply or ground pin

7 Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

DS34T101, DS34T102 and DS34T108 have a 23mm x 23mm 484-lead thermally enhanced ball grid array (TEBGA) package. The TEBGA package dimensions are shown in Maxim document 21-0365.

DS34T108 has a 23mm x 23mm 484-lead ball grid array with embedded heat sink (HSBGA) package. The HSBGA package dimensions are shown in Maxim document 21-0366.

8 Thermal Information

Parameter		TEBGA-484 DS34T101 DS34T102 DS34T104	HSBGA-484 DS34T108
Target Ambient Temperature Range		-40 to 85°C	-40 to 85°C
Die Junction Temperature Range		-40 to 125°C	-40 to 125°C
Theta Jc (junction to top of case)		4.2 °C/W	2.5 °C/W
Theta Jb (junction to bottom pins)		7.1 °C/W	5.5 °C/W
Theta Ja, Still Air (Note 1)		16.1 °C/W	13.0 °C/W
Theta Ja, Moving Air (Note 1)	1m/s	13.3 °C/W	10.7 °C/W
	2m/s	12.5 °C/W	9.6 °C/W

Note 1: These numbers are estimates using JEDEC standard PCB and enclosure dimensions.

9 Document Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	072707	Initial data sheet release.	—
1	121407	Ensured pin name for JTRST_N was used consistently throughout the data sheet.	16, 24, 34, 47, 48, 50
		In Section 7.1, clarified product and package type relationships.	17
		In Section 8.3, expanded explanation of External Mode.	26
		In Section 10.2, clarified the function description for input CLK_HIGH.	45
		In Section 10.2, changed the output type for H_READY_N to three-stateable. This output does not have an internal pullup.	47
		In Section 10.2, corrected SCEN and SCMD pin type and changed the function description to inform users to connect inputs SCEN and SCMD to DVSS because these inputs do not have internal pulldowns. Additionally, simplified the function description for signals only used by the factory (TEST_CLK, TST_CLD, TST_TA, TST_TB, TST_TC, TST_RA, TST_RB, TST_RC).	48
		In Table 11-2, removed the JTAG ID codes for the DS34S108, DS34S104, DS34S102, and DS34S101.	53
		In Section 16 (Thermal Information), updated values for HSBGA and TEBGA packages. Added Theta-JA values for deployments with forced air flow.	75
2	042608	Removed future status from DS34T102, DS34T104 in the *Ordering Information* table.	1
3	071808	Completely revised and simplified. All content derived from the 071108 revision of the full data sheet.	All
4	101708	Removed all references to AAL2 mode. Corrected some spelling errors and other minor typos.	All
5	032609	Removed future status from the DS34T101 in the *Ordering Information* table.	1
6	8/09	Added Doc ID number/matches full data sheet version.	1

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