DN2625

N-Channel Depletion-Mode Vertical DMOS FET in Single and Dual Options

Features

- Very Low Gate Threshold Voltage
- Designed to be Source-driven
- Low Switching Losses
- Low Effective Output Capacitance
- Designed for Inductive Loads

Applications

- Medical Ultrasound Beamforming
- Ultrasonic Array-focusing Transmitter
- Piezoelectric Transducer Waveform Drivers
- High-speed Arbitrary Waveform Generator
- Normally-on Switches
- Solid-state Relays
- Constant Current Sources
- Power Supply Circuits

General Description

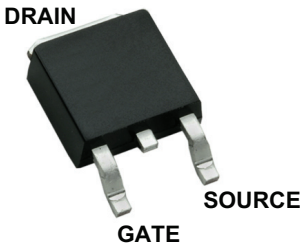
The DN2625 is a low-threshold Depletion-mode (normally-on) transistor that utilizes an advanced vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors as well as the high input impedance and positive temperature coefficient inherent in Metal-Oxide Semiconductor (MOS) devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

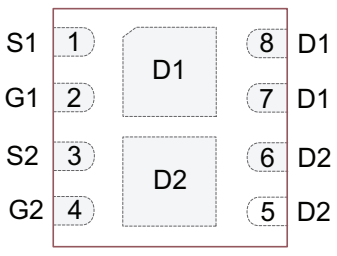
The DN2625DK6-G contains two MOSFETs in an 8-lead, dual-pad DFN package. The DN2625 contains a single MOSFET in a TO-252 D-PAK package.

Package Types

TO-252 D-PAK
(Top view)



8-lead DFN (Dual Pad)
(Top view)



See Table 3-1 and Table 3-2 for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-source Voltage ..... BV_{DSX}
Drain-to-gate Voltage ..... BV_{DGX}
Gate-to-source Voltage ..... ±20V
Operating Ambient Temperature, T_A ..... –55°C to 150°C
Storage Temperature, T_S ..... –55°C to 150°C
Soldering Temperature (**Note 1**) ..... 300°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Distance of 1.6 mm from case for 10 seconds

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = 25°C. (**Note 1**)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-source Breakdown Voltage	BV_{DSX}	250	—	—	V	V_{GS} = –2.5V, I_D = 50 µA
Drain-to-gate Breakdown Voltage	BV_{DGX}	250	—	—	V	V_{GS} = –2.5V, I_D = 50 µA
Gate-to-source Off Voltage	$V_{GS(OFF)}$	–1.5	—	–2.1	V	V_{DS} = 15V, I_D = 100 µA
Change in $V_{GS(OFF)}$ with Temperature	$\Delta V_{GS(OFF)}$	—	—	–4.5	mV/°C	V_{DS} = 15V, I_D = 100 µA (**Note 2**)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ±20V, V_{DS} = 0V
Drain-to-source Leakage Current	$I_{D(OFF)}$	—	—	1	µA	V_{DS} = 250V, V_{GS} = –5V
		—	—	200		V_{DS} = 250V, V_{GS} = –5V, T_A = 125°C (**Note 2**)
Saturated Drain-to-source Current	I_{DSS}	1.1	—	—	A	V_{GS} = 0V, V_{DS} = 15V
Pulsed Drain-to-source Current	$I_{DS(PULSE)}$	3.1	3.3	—	A	V_{GS} = 0.9V, V_{DS} = 15V (With duty cycle of 1%)
Static Drain-to-source On-resistance	$R_{DS(ON)}$	—	—	3.5	Ω	V_{GS} = 0V, I_D = 1A
Change in $R_{DS(ON)}$ with Temperature	$\Delta_{RDS(ON)}$	—	—	1.1	%/°C	V_{GS} = –0V, I_D = 200 mA (**Note 2**)

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = 25°C. (Note 2)						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Forward Transconductance	G_{FS}	100	—	—	mmh0	V_{DS} = 10V, I_D = 150 mA
Input Capacitance	C_{ISS}	—	800	1000	pF	V_{GS} = –2.5V, V_{DS} = 25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	70	210	pF	
Reverse Transfer Capacitance	C_{RSS}	—	18	70	pF	
Turn-on Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = 25V, I_D = 150 mA, R_{GEN} = 3Ω, V_{GS} = 0V to –10V
Rise Time	t_r	—	—	20	ns	
Turn-off Delay Time	$t_{d(OFF)}$	—	—	10	ns	
Fall Time	t_f	—	—	20	ns	
Total Gate Charge	Q_G	—	—	7.04	nC	I_D = 3.5A, V_{DS} = 100V, V_{GS} = 1.5V
Gate-to-source Charge	Q_{GS}	—	—	0.783	nC	
Gate-to-drain Charge	Q_{GD}	—	—	3.73	nC	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	V_{GS} = –2.5V, I_{SD} = 150 mA (Note 1)

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J$ = +25°C.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	150	°C	
Storage Temperature	T_S	–55	—	150	°C	
Soldering Temperature	—	—	—	300	°C	Note 1
PACKAGE THERMAL RESISTANCE						
TO-252 D-PAK	θ_{JA}	—	81	—	°C/W	Note 2
8-lead DFN (Dual Pad)	θ_{JA}	—	29	—	°C/W	Note 3

Note 1: Distance of 1.6 mm from case for 10 seconds

2: Four-layer, 1-oz, 3 x 4-inch PCB with 20 via for drain pad

3: Four-layer, 1-oz, 3 x 4-inch PCB with 12 via for drain pad

THERMAL CHARACTERISTICS

Package	**I_D (1) (Continuous) (A)**	**I_D (Pulsed) (A)**	**I_{DR} (1) (A)**	**I_{DRM} (A)**
TO-252 D-PAK	1.1	3.3	1.1	3.3
8-lead DFN (Dual Pad)	1.1	3.3	1.1	3.3

Note 1: I_D (Continuous) is limited by maximum T_J.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

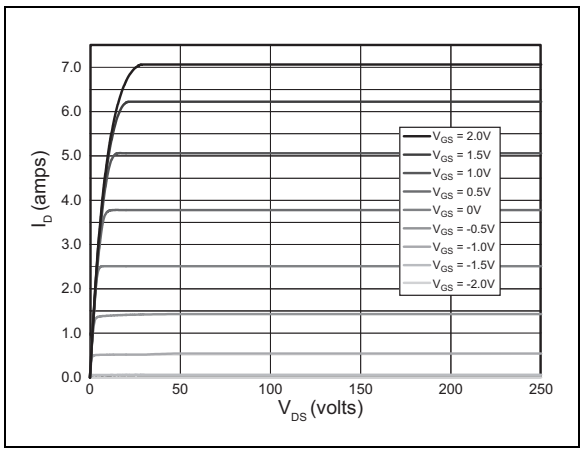


FIGURE 2-1: *Output Characteristics.*

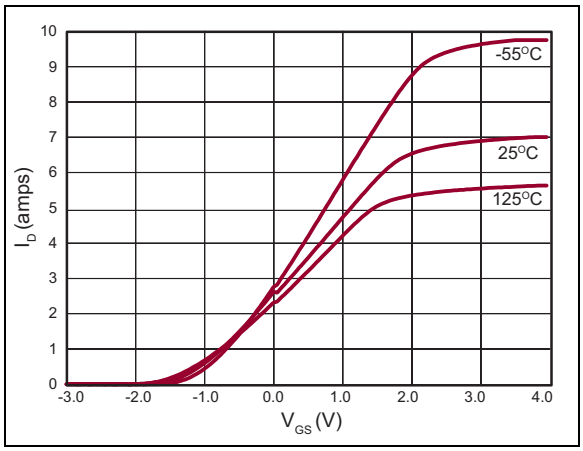


FIGURE 2-2: *Transfer Characteristics.*

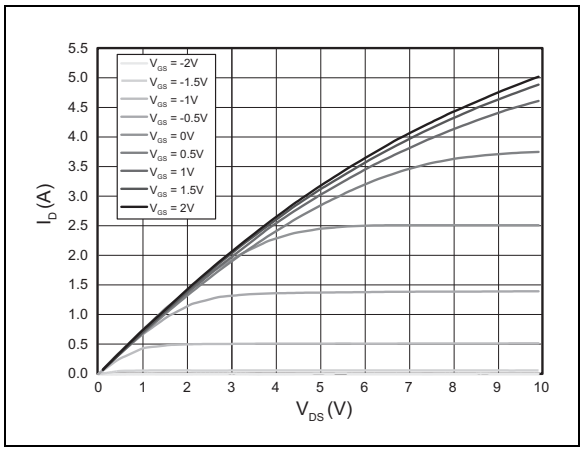


FIGURE 2-3: *Saturation Characteristics.*

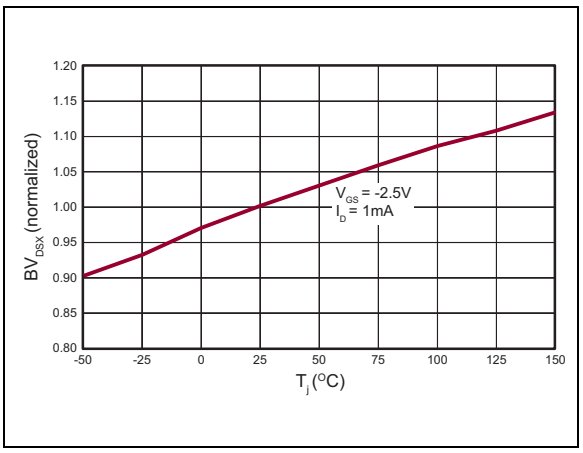


FIGURE 2-4: *BV_{DSX} Variation with Temperature.*

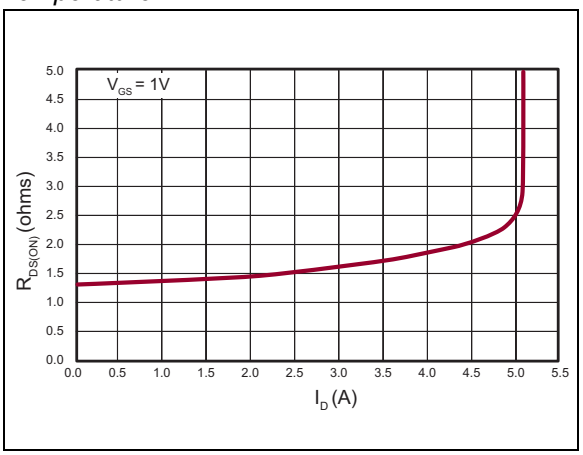


FIGURE 2-5: *On-resistance vs. Drain Current.*

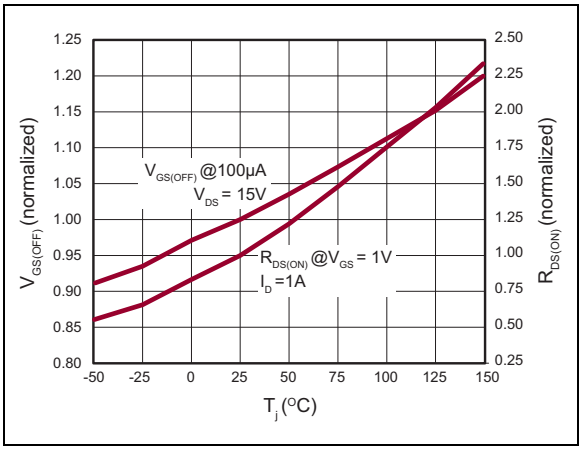


FIGURE 2-6: *$V_{GS(OFF)}$ and $R_{DS(ON)}$ Variation with Temperature.*

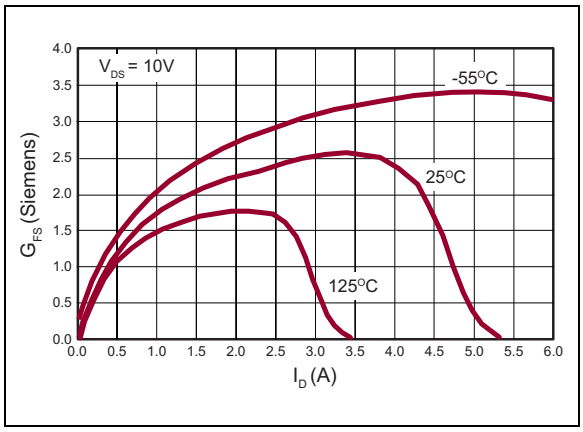


FIGURE 2-7: *Transconductance vs. Drain Current.*

3.0 PIN DESCRIPTION

The details on the pins of TO-252 D-PAK and 8-lead DFN (dual pad) are listed in Table 3-1 and Table 3-2. Refer to **Package Types** for the location of pins.

TABLE 3-1: TO-252 D-PAK PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Drain	Drain
3	Source	Source
4	Drain	Drain

TABLE 3-2: 8-LEAD DFN (DUAL PAD) PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	S1	Device 1 source
2	G1	Device 1 gate
3	S2	Device 2 source
4	G2	Device 2 gate
5	D2	Device 2 drain
6	D2	Device 2 drain
7	D1	Device 1 drain
8	D1	Device 1 drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 shows the switching waveforms and test circuit for DN2625.

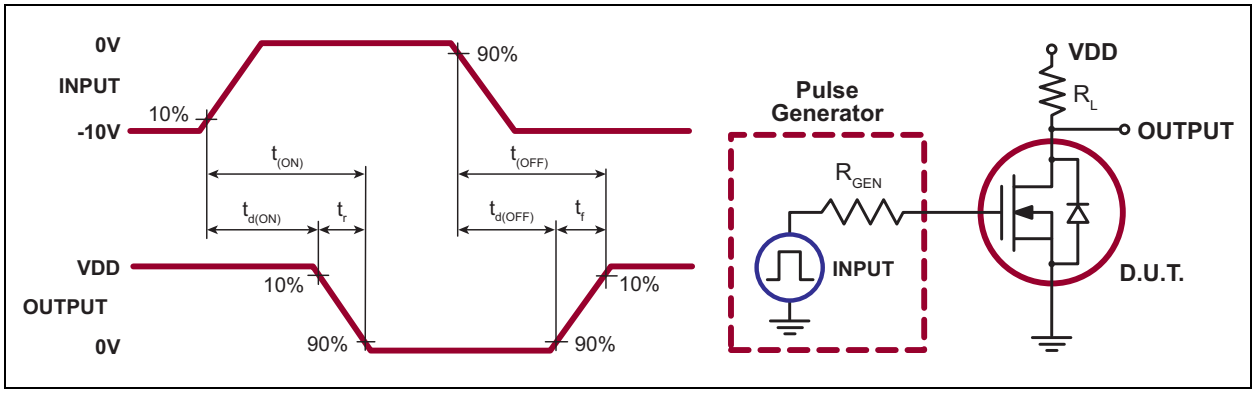


FIGURE 4-1: *Switching Waveforms and Test Circuit.*

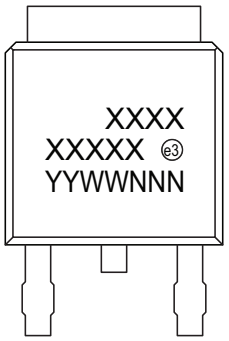
PRODUCT SUMMARY

BV_{DSX}/BV_{DGX} (V)	$V_{GS(OFF)}$ (Maximum) (V)	I_{DS} (Pulsed) (V_{GS} = 0.9V) (Minimum) (A)
250	–2.1	3.3

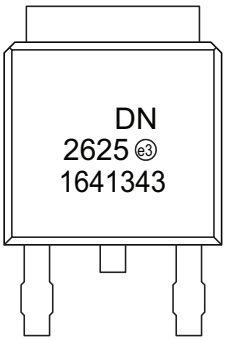
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

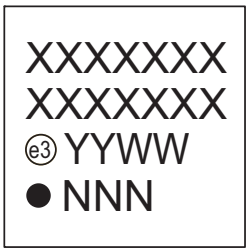
TO-252 (D-PAK)



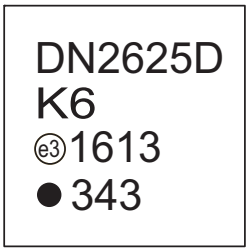
Example



8-lead DFN



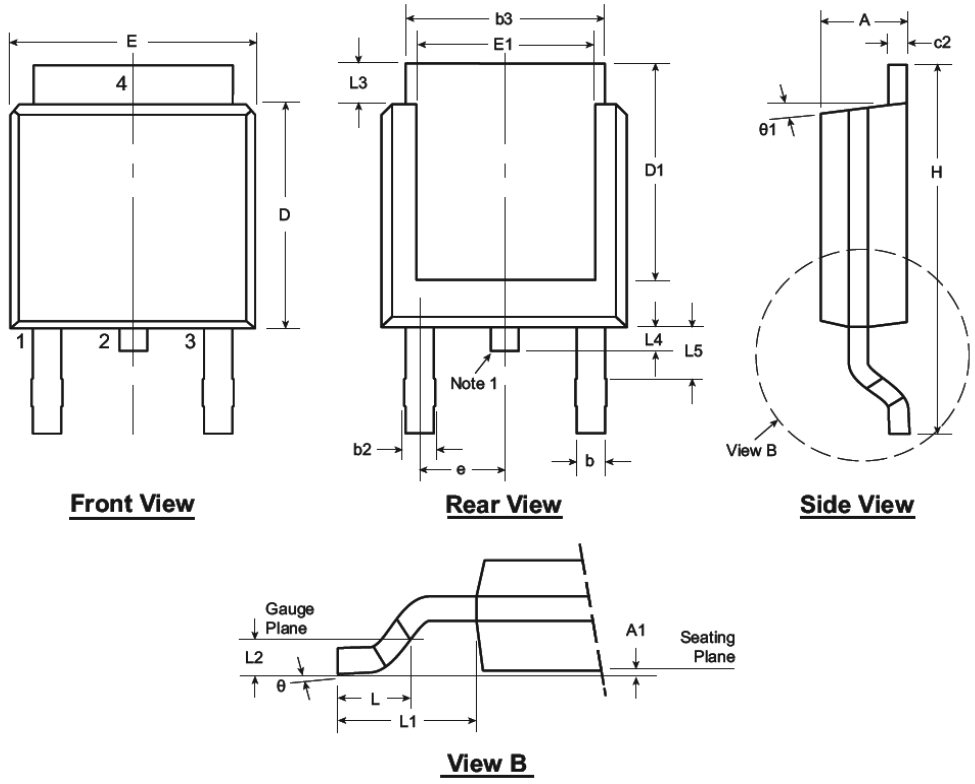
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-252 (D-PAK) Package Outline (K4)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

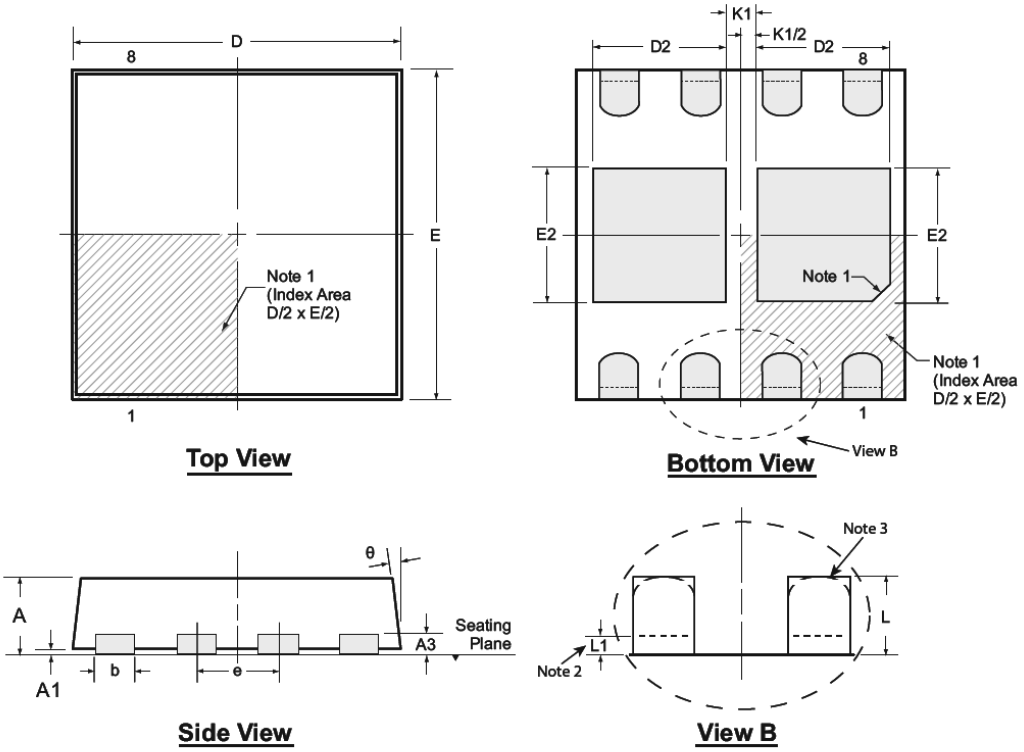
1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimen-sion (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	.025*	.035†	0º	0º
	NOM	-	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*		.410	.070			.050	.040	.060	10º	15º

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

8-Lead DFN Package Outline (K6)

5.00x5.00mm body, 0.90mm height (max), 1.27mm pitch (dual pad)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	K1	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.35	4.90	1.93	4.90	1.90	1.27 BSC	0.40 REF	0.40	0.00	0°
	NOM	0.85	-		0.40	5.00	2.03	5.00	2.00			0.50	-	-
	MAX	0.90	0.05		0.45	5.10	2.13	5.10	2.10			0.60	0.15	14°

Drawings not to scale

APPENDIX A: REVISION HISTORY

Revision A (December 2016)

- Converted Supertex Document DSFP-DN2625 to Microchip DS20005537B
- Removed obsolete package, 14-lead QFN
- Changed the TO-252 D-PAK packaging quantity from 1000/Bag to 2000/Reel
- Revised the Features section

Revision B (May 2017)

- Corrected the 8L DFN Package Outline dimensions by changing it from 4 mm x 4 mm body/1 mm height/1 mm pitch to 5 mm x 5 mm body/0.9 mm height/1.27 mm pitch
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Devices:	DN2625	=	N-Channel Depletion-Mode Vertical DMOS FET (Single Option)
	DN2625D	=	N-Channel Depletion-Mode Vertical DMOS FET (Dual Option)
Packages:	K4	=	TO-252 D-PAK
	K6	=	8-lead DFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	2000/Reel for a K4 Package
		=	490/Tray for a K6 Package

Examples:

a) DN2625K4-G: N-Channel Depletion-Mode Vertical DMOS FET (Single Option), TO-252 D-PAK Package, 2000/Reel

b) DN2625DK6-G: N-Channel Depletion-Mode Vertical DMOS FET (Dual Option), 8-lead DFN Package, 490/Tray

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