DG401, DG403

Monolithic CMOS Analog Switches

FN3284
Rev 11.00
Nov 20, 2006

The DG401 and DG403 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

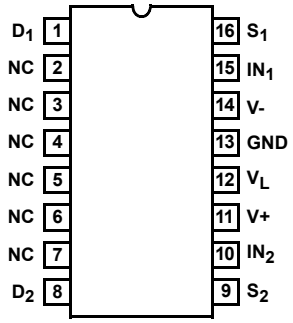
These switches feature low analog ON resistance (<45Ω) and fast switch time (t_{ON}<150ns). Low charge injection simplifies sample and hold applications.

The improvements in the DG401, DG403 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V_{P-P} signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

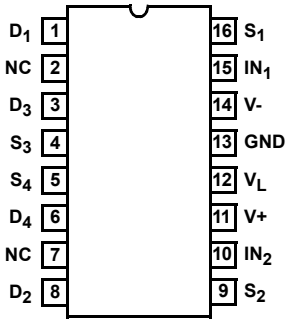
The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The three different devices provide the equivalent of two SPST (DG401) or two SPDT (DG403) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

Pinouts

DG401
(16 LD SOIC, TSSOP)
TOP VIEW



DG403
(16 LD SOIC, TSSOP)
TOP VIEW



NOTE: (NC) No Connection.

Features

- ON Resistance (Max) 45Ω
- Low Power Consumption (P_D) . . . . . <35µW
- Fast Switching Action
  - t_{ON} (Max) 150ns
  - t_{OFF} (Max) 100ns
- Low Charge Injection
- DG401 Dual SPST; Same Pinout as HI-5041
- DG403 Dual SPDT; DG190, IH5043, IH5151, HI-5051
- TTL, CMOS Compatible
- Single or Split Supply Operation
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Ordering Information

PART NUMBER*	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
DG401DY*	DG401DY	-40 to +85	16 Ld SOIC	M16.15
DG401DYZ* (Note)	DG401DYZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
DG401DVZ* (Note)	DG401 DVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173
DG403DY*	DG403DY	-40 to +85	16 Ld SOIC	M16.15
DG403DYZ* (Note)	DG403DYZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
DG403DVZ* (Note)	DG403 DVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173

*Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

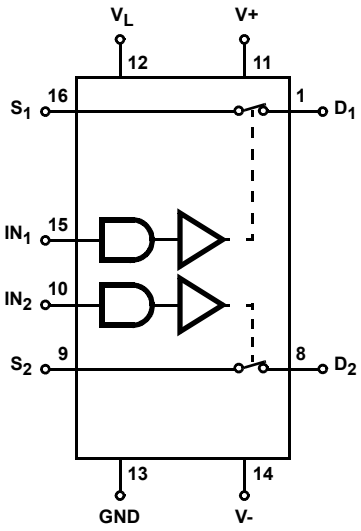
TRUTH TABLE

LOGIC	DG401	DG403	
	SWITCH	SWITCH 1, 2	SWITCH 3, 4
0	OFF	OFF	ON
1	ON	ON	OFF

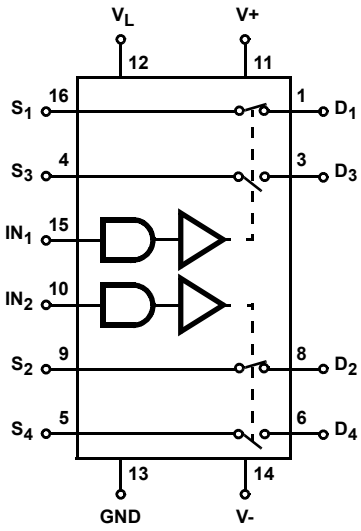
NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V.

Functional Diagrams

DG401

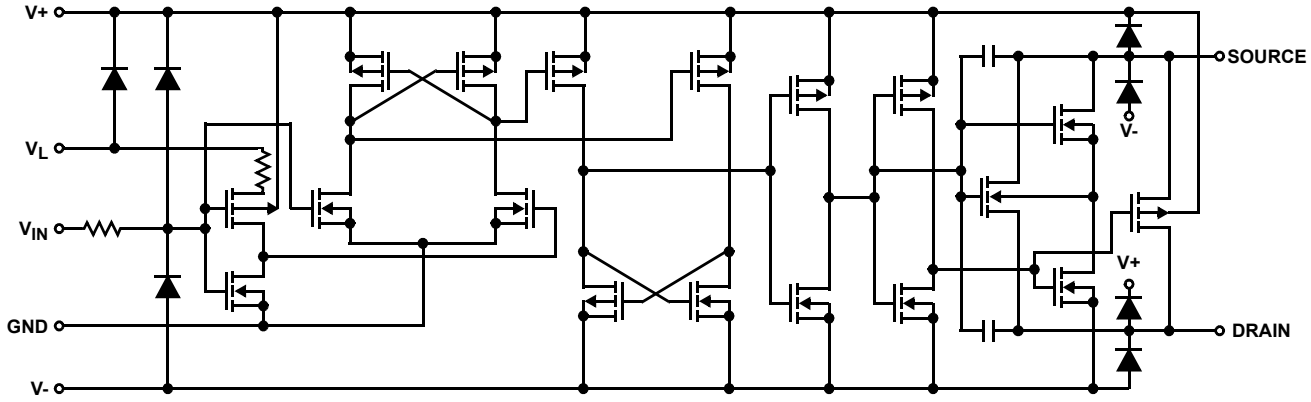


DG403



SWITCHES SHOWN FOR LOGIC “1” INPUT

Schematic Diagram



Absolute Maximum Ratings

V+ to V- 44.0V
GND to V-. 25V
V_L. . . . . (GND - 0.3V) to (V+) +0.3V
Digital Inputs V_S, V_D (Note 1) . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle, Max). . 100mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	115
TSSOP Package	150

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC and TSSOP- Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Voltage Range . . . . . ±20V (Max)
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V (Note 3), V_L = 5V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF	+25	-	100	150	ns
Turn-OFF Time, t_{OFF}		+25	-	60	100	ns
Break-Before-Make Time Delay (DG403), t_D	R_L = 300Ω, C_L = 35pF	+25	5	12	-	ns
Charge Injection, Q (Figure 3)	C_L = 10nF, V_G = 0V, R_G = 0Ω	+25	-	60	-	pC
OFF Isolation (Figure 4)	R_L = 100Ω, C_L = 5pF, f = 1MHz	+25	-	72	-	dB
Crosstalk (Channel-to-Channel) (Figure 6)		+25	-	-90	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_S = V_D = 0V (Figure 7)	+25	-	12	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		+25	-	12	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$		+25	-	39	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Current with V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-1	0.005	1	µA
Input Current with V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-1	0.005	1	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = ∓10mA, V_D = ±10V	+25	-	20	45	Ω
		Full	-	-	55	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V+ = 16.5V, V- = -16.5V, I_S = -10mA, V_D = 5, 0, -5V	+25	-	3	3	Ω
		Full	-	-	5	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5 V_D = ±15.5V, V_S = ∓15.5V	+25	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		+25	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Channel ON Leakage Current, $I_{D(ON)}$ + $I_{S(ON)}$	V± = ±16.5V, V_D = V_S = ±15.5V	+25	-1	-0.04	1	nA
		Full	-10	-	10	nA

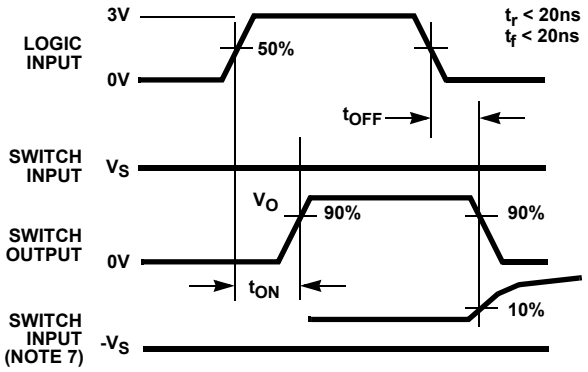
Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V (Note 3), V_L = 5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) MIN	(NOTE 5) TYP	(NOTE 4) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	+25	-	0.01	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-		+25	-1	-0.01	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L		+25	-	0.01	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}		+25	-1	-0.01	-	µA
		Full	-5	-	-	µA

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

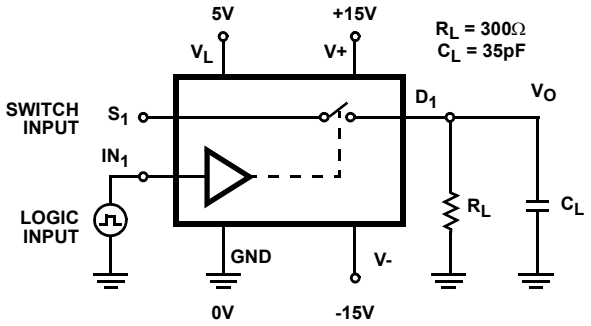
Test Circuits and Waveforms



NOTES:

6. Logic input waveform is inverted for switches that have the opposite logic sense.
7. V_S = 10V for t_{ON}, V_S = -10V for t_{OFF}.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for IN_2 and S_2.
For load conditions, see Specifications. C_L includes fixture and stray capacitance.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

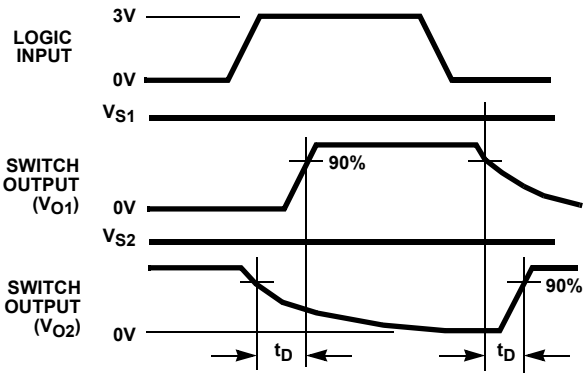
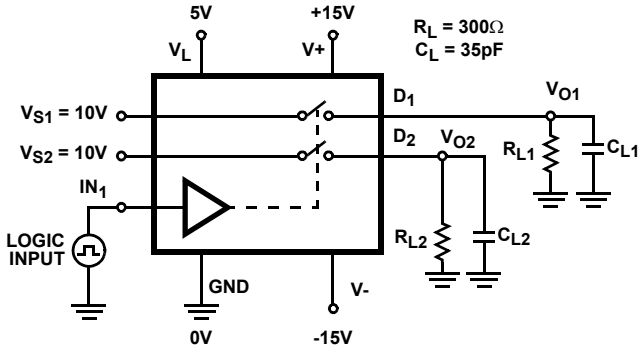


FIGURE 2A. MEASUREMENT POINTS



C_L includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME

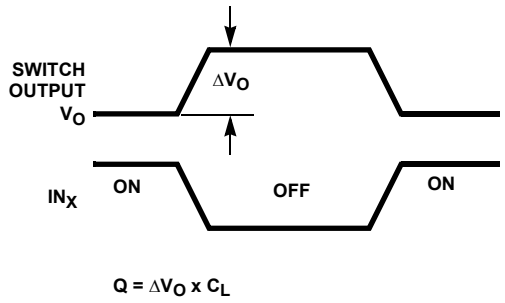


FIGURE 3A. MEASUREMENT POINTS

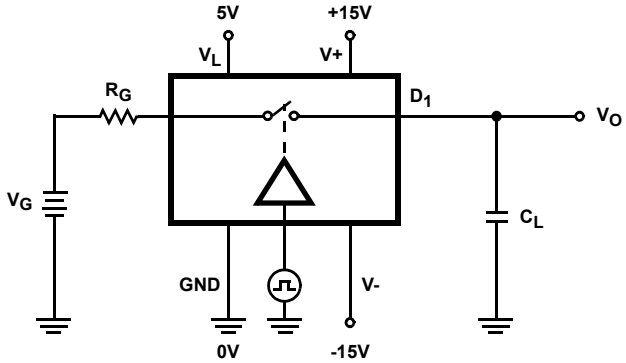


FIGURE 3B. TEST CIRCUIT

FIGURE 3. CHARGE INJECTION

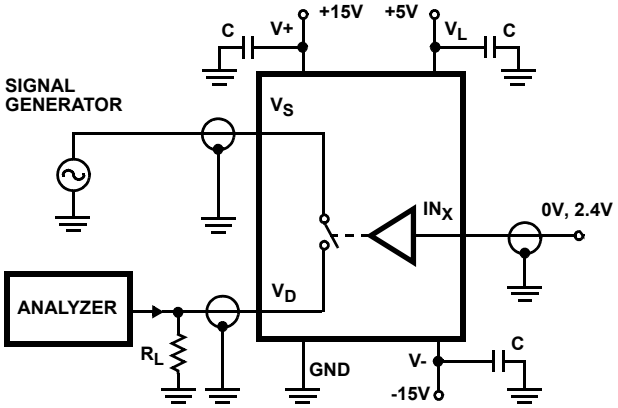


FIGURE 4. OFF ISOLATION TEST CIRCUIT

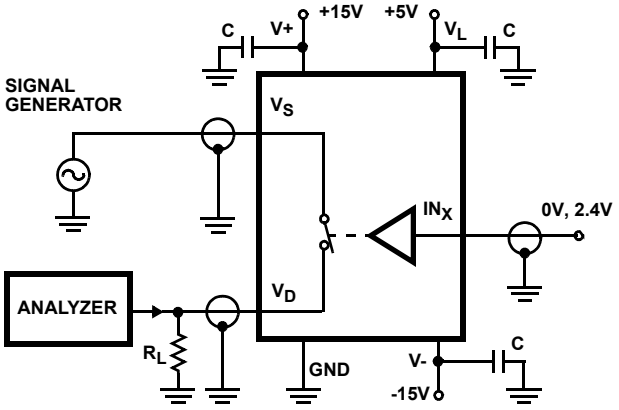


FIGURE 5. INSERTION LOSS TEST CIRCUIT

Test Circuits and Waveforms (Continued)

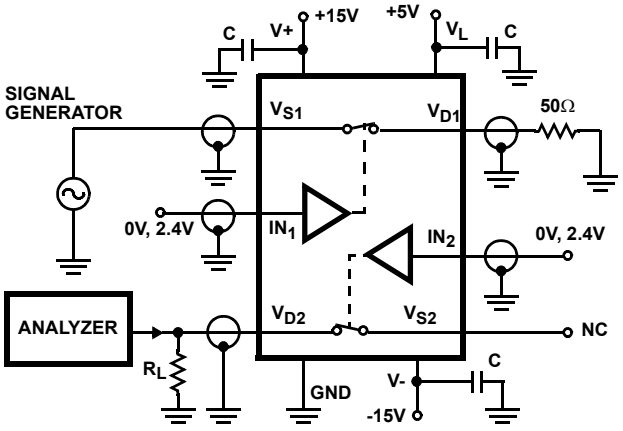


FIGURE 6. CROSSTALK TEST CIRCUIT

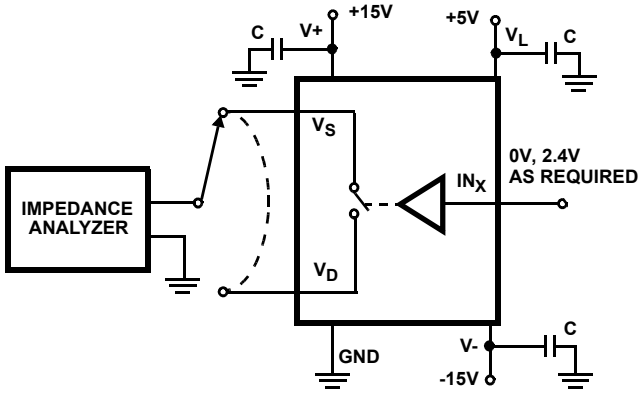


FIGURE 7. CAPACITANCES TEST CIRCUIT

Application Information

Dual Slope Integrators

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{IN} or discharges the capacitor in preparation for the next integration cycle.

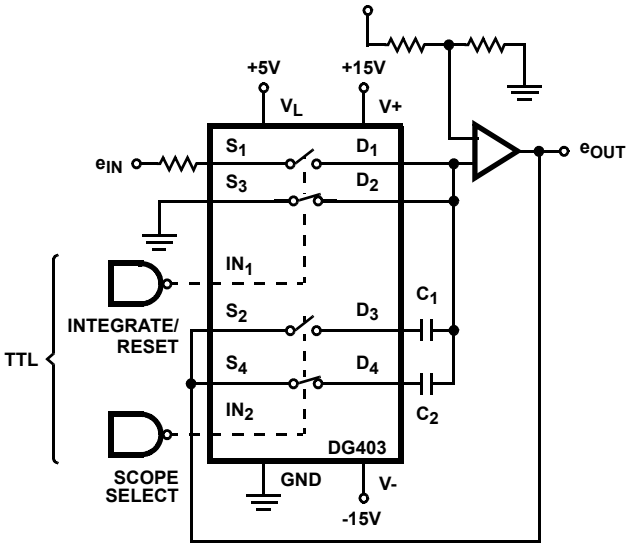


FIGURE 8. DUAL SLOPE INTEGRATOR

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1. The output of A_2 is fed back to A_3 and compared to the analog input e_{IN}. If $e_{IN} > e_{OUT}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{IN} goes below e_{OUT}, A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

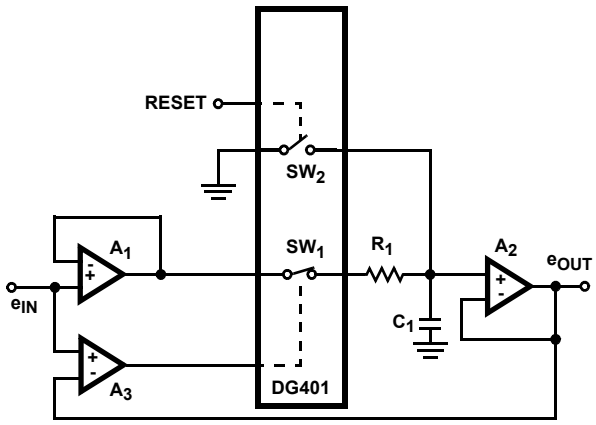


FIGURE 9. POSITIVE PEAK DETECTOR

Typical Performance Curves

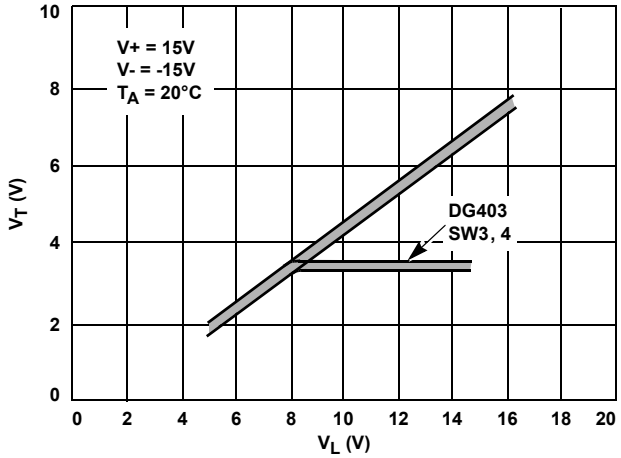


FIGURE 10. INPUT SWITCHING THRESHOLD vs LOGIC SUPPLY VOLTAGE

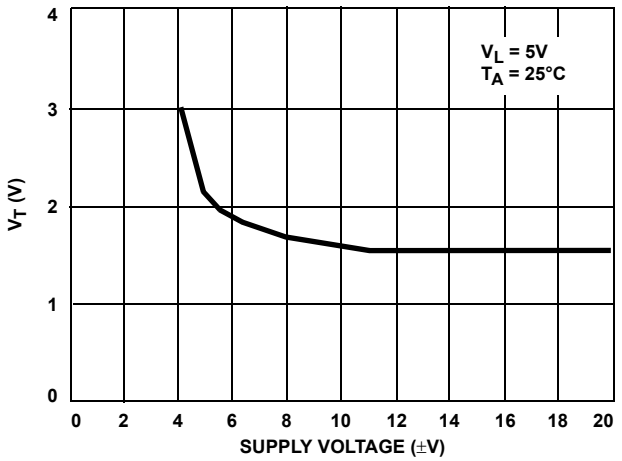


FIGURE 11. INPUT SWITCHING THRESHOLD vs POWER SUPPLY VOLTAGE

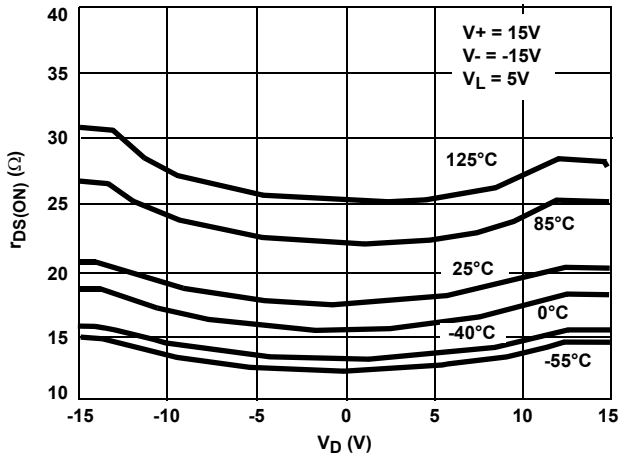


FIGURE 12. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

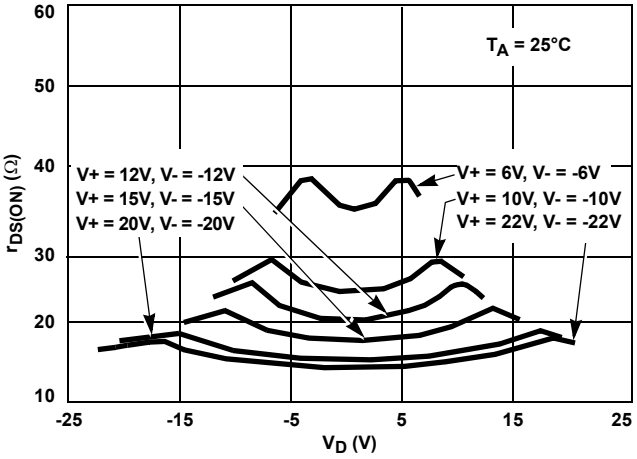


FIGURE 13. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

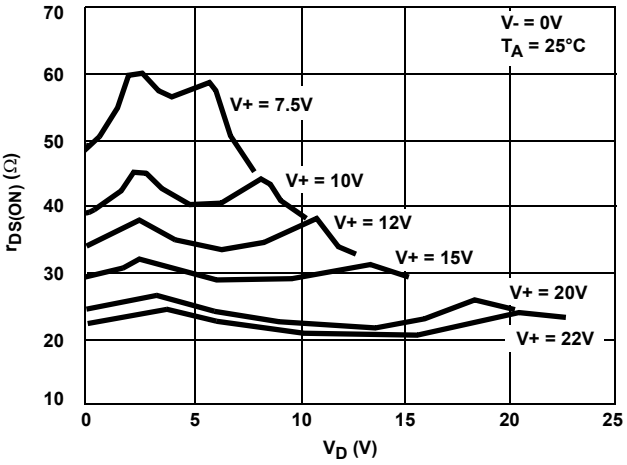


FIGURE 14. $r_{DS(ON)}$ vs V_D AND SINGLE SUPPLY VOLTAGE

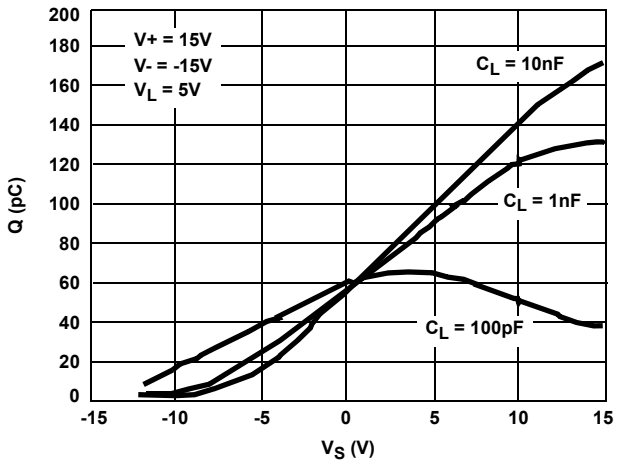


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE

Typical Performance Curves (Continued)

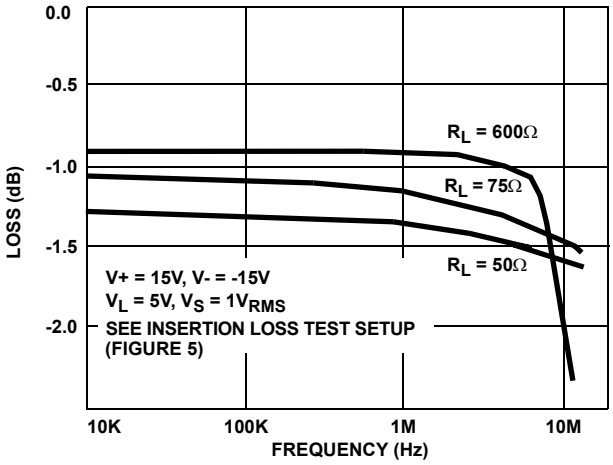


FIGURE 16. INSERTION LOSS vs FREQUENCY

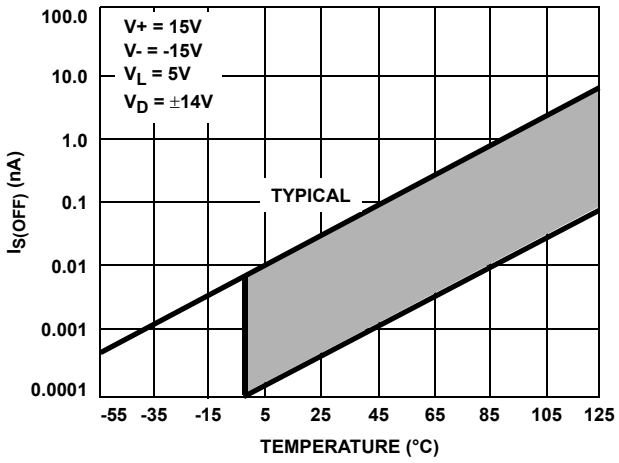


FIGURE 17. $I_{S(OFF)}$ vs TEMPERATURE

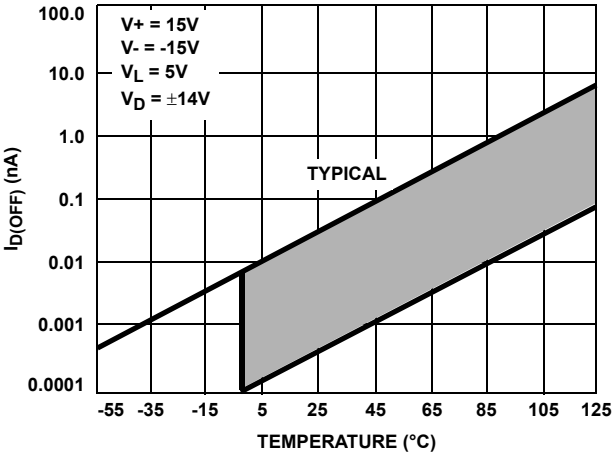


FIGURE 18. $I_{D(OFF)}$ vs TEMPERATURE

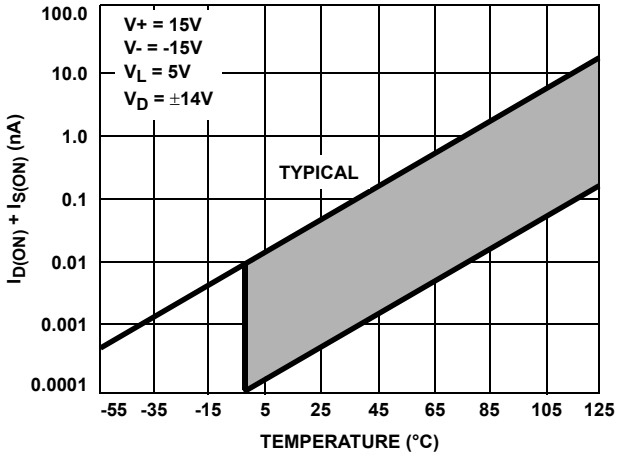


FIGURE 19. $I_{D(ON)} + I_{S(ON)}$ vs TEMPERATURE

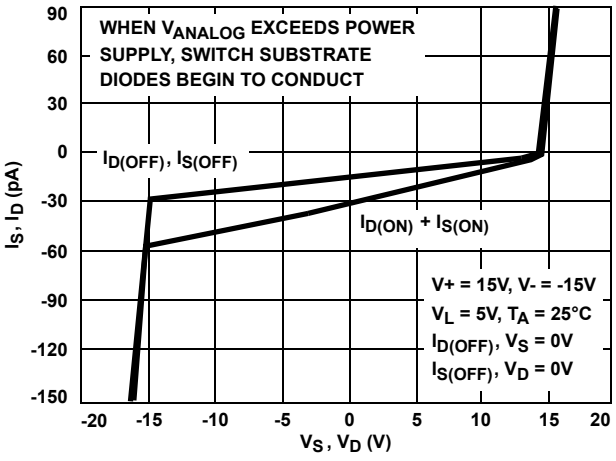


FIGURE 20. LEAKAGE CURRENTS vs ANALOG VOLTAGE

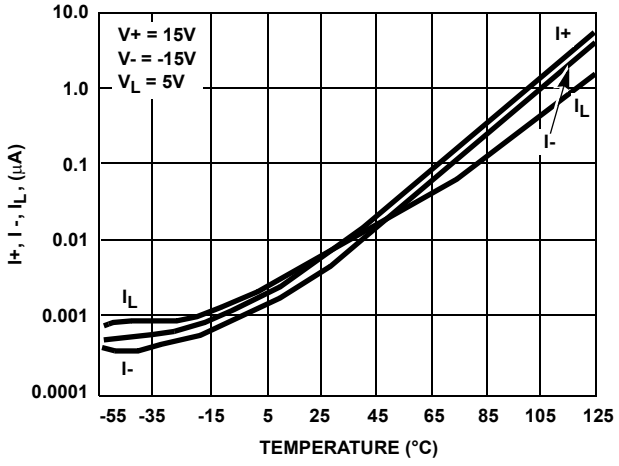


FIGURE 21. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

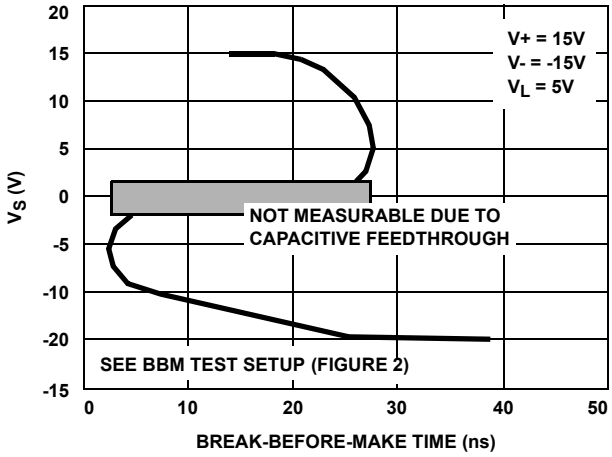


FIGURE 22. BREAK-BEFORE-MAKE vs ANALOG VOLTAGE

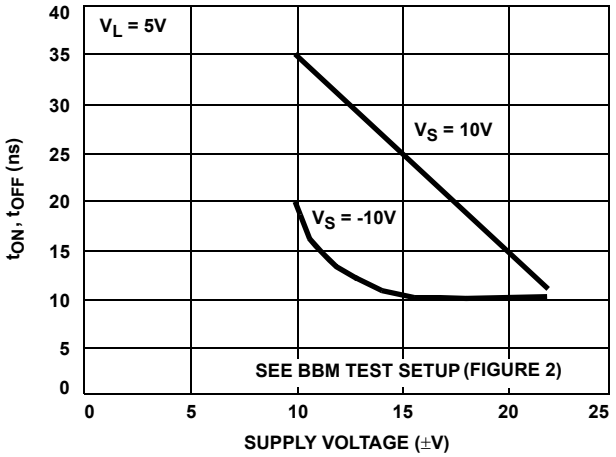


FIGURE 23. BREAK-BEFORE-MAKE vs POWER SUPPLY VOLTAGE

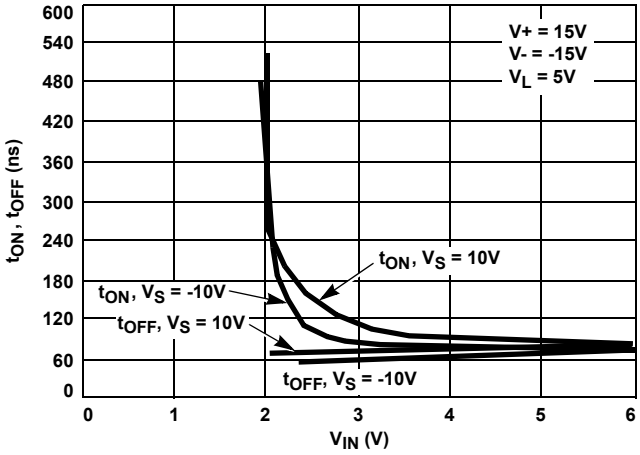


FIGURE 24. SWITCHING TIME vs INPUT LOGIC VOLTAGE (NOTE 8)

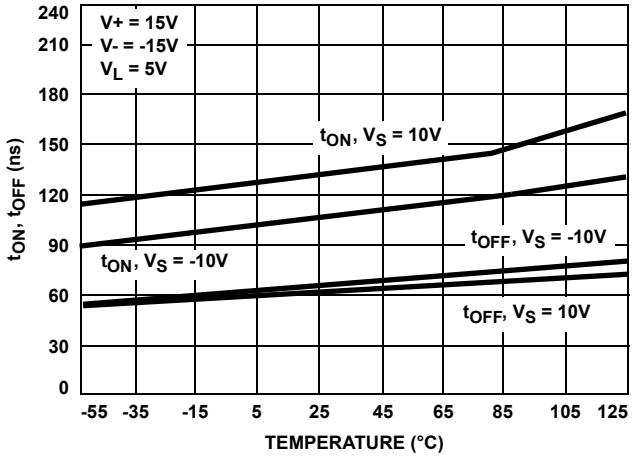


FIGURE 25. SWITCHING TIME vs TEMPERATURE (NOTE 8)

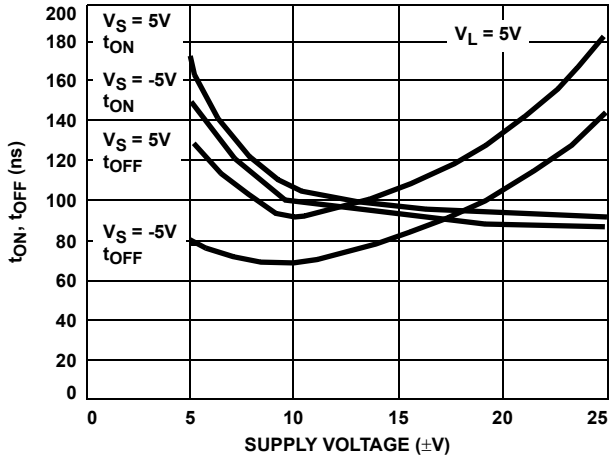


FIGURE 26. SWITCHING TIME vs POWER SUPPLY VOLTAGE (NOTE 8)

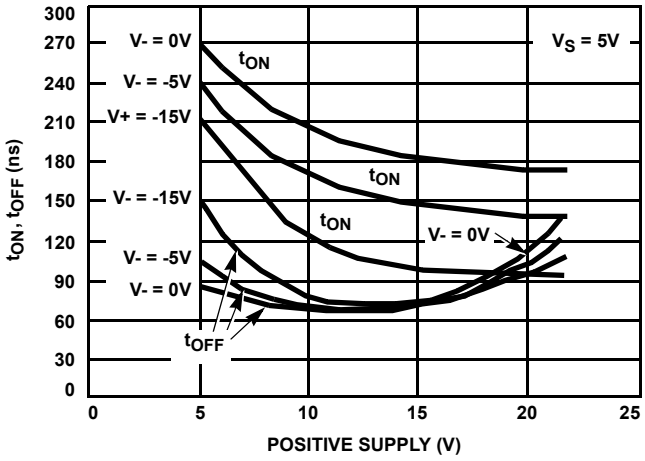


FIGURE 27. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 8)

Typical Performance Curves (Continued)

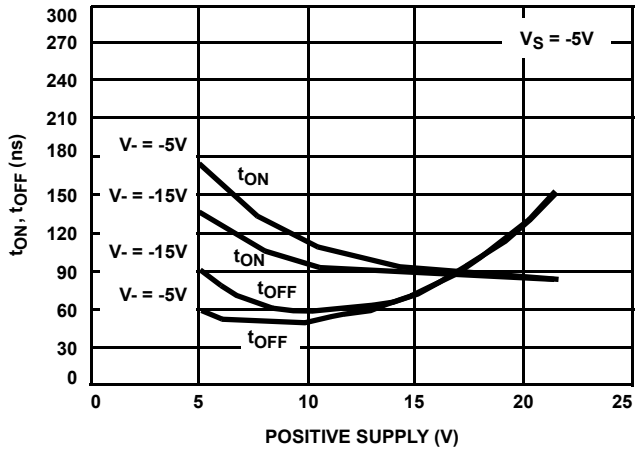
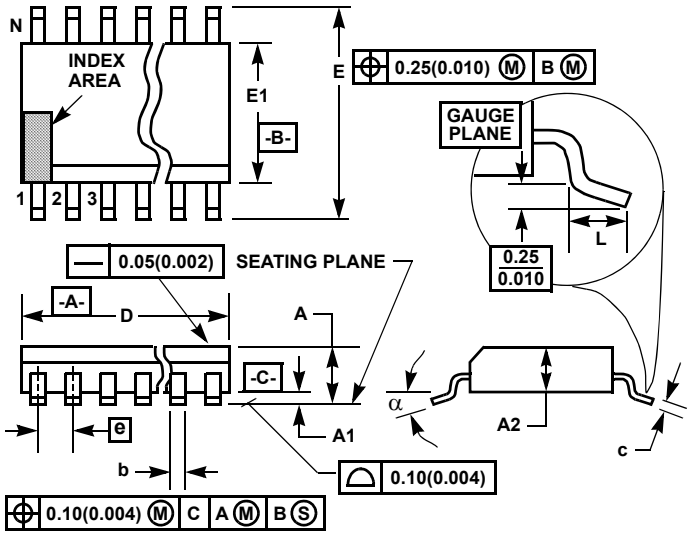


FIGURE 28. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 8)

NOTE:

8. Refer to Figure 1 for test conditions.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0°	8°	0°	8°	-

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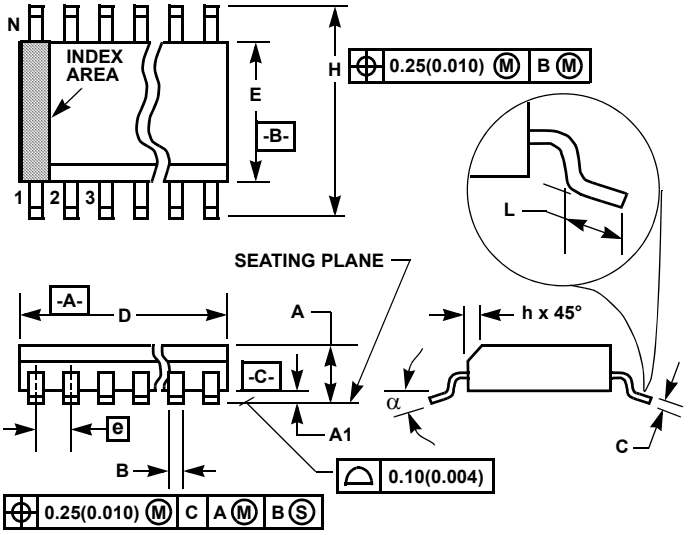
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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