16-BIT, QUAD CHANNEL, ULTRALOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Relative Accuracy: 12 LSB (Max)**
- **Glitch Energy: 0.15 nV-s**
- **Power Supply: +2.7 V to +5.5 V**
- *Micro***Power Operation: 850 µA at 5 V**
- **16-Bit Monotonic Over Temperature**
- **Settling Time: 10 µs to ±0.003% FSR**
- **Ultra-Low AC Crosstalk: −100 dB Typ**
- **Power-On Reset to Zero-Scale**
- **On-Chip Output Buffer Amplifier With Rail-to-Rail Operation**
- **Double Buffered Input Architecture**
- **Simultaneous or Sequential Output Update and Power-Down**
- **16-Channel Broadcast Capability**
- **Schmitt-Triggered Inputs**
- **SPI Compatible Serial Interface: Up to 50 MHz**
- **1.8 V to 5.5 V Logic Compatibility**
- **Available in a TSSOP-16 Package**

APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control**
- **Process Control**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- **PC Peripherals**

DESCRIPTION

The DAC8554 is a 16-bit, quad channel, voltage output, digital-to-analog converter (DAC), offering low-power operation and a flexible serial host interface. It offers monotonicity, good linearity, and exceptionally low glitch. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7 V to 5.5 V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 50 MHz for IOV_{DD} = 5 V.

The DAC8554 requires an external reference voltage to set the output range of each DAC channel. Also incorporated into the device is a power-on reset circuit which ensures that the DAC outputs power up at zero-scale and remain there until a valid write takes place. The DAC8554 provides a per channel power-down feature, accessed over the serial interface, that reduces the current consumption to 200 nA per channel at 5 V.

The low-power consumption of this device in normal operation makes it ideally suited to portable battery-operated equipment and other low-power applications. The power consumption is 4.25 mW at 5 V, reducing to 4 µW in power-down mode.

The DAC8554 is available in a TSSOP-16 package with a specified operating temperature range of −40°C to 105°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. This device is rated at 1500 V HBM and 1000 V CDM.

PACKAGING/ORDERING INFORMATION

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR[1]	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8554	TSSOP-16	PW	−40°C TO 105°C	D8554	DAC8554IPW	Tube, 90
					DAC8554IPWR	Tape and Reel, 2000

(1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

	UNIT
AV_{DD} to GND	−0.3 V to 6 V
Digital input voltage to GND	−0.3 V to AV_{DD} + 0.3 V
$V_{O(A)}$ to $V_{O(D)}$ to GND	−0.3 V to AV_{DD} + 0.3 V
Operating temperature range	−40°C to 105°C
Storage temperature range	−65°C to 150°C
Junction temperature range (T_J max)	150°C
Power dissipation	($T_J$max − T_A)/θ_{JA}
θ_{JA} Thermal impedance	118°C/W
θ_{JC} Thermal impedance	29°C/W
Lead temperature, soldering — Vapor phase (60 s)	215°C
Lead temperature, soldering — Infrared (15 s)	220°C

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE[1]					
Resolution		16			Bits
Relative accuracy	Measured by line passing through codes 485 and 64741		±4	±12	LSB
Differential nonlinearity	16-bit Monotonic		±0.25	±1	LSB
Zero-scale error	Measured by line passing through codes 485 and 64741		±2	±12	mV
Zero-scale error drift			±5		µV/°C
Full-scale error	Measured by line passing through codes 485 and 64741, AV_{DD} = 5 V, V_{ref} = 4.99 V		±0.3	±0.5	% of FSR
Gain error	Measured by line passing through codes 485 and 64741, AV_{DD} = 5 V		±0.05	±0.15	% of FSR
Gain temperature coefficient			±1		ppm of FSR/°C
Power Supply Rejection Ratio (PSRR)	R_L = 2 kΩ, C_L = 200 pF		8		mV
			0.75		mV/V

(1) Linearity calculated using a reduced code range of 485 to 64741; output unloaded.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS[2]					
Output voltage range		0		$V_{ref}H$	V
Output voltage settling time	To ±0.003% FSR, 0200_H to $FD00_H$, R_L = 2 kΩ, 0 pF < C_L < 200 pF		8	10	µs
	R_L = 2 kΩ, C_L = 500 pF		12		µs
Slew rate			1.8		V/µs
Capacitive load stability	$R_L = \infty$		470		pF
	R_L = 2 kΩ		1000		pF
Code change glitch impulse	1 LSB change around major carry		0.15		nV-s
Digital feedthrough			0.15		
DC crosstalk	Full-scale swing on adjacent channel. AV_{DD} = 5 V, V_{ref} = 4.096 V		0.25		LSB
AC crosstalk	1 kHz sine wave		−100		dB
DC output impedance	At mid-point input		1		Ω
Short-circuit current	AV_{DD} = 5 V		50		mA
	AV_{DD} = 3 V		20		
Power-up time	Coming out of power-down mode AV_{DD} = 5 V		2.5		µs
	Coming out of power-down mode AV_{DD} = 3 V		5		
AC PERFORMANCE					
SNR (1st 19 harmonics removed)			95		dB
THD	BW = 20 kHz, AV_{DD} = 5 V, F_{OUT} = 1 kHz		-85		
SFDR			87		
SINAD			84		
REFERENCE INPUT					
$V_{ref(H)}$ Voltage	$V_{ref(L)} < V_{ref(H)}$, $AV_{DD} - (V_{ref(H)} + V_{ref(L)})$ /2 > 1.2 V	0		AV_{DD}	V
$V_{ref(L)}$ Voltage	$V_{ref(L)} < V_{ref(H)}$, $AV_{DD} - (V_{ref(H)} + V_{ref(L)})$ /2 > 1.2 V	0		$AV_{DD}/2$	V
Reference input current	$V_{ref(L)}$ = GND, $V_{ref(H)} = AV_{DD}$ = 5 V		180	250	µA
	$V_{ref(L)}$ = GND, $V_{ref(H)} = AV_{DD}$ = 3 V		120	200	µA
Reference input impedance	$V_{ref(L)} < V_{ref(H)}$		31		kΩ
LOGIC INPUTS [3]					
$V_{I(L)}$, logic input LOW voltage	2.7 V ≤ IOV_{DD} ≤ 5.5 V			$0.3 \times IOV_{DD}$	V
	1.8 V ≤ IOV_{DD} ≤ 2.7 V			$0.1 \times IOV_{DD}$	
$V_{I(H)}$, logic input HIGH voltage	2.7 ≤ IOV_{DD} ≤ 5.5 V	$0.7 \times IOV_{DD}$			V
	1.8 ≤ IOV_{DD} < 2.7 V	$0.95 \times IOV_{DD}$			
Pin capacitance				3	pF
POWER REQUIREMENTS					
AV_{DD}		2.7		5.5	V
IOV_{DD}		1.8		5.5	
AI_{DD} (normal mode)	Input code = 32768, reference current included, no load				

(2) Ensured by design and characterization, not production tested.
(3) Ensured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IOI_{DD}			10	20	µA
AV_{DD} = 3.6 V to 5.5 V	V_{IH} = IOV_{DD} and V_{IL} = GND		0.65	1.0	mA
AV_{DD} = 2.7 V to 3.6 V			0.6	0.96	
AI_{DD} (all power-down modes)					
AV_{DD} = 3.6 V to 5.5 V	V_{IH} = IOV_{DD} and V_{IL} = GND		0.2	2	µA
AV_{DD} = 2.7 V to 3.6 V			0.05	2	
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_L = 2 mA, AV_{DD} = 5 V		89%		
TEMPERATURE RANGE					
Specified performance		−40		105	°C

PIN CONFIGURATION

V_{OUT}A	1		16	LDAC	
V_{OUT}B	2		15	$\overline{ENABLE}$	
V_{REF}H	3		14	A1	
AV_{DD}	4	DAC8554	13	A0	
V_{REF}L	5		12	IOV_{DD}	
GND	6		11	D_{IN}	
V_{OUT}C	7		10	SCLK	
V_{OUT}D	8		9	$\overline{SYNC}$	
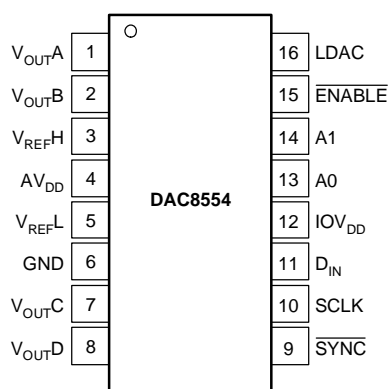
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{OUT}A	Analog output voltage from DAC A.
2	V_{OUT}B	Analog output voltage from DAC B.
3	V_{ref}H	Positive reference voltage input.
4	AV_{DD}	Power supply input, 2.7 V to 5.5 V.
5	V_{ref}L	Negative reference voltage input.
6	GND	Ground reference point for all circuitry on the part.
7	V_{OUT}C	Analog output voltage DAC C.
8	V_{OUT}D	Analog output voltage DAC D.
9	$\overline{SYNC}$	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock (unless $\overline{SYNC}$ is taken HIGH before this edge in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8554).
10	SCLK	Serial clock input. Data can be transferred at rates up to 50 MHz.
11	D_{IN}	Serial data input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input.
12	IOV_{DD}	Digital input-output power supply
13	A0	Address 0 — sets device address, see Table 2
14	A1	Address 1 — sets device address, see Table 2
15	ENABLE	Active LOW, $\overline{ENABLE}$ LOW connects the SPI interface to the serial port.

PIN DESCRIPTIONS (continued)

PIN	NAME	DESCRIPTION
16	LDAC	Load DACs, rising edge triggered, loads all DAC registers.

TIMING REQUIREMENTS[(1)(2)]

AV_{DD} = 2.7 V to 5.5 V, all specifications −40°C to 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1[(3)]	SCLK cycle time	$IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V	40			ns
		$IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V	20			
t_2	SCLK HIGH time	$IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V	20			ns
		$IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V	10			
t_3	SCLK LOW time	$IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V	20			ns
		$IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V	10			
t_4	$\overline{SYNC}$ falling edge to SCLK rising edge setup time	$IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V	0			ns
		$IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V	0			
t_5	Data setup time	$IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V	5			ns
		$IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V	5			
t_6	Data hold time	$IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V	4.5			ns
		$IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V	4.5			
t_7	24th SCLK falling edge to $\overline{SYNC}$ rising edge	$IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V	0			ns
		$IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V	0			
t_8	Minimum $\overline{SYNC}$ HIGH time	$IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V	40			ns
		$IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V	20			
t_9	24th $\overline{SCLK}$ falling edge to SYNC falling edge	$IOV_{DD} = AV_{DD}$ = 2.7 V to 5.5 V	130			ns

(1) All input signals are specified with $t_R = t_F$ = 3 ns (10% to 90% of AV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See Serial Write Operation timing diagram.
(3) Maximum SCLK frequency is 50 MHz at $IOV_{DD} = AV_{DD}$ = 3.6 V to 5.5 V and 25 MHz at $IOV_{DD} = AV_{DD}$ = 2.7 V to 3.6 V.

SERIAL WRITE OPERATION

TEXAS
INSTRUMENTS
www.ti.com
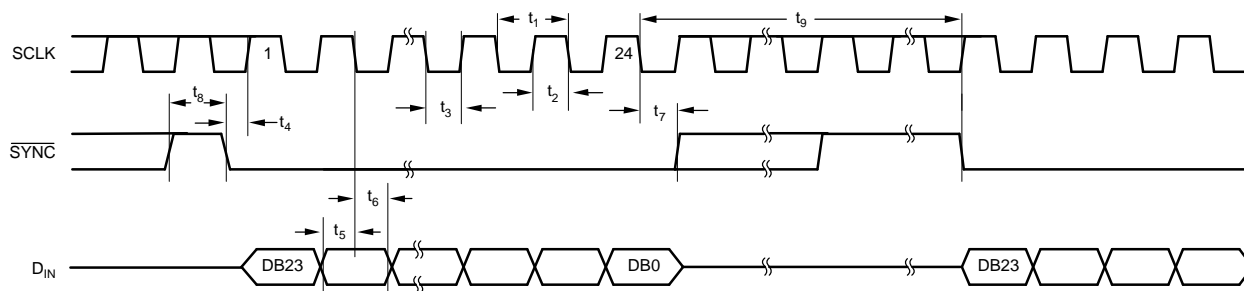
TYPICAL CHARACTERISTICS

At $T_A = 25°C$, unless otherwise noted

**LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR
vs
DIGITAL INPUT CODE**

Figure 1.

**LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR
vs
DIGITAL INPUT CODE**

Figure 2.

**LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR
vs
DIGITAL INPUT CODE**

Figure 3.

**LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR
vs
DIGITAL INPUT CODE**

Figure 4.

**LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR
vs
DIGITAL INPUT CODE**

Figure 5.

**LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR
vs
DIGITAL INPUT CODE**

Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, unless otherwise noted

**LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR
vs
DIGITAL INPUT CODE**

Channel C — AV_{DD} = 2.7 V, V_{ref} = 2.69 V

Figure 7.

**LINEARITY ERROR AND DIFFERENTIAL
LINEARITY ERROR
vs
DIGITAL INPUT CODE**

Channel D — AV_{DD} = 2.7 V, V_{ref} = 2.69 V

Figure 8.

**ZERO-SCALE ERROR
vs
TEMPERATURE**

AV_{DD} = 5 V, V_{ref} = 4.99 V

Figure 9.

**ZERO-SCALE ERROR
vs
TEMPERATURE**

AV_{DD} = 2.7 V, V_{ref} = 2.69 V

Figure 10.

**FULL-SCALE ERROR
vs
TEMPERATURE**

AV_{DD} = 5 V, V_{ref} = 4.99 V

Figure 11.

**FULL-SCALE ERROR
vs
TEMPERATURE**

AV_{DD} = 2.7 V, V_{ref} = 2.69 V
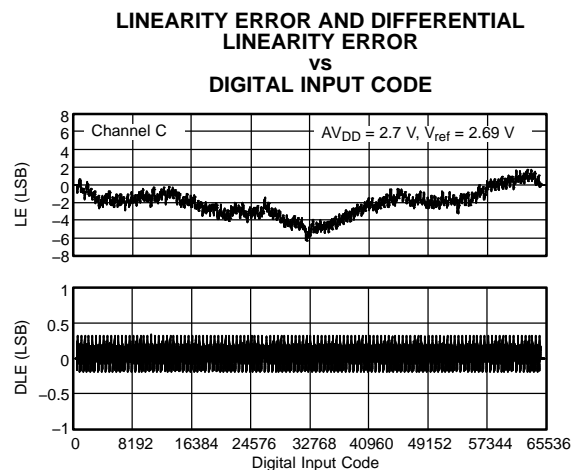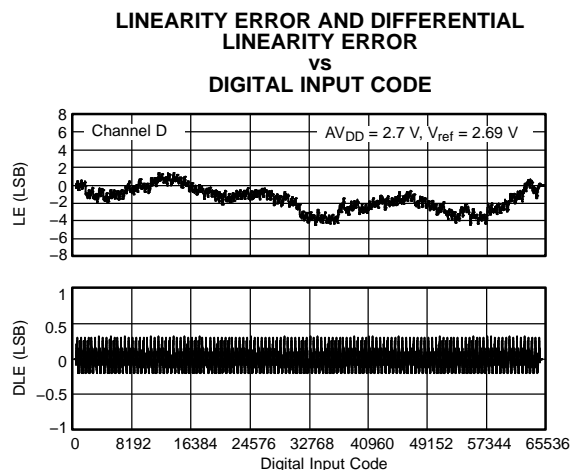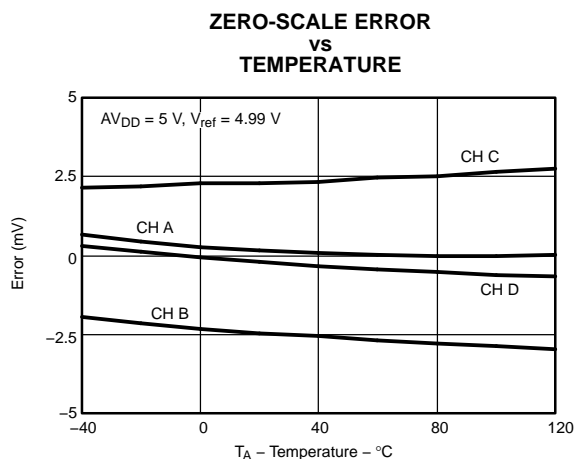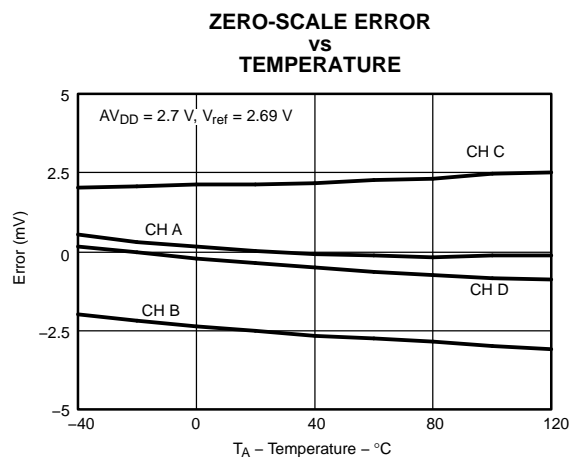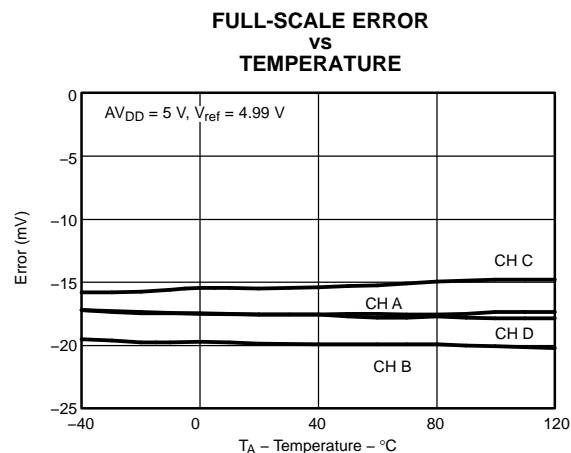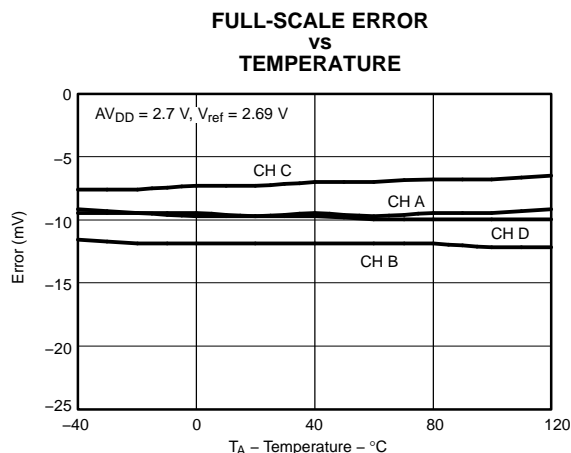
Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, unless otherwise noted

SINK CURRENT CAPABILITY (ALL CHANNELS)

Figure 13.

SOURCE CURRENT CAPABILITY (ALL CHANNELS)

Figure 14.

SOURCE CURRENT CAPABILITY (ALL CHANNELS)

Figure 15.

SUPPLY CURRENT
vs
DIGITAL INPUT CODE

Figure 16.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 17.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE
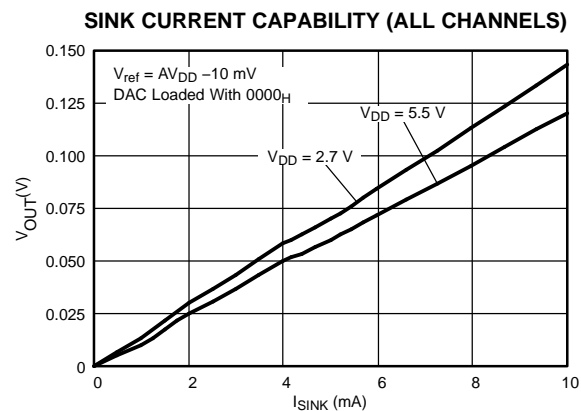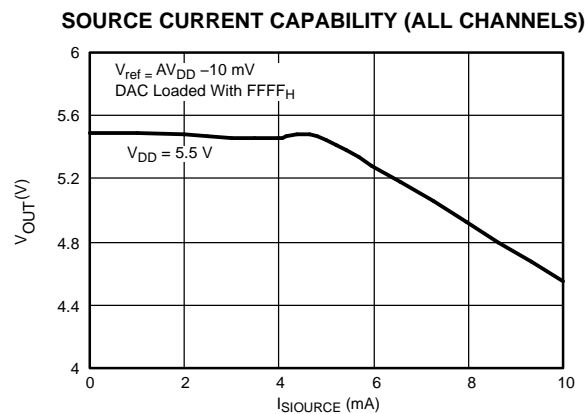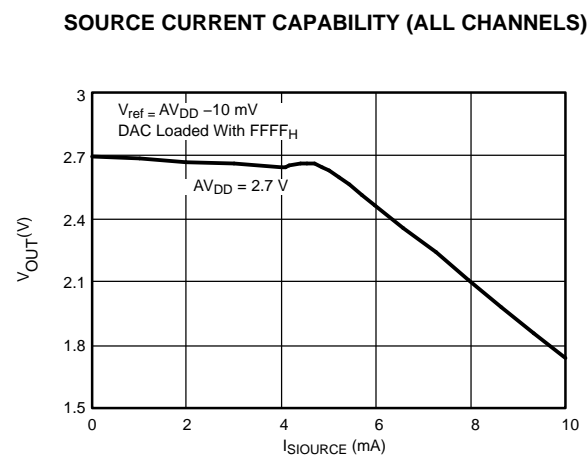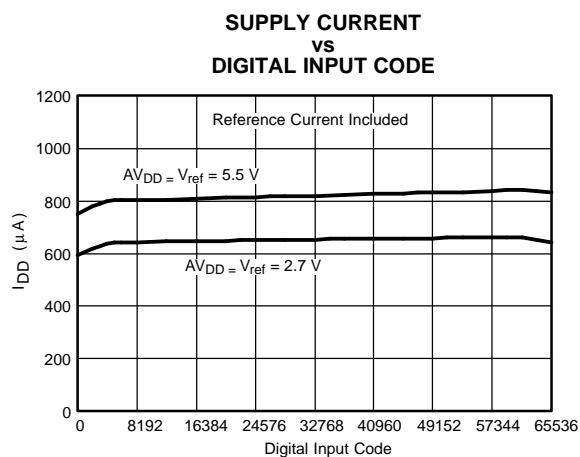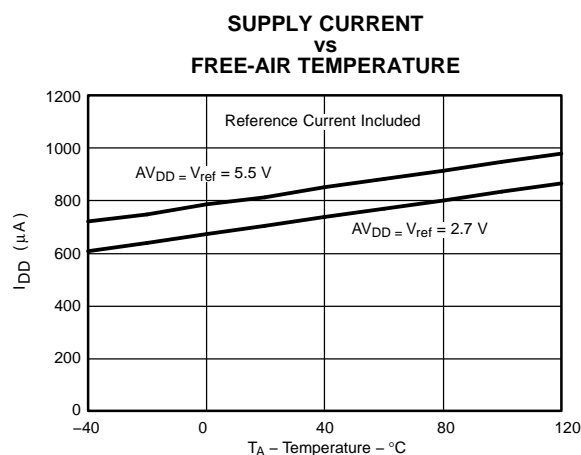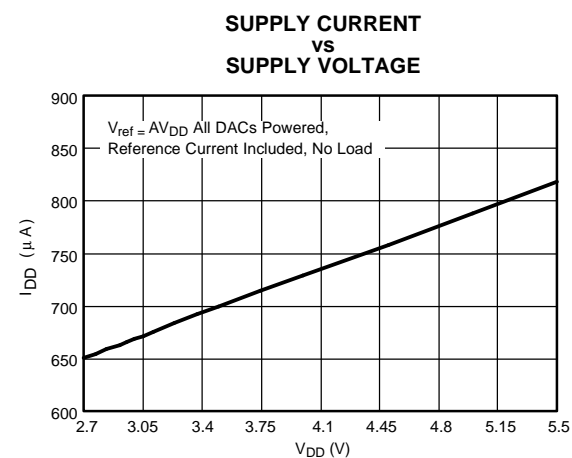
Figure 18.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25°C$, unless otherwise noted

SUPPLY CURRENT
vs
LOGIC INPUT VOLTAGE

$T_A = 25°C$, SYNC Input (All Other Inputs = GND
CHA Powered Up; All Other Channels in Powerdown
Reference Current Included

$IOV_{DD} = AV_{DD} = V_{ref} = 5$ V

Figure 19.

SUPPLY CURRENT
vs
LOGIC INPUT VOLTAGE

$T_A = 25°C$, SYNC Input (All Other Inputs = GND
CHA Powered Up; All Other Channels in Powerdown
Reference Current Included

$IOV_{DD} = AV_{DD} = V_{ref} = 2.7$ V

Figure 20.

HISTOGRAM OF CURRENT CONSUMPTION

$AV_{DD} = V_{ref} = 5$ V
Reference Current Included

Figure 21.

HISTOGRAM OF CURRENT CONSUMPTION

$AV_{DD} = V_{ref} = 2.7$ V
Reference Current Included

Figure 22.

POWER SPECTRAL DENSITY

$AV_{DD} = 5$ V,
$V_{ref} = 4.096$,
$f_{clk} = 1$ MSPS,
$F_{out} = 1$ kHz,
THD = 79 dB,
SNR = 96 dB

Figure 23.

TOTAL HARMONIC DISTORTION
vs
OUTPUT FREQUENCY

$AV_{DD} = V_{ref} = 5$ V,
−1 dB FSR Digital Input, $F_S = 1$ MSPS
Measurement Bandwidth = 20 kHz

THD

2nd Harmonic

3rd Harmonic

Figure 24.

TEXAS INSTRUMENTS
www.ti.com

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25°C$, unless otherwise noted

FULL-SCALE SETTLING TIME: 5 V RISING EDGE
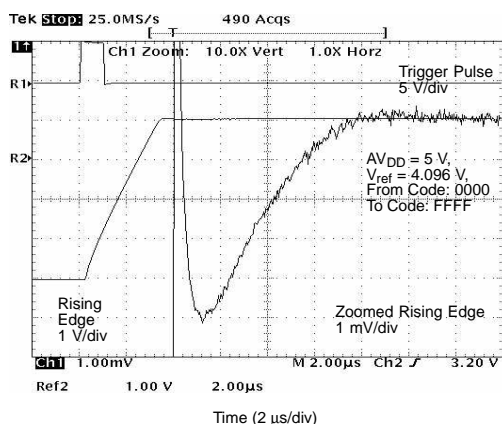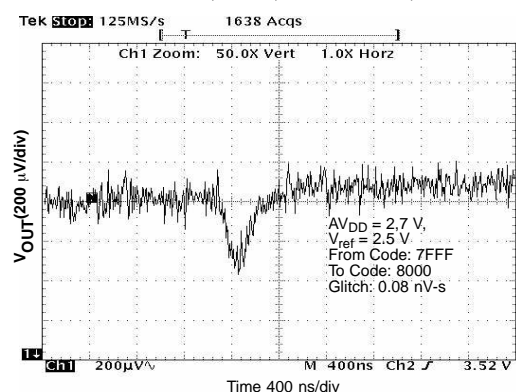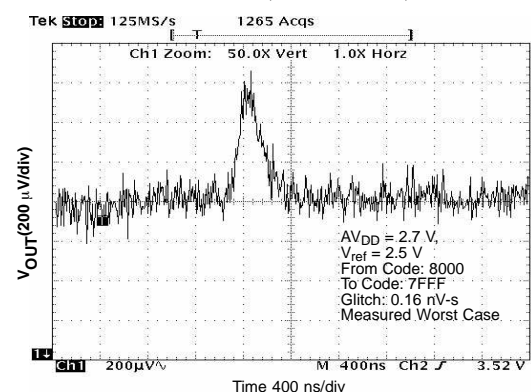

Figure 25.

FULL-SCALE SETTLING TIME: 5 V FALLING EDGE
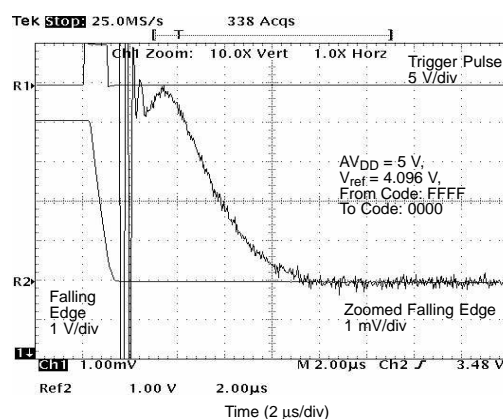
Figure 26.

HALF-SCALE SETTLING TIME: 5 V RISING EDGE
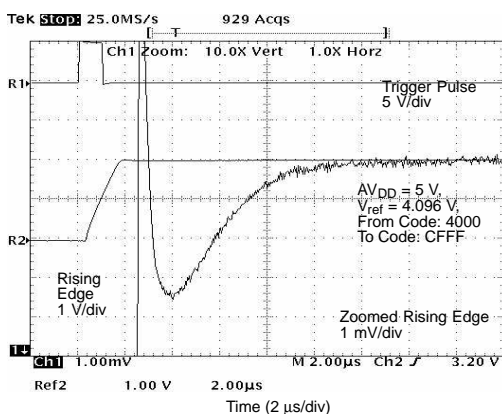
Figure 27.

HALF-SCALE SETTLING TIME: 5 V FALLING EDGE
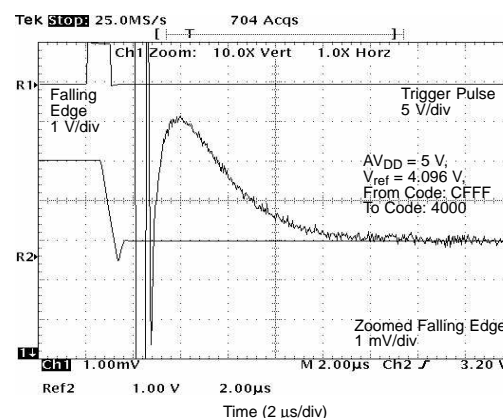
Figure 28.

FULL-SCALE SETTLING TIME: 2.7 V RISING EDGE
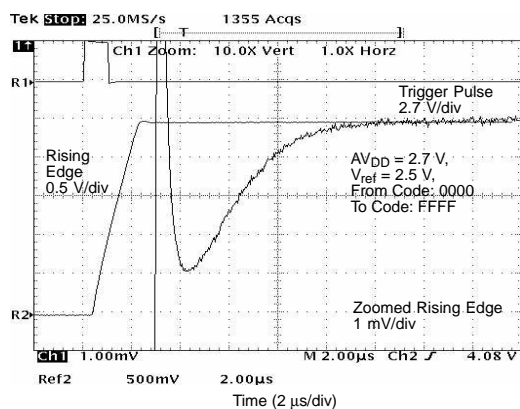
Figure 29.

FULL-SCALE SETTLING TIME: 2.7 V FALLING EDGE
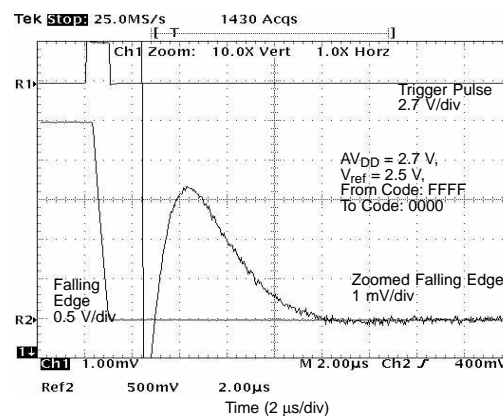
Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, unless otherwise noted

HALF-SCALE SETTLING TIME: 2.7 V RISING EDGE

Figure 31.

HALF-SCALE SETTLING TIME: 2.7 V FALLING EDGE

Figure 32.

GLITCH ENERGY: 5 V, 1 LSB STEP, RISING EDGE

Figure 33.

GLITCH ENERGY: 5 V, 1 LSB STEP, FALLING EDGE

Figure 34.

GLITCH ENERGY: 5 V, 16 LSB STEP, RISING EDGE

Figure 35.

GLITCH ENERGY: 5 V, 16 LSB STEP, FALLING EDGE

Figure 36.

TEXAS
INSTRUMENTS
www.ti.com
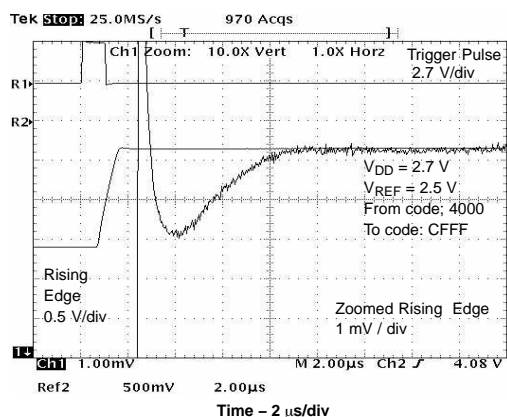
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, unless otherwise noted

GLITCH ENERGY: 5 V, 256 LSB STEP, RISING EDGE
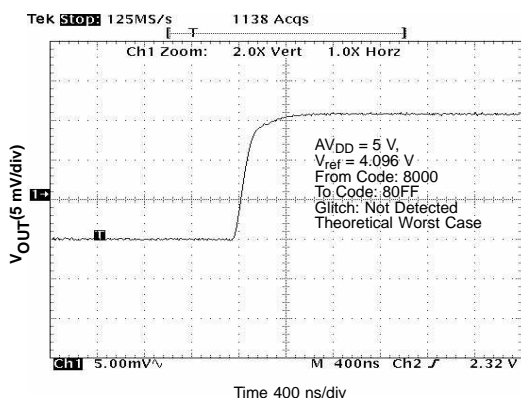
Figure 37.

GLITCH ENERGY: 5 V, 256 LSB STEP, FALLING EDGE
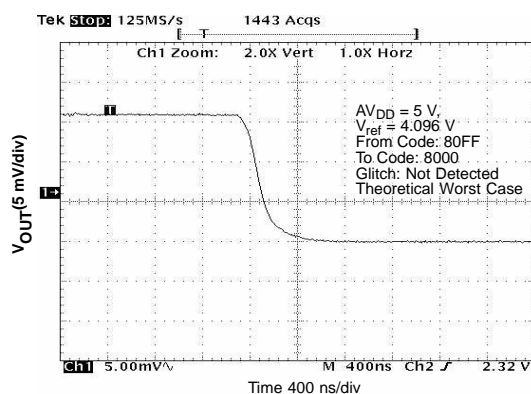
Figure 38.

GLITCH ENERGY:; 2.7 V, 1 LSB STEP, RISING EDGE

Figure 39.

GLITCH ENERGY: 2.7 V, 1 LSB STEP, FALLING EDGE

Figure 40.

GLITCH ENERGY: 2.7 V, 16 LSB STEP, RISING EDGE
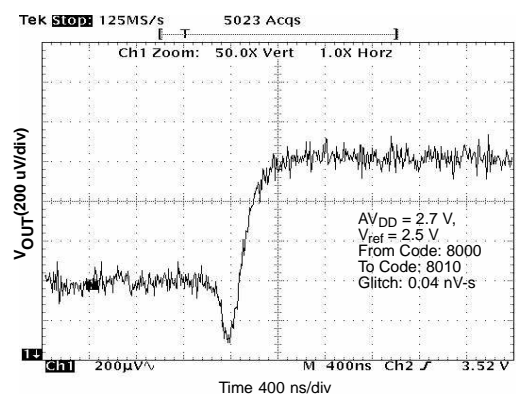
Figure 41.

GLITCH ENERGY: 2.7 V, 16 LSB STEP, FALLING EDGE
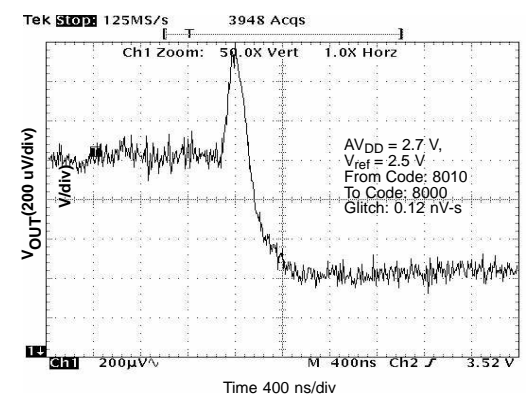
Figure 42.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25°C$, unless otherwise noted

GLITCH ENERGY: 2.7 V, 16 LSB STEP, RISING EDGE

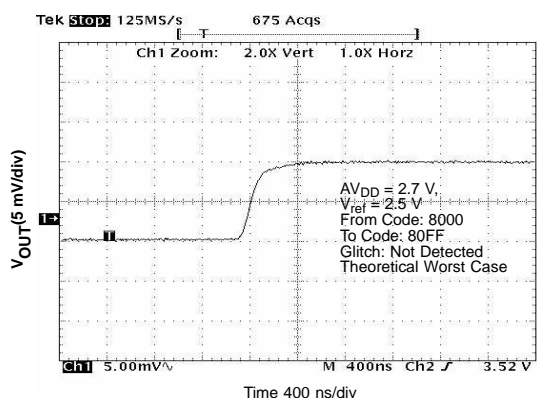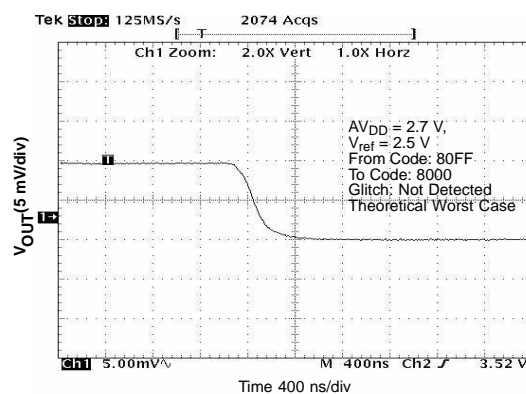**Figure 43.**

GLITCH ENERGY: 2.7 V, 16 LSB STEP, FALLING EDGE
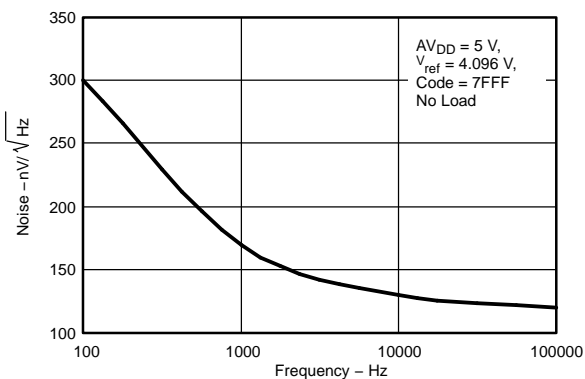

Figure 44.

OUTPUT NOISE DENSITY

Figure 45.

**SIGNAL-TO-NOISE RATIO
vs
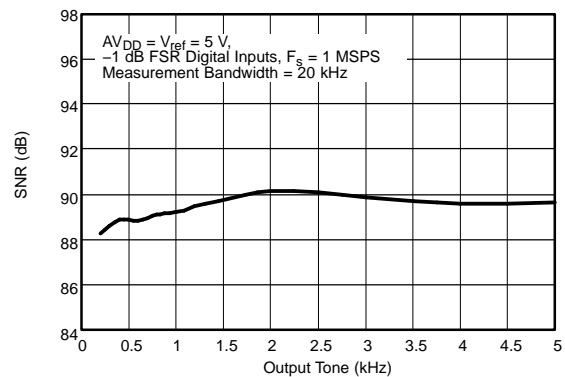OUTPUT FREQUENCY**

Figure 46.

TEXAS INSTRUMENTS
www.ti.com

THEORY OF OPERATION

DAC SECTION

The architecture of each channel of the DAC8554 consists of a resistor-string DAC followed by an output buffer amplifier. Figure 47 shows a simplified block diagram of the DAC architecture.
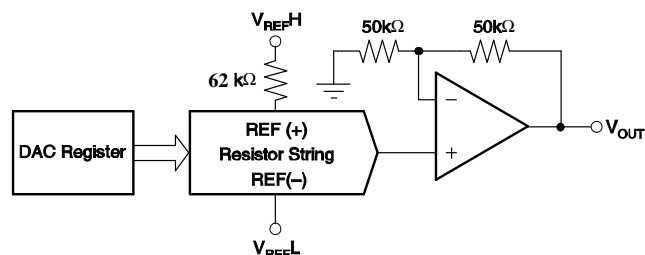
Figure 47. DAC8554 Architecture

The input coding for each device is unipolar straight binary, so the ideal output voltage is given by:

$$V_{OUT}X = 2 \times V_{REF}L + \left[V_{REF}H - V_{REF}L \right] \times \frac{D_{IN}}{65536}$$

where D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

The resistor string section is shown in Figure 48. It is simply a divide-by-2 resistor followed by a string of resistors. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. This voltage is then applied to the output amplifier by closing one of the switches connecting the string to the amplifier.

OUTPUT AMPLIFIER

Each output buffer amplifier is capable of generating rail-to-rail voltages on its output which approaches an output range of 0 V to AV_{DD} (gain and offset errors must be taken into account). Each buffer is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics.

SERIAL INTERFACE

The DAC8554 uses a 3-wire serial interface (SYNC, SCLK, and D_{IN}), which is compatible with SPI™, QSPI™, and Microwire™ interface standards, as well as most DSPs. See the serial write operation timing diagram for an example of a typical write sequence.
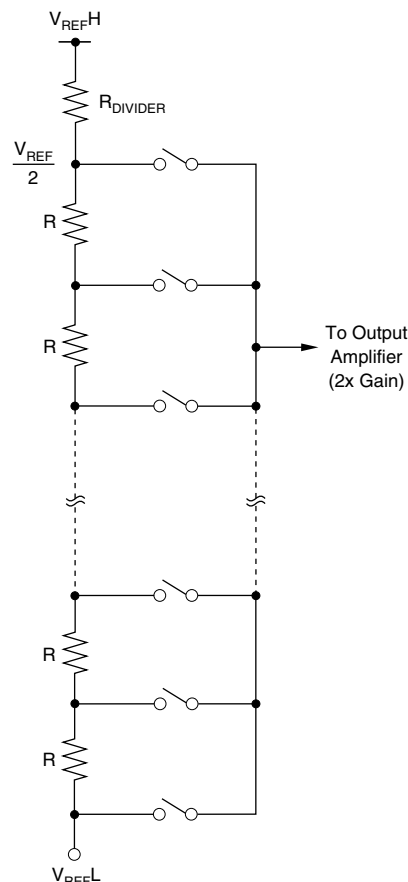
Figure 48. Resistor String

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line is clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the DAC8554 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register gets locked. Further clocking does not change the shift register data. Once 24 bits are locked into the shift register, the 8 MSBs are used as control bits and the 16 LSBs are used as data. After receiving the 24th falling clock edge, DAC8554 decodes the 8 control bits and 16 data bits to perform the required function, without waiting for a $\overline{SYNC}$ rising edge. A new SPI sequence starts at the next falling edge of $\overline{SYNC}$. A rising edge of $\overline{SYNC}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs.

After the 24th falling edge of SCLK is received, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to properly begin the next cycle.

To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible. (Refer to the *Typical Characteristics* section for the *Supply Current vs Logic Input Voltage* transfer characteristic curve.

IOV$_{DD}$ AND VOLTAGE TRANSLATORS

The IOV$_{DD}$ pin powers the digital input structures of the DAC8554. For single-supply operation, it can be tied to AV$_{DD}$. For dual-supply operation, the IOV$_{DD}$ pin provides interface flexibility with various CMOS logic families and it should be connected to the logic supply of the system. Analog circuits and internal logic of the DAC8554 use AV$_{DD}$ as the supply voltage. The external logic high inputs get translated to AV$_{DD}$ by level shifters. These level shifters use the IOV$_{DD}$ voltage as a reference to shift the incoming logic HIGH levels to AV$_{DD}$. IOV$_{DD}$ is ensured to operate from 2.7 V to 5.5 V regardless of the AV$_{DD}$ voltage, which ensures compatibility with various logic families. Although specified down to 2.7 V, IOV$_{DD}$ will operate at as low as 1.8 V with degraded timing and temperature performance. For lowest power consumption, logic V$_{IH}$ levels should be as close as possible to IOV$_{DD}$, and logic V$_{IL}$ levels should be as close as possible to GND voltages

INPUT SHIFT REGISTER

The input shift register (SR) of the DAC8554 is 24 bits wide, as shown in Figure 49, and is made up of 8 control bits (DB23–DB16) and 16 data bits (DB15–DB0). The first two control bits (DB23 and DB22) are the address match bits. The DAC8554 offers additional hardware-enabled addressing capability allowing a single host to talk to up to four DAC8554s through a single SPI bus without any glue logic, enabling up to 16-channel operation. The state of DB23 should match the state of pin A1; similarly, the state of DB22 should match the state of pin A0. If there is no match, the control command and the data (DB21...DB0) are ignored by the DAC8554. That is, if there is no match, the DAC8554 is not addressed. Address matching can be overridden by the broadcast update, as will be explained.

LD1 (DB21) and LD0 (DB20) control the updating of each analog output with the specified 16-bit data value or power-down command. Bit DB19 is a *Don't*

Care bit which does not affect the operation of the DAC8554 and can be 1 or 0. The DAC channel select bits (DB18, DB17) control the destination of the data (or power-down command) from DAC A through DAC D. The final control bit, PD0 (DB16), selects the power-down mode of the DAC8554 channels.

The DAC8554 also supports a number of different load commands. The load commands include broadcast commands to address all the DAC8554s on an SPI bus. The load commands can be summarized as follows:

DB21 = 0 and DB20 = 0: Single-channel store. The temporary register (data buffer) corresponding to a DAC selected by DB18 and DB17 is updated with the contents of SR data (or power-down).

DB21 = 0 and DB20 = 1: Single-channel update. The temporary register and DAC register corresponding to a DAC selected by DB18 and DB17 are updated with the contents of SR data (or power-down).

DB21 = 1 and DB20 = 0: Simultaneous update. A channel selected by DB18 and DB17 gets updated with the SR data, and simultaneously, all the other channels get updated with previous stored data (or power-down) from temporary registers.

DB21 = 1 and DB20 = 1: Broadcast update. All the DAC8554s on the SPI bus respond, regardless of address matching. If DB18 = 0, then SR data gets ignored, all channels from all DAC8554s get updated with previously stored data (or power-down). If DB18 = 1, then SR data (or power-down) updates all channels of all DAC8554s in the system. This broadcast update feature allows the simultaneous update of up to 16 channels.

Power-down/data selection is as follows:

DB16 is a power-down flag. If this flag is set, then DB15 and DB14 select one of the four power-down modes of the device as described in Table 1. If DB16 = 1, DB15 and DB14 no longer represent the two MSBs of data, they represent a power-down condition described in Table 1. Similar to data, power-down conditions can be stored at the temporary registers of each DAC. It is possible to update DACs simultaneously either with data, power-down, or a combination of both.

Refer to Table 2 for more information.

Table 1. DAC8554 Power-Down Modes

PD0 (DB16)	PD1 (DB15)	PD2 (DB14)	OPERATING MODE
1	0	0	Output high impedance
1	0	1	Output typically 1 kΩ to GND
1	1	0	Output typically 100 kΩ to GND
1	1	1	Output high impedance

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the addressed DAC register is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register is reset and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (see Figure 50).

POWER-ON RESET

The DAC8554 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC registers are filled with zeros and the output voltages are set to zero-scale; they remain there until a valid write sequence and load command is made to the respective DAC channel. This is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before power is applied to the device.

DB23   DB12

A1	A0	LD1	LD0	X	DAC Select 1	DAC Select 0	PD0	D15	D14	D13	D12

DB11   DB0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 49. DAC8554 Data Input Register Format

Table 2. Control Matrix

| DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13-DB0	DESCRIPTION
A1	A0	LD 1	LD 0	Don't Care	DAC Sel 1	DAC Sel 0	PD0	MSB	MSB-1	MSB-2...LSB	
(Address Select)											
0/1	0/1					See Below					This address selects 1 of 4 possible devices on a single SPI data bus based on each device's address pin(s) state.
A0 and A1 should correspond to the package address set via pins 13 and 14.		0	0	X	0	0	0		Data		Write to buffer A with data
		0	0	X	0	1	0		Data		Write to buffer B with data
		0	0	X	1	0	0		Data		Write to buffer C with data
		0	0	X	1	1	0		Data		Write to buffer D with data
		0	0	X	(00, 01, 10, or 11)		1	See Table 1		0	Write to buffer (selected by DB17 and DB18) with power-down command
		0	1	X	(00, 01, 10, or 11)		0		Data		Write to buffer with data and load DAC (selected by DB17 and DB18)
		0	1	X	(00, 01, 10, or 11)		1	See Table 1		0	Write to buffer with power-down command and load DAC (selected by DB17 and DB18)
		1	0	X	(00, 01, 10, or 11)		0		Data		Write to buffer with data (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers.
		1	0	X	(00, 01, 10, or 11)		1	See Table 1		0	Write to buffer with power-down command (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers.
Broadcast Modes											
X	X	1	1	X	0	X	X		X		Simultaneously update all channels of all DAC8554 devices in the system with data stored in each channels temporary register.
X	X	1	1	X	1	X	0		Data		Write to all devices and load all DACs with SR data
X	X	1	1	X	1	X	1	See Table 1		0	Write to all devices and load all DACs with power-down command in SR.
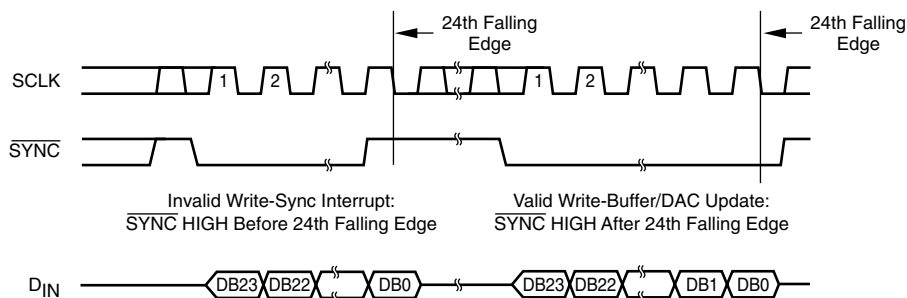
Figure 50. Interrupt and Valid $\overline{SYNC}$ Timing

POWER-DOWN MODES

The DAC8554 utilizes four modes of operation. These modes are accessed by setting three bits (PD2, PD1, and PD0) in the shift register and performing a *Load* action to the DACs. The DAC8554 offers a very flexible power-down interface based on channel register operation. A channel consists of a single 16-bit DAC with power-down circuitry, a temporary storage register (TR), and a DAC register (DR). TR and DR are both 18-bit wide. Two MSBs represent power-down condition and 16 LSBs represent data for TR and DR. By adding bits 17 and 18 to TR and DR, a power-down condition can be temporarily stored and used just like data. Internal circuits ensure that DB15 and DB14 get transferred to TR17 and TR16 (DR17 and DR16), when DB16 = 1.

The DAC8554 treats the power-down condition like data and all the operational modes are still valid for power-down. It is possible to broadcast a power-down condition to all the DAC8554s in a system, or it is possible to simultaneously power-down a channel while updating data on other channels.

DB16, DB15, and DB14 = 100 (or 111) represent a power-down condition with Hi-Z output impedance for a selected channel. 101 represents a power-down condition with 1k output impedance and 110 represents a power-down condition with 100k output impedance.

Individual channels can separately be powered down, reducing the total power consumption. When all channels are powered down, the DAC8554 power consumption drops below 2 µA. There is no power -up command. When a channel is updated with data, it automatically exits power-down. All channels exit power-down simultaneously after a broadcast data update. The time to exit power-down is approximately 5 µs. See *Table 1 and Table 2* for power-down operation details.
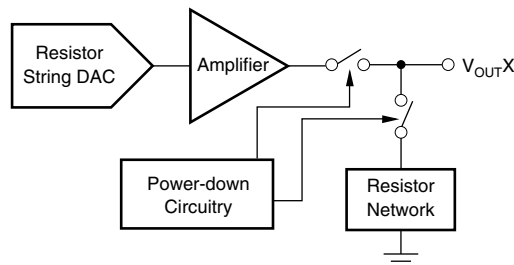

Figure 51. Output Stage During Power-Down (High-Impedance)

OPERATION EXAMPLES

Example 1: Write to data buffer A; through buffer D; load DAC A through DAC D simultaneously

- 1st — Write to data buffer A:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	0	X	0	0	0	D15	—	D1	D0

- 2nd — Write to data buffer B:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	0	X	0	1	0	D15	—	D1	D0

- 3rd — Write to data buffer C:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	0	X	1	0	0	D15	—	D1	D0

- 4th — Write to data buffer D and simultaneously update all DACs:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	1	0	X	1	1	0	D15	—	D1	D0

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the 4th write sequence. (The DAC voltages update simultaneously after the 24th SCLK falling edge of the 4th write cycle).

Example 2: Load New Data to DAC A through DAC D sequentially

- 1st — Write to data buffer A and load DAC A: DAC A output settles to specified value upon completion:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	1	X	0	0	0	D15	—	D1	D0

- 2nd — Write to data buffer B and load DAC B: DAC B output settles to specified value upon completion:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	1	X	0	1	0	D15	—	D1	D0

- 3rd — Write to data buffer C and load DAC C: DAC C output settles to specified value upon completion:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	1	X	1	0	0	D15	—	D1	D0

- 4th — Write to data buffer D and load DAC D: DAC D output settles to specified value upon completion:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	1	X	1	1	0	D15	—	D1	D0

After completion of each write cycle, DAC analog output settles to the voltage specified.

Example 3: Power-down DAC A and DAC B to 1 kΩ and Power-down DAC C and DAC D to 100 kΩ simultaneously

- Write power-down command to data buffer A: DAC A to 1 kΩ.

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	0	X	0	0	1	0	1	X	—

- Write power-down command to data buffer B: DAC B to 1 kΩ.

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	0	X	0	1	1	0	1	X	—

- Write power-down command to data buffer C: DAC C to 1 kΩ.

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	0	X	1	0	1	1	0	X	—

- Write power-down command to data buffer D: DAC D to 100 kΩ and simultaneously update all DACs.

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	1	0	X	1	1	1	1	0	X	—

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously power-down to each respective specified mode upon completion of the 4th write sequence.

Example 4: Power-Down DAC A Through DAC D to High-Impedance Sequentially:

- Write power-down command to data buffer A and load DAC A: DAC A output = Hi-Z:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	1	X	0	0	1	1	1	X	—

- Write power-down command to data buffer B and load DAC B: DAC B output = Hi-Z:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	1	X	0	1	1	1	1	x	—

- Write power-down command to data buffer C and load DAC C: DAC C output = Hi-Z:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	1	X	1	0	1	1	1	X	—

- Write power-down command to data buffer D and load DAC D: DAC D output = Hi-Z:

A1	A0	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	1	X	1	1	1	1	1	X	—

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power-down to high-impedance upon completion of the 1st, 2nd, 3rd, and 4th write sequences, respectively.

LDAC FUNCTIONALITY

The DAC8554 offers both a software and hardware simultaneous update function. The DAC8554 double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. The software simultaneous update capability is controlled by the load 1 (LD1) and load 0 (LD0) control bits. By setting load 1 equal to 1 all of the DAC registers will be updated on the falling edge of the 24th clock signal. When the new data has been entered into the device, all of the DAC outputs can be updated simultaneously and synchronously with the clock.

DAC8554 data updates are *synchronized* with the falling edge of the 24th SCLK cycle, which follows a falling edge of SYNC. For such *synchronous* updates, the LDAC pin is not required and it must be connected to GND permanently. The LDAC pin is used as a positive edge triggered timing signal for *asynchronous* DAC updates. Data buffers of all channels must be loaded with desired data before LDAC is triggered. After a low-to-high LDAC transition, all DACs are simultaneously updated with the contents of their corresponding data buffers. If the content of a data buffer is not changed by the serial interface, the corresponding DAC output will remain unchanged after the LDAC trigger.

ENABLE PIN

For normal operation, the enable pin must be tied to a logic low. If the enable pin is tied high, the DAC8554 stops listening to the serial port. This can be useful for applications that share the same serial port.

MICROPROCESSOR INTERFACING

DAC8554 TO 8051 Interface

See Figure 52 for a serial interface between the DAC8554 and a typical 8051-type micro controller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8554, while RXD drives the serial data line of the device. The SYNC signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8554, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second and third write cycle is initiated to transmit the remaining data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which presents the LSB first, while the DAC8554 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed.
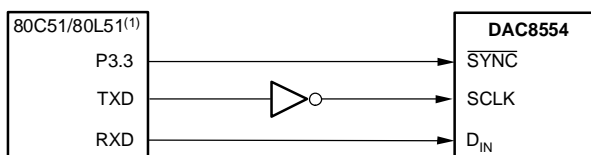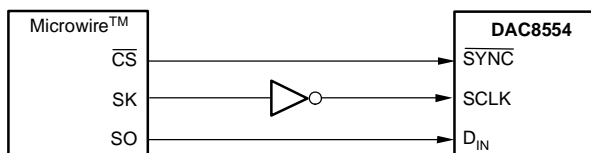
(1) Additional pins omitted for clarity.

Figure 52. DAC8554 to 80C51/80L51 Interface

DAC8554 to Microwire Interface

Figure 53 shows an interface between the DAC8554 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8554 on the rising edge of the CK signal.
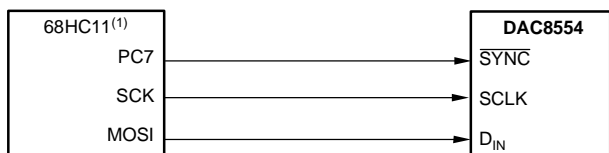

(1) Additional pins omitted for clarity.

Microwire is a registered trademark of National Semiconductor.

Figure 53. DAC8554 to Microwire Interface

DAC8554 to 68HC11 Interface

Figure 54 shows a serial interface between the DAC8554 and the 68HC11 micro controller. SCK of the 68HC11 drives the SCLK of the DAC8554, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7), similar to the 8051 diagram.

(1) Additional pins omitted for clarity.

Figure 54. DAC8554 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is 0 and its CPHA bit is 1. This configuration

causes data appearing on the MOSI output to be valid on the falling edge of SCLK. When data is being transmitted to the DAC, the SYNC line is held LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data is transmitted MSB first.) In order to load data to the DAC8554, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC. PC7 is taken HIGH at the end of this procedure.

DAC8554 to TMS320 DSP Interface

Figure 55 shows the connections between the DAC8554 and a TMS320 Digital Signal Processor (DSP). A Single DSP can control up to four DAC8554s without any interface logic.
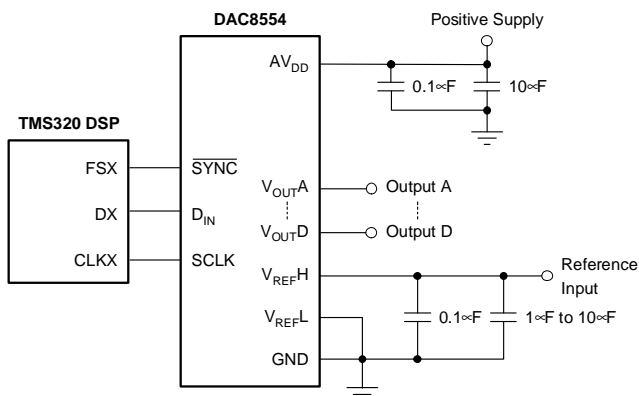
Figure 55. DAC8554 to TMS320 DSP

APPLICATION INFORMATION

CURRENT CONSUMPTION

The DAC8554 consumes a maximum of 250 µA at AV_{DD} = 5 V and 240 µA at AV_{DD} = 3 V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if V_{IH} << IOV_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC.

In power-down mode, typical current consumption is 200 nA per channel. A delay time of 10 ms to 20 ms after a power-down command is issued to the DAC is typically sufficient for the power-down current to drop below 10 µA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC8554 output stage is capable of driving loads of up to 1000 pF while remaining stable. Within the offset and gain error margins, the DAC8554 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2 kΩ can be driven by the DAC8554 while achieving good load regulation. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 100 mV of the DAC's output voltage characteristic. Under resistive loading conditions, good linearity is preserved as long as the output voltage is at least 100 mV below the AVDD voltage.

CROSSTALK AND AC PERFORMANCE

The DAC8554 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.5LSBs. The AC crosstalk measured (for a full-scale, 1 kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under −100 dB.

In addition, the DAC8554 can achieve typical AC performance of 96 dB signal-to-noise ratio (SNR) and 85 dB total harmonic distortion (THD), making the DAC8554 a solid choice for applications requiring high SNR at output frequencies at or below 10 kHz.

OUTPUT VOLTAGE STABILITY

The DAC8554 exhibits excellent temperature stability of 5 ppm/°C typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a ±25 µV window for a ±1°C ambient temperature change.

Good power-supply rejection ratio (PSRR) performance reduces supply noise present on AV_{DD} from appearing at the outputs to well below 10 µV-s. Combined with good dc noise performance and true 16-bit differential linearity, the DAC8554 becomes a perfect choice for closed-loop control applications.

SETTLING TIME AND OUTPUT GLITCH PERFORMANCE

DAC8554 settles to ±0.003% of its full-scale range within 10 µs, driving a 200 pF 2 KΩ load. For good settling performance the outputs should not approach the top and bottom rails. Small signal settling time is under 1 µs, enabling data update rates exceeding 1 MSPS for small code changes.

Many applications are sensitive to undesired transient signals such as glitch. DAC8554 has a proprietary, ultra-low glitch architecture addressing such applications. Code-to-code glitches rarely exceed millivolt and they last under 0.3 µs. Typical glitch energy is an outstanding 0.15 nV-s. Theoretical worst cast glitch should occur during a 256 LSB step, but it is so low, it cannot be detected.

DIFFERENTIAL AND INTERGRAL NONLINEARITY

DAC8554 uses precision thin film resistors to achieve monotonicity and good linearity. Typical linearity error is ±4 LSBs; ±0.3 mV error for a 5 V range. Differential linearity is typically ±0.25 LSBs, ±19 µV error for a consecutive code change.

USING THE REF02 AS A POWER SUPPLY FOR THE DAC8554

Due to the extremely low supply current required by the DAC8554, a possible configuration is to use a REF02 +5 V precision voltage reference to supply the required voltage to the DAC8554s supply input as well as the reference input, as shown in Figure 56. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 will output a steady supply voltage for the DAC8554. If the REF02 is

used, the current it needs to supply to the DAC8554 is 0.85 mA typical for AV_{DD} = 5 V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5 kΩ load on a given DAC output) is:

0.85 mA + (5V/5 kΩ) = 1.085 mA
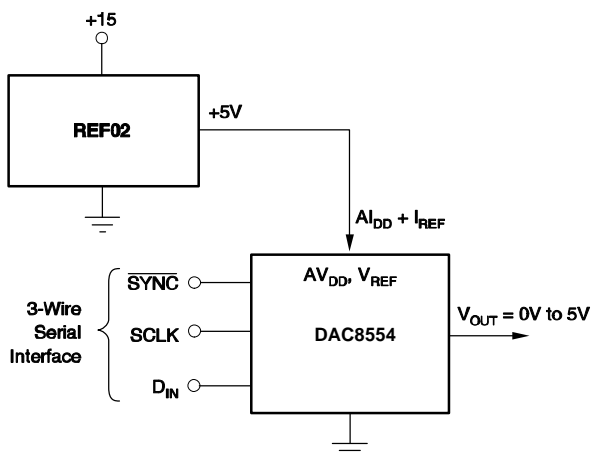
Figure 56. REF02 as a Power Supply to the DAC8554

BIPOLAR OPERATION USING THE DAC8554

The DAC8554 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 57. The circuit shown will give an output voltage range of $\pm V_{ref}$. Rail-to-rail operation at the amplifier output is achievable using an amplifier such as the OPA703, as shown in REFFigure 57.

The output voltage for any input code can be calculated as follows:

$$V_{OUT}X = \left[V_{ref} \times \frac{D}{65536} \times \frac{R1 + R2}{R1} - V_{ref} \times \frac{R2}{R1} \right]$$

where D represents the input code in decimal (0–65535).

With V_{ref} = 5 V, R1 = R2 = 10 kΩ.

$$V_{OUT}X - \frac{10 \times D}{65536} \left[+ 5 \text{ V} \right.$$

This is an output voltage range of ± 5 V with 0000_H corresponding to a –5 V output and $FFFF_H$ corresponding to a 5 V output. Similarly, using V_{ref} = 2.5 V a ± 2.5 V output voltage range can be achieved.
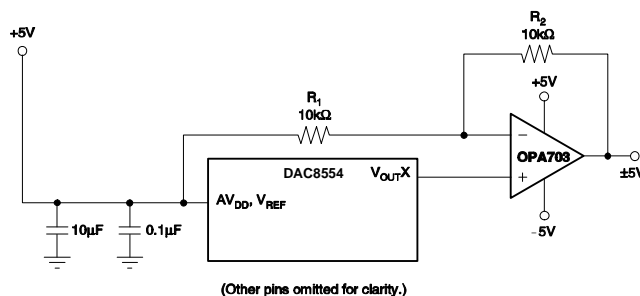
Figure 57. Bipolar Operation With the DAC8554

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8554 offers single-supply operation, and it will often be used in close proximity with digital logic, micro controllers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8554, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to AV_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, AV_{DD} should be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1 µF to 10 µF capacitor in parallel with a 0.1 µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100 µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors – all designed to essentially low-pass filter the supply, removing the high-frequency noise.

Up to four DAC8554 devices can be used on a single SPI bus without any glue logic to create a high channel count solution. Special attention is required to avoid digital signal integrity problems when using multiple DAC8554s on the same SPI bus. Signal integrity of $\overline{\text{SYNC}}$, SCLK, and D_{IN} lines will not be an issue as long as the rise times of these digital signals are longer than six times the propagation delay between any two DAC8554 devices. Propagation speed is approximately six inches/ns on standard PCBs. Therefore, if the digital signal rise time is 1 ns, the distance between any two DAC8554s have to be further apart on the PCB, the signal rise times should be reduced by placing series resistors at the drivers for $\overline{\text{SYNC}}$, SCLK, and D_{IN} lines. If the largest distance between any two DAC8554s must to be six inches, the rise time should be reduced to 6 ns with an RC network formed by the series resistor at the digital driver and the total trace and input capacitance on the PCB.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC8554IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8554IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8554IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8554IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PW (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS
INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
                     Post Office Box 655303 Dallas, Texas 75265