CY7C1020CV33

512 K (32 K × 16) Static RAM

Features

- Pin- and function-compatible with CY7C1020CV33
- Temperature Ranges
  - Commercial: 0 °C to 70 °C
  - Industrial: –40 °C to 85 °C
  - Automotive: –40 °C to 125 °C
- High speed
  - t_{AA} = 10 ns
- CMOS for optimum speed/power
- Low active power
  - 325 mW (max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin TSOP II package

Functional Description

The CY7C1020CV33 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

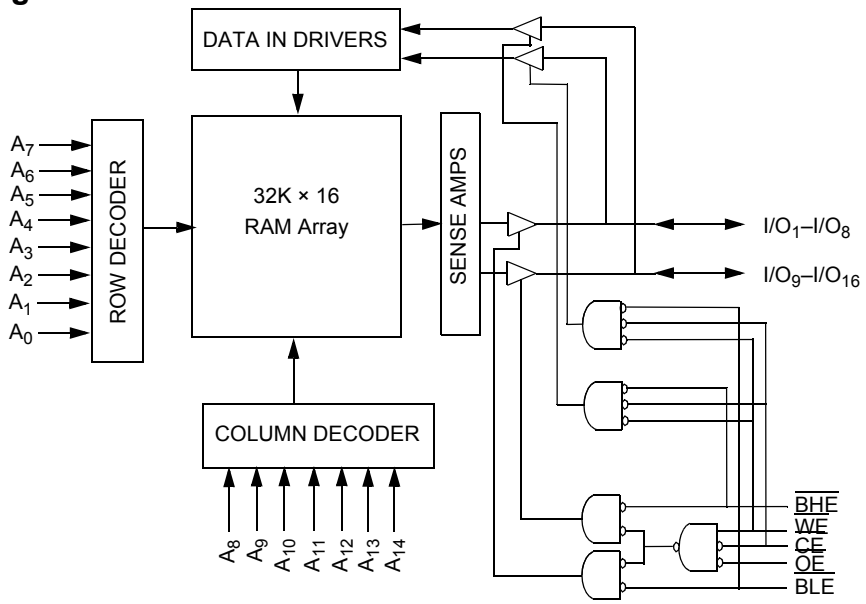
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{14}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_9 to I/O_{16}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1020CV33 is available in standard 44-pin TSOP Type II package.

Logic Block Diagram



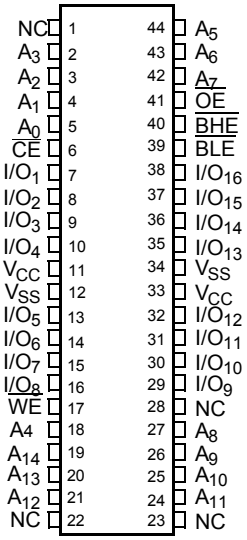
Contents

Selection Guide

		–10	–12	–15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial/Industrial	90	85	80	mA
	Automotive	–	–	85	mA
Maximum CMOS Standby Current	Commercial/Industrial	5	5	5	mA
	Automotive	–	–	10	mA

Pin Configuration [1]

TSOP II
Top View



Note
1. NC pins are not connected on the die.

Pin Definitions

Pin Name	TSOP - Pin Number	I/O Type	Description
A_0–A_{14}	5, 4, 3, 2, 18, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19	Input	**Address Inputs used to select one of the address locations**.
I/O_1–I/O_{16}	7-10, 13-16, 29-32, 35-38	Input/Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	1, 22, 23, 28	No Connect	**No Connects**. Not connected to the die.
$\overline{WE}$	17	Input/Control	**Write Enable Input, active LOW**. When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{CE}$	6	Input/Control	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	Input/Control	**Byte Write Select Inputs, active LOW**. $\overline{BHE}$ controls I/O_{16}–I/O_9, $\overline{BLE}$ controls I/O_8–I/O_1.
$\overline{OE}$	41	Input/Control	**Output Enable, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V_{SS}	12, 34	Ground	**Ground for the device**. Should be connected to ground of the system.
V_{CC}	11, 33	Power Supply	**Power Supply inputs to the device.**

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[2] .....–0.5 V to +4.6 V

DC voltage applied to outputs in high Z State[2] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage[2] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 10%
Industrial	–40 °C to +85 °C	3.3 V ± 10%
Automotive	–40 °C to +125 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		–10		–12		–15		Unit
				Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	–	0.4	–	0.4	V
V_{IH}	Input HIGH voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage[2]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	Commercial/ Industrial	–1	+1	–1	+1	–1	+1	µA
			Automotive	–	–	–	–	–20	+20	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, Output Disabled	Commercial/ Industrial	–1	+1	–1	+1	–1	+1	µA
			Automotive	–	–	–	–	–20	+20	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Commercial/ Industrial	–	90	–	85	–	80	mA
			Automotive	–	–	–	–	–	85	mA
I_{SB1}	Automatic CE power-down current —TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Commercial/ Industrial	–	15	–	15	–	15	mA
			Automotive	–	–	–	–	–	20	mA
I_{SB2}	Automatic CE power-down current —CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	Commercial/ Industrial	–	5	–	5	–	5	mA
			Automotive	–	–	–	–	–	10	mA

Capacitance[3]

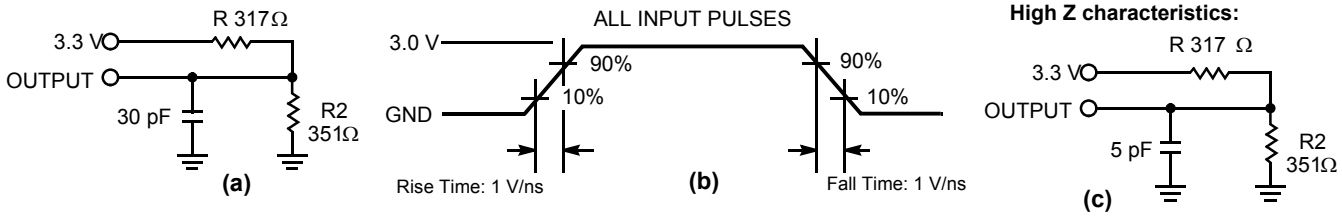
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance[3]

Parameter	Description	Test Conditions	44-pin TSOP-II	Unit
Θ_{JA}	Thermal resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	76.92	°C/W
Θ_{JC}	Thermal resistance (Junction to Case)		15.86	°C/W

Notes
2. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 0.5 V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[4]



Switching Characteristics

Over the Operating Range[4]

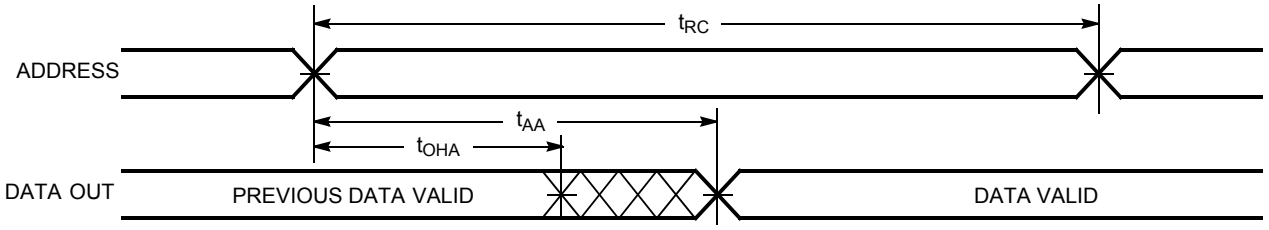
Parameter	Description	–10		–12		–15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read cycle time	10	–	12	–	15	–	ns
t_{AA}	Address to data valid	–	10	–	12	–	15	ns
t_{OHA}	Data hold from address change	3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	–	12	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	–	6	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[5]	0	–	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[5, 6]	–	5	–	6	–	7	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[5]	3	–	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[5, 6]	–	5	–	6	–	7	ns
t_{PU}[7]	$\overline{CE}$ LOW to power-up	0	–	0	–	0	–	ns
t_{PD}[7]	$\overline{CE}$ HIGH to power-down	–	10	–	12	–	15	ns
t_{DBE}	Byte enable to data valid	–	5	–	6	–	7	ns
t_{LZBE}	Byte enable to low Z	0	–	0	–	0	–	ns
t_{HZBE}	Byte disable to high Z	–	5	–	6	–	7	ns
Write Cycle[8]								
t_{WC}	Write cycle time	10	–	12	–	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	8	–	9	–	10	–	ns
t_{AW}	Address set-up to write end	7	–	8	–	10	–	ns
t_{HA}	Address hold from write end	0	–	0	–	0	–	ns
t_{SA}	Address set-up to write start	0	–	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	8	–	10	–	ns
t_{SD}	Data set-up to write end	5	–	6	–	8	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[5]	3	–	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[5, 6]	–	5	–	6	–	7	ns
t_{BW}	Byte enable to end of write	7	–	8	–	9	–	ns

Notes

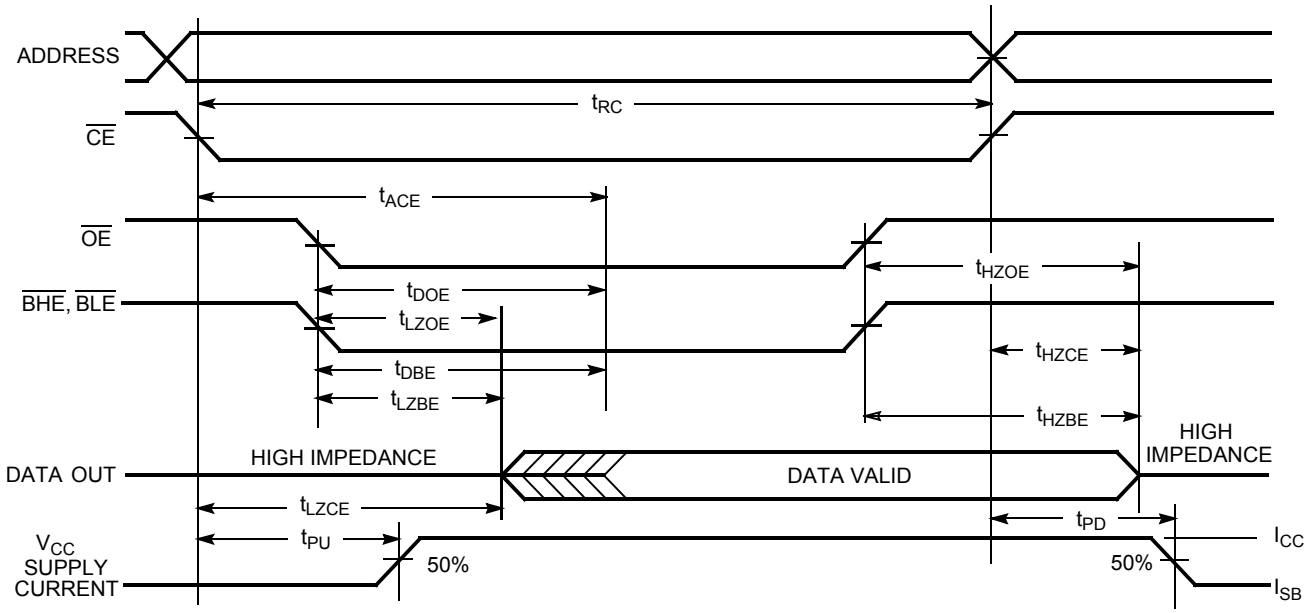
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
6. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
7. This parameter is guaranteed by design and is not tested.
8. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle No. 1[9, 10]



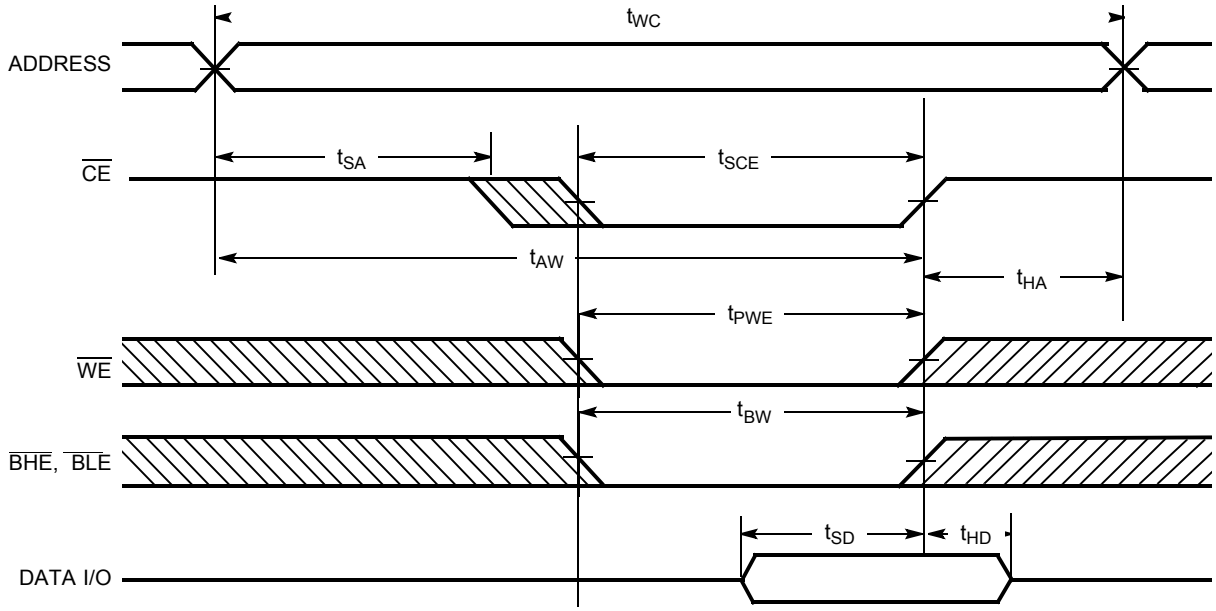
Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]



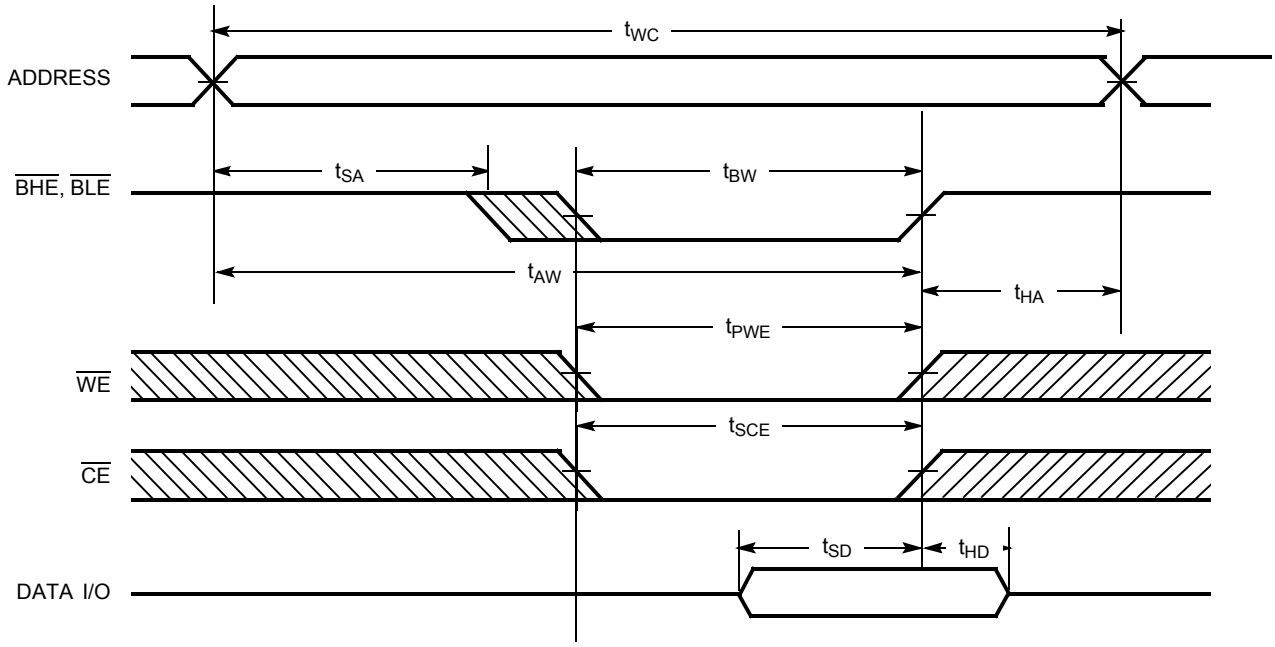
Notes
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
10. $\overline{WE}$ is HIGH for Read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Write Cycle No. 1 ($\overline{CE}$ Controlled)[12, 13]



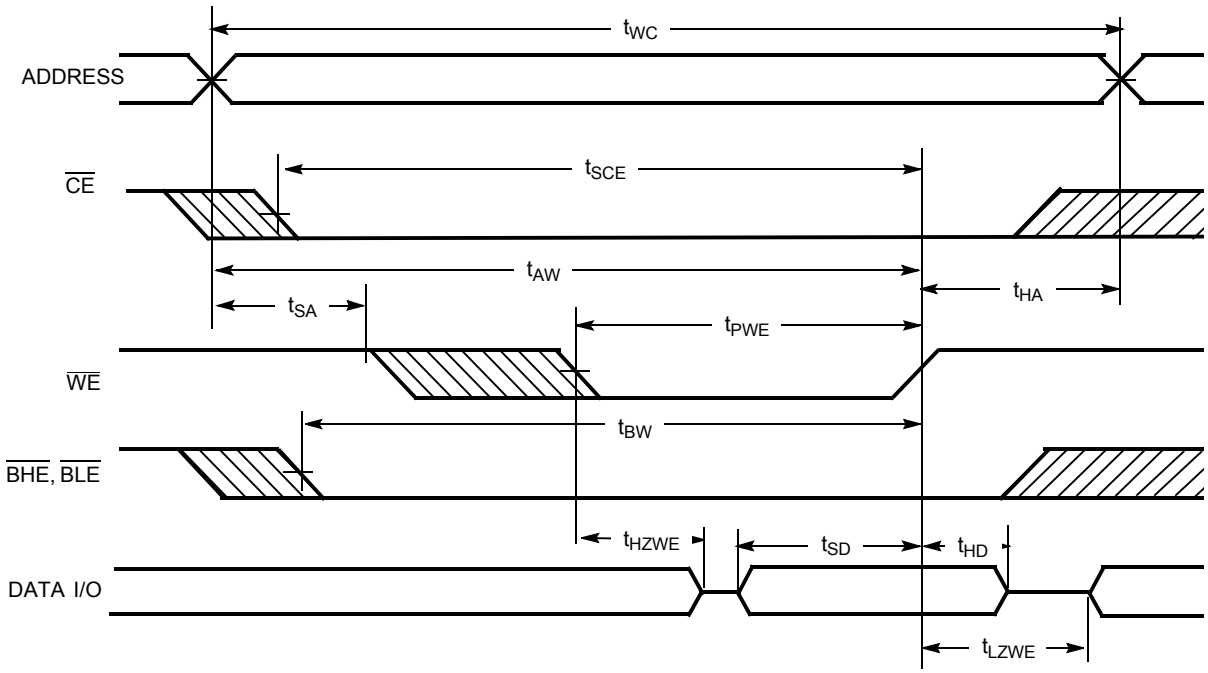
Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
12. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms *(continued)*

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read—All bits	Active (I_{CC})
			L	H	Data out	High Z	Read—Lower bits only	Active (I_{CC})
			H	L	High Z	Data out	Read—Upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write—All bits	Active (I_{CC})
			L	H	Data in	High Z	Write—Lower bits only	Active (I_{CC})
			H	L	High Z	Data in	Write—Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1020CV33-15ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1020CV33-15ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	Automotive

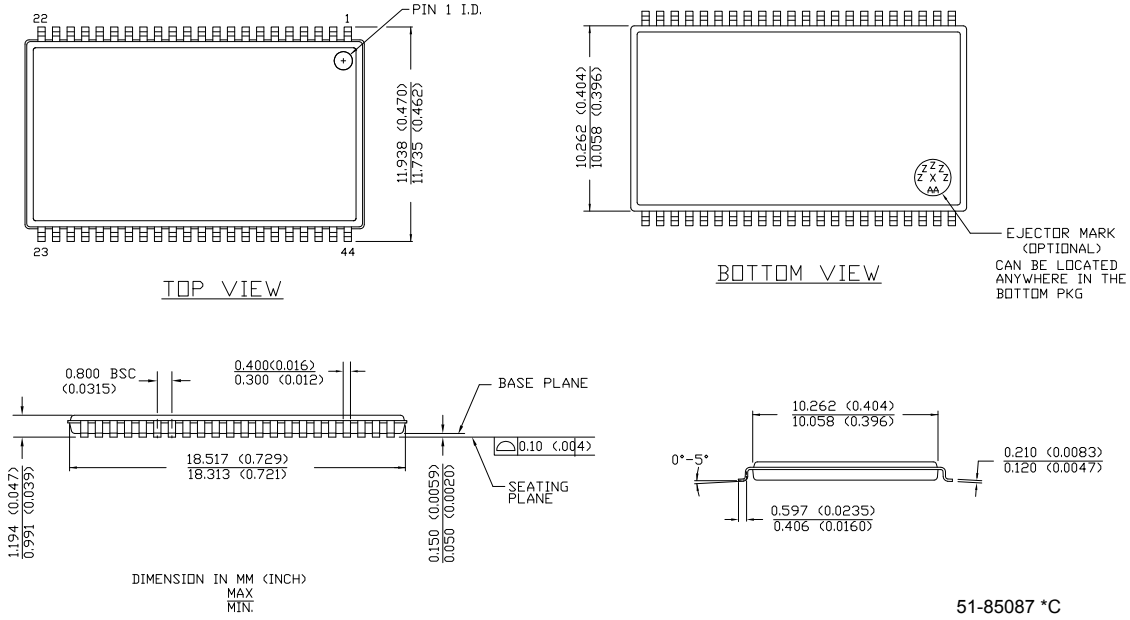
Ordering Code Definitions

CY7C 1020 C V33 - 15 ZSX E X

- X = T or Blank
T = Tape and Reel; Blank = Tube
- Temperature Range:
E = Automotive
- Package Type:
ZSX = 44-pin TSOP Type II (Pb-free)
- Speed Grade = 15 ns
- V33 = 3.3 V
- Process Technology = 0.16 µm
- 1020 = Part Identifier
- CY7C = Cypress SRAMs

Package Diagrams

Figure 1. 44-pin TSOP II, 51-85087



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small-outline package
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent

Document History Page

Document Title: CY7C1020CV33 512 K (32 K × 16) Static RAM Document Number: 38-05133				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109428	12/16/01	HGK	New Data Sheet
*A	115045	05/30/02	HGK	I_{CC} and I_{SB1} data modified
*B	117615	08/14/02	DFP	Pin 1= NC Pin 18 = A4; remove SOJ package option; remove 8ns option.
*C	262949	See ECN	RKF	Added Automotive Specs to Data sheet
*D	334398	See ECN	SYT	Added Lead-Free Product Information
*E	493543	See ECN	NXR	Added note #1 on page #1 Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated Ordering Information Table
*F	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagram
*G	3057593	10/13/2010	PRAS	Updated Ordering Information and added Ordering Code Definitions.
*H	3100106	12/02/2010	PRAS	Added Acronyms and Units of Measure. Minor edits and updated in new template.

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