16-Mbit (2M x 8) MoBL® Static RAM

Features

- Very high speed
  - 55 ns
- Wide voltage range
  - 2.2 V – 3.6 V
- Ultra-low active power
  - Typical active current: 2 mA @ f = 1 MHz
  - Typical active current: 15 mA @ f = f_{Max} (55 ns Speed)
- Ultra-low standby power
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Available in non Pb-free 48-ball very fine ball grid array (VFBGA) package.

Functional Description[1]

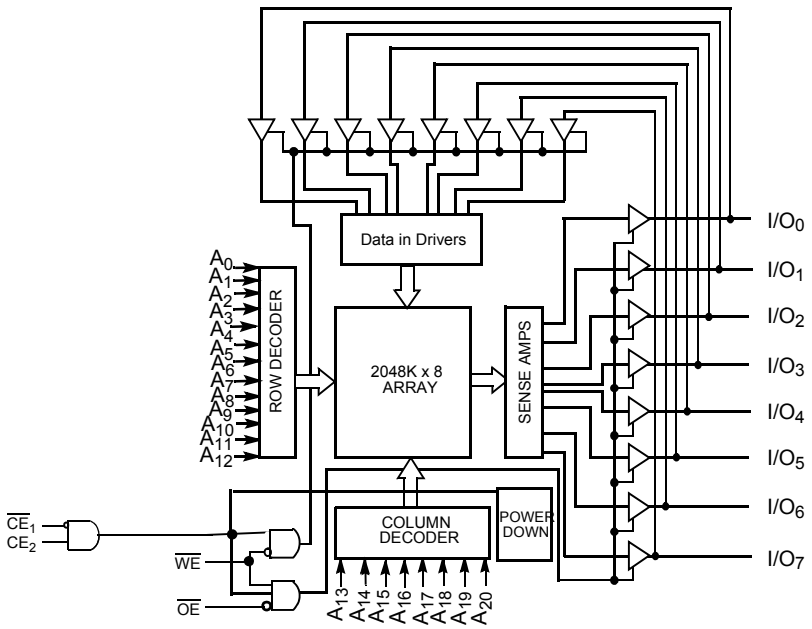
The CY62168DV30 is a high-performance CMOS static RAMs organized as 2048Kbit words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW. The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when: deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW, outputs are disabled ($\overline{OE}$ HIGH), or during a write operation (Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins(A_0 through A_{20}).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE_2) HIGH while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ LOW and CE_2 HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the "Truth Table" on page 10 for a complete description of read and write modes.

Logic Block Diagram

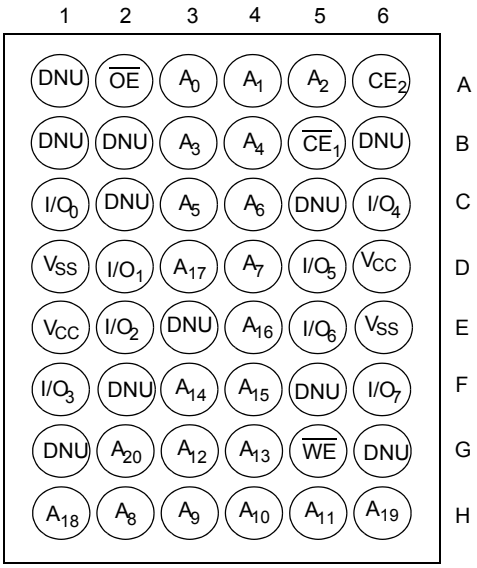


Note
1. For best-practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, available at http://www.cypress.com.

Contents

Pin Configuration[2]

48-ball VFBGA
Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2}(μA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ[3]	Max		Typ [3]	Max	Typ[3]	Max	Typ[3]	Max
CY62168DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22

Notes
2.DNU pins have to be left floating or tied to V_{SS} to ensure proper operation.
3.Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High-Z state[4, 5] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage[4, 5] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)[6]	V_{CC}[7]
Industrial	–40 °C to +85 °C	2.2 V – 3.6 V

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		CY62168DV30-55			Unit
				Min	Typ[8]	Max	
V_{OH}	Output HIGH voltage	2.2 V ≤ V_{CC} ≤ 2.7 V	I_{OH} = –0.1 mA	2.0	–	–	V
		2.7 V ≤ V_{CC} ≤ 3.6 V	I_{OH} = –1.0 mA	2.4	–	–	
V_{OL}	Output LOW voltage	2.2 V ≤ V_{CC} ≤ 2.7 V	I_{OL} = 0.1 mA	–	–	0.4	V
		2.7 V ≤ V_{CC} ≤ 3.6 V	I_{OL} = 2.1 mA	–	–	0.4	
V_{IH}	Input HIGH voltage	2.2 V ≤ V_{CC} ≤ 2.7 V		1.8	–	V_{CC} + 0.3	V
		2.7 V ≤ V_{CC} ≤ 3.6 V		2.2	–	V_{CC} + 0.3	
V_{IL}	Input LOW voltage	2.2 V ≤ V_{CC} ≤ 2.7 V		–0.3	–	0.6	V
		2.7 V ≤ V_{CC} ≤ 3.6 V		–0.3	–	0.8	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{Max} = 1/t_{RC}	V_{CC} = 3.6 V, I_{OUT} = 0 mA, CMOS level	–	15	30	mA
		f = 1 MHz		–	2	4	
I_{SB1}	Automatic CE Power-down current — CMOS inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2 V, CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V, f = f_{Max} (Address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$)		–	2.5	22	µA
I_{SB2}	Automatic CE Power-down current— CMOS inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2 V, CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.6 V		–	2.5	22	µA

Notes
4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. T_A is the “Instant-On” case temperature.
7. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 100 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C

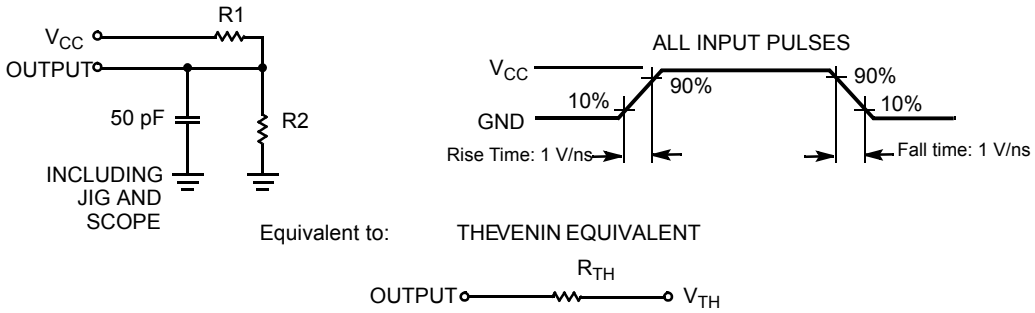
Capacitance

Parameter[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	8	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter[9]	Description	Test Conditions	VFBGA	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	55	°C / W
Θ_{JC}	Thermal resistance (Junction to case)		16	°C / W

AC Test Loads and Waveforms



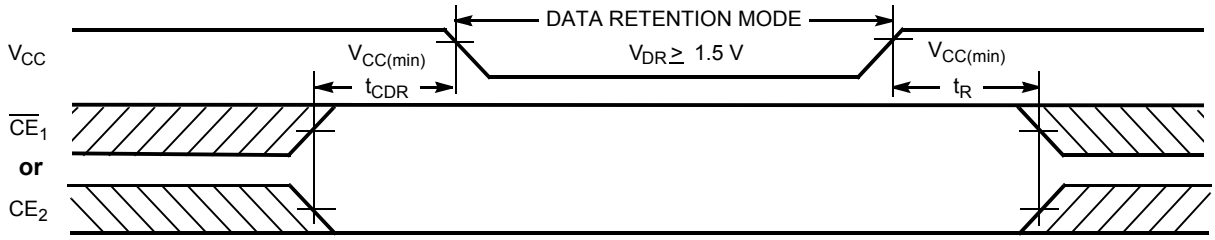
Parameters	2.5 V	3.0 V	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.2	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	3.6	V
I_{CCDR}	Data retention current	V_{CC} = 1.5 V $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	10	µA
t_{CDR}[9]	Chip deselect to data retention time		0	–	–	ns
t_R[11]	Operation recovery time		55	–	–	ns

Notes
9. Tested initially and after any design or process changes that may affect these parameters.
10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C
11. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 µs or stable at $V_{CC(min)}$ > 100 µs..

Data Retention Waveform



Switching Characteristics Over the Operating Range

Parameter[12]	Description	55 ns		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[13]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[13, 14]	–	20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[13]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[13, 14]	–	20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power-down	–	55	ns
Write Cycle[15]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	40	–	ns
t_{AW}	Address set-up to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse width	40	–	ns
t_{SD}	Data set-up to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[13, 14]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[13]	10	–	ns

Notes
12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns or less (1V/ns), timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the “AC Test Loads and Waveforms” section.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
14. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
15. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 1. Read Cycle No. 1 (Address Transition Controlled)[16, 17]

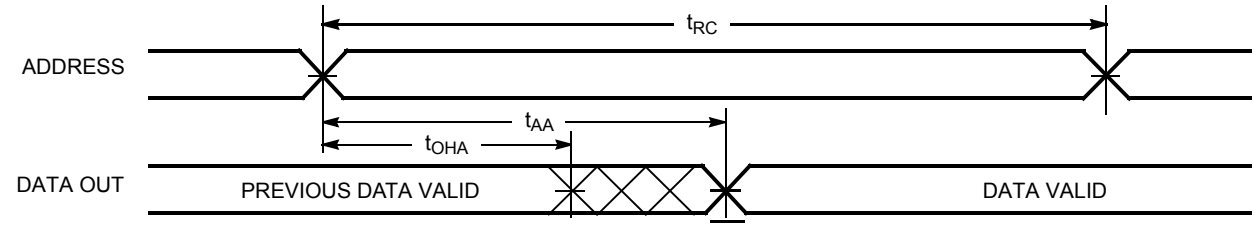


Figure 2. Read Cycle No. 2 (OE Controlled)[17, 18]

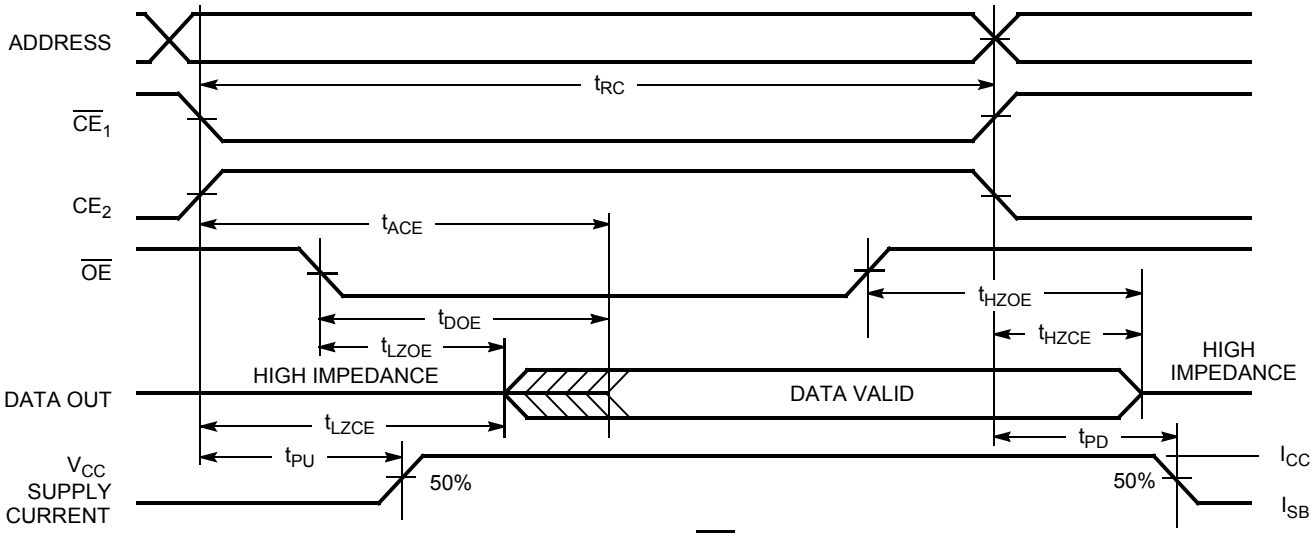
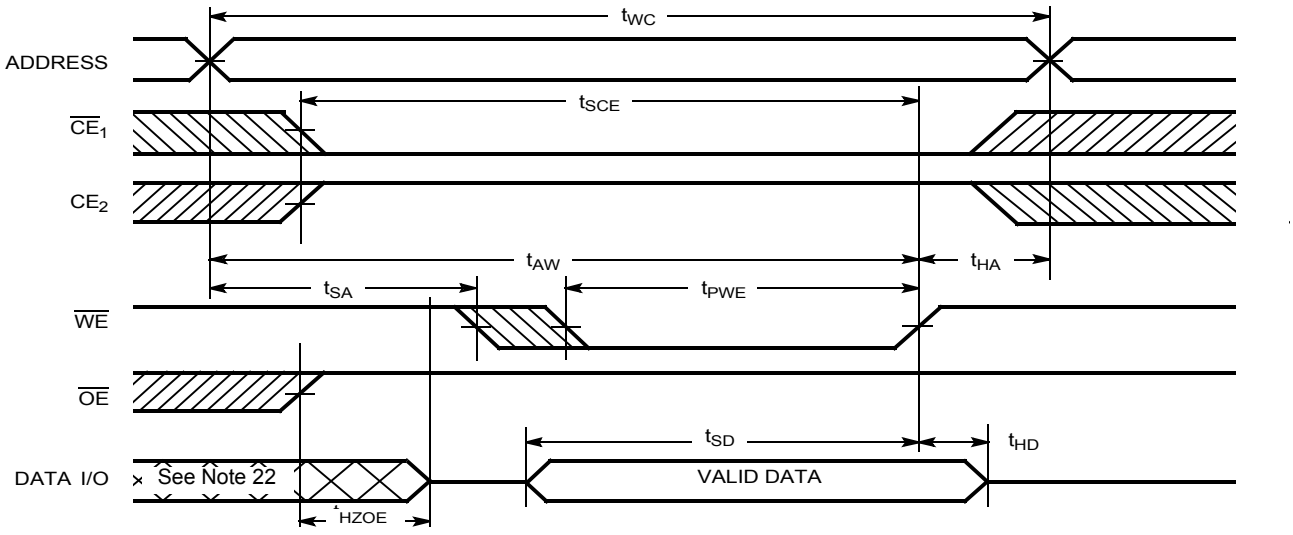


Figure 3. Write Cycle No. 1 (WE Controlled)[19, 20, 21]



Notes

16. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
20. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
21. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.
22. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 4. Write Cycle No. 2 ($\overline{CE}_1$ or CE_2 Controlled)[23, 24, 25]

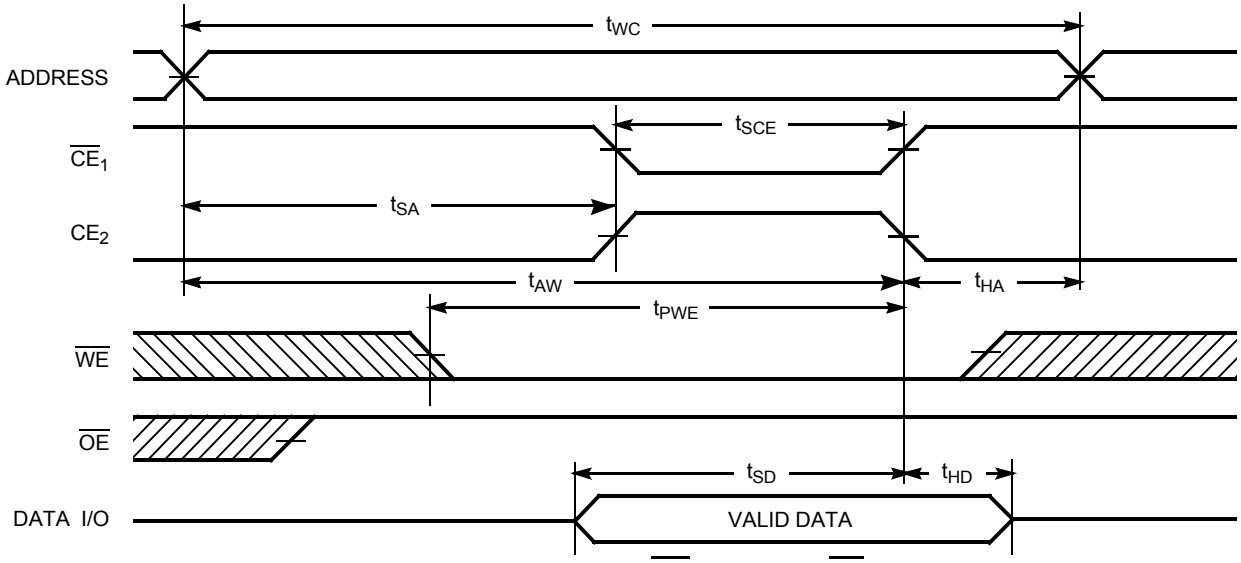
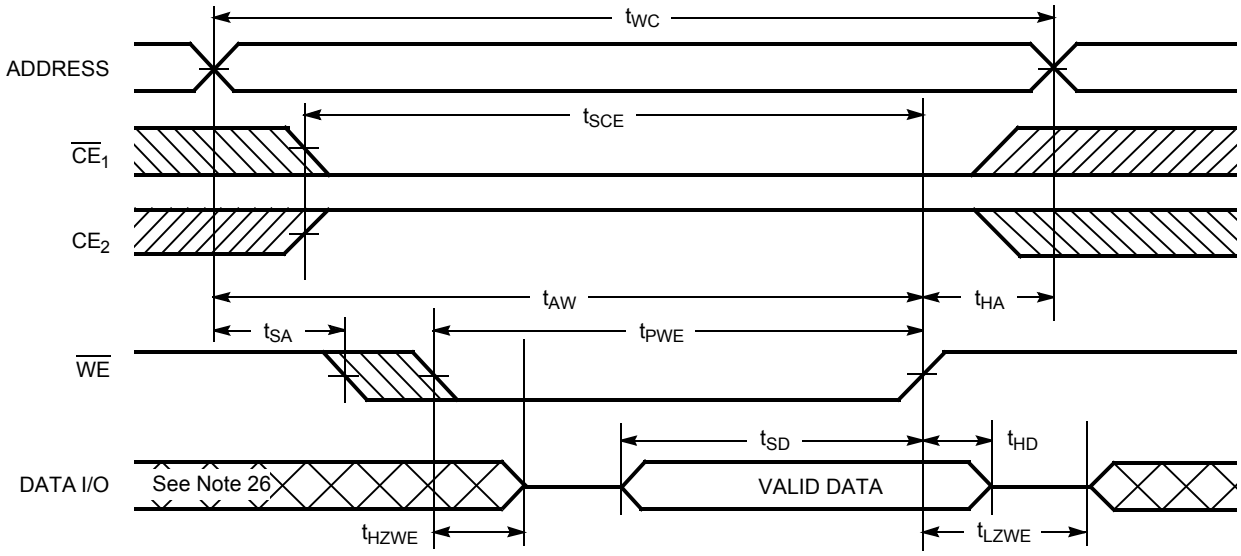


Figure 5. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[26]



Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}
25. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.
26. During this period, the I/Os are in output state and input signals should not be applied

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data out (I/O_0-I/O_7)	Read	Active (I_{CC})
L	H	L	X	Data in (I/O_0-I/O_7)	Write	Active (I_{CC})
L	H	H	H	High Z	Output disabled	Active (I_{CC})

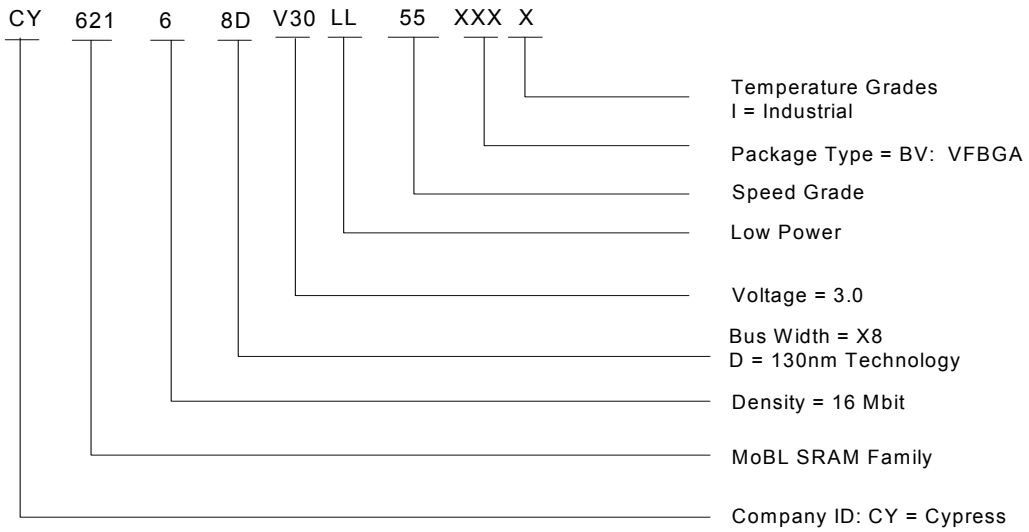
Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at http://www.cypress.com and refer to the product summary page at http://www.cypress.com/products. Cypress maintains a worldwide network of offices, solution centers, manufacturers representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

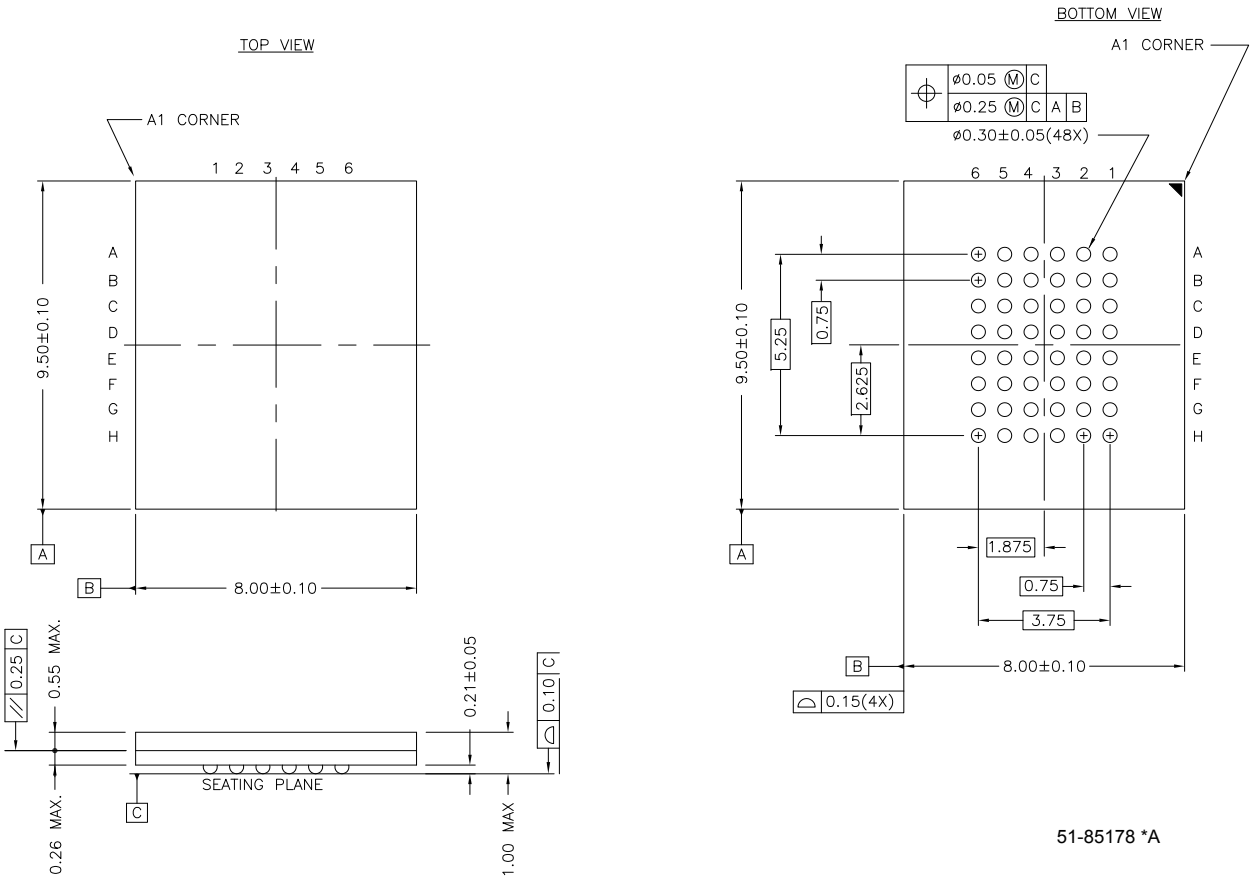
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62168DV30LL-55BVI	51-85178	48-ball Fine Pitch BGA (8 x 9.5 x 1 mm)	Industrial

Please contact your local Cypress sales representative for availability of these parts

Ordering Code Definition



Package Diagram



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball grid array
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62168DV30 MoBL®, 16-Mbit (2M x 8) MoBL® Static RAM Document Number: 38-05329				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	118409	09/30/02	GUG	New Data Sheet
*A	123693	02/05/03	DPM	Changed Advance Information to Preliminary Added package diagram
*B	126556	04/24/03	DPM	Minor change: Change sunset owner from DPM to HRT
*C	132869	01/15/04	XRJ	Changed Preliminary to Final
*D	272589	See ECN	PCI	Updated Final data sheet and added Pb-free package.
*E	335864	See ECN	PCI	Removed redundant packages from Ordering Information Table Added Address A_{20} to ball G2 in the Pin Configuration
*F	492895	See ECN	VKN	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Removed 70 ns speed bin Removed L power bin from product offering Updated Ordering Information Table
*G	2914085	04/15/10	NIKM	Removed inactive part from Ordering Information. Updated Packaging Information
*H	3070774	10/27/2010	RAME	Updated Template Added Acronyms and Units of Measure Added Ordering Code Definition Converted all tablenotes to footnote as per latest template
*I	3090588	11/19/2010	AJU	Post to external web.

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