



CSD18534Q5A 60 V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5 mm × 6 mm Plastic Package

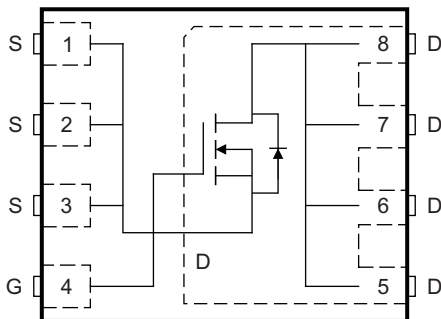
2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

3 Description

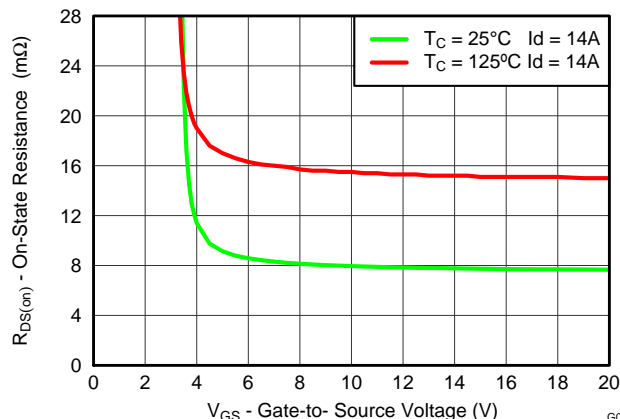
This 7.8 mΩ, 60 V, SON 5 × 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



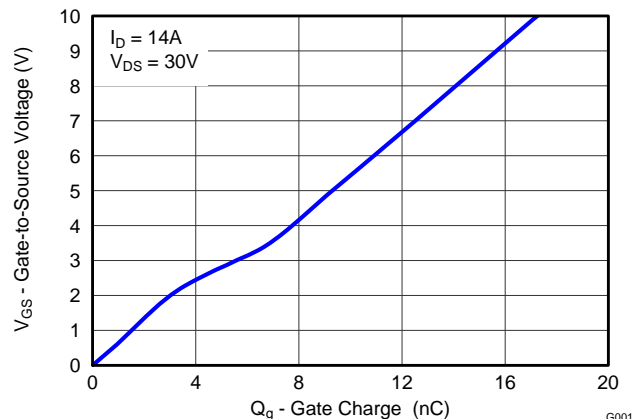
P0093-01

$R_{DS(on)}$ vs V_{GS}



G001

Gate Charge



G001

Product Summary

| $T_A = 25^\circ\text{C}$ | | TYPICAL VALUE | | UNIT |
|--------------------------|-------------------------------|-------------------------|-----|------|
| V_{DS} | Drain-to-source voltage | 60 | | V |
| Q_g | Gate charge total (10 V) | 17 | | nC |
| Q_{gd} | Gate charge gate-to-drain | 3.5 | | nC |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS} = 4.5\text{ V}$ | 9.9 | mΩ |
| | | $V_{GS} = 10\text{ V}$ | 7.8 | mΩ |
| $V_{GS(th)}$ | Threshold voltage | 1.9 | | V |

Ordering Information⁽¹⁾

| DEVICE | QTY | MEDIA | PACKAGE | SHIP |
|--------------|------|--------------|---------------------------------|---------------|
| CSD18534Q5A | 2500 | 13-Inch Reel | SON 5 mm × 6 mm Plastic Package | Tape and Reel |
| CSD18534Q5AT | 250 | 7-Inch Reel | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

| $T_A = 25^\circ\text{C}$ | | VALUE | UNIT |
|--------------------------|--|------------|------|
| V_{DS} | Drain-to-source voltage | 60 | V |
| V_{GS} | Gate-to-source voltage | ±20 | V |
| I_D | Continuous drain current (package limited) | 50 | A |
| | Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$ | 69 | |
| | Continuous drain current, $T_A = 25^\circ\text{C}^{(1)}$ | 13 | |
| I_{DM} | Pulsed drain current, $T_A = 25^\circ\text{C}^{(2)}$ | 229 | A |
| P_D | Power dissipation ⁽¹⁾ | 3.1 | W |
| | Power dissipation, $T_C = 25^\circ\text{C}$ | 77 | |
| T_J, T_{stg} | Operating junction, Storage temperature | –55 to 150 | °C |
| E_{AS} | Avalanche energy, single pulse $I_D = 40\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$ | 80 | mJ |

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1 inch², 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 2.0^\circ\text{C/W}$, pulse duration ≤100 μs, duty cycle ≤1%



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (August 2014) to Revision D | Page |
|--|-------------|
| • Changed description to read 60 V | 1 |
| • Added Community Resources | 7 |

| Changes from Revision B (July 2014) to Revision C | Page |
|--|-------------|
| • Added 7-inch reel to Ordering Information table | 1 |
| • Increased pulsed current to 229 A | 1 |
| • Updated the SOA in Figure 10 | 6 |

| Changes from Revision A (January 2013) to Revision B | Page |
|--|-------------|
| • Added parameter for power dissipation with case temperature held to 25°C | 1 |
| • Updated pulsed current conditions | 1 |
| • Updated Figure 1 to a normalized $R_{\theta JC}$ curve | 4 |

| Changes from Original (October 2012) to Revision A | Page |
|--|-------------|
| • Changed g_{fs} , Transconductance from: 122 to: 72 | 3 |

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|----------------------------------|--|------|-----|------|------|
| STATIC CHARACTERISTICS | | | | | | |
| BV _{DSS} | Drain-to-source voltage | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| I _{DSS} | Drain-to-source leakage current | V _{GS} = 0 V, V _{DS} = 48 V | | | 1 | μA |
| I _{GSS} | Gate-to-source leakage current | V _{DS} = 0 V, V _{GS} = 20 V | | | 100 | nA |
| V _{GS(th)} | Gate-to-source threshold voltage | V _{DS} = V _{GS} , I _D = 250 μA | 1.5 | 1.9 | 2.3 | V |
| R _{DS(on)} | Drain-to-source on-resistance | V _{GS} = 4.5 V, I _D = 14 A | 9.9 | | 12.4 | mΩ |
| | | V _{GS} = 10 V, I _D = 14 A | 7.8 | | 9.8 | mΩ |
| g _{fs} | Transconductance | V _{DS} = 30 V, I _D = 14 A | 72 | | | S |
| DYNAMIC CHARACTERISTICS | | | | | | |
| C _{iss} | Input capacitance | V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz | 1360 | | 1770 | pF |
| C _{oss} | Output capacitance | | 167 | | 217 | pF |
| C _{rss} | Reverse transfer capacitance | | 5 | | 6.5 | pF |
| R _G | Series gate resistance | | 1.5 | | 3 | Ω |
| Q _g | Gate charge total (4.5 V) | V _{DS} = 30 V, I _D = 14 A | 8.5 | | 11.1 | nC |
| Q _g | Gate charge total (10 V) | | 17 | | 22 | |
| Q _{gd} | Gate charge gate-to-drain | | 3.5 | | | nC |
| Q _{gs} | Gate charge gate-to-source | | 3.2 | | | nC |
| Q _{g(th)} | Gate charge at V _{th} | | 2.6 | | | nC |
| Q _{oss} | Output charge | V _{DS} = 30 V, V _{GS} = 0 V | 19 | | | nC |
| t _{d(on)} | Turn on delay time | V _{DS} = 30 V, V _{GS} = 10 V, I _{DS} = 14 A, R _G = 0 Ω | 5.2 | | | ns |
| t _r | Rise time | | 5.5 | | | ns |
| t _{d(off)} | Turn off delay time | | 15 | | | ns |
| t _f | Fall time | | 2 | | | ns |
| DIODE CHARACTERISTICS | | | | | | |
| V _{SD} | Diode forward voltage | I _{SD} = 14 A, V _{GS} = 0 V | 0.8 | | 1 | V |
| Q _{rr} | Reverse recovery charge | V _{DS} = 30 V, I _F = 14 A, di/dt = 300 A/μs | 54 | | | nC |
| t _{rr} | Reverse recovery time | | 40 | | | ns |

5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

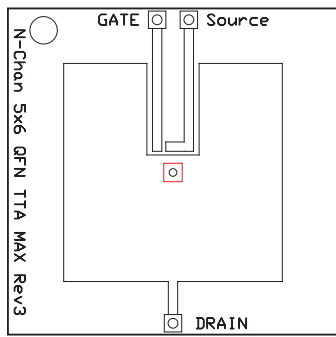
| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|-----------------|--|-----|-----|-----|---------------------------|
| $R_{\theta JC}$ | Junction-to-case thermal resistance ⁽¹⁾ | | | 2.0 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾ | | | 50 | $^\circ\text{C}/\text{W}$ |

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

CSD18534Q5A

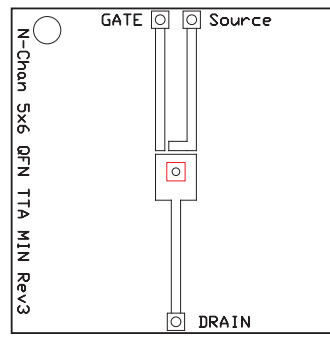
SLPS389D –OCTOBER 2012–REVISED JUNE 2015

www.ti.com



M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2 oz. (0.071 mm thick)
Cu.

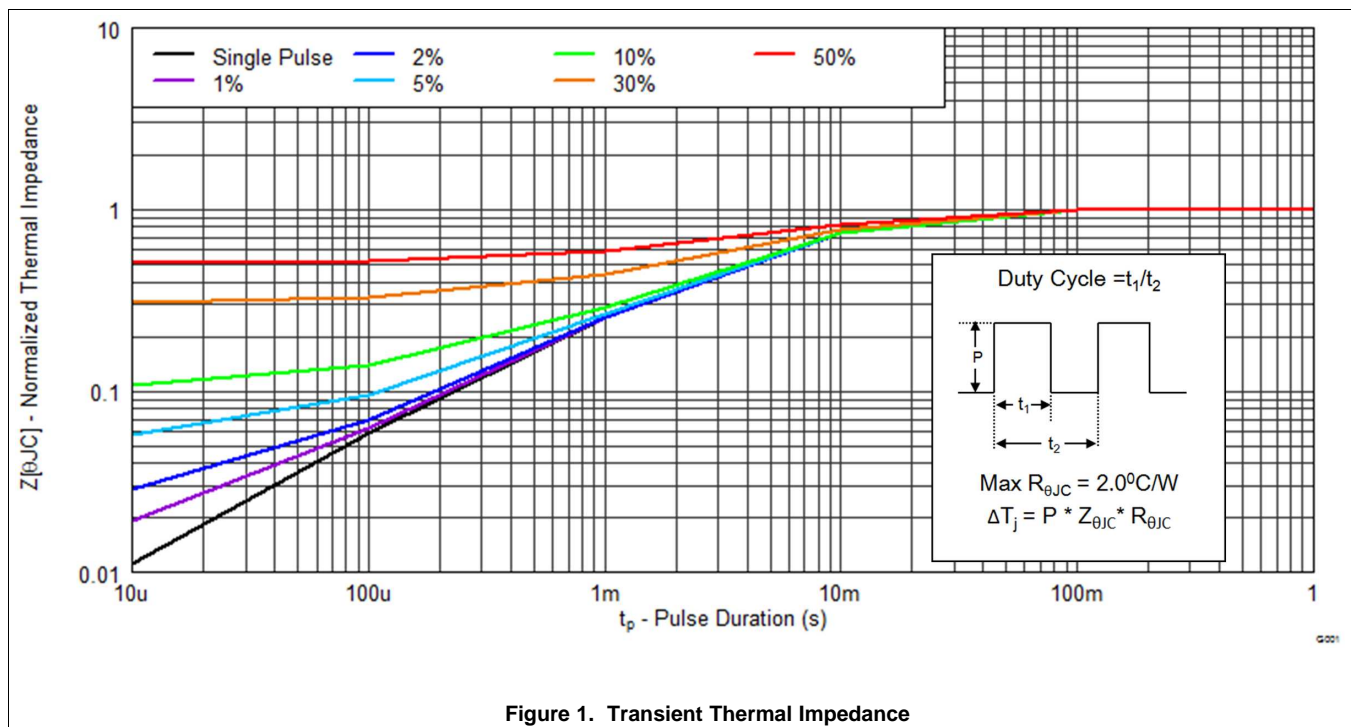


M0137-02

Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2 oz. (0.071 mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

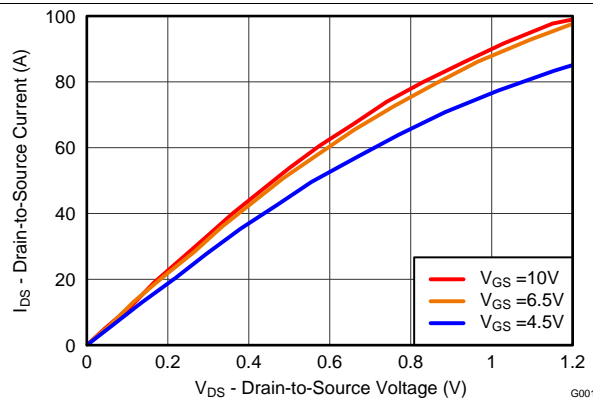


Figure 2. Saturation Characteristics

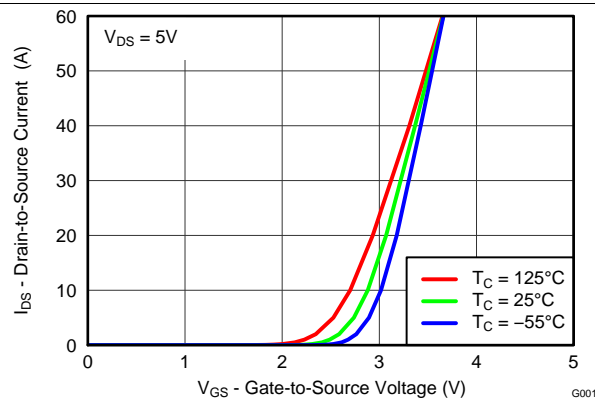


Figure 3. Transfer Characteristics

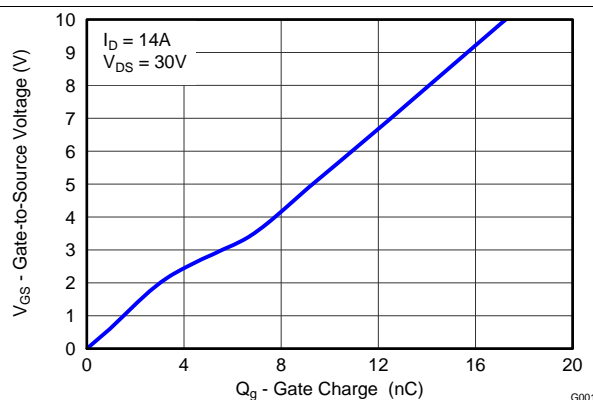


Figure 4. Gate Charge

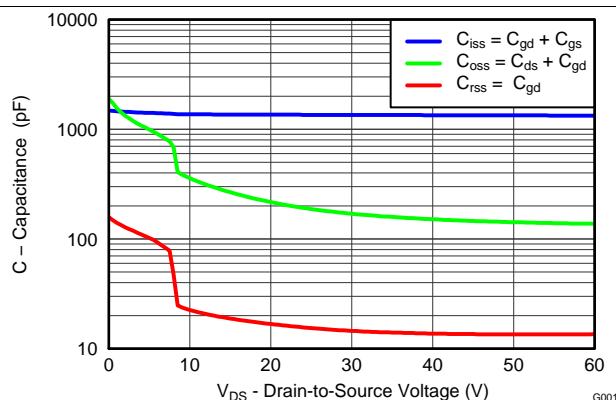


Figure 5. Capacitance

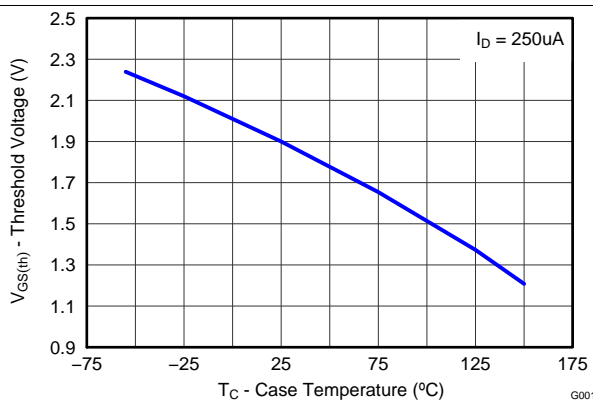


Figure 6. Threshold Voltage vs Temperature

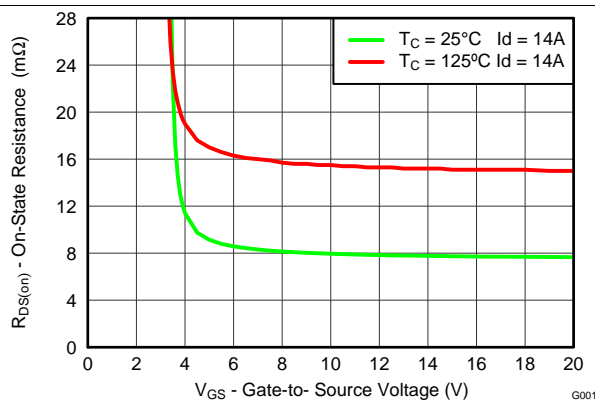


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

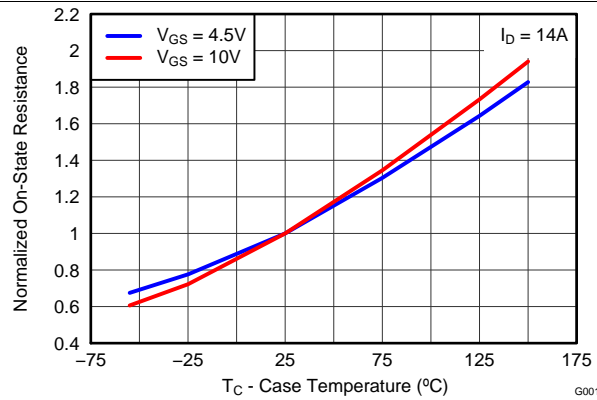


Figure 8. Normalized On-State Resistance vs Temperature

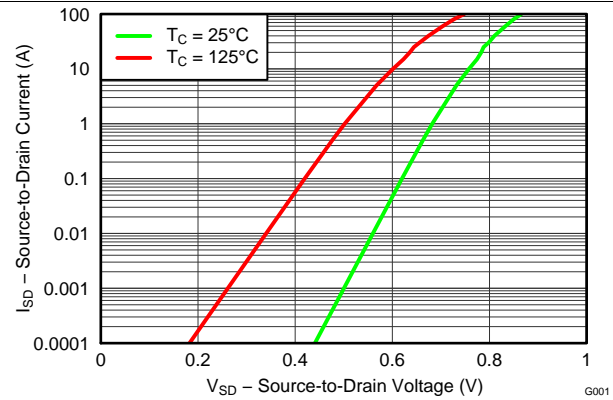


Figure 9. Typical Diode Forward Voltage

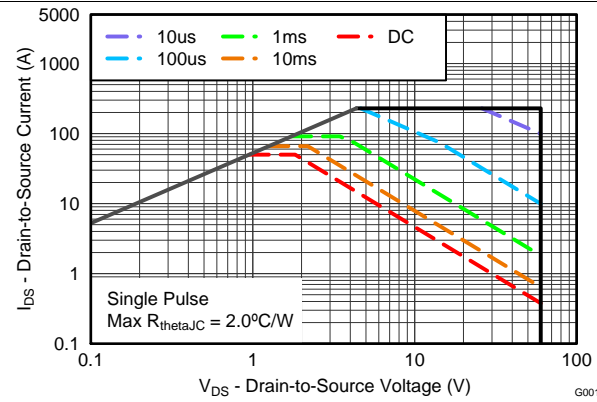


Figure 10. Maximum Safe Operating Area

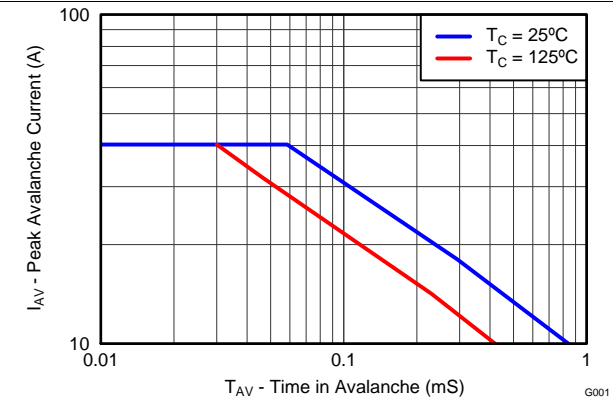


Figure 11. Single Pulse Unclamped Inductive Switching

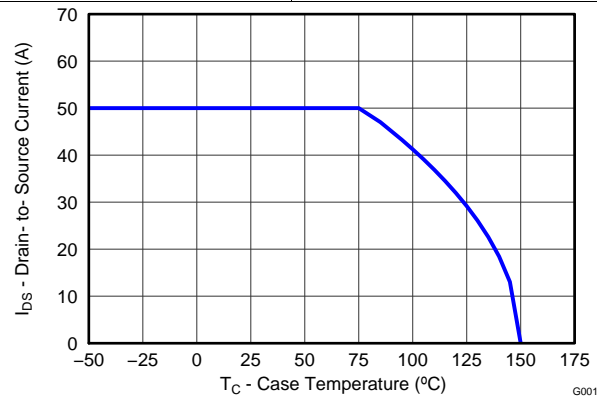


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

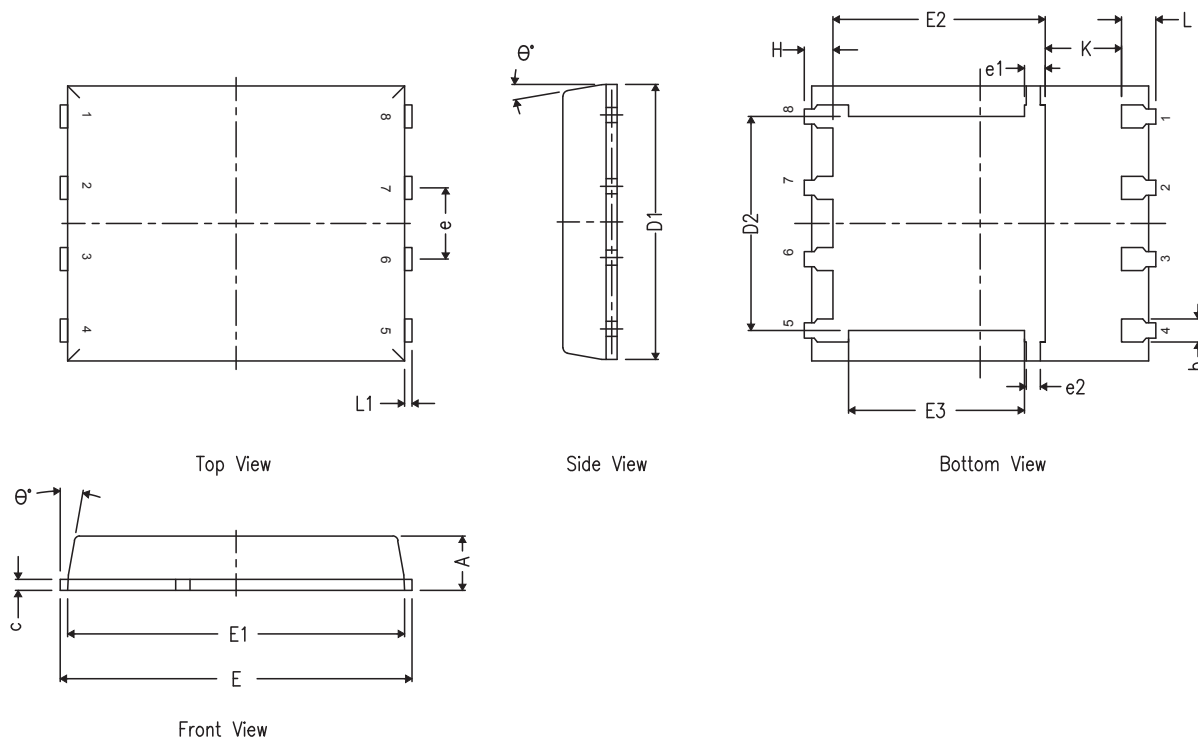
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

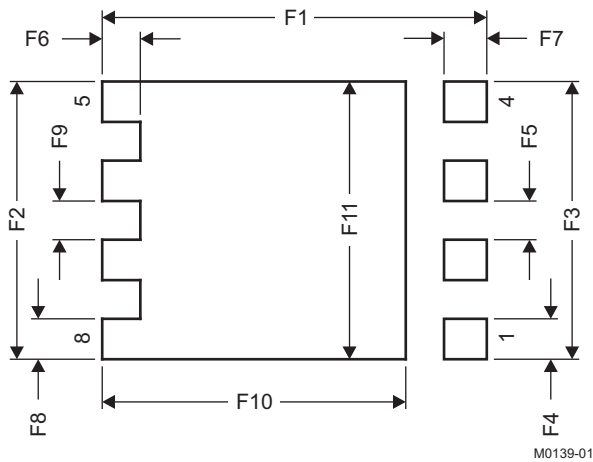
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5A Package Dimensions



| DIM | MILLIMETERS | | |
|----------|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.20 | 0.25 | 0.34 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 4.02 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.38 | 3.58 | 3.78 |
| E3 | 3.03 | 3.13 | 3.23 |
| e | 1.17 | 1.27 | 1.37 |
| e1 | 0.27 | 0.37 | 0.47 |
| e2 | 0.15 | 0.25 | 0.35 |
| H | 0.41 | 0.56 | 0.71 |
| K | 1.10 | — | — |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| θ | 0° | — | 12° |

7.2 Recommended PCB Pattern

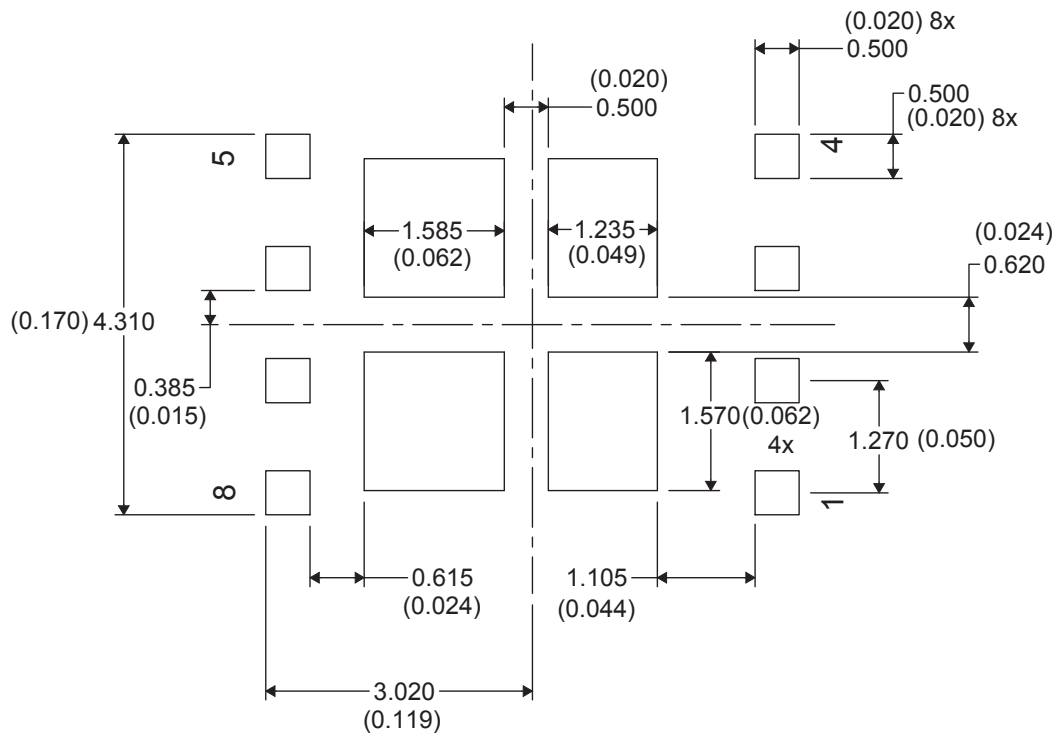


Recommended PCB Pattern (continued)

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| F1 | 6.205 | 6.305 | 0.244 | 0.248 |
| F2 | 4.46 | 4.56 | 0.176 | 0.18 |
| F3 | 4.46 | 4.56 | 0.176 | 0.18 |
| F4 | 0.65 | 0.7 | 0.026 | 0.028 |
| F5 | 0.62 | 0.67 | 0.024 | 0.026 |
| F6 | 0.63 | 0.68 | 0.025 | 0.027 |
| F7 | 0.7 | 0.8 | 0.028 | 0.031 |
| F8 | 0.65 | 0.7 | 0.026 | 0.028 |
| F9 | 0.62 | 0.67 | 0.024 | 0.026 |
| F10 | 4.9 | 5 | 0.193 | 0.197 |
| F11 | 4.46 | 4.56 | 0.176 | 0.18 |

For recommended circuit layout for PCB designs, see application note *Reducing Ringing Through PCB Layout Techniques*, [SLPA005](#).

7.3 Recommended Stencil Opening



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|--------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CSD18534Q5A | ACTIVE | VSONP | DQJ | 8 | 2500 | Pb-Free (RoHS Exempt) | CU SN | Level-1-260C-UNLIM | -55 to 150 | CSD18534 | Samples |
| CSD18534Q5AT | ACTIVE | VSONP | DQJ | 8 | 250 | Pb-Free (RoHS Exempt) | CU SN | Level-1-260C-UNLIM | -55 to 150 | CSD18534 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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Applications

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