

CMOS High Voltage Logic – CD4081B

Quad 2-Input AND Gate Logic IC in bare die form

Description

The CD4081B Quad 2-Input AND Gate is fabricated using a 3µm 15CMOS process. The device has equal source and sink current capabilities and conforms to standard B series output drive. Device outputs are buffered which improves transfer characteristics by providing very high gain. The device is capable of driving x2 low power TTL loads or x1 LSTTL load.

Features:

- High Input Voltage up to 20V
- Symmetrical Output Characteristics
- Max input current 1µA at 18V over full Military Temperature Range
- Low Power TTL compatible
- Specified at 5V, 10V & 15V
- Direct drop-in replacement for obsolete components in long term programs.

Die Dimensions in µm (mils)

Ordering Information

The following part suffixes apply:

- No suffix MIL-STD-883 /2010B Visual Inspection
- "H" MIL-STD-883 /2010B Visual Inspection
 + MIL-PRF-38534 Class H LAT
- "K" MIL-STD-883 /2010A Visual Inspection (Space)
 + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

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Supply Formats:

- Default Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request



Mechanical Specification

Die Size (Unsawn)	1550 x 1500 61 x 59	µm mils	
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils	
Top Metal Composition	Al 1%Si 1.1µm		
Back Metal Composition	N/A – Bare Si		

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Pad Layout and Functions



Logic Diagram



Pad 14 = V_{DD} Pad 7 = V_{SS}

PAD	FUNCTION	COORDINATES (mm)				
FAD		X	Y			
1	A1	0.108	0.640			
2	B1	0.108	0.108			
3	Y1	0.548	0.108			
4	Y2	0.880	0.108			
5	A2	1.336	0.108			
6	B2	1.336	0.450			
7	V _{SS}	1.336	0.650			
8	A3	1.336	1.030			
9	B3	1.336	1.278			
10	Y3	1.064	1.278			
11	Y4	0.874	1.278			
12	A4	0.549	1.278			
13	B4	0.108	1.278			
14	V _{DD}	0.108	0.916			
CONNECT CHIP BACK TO VDD OR FLOAT						

Truth Table

INP	JTS	OUTPUT			
Α	В	Y			
L L H H	L H L H	L L L H			
H = High level (steady state)					
L = Low level (steady state)					







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Absolute Maximum Ratings¹

0			
PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V _{SS})	V _{DD}	-0.5 to +20	V
DC Input or Output Voltage(Referenced to V _{SS})	V _{IN} , V _{OUT}	-0.5 to V _{DD} +0.5	V
Storage Temperature Range	T _{STG}	-65 to 150	°C
Input Current or Output Current (per Pad)	I _{IN} , I _{OUT}	±10	mA
Power Dissipation in Still Air ²	PD	750	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to V_{ss})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V _{DD}	3.0	18	V
DC Input Voltage, Output Voltage	V _{IN} , V _{OUT}	0	V _{DD}	V
Operating Temperature Range	TJ	-55	+125	°C

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $V_{SS} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to V_{ss})

PARAMETER	SYMBOL		CONDITIONS		LIMITS		UNITS
		♥ DD	CONDITIONS	25°C	85°C	FULL RANGE ⁴	
Minimum High-		5V	V_{OUT} = 0.5 or V_{DD} -0.5	3.5	3.5	3.5	V
Level Input	V _{IH}	10V	V_{OUT} = 1.0 or V_{DD} -1.0	7	7	7	
Voltage		15V	V_{OUT} = 1.5 or V_{DD} -1.5	11	11	11	
Maximum Low-		5V	V _{OUT} = 0.5V	1.5	1.5	1.5	
Level Input	V _{IL}	10V	V _{OUT} = 1.0V	3	3	3	V
Voltage		15V	V _{OUT} = 1.5V	4	4	4	
Minimum High-	V _{OH}	5V	V _{IN} = V _{DD}	4.95	4.95	4.95	V
Level Output Voltage		10V		9.95	9.95	9.95	
		15V		14.95	14.95	14.95	
Maximum Low-	V _{OL}	5V	V_{IN} = V_{DD} or V_{SS}	0.05	0.05	0.05	V
Level Output		10V		0.05	0.05	0.05	
Voltage		15V		0.05	0.05	0.05	
Maximum Input Leakage Current	I _{IN}	18V	V_{IN} = V_{DD} or V_{SS}	±0.1	±.0.1	±1.0	μA
	it	5V	V _{IN} = V _{DD} or V _{SS} I _{OUT} = 0µA	0.25	7.5	7.5	μA
Maximum		10V		0.5	15	15	
Quiescent Supply Current		15V		1.0	30	30	
		20V		5.0	150	150	

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DC Electrical Characteristics Continued (Voltages referenced to V_{SS}) LIMITS PARAMETER SYMBOL VDD CONDITIONS UNITS FULL RANGE⁴ 25°C 85°C $V_{IN} = V_{DD}$ or V_{SS} 5V 0.64 0.42 0.36 $V_{01} = 0.4V$ $V_{IN} = V_{DD} \text{ or } V_{SS}$ Minimum Output I_{OL} 10V 1.6 1.1 0.9 mΑ Low (Sink) Current $V_{OI} = 0.5V$ $V_{IN} = V_{DD} \text{ or } V_{SS}$ 15V 4.2 2.8 2.4 V_{OL} = 1.5V $V_{IN} = V_{DD}$ or V_{SS} 5V -1.3 -2.0 -1.15 V_{OH} = 2.5V V_{IN} = V_{DD} or V_{SS} 5V -0.64 Minimum Output -0.42 -0.36 V_{OH} = 4.6V High (Source) mΑ I_{OH} $V_{IN} = V_{DD}$ or GND Current 10V -1.1 -1.6 -0.9 $V_{OH} = 9.5V$ $V_{IN} = V_{DD} \text{ or } V_{SS}$ $V_{OH} = 13.5V$ 15V -4.2 -2.4 -2.8

4. -55°C ≤ T_J ≤ +125°C.

AC Electrical Characteristics⁵

PARAMETER	SYMBOL	V _{DD}	CONDITIONS	TYPICAL	LIMITS		UNITS
				25°C	85°C	FULL RANGE ⁴	
Propagation Delay, Input A or B to		5V	$R_L = 200k\Omega$	250	250	500	ns
	t _{PLH} , t _{PHL}	10V		120	120	240	
Output Y (Figure 1)		15V	$t_r = t_f = 20$ ns	90	90	180	
Output Transition Time, Any Output (Figure 1)	t _{tlh} , t _{thl}	5V	$\begin{array}{l} C_{L} = 50 \text{pF}, \\ R_{L} = 200 \text{k}\Omega \\ t_{r} = t_{\text{f}} = 20 \text{ns} \end{array}$	200	200	400	
		10V		100	100	200	ns
		15V		80	80	160	
Input Capacitance	C _{IN}	-	$C_{L} = 50 \text{pF},$ $R_{L} = 200 \text{k}\Omega$ $t_{r} = t_{f} = 20 \text{ns}$	5	7.5	7.5	pF

5. Not production tested in die form, characterized by chip design and tested in package.

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