CC1352P SimpleLink™ High-Performance Dual-Band Wireless MCU With Integrated Power Amplifier

1 Device Overview

1.1 Features

- Microcontroller
  - Powerful Arm® Cortex®-M4F Processor
  - EEMBC CoreMark® Score: 148
  - Clock Speed Up to 48 MHz
  - 352KB of In-System Programmable Flash
  - 256KB of ROM for Protocols and Firmware
  - 8KB of Cache SRAM (Available as General-Purpose RAM)
  - 80KB of Ultra-Low Leakage SRAM
  - 2-Pin cJTAG and JTAG Debugging
  - Supports Over-the-Air Upgrade (OTA)
- Ultra-Low Power Sensor Controller With 4KB of SRAM
  - Sample, Store, and Process Sensor Data
  - Operation Independent From System CPU
  - Fast Wake-Up for Low-Power Operation
- TI-RTOS, Drivers, Bootloader, *Bluetooth*® 5 low energy Controller, and IEEE 802.15.4 MAC in ROM for Optimized Application Size
- RoHS-Compliant Package
  - 7-mm × 7-mm RGZ VQFN48 (26 GPIOs)
- Peripherals
  - Digital Peripherals Can be Routed to Any GPIO
  - 4× 32-Bit or 8× 16-Bit General-Purpose Timers
  - 12-Bit ADC, 200 kSamples/s, 8 Channels
  - 2× Comparators With Internal Reference DAC (1× Continuous Time, 1× Ultra-Low Power)
  - Programmable Current Source
  - 2× UART
  - 2× SSI (SPI, MICROWIRE, TI)
  - I^2C
  - I^2S
  - Real-Time Clock (RTC)
  - AES 128- and 256-bit Crypto Accelerator
  - ECC and RSA Public Key Hardware Accelerator
  - SHA2 Accelerator (Full Suite Up to SHA-512)
  - True Random Number Generator (TRNG)
  - Capacitive Sensing, Up to 8 Channels
  - Integrated Temperature and Battery Monitor
- External System
  - On-Chip Buck DC/DC Converter
- Low Power
  - Wide Supply Voltage Range: 1.8 V to 3.8 V
  - Active-Mode RX: 5.8 mA (868 MHz)
  - Active-Mode TX at +20 dBm: 65 mA (868 MHz)
  - Active-Mode MCU 48 MHz (CoreMark): 2.82 mA (59 µA/MHz)
  - Sensor Controller 16-Hz Flow Metering: 1.7 µA
  - Sensor Controller 100-Hz Comp A Reading: 1.5 µA
  - Sensor Controller, 1-Hz ADC Sampling: 1 µA
  - Standby: 0.83 µA (RTC on, 80KB RAM and CPU Retention)
  - Shutdown: 125 nA (Wakeup on External Events)
- Radio Section
  - Dual-Band Sub-1 GHz and 2.4-GHz RF Transceiver Compatible With Bluetooth 5 low energy and IEEE 802.15.4 PHY and MAC
  - Excellent Receiver Sensitivity: –122 dBm for SimpleLink Long Range, –110 dBm at 50 kbps, –103 dBm for Bluetooth 5 low energy Coded
  - Excellent Selectivity: 48 dB at 50 kbps
  - Programmable Output Power Up to +20 dBm
  - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations
    - ETSI EN 300 220, EN 300 328, EN 303 131, EN 303 204 (Europe)
    - EN 300 440 Class 2 (Europe)
    - FCC CFR47 Part 15 (US)
    - ARIB STD-T108 and STD-T66 (Japan)
  - Wide Standard Support
- Development *Tools and Software*
  - LAUNCHXL-CC1352P1, P1-2, and P1-4 Development Kits
  - SimpleLink CC13X2 Software Development Kit
  - SmartRF™ Software Studio for Simple Radio Configuration
  - Sensor Controller Studio for Building Low-Power Sensing Applications

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1.2 Applications

- 433-, 470- to 510-, 868-, 902- to 928-, and 2400- to 2480-MHz ISM and SRD Systems (1) With Down to 4 kHz of Receive Bandwidth
- Smart Grid and Automatic Meter Reading
  - Water, Gas, and Electricity Meters
  - Heat Cost Allocators
  - Gateways
- Wireless Sensor Networks
  - Long-Range Sensor Applications
- Industrial
  - Asset Tracking and Management
  - Factory Automation
  - Remote Display
- Wireless Healthcare Applications
- Energy Harvesting Applications
- Electronic Shelf Label (ESL)
- Home and Building Automation
  - Wireless Alarms and Security Systems
  - Locks
  - Lightning Control
  - Motion Detectors
  - Connected Appliances
  - HVAC
  - Garage Door Openers

(1) See *RF Core* for additional details on support protocol standards, modulation formats, and data rates.

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1.3 Description

The CC1352P device is a multiprotocol Sub-1 and 2.4-GHz wireless MCU targeting Wireless M-Bus, IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), Thread, Zigbee®, KNX RF, Wi-SUN®, *Bluetooth*® 5 low energy, and proprietary systems. The device contains a +20-dBm integrated high-power amplifier with best-in-class efficiency for long-range applications.

The CC1352P device is a member of the CC26xx and CC13xx family of cost-effective, ultra-low power, 2.4-GHz and Sub-1 GHz RF devices. Very low active RF and microcontroller (MCU) current, in addition to sub-μA sleep current with up to 80KB of RAM retention, provide excellent battery lifetime and allow operation on small coin-cell batteries and in energy-harvesting applications.

The CC1352P device combines a flexible, very low-power RF transceiver with a powerful 48-MHz Arm® Cortex®-M4F CPU in a platform supporting multiple physical layers and RF standards. A dedicated Radio Controller (Arm® Cortex®-M0) handles low-level RF protocol commands that are stored in ROM or RAM, thus ensuring ultra-low power and great flexibility. The low power consumption of the CC1352P device does not come at the expense of RF performance; the CC1352P device has excellent sensitivity and robustness (selectivity and blocking) performance.

The CC1352P device is a highly integrated, true single-chip solution incorporating a complete RF system and an on-chip DC/DC converter.

Sensors can be handled in a very low-power manner by a programmable, autonomous ultra-low power Sensor Controller CPU with 4KB of SRAM for program and data. The Sensor Controller, with its fast wake-up and ultra-low-power 2-MHz mode is designed for sampling, buffering, and processing both analog and digital sensor data; thus the MCU system can maximize sleep time and reduce active power.

The CC1352P device is part of the SimpleLink™ microcontroller (MCU) platform, which consists of Wi-Fi®, *Bluetooth*® low energy, Thread, Zigbee, Sub-1 GHz MCUs, and host MCUs, which all share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit ti.com/simplelink.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CC1352P1F3RGZ	VQFN (48)	7.00 mm × 7.00 mm

(1) For the most current part, package, and ordering information for all available devices, see the Package Option Addendum in Section 9 , or see the TI website.

1.4 Functional Block Diagram

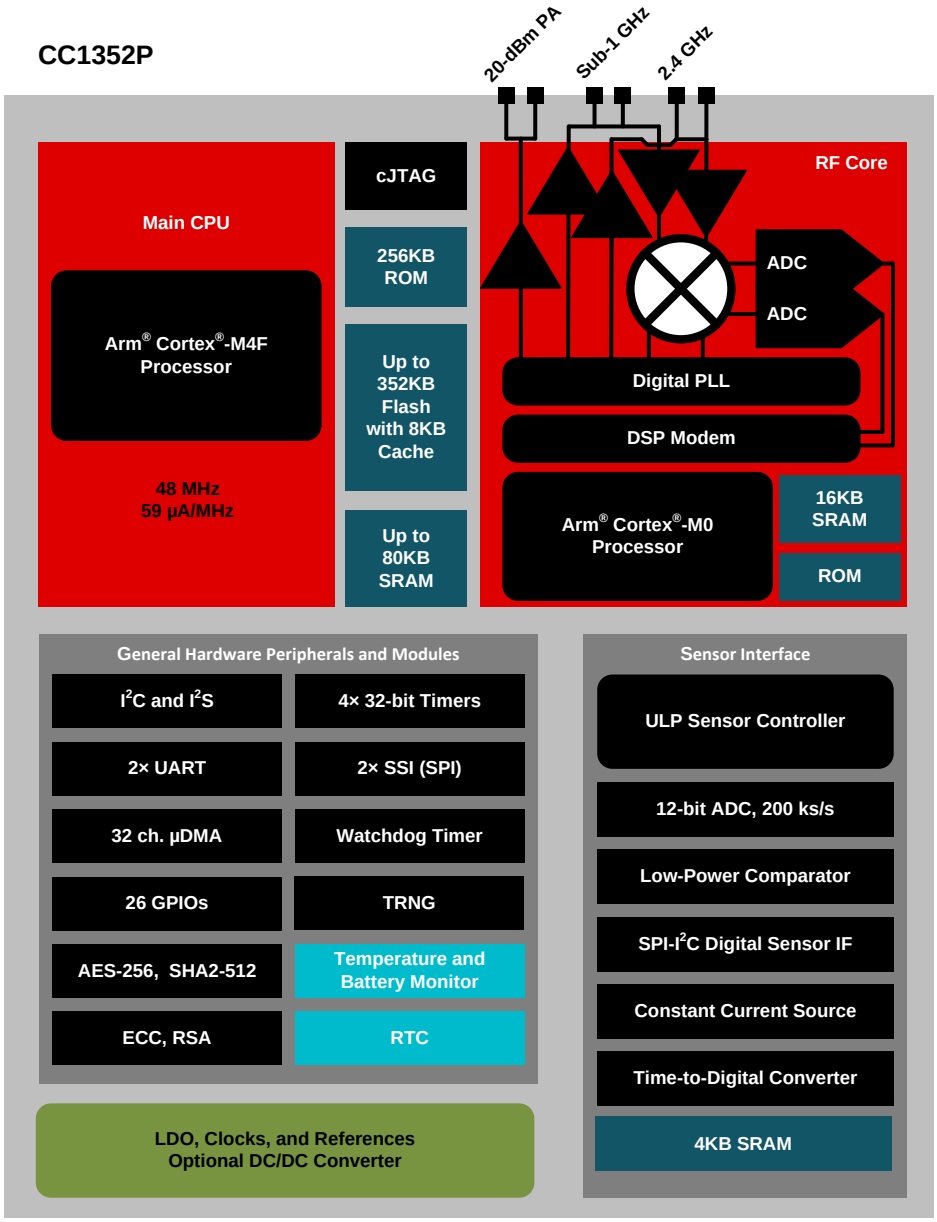

Figure 1-1. CC1352P Block Diagram

ADVANCE INFORMATION

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2 Revision History

DATE	REVISION	NOTES
July 2018	*	Initial Release

3 Device Comparison

Table 3-1. Device Family Overview

DEVICE	RADIO SUPPORT	FLASH (KB)	RAM (KB)	GPIO	PACKAGE SIZE
CC1312R	Sub-1 GHz	352	80	30	RGZ (7-mm × 7-mm VQFN48)
CC1352P	Dual-band (2.4-GHz and Sub-1 GHz) Multiprotocol +20-dBm high-power amplifier	352	80	26	RGZ (7-mm × 7-mm VQFN48)
CC1352R	Dual-band (2.4-GHz and Sub-1 GHz) Multiprotocol	352	80	28	RGZ (7-mm × 7-mm VQFN48)
CC2642R	Bluetooth 5 low energy 2.4-GHz proprietary FSK-based formats	352	80	31	RGZ (7-mm × 7-mm VQFN48)
CC2652R	Multiprotocol Bluetooth 5 low energy Zigbee Thread 2.4-GHz proprietary FSK-based formats	352	80	31	RGZ (7-mm × 7-mm VQFN48)
CC1310	Sub-1 GHz	32–128	16–20	10–31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32)
CC1350	Sub-1 GHz Bluetooth 5 low energy	128	20	10–31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32)
CC2640R2	Bluetooth 5 low energy 2.4-GHz proprietary FSK-based formats	128	20	10–31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32) YFV (2.7-mm × 2.7-mm DSBGA34)

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4 Terminal Configuration and Functions

4.1 Pin Diagram – RGZ Package (Top Side View)

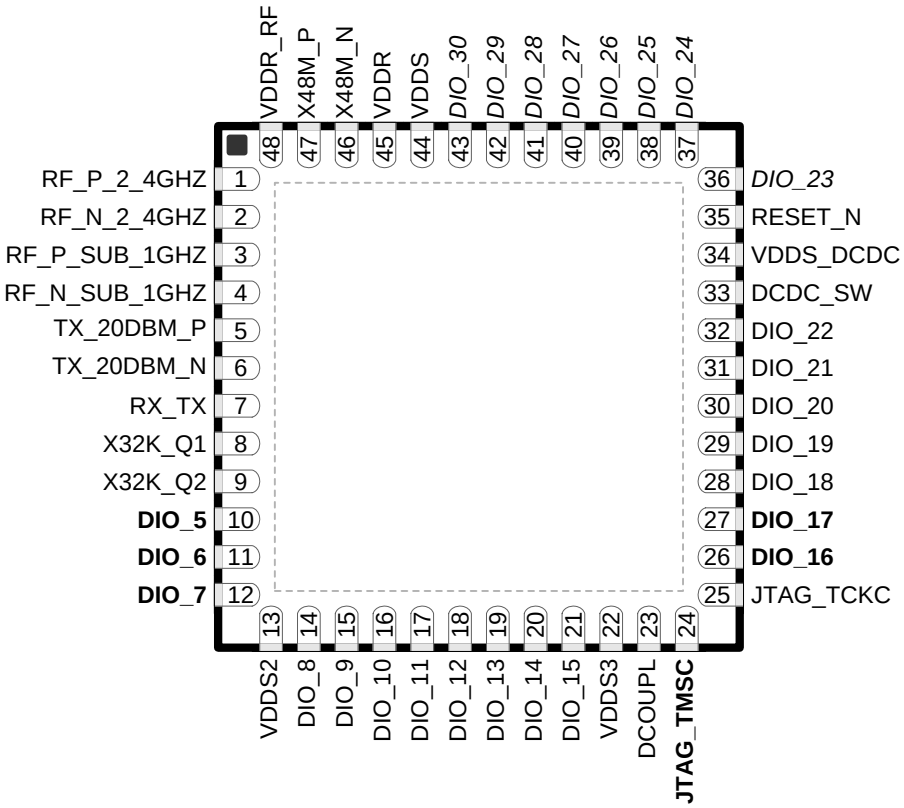

Figure 4-1. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch

The following I/O pins marked in Figure 4-1 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

The following I/O pins marked in Figure 4-1 in *italics* have analog capabilities:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

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4.2 Signal Descriptions – RGZ Package

Table 4-1. Signal Descriptions – RGZ Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	33	—	Power	Output from internal DC/DC converter(1)
DCOUPL	23	—	Power	1.27-V regulated digital-supply (decoupling capacitor)(2)
DIO_5	10	I/O	Digital	GPIO, Sensor Controller, high-drive capability
DIO_6	11	I/O	Digital	GPIO, Sensor Controller, high-drive capability
DIO_7	12	I/O	Digital	GPIO, Sensor Controller, high-drive capability
DIO_8	14	I/O	Digital	GPIO
DIO_9	15	I/O	Digital	GPIO
DIO_10	16	I/O	Digital	GPIO
DIO_11	17	I/O	Digital	GPIO
DIO_12	18	I/O	Digital	GPIO
DIO_13	19	I/O	Digital	GPIO
DIO_14	20	I/O	Digital	GPIO
DIO_15	21	I/O	Digital	GPIO
DIO_16	26	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	I/O	Digital	GPIO
DIO_19	29	I/O	Digital	GPIO
DIO_20	30	I/O	Digital	GPIO
DIO_21	31	I/O	Digital	GPIO
DIO_22	32	I/O	Digital	GPIO
DIO_23	36	I/O	Digital or Analog	GPIO, Sensor Controller, analog
DIO_24	37	I/O	Digital or Analog	GPIO, Sensor Controller, analog
DIO_25	38	I/O	Digital or Analog	GPIO, Sensor Controller, analog
DIO_26	39	I/O	Digital or Analog	GPIO, Sensor Controller, analog
DIO_27	40	I/O	Digital or Analog	GPIO, Sensor Controller, analog
DIO_28	41	I/O	Digital or Analog	GPIO, Sensor Controller, analog
DIO_29	42	I/O	Digital or Analog	GPIO, Sensor Controller, analog
DIO_30	43	I/O	Digital or Analog	GPIO, Sensor Controller, analog
EGP	—	—	GND	Ground – exposed ground pad
JTAG_TMSC	24	I/O	Digital	JTAG TMSC, high-drive capability
JTAG_TCKC	25	I	Digital	JTAG TCKC
RESET_N	35	I	Digital	Reset, active low. No internal pullup resistor
RF_P_2_4GHZ	1	—	RF	Positive 2.4-GHz RF input signal to LNA during RX Positive 2.4-GHz RF output signal from PA during TX
RF_N_2_4GHZ	2	—	RF	Negative 2.4-GHz RF input signal to LNA during RX Negative 2.4-GHz RF output signal from PA during TX
RF_P_SUB_1GHZ	3	—	RF	Positive Sub-1 GHz RF input signal to LNA during RX Positive Sub-1 GHz RF output signal from PA during TX
RF_N_SUB_1GHZ	4	—	RF	Negative Sub-1 GHz RF input signal to LNA during RX Negative Sub-1 GHz RF output signal from PA during TX
RX_TX	7	—	RF	Optional bias pin for the RF LNA
TX_20DBM_P	5	—	RF	Positive Sub-1 GHz or 2.4-GHz high-power TX signal
TX_20DBM_N	6	—	RF	Negative Sub-1 GHz or 2.4-GHz high-power TX signal

(1) For more details, see technical reference manual listed in Section 8.3.
(2) Do not supply external circuitry from this pin.

Table 4-1. Signal Descriptions – RGZ Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDR	45	—	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC/DC converter(3)(2)
VDDR_RF	48	—	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC/DC converter(4)(2)
VDDS	44	—	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	13	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS3	22	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS_DCDC	34	—	Power	1.8-V to 3.8-V DC/DC converter supply
X48M_N	46	—	Analog	48-MHz crystal oscillator pin 1
X48M_P	47	—	Analog	48-MHz crystal oscillator pin 2
X32K_Q1	8	—	Analog	32-kHz crystal oscillator pin 1
X32K_Q2	9	—	Analog	32-kHz crystal oscillator pin 2

(3) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
(4) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.

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4.3 Connections for Unused Pins and Modules

Table 4-2. Connections for Unused Pins

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO	DIO_n	10–12 14–21 26–32 36–43	NC or GND	NC
32.768-kHz crystal	X32K_Q1 X32K_Q2	8–9	NC	NC
DC/DC converter(2)	DCDC_SW	33	NC	NC
	VDDS_DCDC	34	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the VDDR decoupling capacitor must connected and moved close to VDDR.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
VDDS(3)	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin(4)		–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P		–0.3	VDDR + 0.3, max 2.25	V
V_{in}	Voltage on ADC input	Voltage scaling enabled	–0.3	VDDS	V
		Voltage scaling disabled, internal reference	–0.3	1.49	
		Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
	Input level, Sub-1 GHz RF pins			10	dBm
	Input level, 2.4 GHz RF pins			5	dBm
T_{stg}	Storage temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog capable DIO.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	X48_N X48_P	±2000	V
			TX_20DBM_P TX_20DBM_N	±1000	V
			All other pins	±2000	V
		Charged device model (CDM), per JESD22-C101(2)	X48_N X48_P	±500	V
			TX_20DBM_P TX_20DBM_N	±250	V
			All other pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Ambient temperature		–40	85	°C
Operating supply voltage (VDDS)		1.8	3.8	V
Operating supply voltage (VDDS), boost mode	VDDR = 1.95V (For +14dBm RF output on regular power amplifier)	2.1	3.8	
Rising supply voltage slew rate		0	100	mV/µs
Falling supply voltage slew rate(1)		0	20	mV/µs

(1) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor must be used to ensure compliance with this slew rate.

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5.4 Power Consumption - Power Modes

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.6 V with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
CORE CURRENT CONSUMPTION				
I_{core}	Reset and Shutdown	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	125	nA
		Shutdown. No clocks running, no retention	125	
	Standby without cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	0.83	µA
		RTC running, CPU, 80KB RAM and (partial) register retention XOSC_LF	0.95	µA
	Standby with cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	2.60	µA
		RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF	2.70	µA
	Idle	Supply Systems and RAM powered	580	µA
	Active	MCU running CoreMark at 48 MHz	2.82	mA
PERIPHERAL CURRENT CONSUMPTION(1) (2) (3)				
I_{peri}	Peripheral power domain	Delta current with domain enabled		µA
	Serial power domain	Delta current with domain enabled		
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle		
	µDMA	Delta current with clock enabled, module is idle		
	Timers	Delta current with clock enabled, module is idle		
	I2C	Delta current with clock enabled, module is idle		
	I2S	Delta current with clock enabled, module is idle		
	SSI	Delta current with clock enabled, module is idle		
	UART	Delta current with clock enabled, module is idle		
	CRYPTO	Delta current with clock enabled, module is idle		

(1) Adds to core current I_{core} for each peripheral unit activated.
(2) I_{peri} is not supported in Standby or Shutdown modes.
(3) Measured at VDDS = 3.0 V

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5.5 Power Consumption - Radio Modes

Measured on a Texas Instruments reference design with T_c = 25°C,V_{DDS} = 3.6 V with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
Using boost mode (increasing VDDR up to 1.95 V), will increase system current by 15% (does not apply to TX +14-dBm setting where this current is already included).
Relevant I_{core} and I_{peri} currents are included in below numbers.

PARAMETER	TEST CONDITIONS	TYP	UNIT
Radio receive current	868 MHz	5.8	mA
Radio transmit current Sub-1 GHz PA	0-dBm output power 868 MHz		mA
	+10-dBm output power 868 MHz	14.3	mA
Radio transmit current Boost mode, Sub-1 GHz PA	+14-dBm output power 868 MHz	24.3	mA
Radio transmit current 2.4 GHz PA	0-dBm output power 2440MHz	6.3	mA
	+5-dBm output power 2440MHz	8.2	mA
Radio transmit current High-power PA	Transmit (TX), +20-dBm output power 915 MHz, VDDS = 3.3V	65	mA
Radio transmit current High-power PA	Transmit (TX), +19.5-dBm output power 2440 MHz, VDDS = 3.3V	79	mA

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5.6 Nonvolatile (Flash) Memory Characteristics

over operating free-air temperature range and V_{DDS} = 3.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			8		KB
Supported flash erase cycles before failure, full bank		30			k Cycles
Supported flash erase cycles before failure, single sector		60			k Cycles
Maximum number of write operations per row before sector erase (1)				83	write operations
Flash retention	105 °C	11.4			years at 105 °C
Flash sector erase current	Average delta current		10.4		mA
Flash sector erase time (2)			8		ms
Flash write current	Average delta current, 4 bytes at a time		6		mA
Flash write time (2)	4 bytes at a time		21		µs

(1) Each row is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole flash sector before a sector erase is required.
(2) This number is dependent on Flash aging and increases over time and erase cycles.

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5.7 RF Frequency Bands

over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2500	MHz
	1069		1329	
	861		1054	
	431		527	

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5.8 861 MHz to 1054 MHz — Receive (RX)

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Digital channel filter programmable receive bandwidth		4		4000	kHz
Data rate step size			1.5		bps
Spurious emissions 25 MHz to 1 GHz	868 MHz Conducted emissions measured according to ETSI EN 300 220		-77		dBm
Spurious emissions 1 GHz to 13 GHz			-70		dBm
802.15.4g Mandatory Mode (50 kbps, 2-GFSK, 100-kHz RX Bandwidth)					
Sensitivity	BER = 10^{-2}, 868 MHz		–110		dBm
Saturation limit	BER = 10^{-2}		10		dBm
Selectivity, +200 kHz			(1)44		dB
Selectivity, +400 kHz	(1)		48		dB
Blocking, +1 MHz	(1)		61		dB
Blocking, +2 MHz	(1)		64		dB
Blocking, +5 MHz	(1)		68		dB
Blocking, +10 MHz	(1)		74		dB
Image rejection (image compensation enabled)	(1)		40		dB
RSSI dynamic range	Starting from the sensitivity limit.		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±2		dB
SimpleLink™ Long Range 2.5 kbps or 5 kbps (20 ksym/s, 2-GFSK, 5-kHz Deviation, FEC (Half Rate), DSSS = 1:2 or 1:4, 40-kHz RX Bandwidth					
Sensitivity (2.5 kbps)	BER = 10^{-2}, 868 MHz		-122		dBm
Sensitivity (5 kbps)			-120		dBm
Saturation limit	BER = 10^{-2}		10		dBm
Selectivity, ±100 kHz	2.5 kbps(1)		47		dB
Selectivity, ±200 kHz	2.5 kbps(1)		54		dB
Selectivity, ±300 kHz	2.5 kbps(1)		57		
Blocking, ±1 MHz	2.5 kbps(1)		55		dB
Blocking, ±2 MHz	2.5 kbps(1)		68		dB
Blocking, ±5 MHz	2.5 kbps(1)		74		dB
Blocking, ±10 MHz	2.5 kbps(1)		85		dB
Image rejection (image compensation enabled)			51		dB
RSSI dynamic range	Starting from the sensitivity limit.		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±2		dB

(1) Wanted signal 3 dB above usable sensitivity limit according to ETSI EN 300 220. BER = 10^{-2}, 868 MHz

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5.9 861 MHz to 1054 MHz — Transmit (TX)

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General parameters						
Max output power, boost mode Sub-1 GHz PA		VDDR = 1.95 V Minimum supply voltage (VDDS) for boost mode is 2.1 V 868 MHz and 915 MHz		14		dBm
Max output power, Sub-1 GHz PA		868 MHz and 915 MHz		12		dBm
Max output power, High power PA		868 MHz and 915 MHz VDDS = 3.3V		20		dBm
Output power programmable range Sub-1 GHz PA		868 MHz and 915 MHz				dB
Output power programmable range High power PA		868 MHz and 915 MHz VDDS = 3.3V				dB
Output power variation over temperature Sub-1 GHz PA		+10-dBm setting Over recommended temperature operating range				dB
Output power variation over temperature Boost mode, Sub-1 GHz PA		+14-dBm setting Over recommended temperature operating range				dB
Output power variation over temperature High power PA		+20-dBm setting, VDDS = 3.3V Over recommended temperature operating range				dB
Spurious emissions and harmonics						
Spurious emissions (excluding harmonics) Sub-1 GHz PA, 868 MHz[1]	30 MHz to 1 GHz	+14-dBm setting ETSI restricted bands		-62		dBm
		+14-dBm setting ETSI outside restricted bands		-62		dBm
	1 GHz to 12.75 GHz (outside ETSI restricted bands)	+14-dBm setting measured in 1 MHz bandwidth (ETSI)		-51		dBm
Spurious emissions (excluding harmonics) High power PA, 868 MHz[1]	30 MHz to 1 GHz	+20-dBm setting, VDDS = 3.3V ETSI restricted bands				dBm
		+20-dBm setting, VDDS = 3.3V ETSI outside restricted bands				dBm
	1 GHz to 12.75 GHz (outside ETSI restricted bands)	+20-dBm setting, VDDS = 3.3V measured in 1 MHz bandwidth (ETSI)				dBm

(1) Suitable for systems targeting compliance with EN 300 220, EN 54-25, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

ADVANCE INFORMATION

861 MHz to 1054 MHz — Transmit (TX) *(continued)*

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious emissions out-of-band Sub-1 GHz PA, 915 MHz[1]	30 MHz to 88 MHz (within FCC restricted bands)	+14-dBm setting		–66		dBm
	88 MHz to 216 MHz (within FCC restricted bands)	+14-dBm setting		–67		dBm
	216 MHz to 960 MHz (within FCC restricted bands)	+14-dBm setting		–67		dBm
	960 MHz to 2390 MHz and above 2483.5 MHz (within FCC restricted band)	+14-dBm setting		-64		dBm
	1 GHz to 12.75 GHz (outside FCC restricted bands)	+14-dBm setting		-64		dBm

ADVANCE INFORMATION

861 MHz to 1054 MHz — Transmit (TX) *(continued)*

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious emissions out-of-band High power PA, 915 MHz[1]	30 MHz to 88 MHz (within FCC restricted bands)	+20-dBm setting, VDDS = 3.3V				dBm
	88 MHz to 216 MHz (within FCC restricted bands)	+20-dBm setting, VDDS = 3.3V				dBm
	216 MHz to 960 MHz (within FCC restricted bands)	+20-dBm setting, VDDS = 3.3V				dBm
	960 MHz to 2390 MHz and above 2483.5 MHz (within FCC restricted band)	+20-dBm setting, VDDS = 3.3V				dBm
	1 GHz to 12.75 GHz (outside FCC restricted bands)	+20-dBm setting, VDDS = 3.3V				dBm
Spurious emissions out-of-band Sub-1 GHz PA, 920.6 MHz[1]	Below 710 MHz (ARIB T-108)	+14-dBm setting			<–50	dBm
	710 MHz to 900 MHz (ARIB T-108)	+14-dBm setting			<–63	dBm
	900 MHz to 915 MHz (ARIB T-108)	+14-dBm setting			<–61	dBm
	930 MHz to 1000 MHz (ARIB T-108)	+14-dBm setting			<–60	dBm
	1000 MHz to 1215 MHz (ARIB T-108)	+14-dBm setting			<–58	dBm
	Above 1215 MHz (ARIB T-108)	+14-dBm setting			<–39	dBm
Harmonics Sub-1 GHz PA	Second harmonic	+14-dBm setting, 868 MHz			-50	dBm
		+14-dBm setting, 915 MHz			-53	
	Third harmonic	+14-dBm setting, 868 MHz			-55	dBm
		+14-dBm setting, 915 MHz			-54	
	Fourth harmonic	+14-dBm setting, 868 MHz			-70	dBm
		+14-dBm setting, 915 MHz			-70	
	Fifth harmonic	+14-dBm setting, 868 MHz			-67	dBm
		+14-dBm setting, 915 MHz			-67	
Harmonics High power PA	Second harmonic	+20-dBm setting, VDDS = 3.3V, 868 MHz				dBm
		+20-dBm setting, VDDS = 3.3V, 915 MHz				
	Third harmonic	+20-dBm setting, VDDS = 3.3V, 868 MHz				dBm
		+20-dBm setting, VDDS = 3.3V, 915 MHz				
	Fourth harmonic	+20-dBm setting, VDDS = 3.3V, 868 MHz				dBm
		+20-dBm setting, VDDS = 3.3V, 915 MHz				
	Fifth harmonic	+20-dBm setting, VDDS = 3.3V, 868 MHz				dBm
		+20-dBm setting, VDDS = 3.3V, 915 MHz				

ADVANCE INFORMATION

5.10 861 MHz to 1054 MHz — PLL Phase Noise

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868- and 915-MHz band	±10 kHz offset		–76		dBc/Hz
	±100 kHz offset		–100		dBc/Hz
	±200 kHz offset		–108		dBc/Hz
	±400 kHz offset		–115		dBc/Hz
	±1000 kHz offset		–123		dBc/Hz
	±2000 kHz offset		–127		dBc/Hz
	±10000 kHz offset		–141		dBc/Hz

ADVANCE INFORMATION

5.11 Bluetooth low energy — Receive (RX)

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125-kbps (Bluetooth 5 coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		-103		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		>5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	-260		310	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)	-260		260	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)	-140		150	ppm
Co-channel rejection(1)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		-3		dB
Selectivity, ±1 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		9 / 5(1)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		43 / 32(1)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		47 / 42(1)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		46 / 47(1)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		49 / 46(1)		dB
Alternate channel rejection, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		50 / 47(1)		dB
Selectivity, Image frequency(1)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		32		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co-channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 32(1)		dB
Blocker rejection, ±8 MHz and above(1)	Wanted signal at –79 dBm, modulated interferer at ≥ ±8 MHz and above, BER = 10^{-3}		> 46		dB
Out-of-band blocking(2)	30 MHz to 2000 MHz		-40		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		-19		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		-22		dBm
Intermodulation	Wanted signal at 2402 MHz, –76 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		-42		dBm
500-kbps (Bluetooth 5 coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		-101		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		> 5		dBm

(1) Numbers given as I/C dB.
(2) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification.

ADVANCE INFORMATION

Bluetooth low energy — Receive (RX) *(continued)*

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	-240		240	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)	-500		500	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)	-310		330	ppm
Co-channel rejection(1)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		-5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		9 / 5(1)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		41 / 31(1)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		44 / 41(1)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		44 / 44(1)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		44 / 44(1)		dB
Alternate channel rejection, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		44 / 44(1)		dB
Selectivity, Image frequency(1)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co-channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 41(1)		dB
Blocker rejection, ±8 MHz and above	Wanted signal at –79 dBm, modulated interferer at ≥ ±8 MHz and above, BER = 10^{-3}		44		dB
Out-of-band blocking(2)	30 MHz to 2000 MHz		-35		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		-19		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		-19		dBm
Intermodulation	Wanted signal at 2402 MHz, –76 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		-37		dBm
1-Mbps 2-GFSK (Bluetooth 4 and Bluetooth 5 low energy)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–97		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		4		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–350		350	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	–750		750	ppm

ADVANCE INFORMATION

Bluetooth low energy — Receive (RX) *(continued)*

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 3(3)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		34 / 25(3)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		38 / 26(3)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		42 / 29(3)		dB
Selectivity, ±5 MHz or more(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = 10^{-3}		32		dB
Selectivity, Image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		25		dB
Selectivity, Image frequency ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		3 / 26(3)		dB
Out-of-band blocking(2)	30 MHz to 2000 MHz		–20		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–5		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–8		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–8		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–34		dBm
Spurious emissions, 30 to 1000 MHz(4)	Measurement in a 50-Ω single-ended load.		–71		dBm
Spurious emissions, 1 to 12.75 GHz(4)	Measurement in a 50 Ω single-ended load.		–62		dBm
RSSI dynamic range			70		dB
RSSI accuracy					dB
2-Mbps 2-GFSK (Bluetooth 5)					
Receiver sensitivity	Differential mode. Measured at SMA connector, BER = 10^{-3}		–92		dBm
Receiver saturation	Differential mode. Measured at SMA connector, BER = 10^{-3}		4		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–300		500	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	–1000		1000	ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–7		dB

(3) X / Y, where X is +N MHz and Y is –N MHz.
(4) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

ADVANCE INFORMATION

Bluetooth low energy — Receive (RX) *(continued)*

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz BER = 10^{-3}		8 / 4(3)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		31 / 26(3)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		37 / 38(3)		dB
Alternate channel rejection, ±7 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		37 / 36(3)		dB
Selectivity, Image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		4		dB
Selectivity, Image frequency ±2 MHz(1)	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = 10^{-3}		–7 / 26(3)		dB
Out-of-band blocking(2)	30 MHz to 2000 MHz		–33		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–15		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–10		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–45		dBm

ADVANCE INFORMATION

5.12 Bluetooth low energy — Transmit (TX)

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power, High power PA	Differential mode, delivered to a single-ended 50 Ω load through a balun VDDS = 3.3V			19.5		dBm
Max output power, 2.4-GHz PA	Differential mode, delivered to a single-ended 50 Ω load through a balun			5		dBm
Output power programmable range High power PA	Differential mode, delivered to a single-ended 50 Ω load through a balun VDDS = 3.3V					dB
Output power programmable range, 2.4-GHz PA	Differential mode, delivered to a single-ended 50 Ω load through a balun			26		dB
Output power variation over temperature, High power PA	Over recommended temperature operating range VDDS = 3.3V					dB
Output power variation over temperature, 2.4-GHz PA	Over recommended temperature operating range					dB
Spurious emissions and harmonics						
Spurious emissions, High-power PA(1)	f < 1 GHz, outside restricted bands	+20-dBm setting VDDS = 3.3V				dBm
	f < 1 GHz, restricted bands ETSI	+20-dBm setting VDDS = 3.3V				dBm
	f < 1 GHz, restricted bands FCC	+20-dBm setting VDDS = 3.3V				dBm
	f > 1 GHz, including harmonics	+20-dBm setting VDDS = 3.3V				dBm
Spurious emissions, 2.4-GHz PA(1)	f < 1 GHz, outside restricted bands	+5-dBm setting		–43		dBm
	f < 1 GHz, restricted bands ETSI	+5-dBm setting		–65		dBm
	f < 1 GHz, restricted bands FCC	+5-dBm setting		–76		dBm
	f > 1 GHz, including harmonics	+5-dBm setting		–46		dBm
Harmonics, High-power PA(1)	Second harmonic	+20-dBm setting VDDS = 3.3V				dBm
	Third harmonic	+20-dBm setting VDDS = 3.3V				dBm
	Fourth harmonic	+20-dBm setting VDDS = 3.3V				dBm
	Fifth harmonic	+20-dBm setting VDDS = 3.3V				dBm
Harmonics, 2.4-GHz PA(1)	Second harmonic	+5-dBm setting				dBm
	Third harmonic	+5-dBm setting				dBm
	Fourth harmonic	+5-dBm setting				dBm
	Fifth harmonic	+5-dBm setting				dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

ADVANCE INFORMATION

5.13 Zigbee and Thread — IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) — RX

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	PER = 1%		–101		dBm
Receiver saturation	PER = 1%		+4		dBm
Adjacent channel rejection	Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1%		39		dB
Alternate channel rejection	Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1%		52		dB
Channel rejection, ±15 MHz or more	Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		57		dB
Blocking and desensitization, 5 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking and desensitization, 10 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking and desensitization, 20 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking and desensitization, 50 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		68		dB
Blocking and desensitization, –5 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –10 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –20 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking and desensitization, –50 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		67		dB
Spurious emissions, 30 MHz to 1000 MHz	Measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–71		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–62		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		>200		ppm
Symbol rate error tolerance	Difference between incoming symbol rate and the internally generated symbol rate		>1000		ppm
RSSI dynamic range			100		dB
RSSI accuracy					dB

5.14 Zigbee and Thread — IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) — TX

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power, high power PA	Differential mode, delivered to a single-ended 50-Ω load through a balun VDDS = 3.3V			19.5		dBm
Max output power, 2.4-GHz PA	Differential mode, delivered to a single-ended 50-Ω load through a balun			5		dBm
Output power programmable range, High power PA	Differential mode, delivered to a single-ended 50-Ω load through a balun VDDS = 3.3V					dB
Output power programmable range, 2.4-GHz PA	Differential mode, delivered to a single-ended 50-Ω load through a balun			26		dB
Output power variation over temperature, High power PA	Over recommended temperature operating range VDDS = 3.3V					dB
Output power variation over temperature, 2.4-GHz PA	Over recommended temperature operating range					dB
Spurious emissions and harmonics						
Spurious emissions, High-power PA(1)	f < 1 GHz, outside restricted bands	+20-dBm setting VDDS = 3.3V				dBm
	f < 1 GHz, restricted bands ETSI	+20-dBm setting VDDS = 3.3V				dBm
	f < 1 GHz, restricted bands FCC	+20-dBm setting VDDS = 3.3V				dBm
	f > 1 GHz, including harmonics	+20-dBm setting VDDS = 3.3V				dBm
Spurious emissions, 2.4-GHz PA(1)	f < 1 GHz, outside restricted bands	+5-dBm setting		–43		dBm
	f < 1 GHz, restricted bands ETSI	+5-dBm setting		–65		dBm
	f < 1 GHz, restricted bands FCC	+5-dBm setting		–76		dBm
	f > 1 GHz, including harmonics	+5-dBm setting		–46		dBm
Harmonics, High-power PA(1)	Second harmonic	+20-dBm setting VDDS = 3.3V				dBm
	Third harmonic	+20-dBm setting VDDS = 3.3V				dBm
	Fourth harmonic	+20-dBm setting VDDS = 3.3V				dBm
	Fifth harmonic	+20-dBm setting VDDS = 3.3V				dBm
Harmonics, 2.4-GHz PA(1)	Second harmonic	+5-dBm setting				dBm
	Third harmonic	+5-dBm setting				dBm
	Fourth harmonic	+5-dBm setting				dBm
	Fifth harmonic	+5-dBm setting				dBm
IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)						

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

ADVANCE INFORMATION

Zigbee and Thread — IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) — TX *(continued)*

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection.
All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Error vector magnitude, High power PA	+20-dBm setting VDDS = 3.3V				%
Error vector magnitude, 2.4-GHz PA	+5-dBm setting		2		%

ADVANCE INFORMATION

5.15 Thermal Resistance Characteristics

THERMAL METRIC(1)		PACKAGE	UNIT(2)
		RGZ (VQFN)	
		48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.

ADVANCE INFORMATION

5.16 Timing and Switching Characteristics

Table 5-1. Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

Table 5-2. Wakeup Timing(1)

Measured over operating free-air temperature with V_{DDS} = 3.0 V (unless otherwise noted). The times listed here do not include software overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset to Active			750-2500		µs
MCU, Shutdown to Active			750-2500		µs
MCU, Standby to Active			160		µs
MCU, Active to Standby			36		µs
MCU, Idle to Active			14		µs

(1) Duration of wakeup sequence is dependent on VDDR capacitor size and remaining charge on VDDR capacitor when starting the device again.

ADVANCE INFORMATION

5.16.1 Clock Specifications

Table 5-3. 48-MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance			60	Ω
L_M	Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads)		$< 0.5 \times 10^{-24} / C^2_L$		H
C_L	Crystal load capacitance(2)	5	7(3)	9	pF
	Start-up time(4)		250		µs

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
(2) Adjustable load capacitance is integrated into the device. **External load capacitors are required for systems targeting compliance with ARIB T-108 and 470–510 MHz frequency bands.**When external load capacitance is used, the internal capacitance must be set to zero through software configuration in the Customer Configuration Section (CCFG). See the device errata for further details.
(3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG)
(4) Startup time number requires use of TI-provided power driver which performs clock calibration every crystal startup. Startup time may increase if driver is not used.

Table 5-4. 32.768-kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

		MIN	TYP	MAX	UNIT
	Crystal frequency		32.768		kHz
ESR	Equivalent series resistance		30	100	kΩ
C_L	Crystal load capacitance	6	7(2)	12	pF

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
(2) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

Table 5-5. 48-MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1		%
Calibrated frequency accuracy(1)		±0.25		%
Start-up time		5		µs

(1) Accuracy relatively to the calibration source (XOSC_HF).

Table 5-6. 2-MHz RC Oscillator (RCOSC_MF)

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		2		MHz
Start-up time		5		µs

Table 5-7. 32-kHz RC Oscillator (RCOSC_LF)

Measured on the Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		32.768		kHz
Temperature coefficient		50		ppm/°C

ADVANCE INFORMATION

5.16.2 Synchronous Serial Interface (SSI) Characteristics

Table 5-8. Synchronous Serial Interface (SSI) Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	system clocks (1)
S2 (2)	t_{clk_high}	SSIClk high time		0.5		t_{clk_per}
S3 (2)	t_{clk_low}	SSIClk low time		0.5		t_{clk_per}

(1) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.
(2) Refer to SSI timing diagrams Figure 5-1, Figure 5-2, and Figure 5-3.

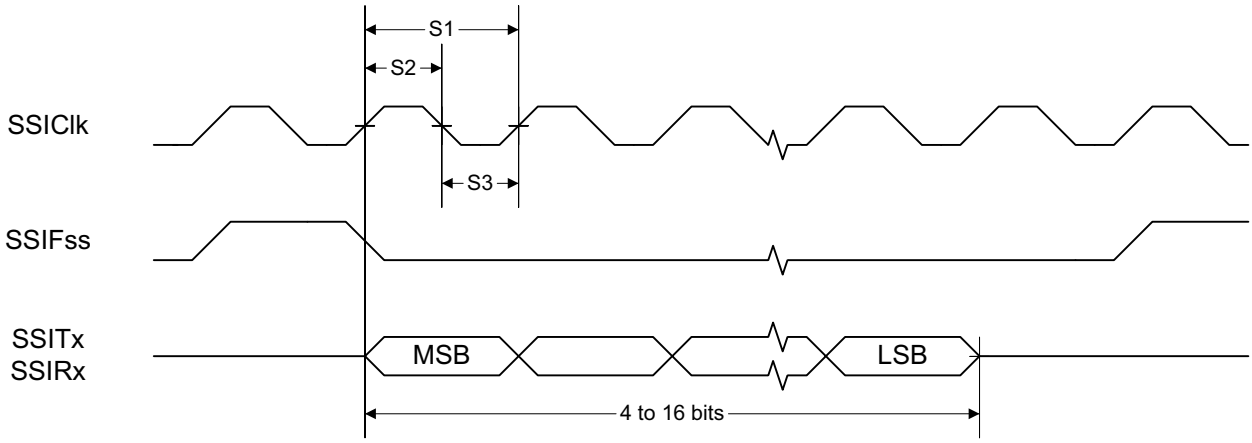

Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

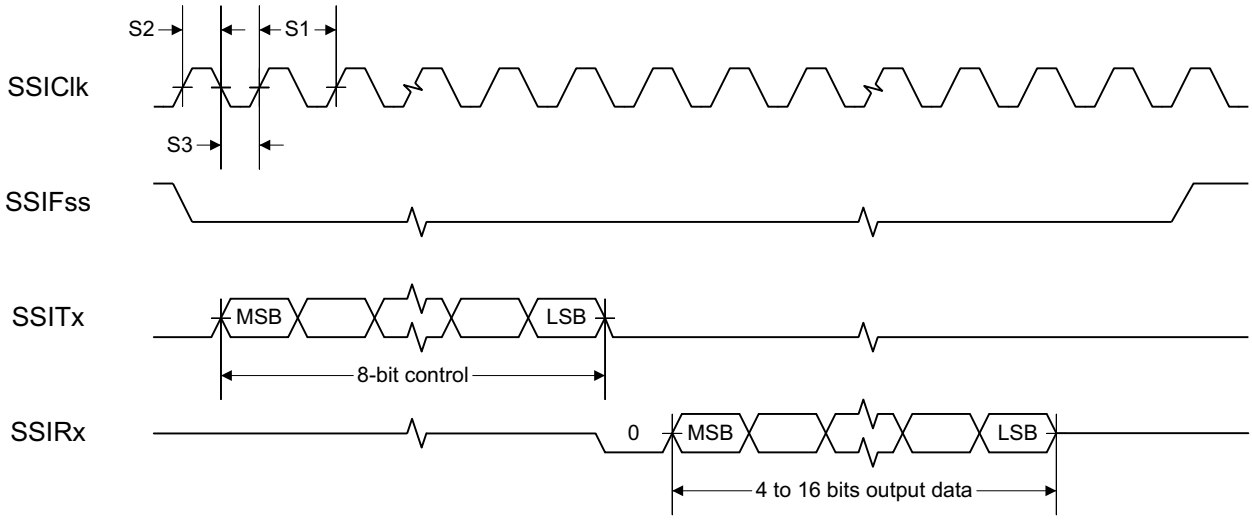

Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

ADVANCE INFORMATION

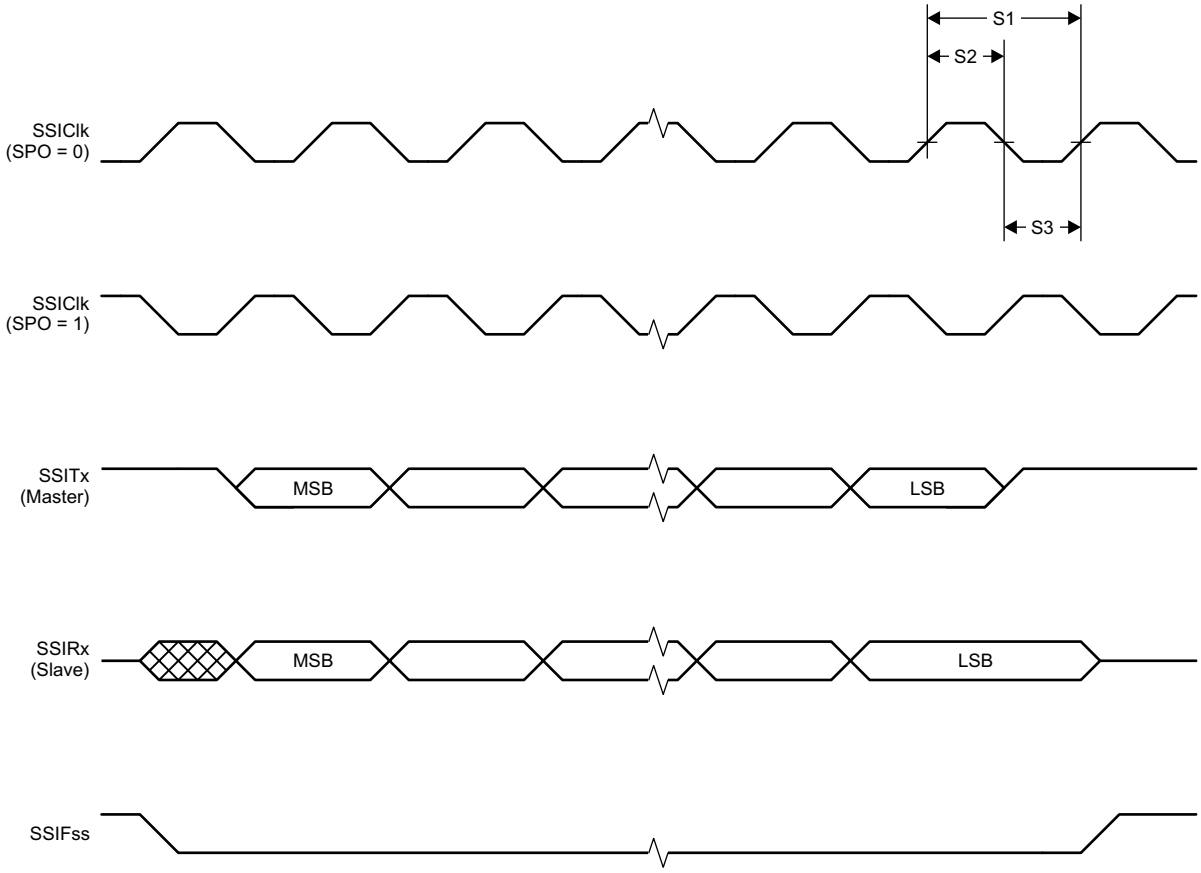

Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.16.3 UART

Table 5-9. UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate	3			MBaud

5.17 Peripheral Characteristics

ADVANCE INFORMATION

5.17.1 ADC

Table 5-10. ADC Characteristics

T_c = 25°C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		VDDS	V
	Resolution			12		Bits
	Sample rate				200	kSamples/s
	Offset	Internal 4.3-V equivalent reference(2)		2		LSB
	Gain error	Internal 4.3-V equivalent reference(2)		7.8		LSB
DNL(3)	Differential nonlinearity			>–1		LSB
INL	Integral nonlinearity			±4		LSB
ENOB	Effective number of bits	Internal 4.3-V equivalent reference(2), 200 kSamples/s, 9.6-kHz input tone		9.5		Bits
		VDDS as reference, 200 kSamples/s, 9.6-kHz input tone		9.8		
		Internal 1.48-V reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300-Hz input tone		9.9		
THD	Total harmonic distortion	Internal 4.3-V equivalent reference(2), 200 kSamples/s, 9.6-kHz input tone		–64		dB
		VDDS as reference, 200 kSamples/s, 9.6-kHz input tone		–68		
		Internal 1.48-V reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300-Hz input tone		–72		
SINAD, SNDR	Signal-to-noise and Distortion ratio	Internal 4.3-V equivalent reference(2), 200 kSamples/s, 9.6-kHz input tone		59		dB
		VDDS as reference, 200 kSamples/s, 9.6-kHz input tone		61		
		Internal 1.48-V reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300-Hz input tone		68		
SFDR	Spurious-free dynamic range	Internal 4.3-V equivalent reference(2), 200 kSamples/s, 9.6-kHz input tone		69		dB
		VDDS as reference, 200 kSamples/s, 9.6-kHz input tone		72		
		Internal 1.48-V reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300-Hz input tone		75		
	Conversion time	Serial conversion, time-to-output, 24-MHz clock		50		clock-cycles
	Current consumption	Internal 4.3-V equivalent reference(2)		0.69		mA
	Current consumption	VDDS as reference		0.93		mA
	Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1.		4.3(2)(4)		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: V_{ref} = 4.3 V × 1408 / 4095		1.48		V

(1) Using IEEE Std 1241-2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.
(3) No missing codes. Positive DNL typically varies up to 1.8 LSB, depending on device.
(4) Applied voltage must be within Absolute Maximum Ratings (see Section 5.1) at all times.

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Table 5-10. ADC Characteristics (continued)

T_c = 25°C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference voltage	VDDS as reference (Also known as *RELATIVE*) (input voltage scaling enabled)		VDDS		V
Reference voltage	VDDS as reference (Also known as *RELATIVE*) (input voltage scaling disabled)		VDDS / 2.82(4)		V
Input impedance	200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		MΩ

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5.17.2 Temperature and Battery Monitor

Table 5-11. Temperature Sensor

Measured on a Texas Instruments reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			2		°C
Measurement range		–40		85	°C
Accuracy	-40 °C		4.4		°C
Accuracy	25 °C		1.9		°C
Accuracy	85 °C		1.8		°C
Supply voltage coefficient(1)			3.8		°C/V

(1) Automatically compensated when using supplied driver libraries.

Table 5-12. Battery Monitor

Measured on a Texas Instruments reference design with T_c = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			25		mV
Range		1.8		3.8	V
INL (max)			23		mV
Accuracy	V_{DDS} = 3.0 V		22.5		mV
Offset error			-32		mV
Gain error			-1		%

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5.17.3 Comparators

Table 5-13. Continuous Time Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
External reference voltage		0		V_{DDS}	V
Internal reference voltage(1)	Using internal DAC with V_{DDS} as reference voltage, DAC code = 0-255		0 - 2.78		V
Offset			±4		mV
Hysteresis			< 2		mV

(1) The comparator can use the output of an internal DAC as its reference. Reference voltages can be derived from V_{DDS}, DCOUPL (1.28V), and the internal ADC reference.

Table 5-14. Low-Power Clocked Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32.768		kHz
Internal reference voltage(1)	Using internal DAC with V_{DDS} as reference voltage, DAC code = 0-255		0 - 2.78		V

(1) The comparator can use the output of an internal DAC as its reference. Reference voltages can be derived from V_{DDS}, DCOUPL (1.28V), and the internal ADC reference.

5.17.4 Current Source

Table 5-15. Programmable Current Source

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range (logarithmic range)			0.25 to 20		µA
Resolution			0.25		µA
Current consumption(1)	Including current source at maximum programmable output		21		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

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5.17.5 GPIO

Table 5-16. GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 1.8 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		1.54		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.25		V
GPIO VOH at 4-mA load	IOCURR = 1		1.58		V
GPIO VOL at 4-mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		68		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		18.5		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.72		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.36		V
T_A = 25°C, V_{DDS} = 3.0 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		2.57		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.45		V
GPIO VOH at 4-mA load	IOCURR = 1		2.61		V
GPIO VOL at 4-mA load	IOCURR = 1		0.40		V

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Table 5-16. GPIO DC Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 3.8V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		265		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		106		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.53		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.43		V
VIH	Lowest GPIO input voltage reliably interpreted as a *High*			0.8	VDDS (1)
VIL	Highest GPIO input voltage reliably interpreted as a *Low*	0.2			VDDS (1)

(1) Each GPIO is referenced to a specific VDDS pin. See the technical reference manual listed in Section 8.3 for more details.

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6 Detailed Description

6.1 Overview

Section 6.2 shows the core modules of the CC1352P device.

6.2 Functional Block Diagram

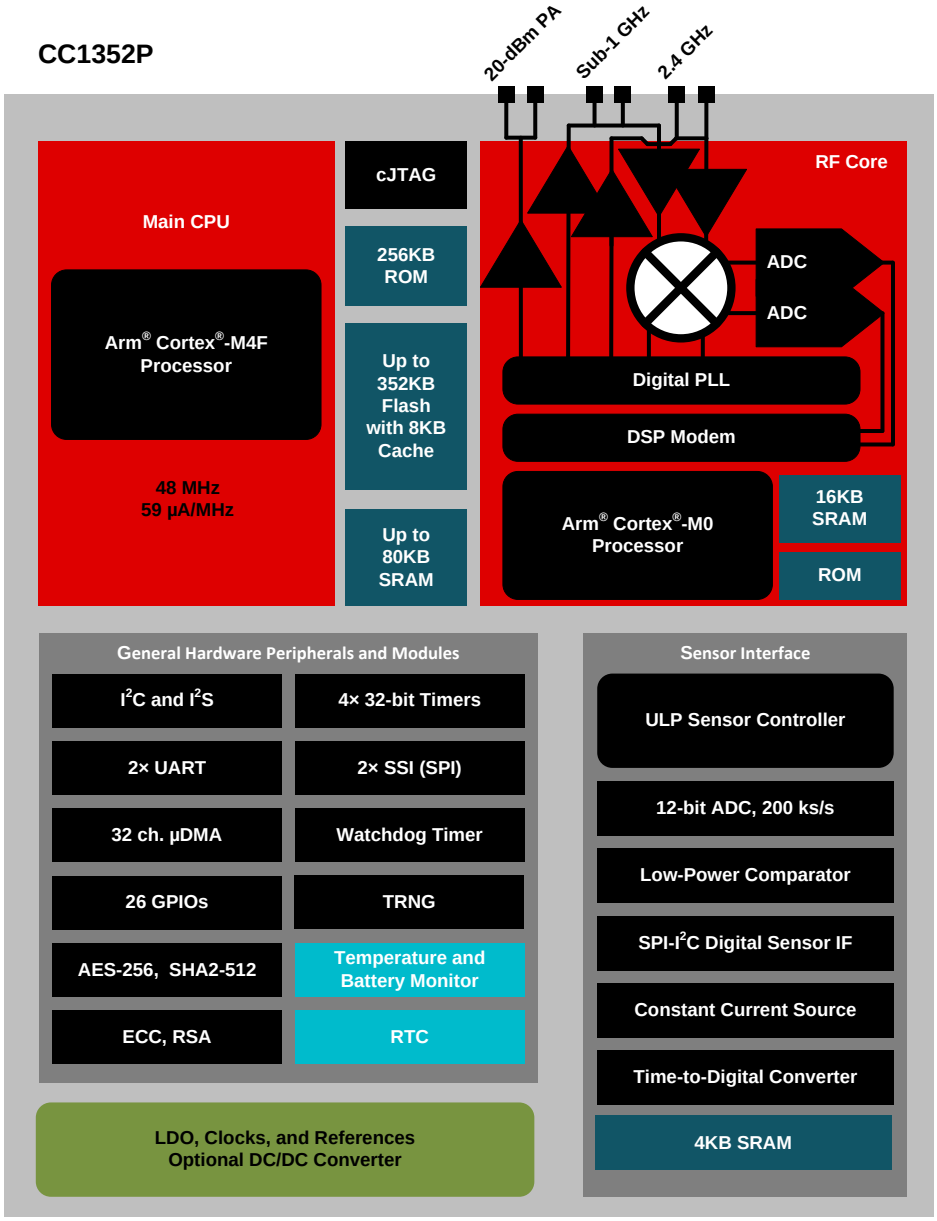

Figure 6-1. CC1352P Block Diagram

6.3 System CPU

The CC1352P SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4F system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Memory Protection Unit (MPU) for safety-critical applications
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48-MHz operation
- 1.25 DMIPS per MHz

6.4 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

Dual-band and multiprotocol solutions are enabled through time-sliced access of the radio, handled transparently for the application through the TI-provided RF driver and dual-mode manager.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

NOTE

Not all combinations of features, frequencies, data rates, and modulation formats described in this chapter are supported. Over time, TI can enable new physical radio formats (PHYs) for the device and provides performance numbers for selected PHYs in the data sheet. Supported radio formats for a specific device, including optimized settings to use with the TI RF driver, are included in the SmartRF Studio tool with performance numbers of selected formats found in Section 5.

6.4.1 Proprietary Radio Formats

The CC1352P radio can support a wide range of physical radio formats through a set of hardware peripherals combined with firmware available in the device ROM, covering various customer needs for optimizing towards parameters such as speed or sensitivity. This allows great flexibility in tuning the radio both to work with legacy protocols as well as customizing the behavior for specific application needs.

Table 6-1 gives a simplified overview of features of the various radio formats available in ROM of the device. Other radio formats may be available in the form of radio firmware patches or programs through the Software Development Kit (SDK) and may combine features in a different manner, as well as add other features.

Table 6-1. Feature Support

Feature	Main 2-(G)FSK Mode	High Data Rates	Low Data Rates	SimpleLink™ Long Range
Programmable preamble, sync word and CRC	Yes	Yes	Yes	No
Programmable receive bandwidth	Yes	Yes	Yes (down to 4 kHz)	Yes
Data / Symbol rate(1)	20 to 1000 kbps	≤ 2 Msps	≤ 100 ksps	≤ 20 ksps
Modulation format	2-(G)FSK	2-(G)FSK 4-(G)FSK	2-(G)FSK 4-(G)FSK	2-(G)FSK
Dual Sync Word	Yes	Yes	No	No
Carrier Sense(2)(3)	Yes	No	No	No
Preamble Detection(3)	Yes	Yes	Yes	No

(1) Data rates are only indicative. Data rates outside this range may also be supported. For some specific combinations of settings, a smaller range might be supported.
(2) Carrier Sense can be used to implement HW-controlled listen-before-talk (LBT) and Clear Channel Assesment (CCA) for compliance with such requirements in regulatory standards. This is available through the CMD_PROP_CS radio API.
(3) Carrier Sense and Preamble Detection can be used to implement sniff modes where the radio is duty cycled to save power.

Table 6-1. Feature Support (continued)

Feature	Main 2-(G)FSK Mode	High Data Rates	Low Data Rates	SimpleLink™ Long Range
Data Whitening	Yes	Yes	Yes	Yes
Digital RSSI	Yes	Yes	Yes	Yes
CRC filtering	Yes	Yes	Yes	Yes
Direct-sequence spread spectrum (DSSS)	No	No	No	1:2 1:4 1:8
Forward error correction (FEC)	No	No	No	Yes
Link Quality Indicator (4) (LQI)	Yes	Yes	Yes	Yes

(4) This feature will only be available in device revision D and later.

6.4.2 Bluetooth 5 low energy

The RF Core offers full support for Bluetooth 5 low energy, including the high-sped 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5 stack or through a high-level Bluetooth API. The Bluetooth 5 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5 enables fast, reliable firmware updates.

6.4.3 802.15.4 (Thread, Zigbee, 6LoWPAN)

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Thread, Zigbee, and 6LoWPAN protocols. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

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6.5 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to five 16-KB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. System SRAM is always initialized to zeroes upon code execution from boot and supports parity checking for detection of bit errors in memory.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4-KB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

6.6 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still ensuring ultra-low power
- Dynamic reuse of hardware resources
- Ability to perform simple data processing without the need for dedicated hardware
- Observability and debugging options

Sensor Controller Studio is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or I^2C (I^2C and UART are bit-banged)
- Capacitive sensing
- Waveform generation
- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs
- Dedicated SPI master with up to 6-MHz clock speed

The peripherals in the Sensor Controller can also be controlled from the main application processor.

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6.7 Cryptography

The CC1352P device comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.
Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- True Random Number Generator (TRNG) module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- Secure Hash Algorithm 2 (SHA-2) with support for SHA224, SHA256, SHA384, and SHA512
- Advanced Encryption Standard (AES) with 128 and 256 bit key lengths
- Public Key Accelerator - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits and RSA key pair generation up to 1024 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for an application or stack:

- Key Agreement Schemes
  - Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- Signature Generation
  - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- Curve Support
  - Short Weierstrass form (full hardware support), such as:
    - NIST-P224, NIST-P256, NIST-P384, NIST-P521
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
    - secp256r1
  - Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- SHA2 based MACs
  - HMAC with SHA224, SHA256, SHA384, or SHA512
- Block cipher mode of operation
  - AESCCM
  - AESGCM
  - AESECB
  - AESCBC
  - AESCBC-MAC
- True random number generation

Other capabilities, such as RSA encryption and signatures as well as Edwards type of elliptic curves such as Curve1174 or Ed25519, can also be implemented using the provided hardware accelerators but are not part of the TI SimpleLink SDK for the CC1352P device.

6.8 Timers

A large selection of timers are available as part of the CC1352P device. These timers are:

- **Real-Time Clock (RTC)**
  - A 70-bit 3-channel timer running on the 32-kHz low frequency system clock (SCLK_LF)

    This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32768 Hz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. The real time clock can also be read by the Sensor Controller Engine to timestamp sensor data and also has dedicated capture channels. By default, the RTC halts when a debugger halts the device.
- **General Purpose Timers (GPTIMER)**

  The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERs are available in Active and Idle power modes.
- **Sensor Controller Timers**

  The Sensor Controller contains 3 timers:

  AUX Timer 0 and 1 are 16-bit timers with a 2^N prescaler. Timers can either increment on a clock or on each edge of a selected tick source. Both one-shot and periodical timer modes are available.

  AUX Timer 2 is a 16-bit timer that can operate at 24-MHz, 2-MHz or 32-kHz independent of the Sensor Controller functionality. There are 4 capture or compare channels, which can be operated in one-shot or periodical modes. The timer can be used to generate events for the Sensor Controller or the ADC, as well as for PWM output or waveform generation.
- **Radio Timer**

  A multichannel 32-bit timer running on 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.
- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5-MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

6.9 Serial Peripherals and I/O

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz. The SSI modules support configurable phase and polarity.

The UARTs implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps.

The I^2S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I^2C interface is also used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100-kHz and 400-kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in Section 4. All digital peripherals can be connected to any digital pin on the device.

For more information, see the CC13x2, CC26x2 SimpleLink™ Wireless MCU Technical Reference Manual.

6.10 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC1352P device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

6.11 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

6.12 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

6.13 Power Management

To minimize power consumption, the CC1352P supports a number of power modes and power management features (see Table 6-2).

Table 6-2. Power Modes, V_{DDS} = 3.0V

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
48 MHz high-speed clock (SCLK_HF)	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
2 MHz medium-speed clock (SCLK_MF)	RCOSC_MF	RCOSC_MF	Available	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	Available	Available	Available	Available	Available
Brownout detector (BOD)	Active	Active	Duty Cycled	Off	N/A
Power-on reset (POR)	Active	Active	Active	Active	N/A
Watchdog timer (WDT)	Available	Available	Paused	Off	N/A

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 6-2).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

NOTE

The power, RF and clock management for the CC1352P device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC1352P software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

6.14 Clock Systems

The CC1352P device has several internal system clocks.

The 48-MHz SCLK_HF is used as the main MCU and peripheral clock. This can be driven by the internal 48-MHz RC Oscillator (RCOSC_HF) or an external 48-MHz crystal (required for radio operation)

SCLK_MF is an internal 2-MHz clock which is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK_MF clock is always driven by an internal 2-MHz RC Oscillator (RCOSC_HF)

SCLK_LF is the 32.768-kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by an internal 32.768-kHz RC Oscillator (RCOSC_LF), a 32.768-kHz watch-type crystal or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32-kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

6.15 Network Processor

Depending on the product configuration, the CC1352P device can function as a wireless network processor (WNP—a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

7 Application, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 LaunchPad™ Development Kit Reference Design

The LaunchPad Development Kit that supports the CC1352P device also functions as a detailed reference design for schematic and layout.

CC1352P LaunchPad™ Development Kit Design Files

The CC1352P LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC1352P device.

Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag

The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual band antennas for 868 and 915 MHz combined with 2.4 GHz

The antenna kit includes a µSMA(JSC) cable to connect the wireless LaunchPad Development Kits and SensorTags.

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, XCC1352P is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of *CC1352P* devices in the RGZ (7-mm x 7-mm) package type, see the *Package Option Addendum* of this document, the Device Information in Section 1.3, the TI website (www.ti.com), or contact your TI sales representative.

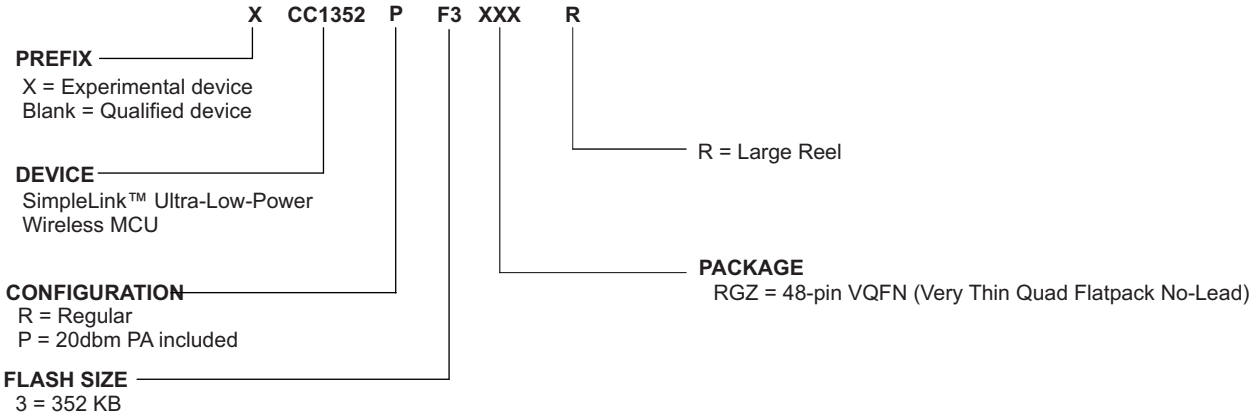


Figure 8-1. Device Nomenclature

ADVANCE INFORMATION

8.2 Tools and Software

The CC1352P device is supported by a variety of software and hardware development tools.

Development Kit

CC1352P LaunchPad™ Development Kit

The CC1352P LaunchPad™ Development Kit enables development of high-performance wireless applications in the 863–930 MHz and 2.4-GHz frequency bands that benefit from low-power operation. The kit features the CC1352P dual-band and multiprotocol SimpleLink Wireless MCU with an integrated High Power Amplifier. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more. The built-in EnergyTrace™ software is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

The RF configuration of the Launchpad enables up to +20-dBm output power for 863-930 MHz and +5-dBm output power for 2.4GHz

CC1352P-2 LaunchPad™ Development Kit

The CC1352P-2 LaunchPad™ Development Kit enables development of high-performance wireless applications in the 863–930 MHz and 2.4-GHz frequency bands that benefit from low-power operation. The kit features the CC1352P dual-band and multiprotocol SimpleLink Wireless MCU with an integrated High Power Amplifier. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more. The built-in EnergyTrace™ software is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

The RF configuration of the Launchpad enables up to +14-dBm output power for 863-930 MHz and +20-dBm output power for 2.4GHz

CC1352P-4 400-MHz LaunchPad™ Development Kit

The CC1352P 400-MHz LaunchPad™ Development Kit enables development of high-performance wireless applications in the 433 MHz, 470–510 MHz, and 2.4-GHz frequency bands that benefit from low-power operation. The kit features the CC1352P dual-band and multiprotocol SimpleLink Wireless MCU with an integrated High Power Amplifier. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more. The built-in EnergyTrace™ software is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

The RF configuration of the Launchpad enables up to +14-dBm output power for 433 MHz, +20-dBm output power for 470-510 MHz and +5-dBm output power for 2.4GHz. The Launchpad can also be used as a development kit when evaluating other device family devices such as CC1312R and CC1352R for use with 400-MHz frequency bands.

Software

SimpleLink™ CC13X2 SDK

The SimpleLink CC13X2 Software Development Kit (SDK) provides a comprehensive Sub-1 GHz software package for the development of applications for the CC1352P wireless MCU. The SimpleLink CC13X2 SDK includes the TI 15.4-Stack software, providing an IEEE 802.15.4e/g-based star topology networking solution for Sub-1 GHz band, along with a large set of proprietary RF examples for Sub-1 GHz based on the RF driver through the EasyLink RF abstraction layer. The SimpleLink CC13X2 SDK also packages the Bluetooth-, Zigbee- and Thread software stacks, enabling the possibility to develop dual-band and multiprotocol solutions with a single system-on-chip.

The SimpleLink CC13X2 SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit http://www.ti.com/simplelink.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests — send and receive packets between nodes
- Antenna and radiation tests — set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

Sensor Controller Studio

Sensor Controller Studio is used to write, test and debug code for the Sensor Controller peripheral. The tool generates a Sensor Controller Interface driver, which is a set of C source files that are compiled into the System CPU application. These source files also contain the Sensor Controller binary image and allow the System CPU application to control and exchange data with the Sensor Controller. Features of the Sensor Controller Studio include:

- Ready-to-use examples for several common use cases
- Full toolchain with built-in compiler and assembler for programming in a C-like programming language
- Provides rapid development by using the integrated sensor controller task testing and debugging functionality, including visualization of sensor data and verification of algorithms

CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

8.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC1352P. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC1352P Silicon Errata The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device.

Technical Reference Manual (TRM)

CC13x2, CC26x2 SimpleLink™ Wireless MCU TRM The TRM provides a detailed description of all modules and peripherals available in the device family.

8.3.1 TI SimpleLink™

TI's new SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

8.3.2 TI Design Network

The TI Design Network is a worldwide community of respected, well-established companies offering products and services that complement TI's semiconductor device solutions. Products and services include a broad range of reference designs, turnkey products and services, system modules, embedded software, engineering services, and development tools that help customers accelerate development efforts and reduce time-to-market.

Search the network on www.ti.com/3p to find a suitable partner for modules, engineering services, or development tools.

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

ADVANCE INFORMATION

8.5 Trademarks

SmartRF, SimpleLink, LaunchPad, EnergyTrace, Code Composer Studio, E2E are trademarks of Texas Instruments.
Arm, Cortex, Arm Thumb are registered trademarks of Arm Limited (or its subsidiaries).
Bluetooth is a registered trademark of Bluetooth SIG Inc.
Eclipse is a registered trademark of Eclipse Foundation.
CoreMark is a registered trademark of Embedded Microprocessor Benchmark Consortium.
I-jet is a trademark of IAR Systems AB.
IAR Embedded Workbench is a registered trademark of IAR Systems AB.
Windows is a registered trademark of Microsoft Corporation.
J-Link is a trademark of SEGGER Microcontroller Systeme GmbH.
Wi-Fi is a registered trademark of Wi-Fi Alliance.
Wi-SUN is a registered trademark of Wi-SUN Alliance Inc.
Zigbee is a registered trademark of Zigbee Alliance Inc.
All other trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1352P1F3RGZR	PREVIEW	VQFN	RGZ	48	2500	TBD	Call TI	Call TI	-40 to 85		
CC1352P1F3RGZT	PREVIEW	VQFN	RGZ	48	250	TBD	Call TI	Call TI	-40 to 85		
XCC1352P1F3RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1352 P1F3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

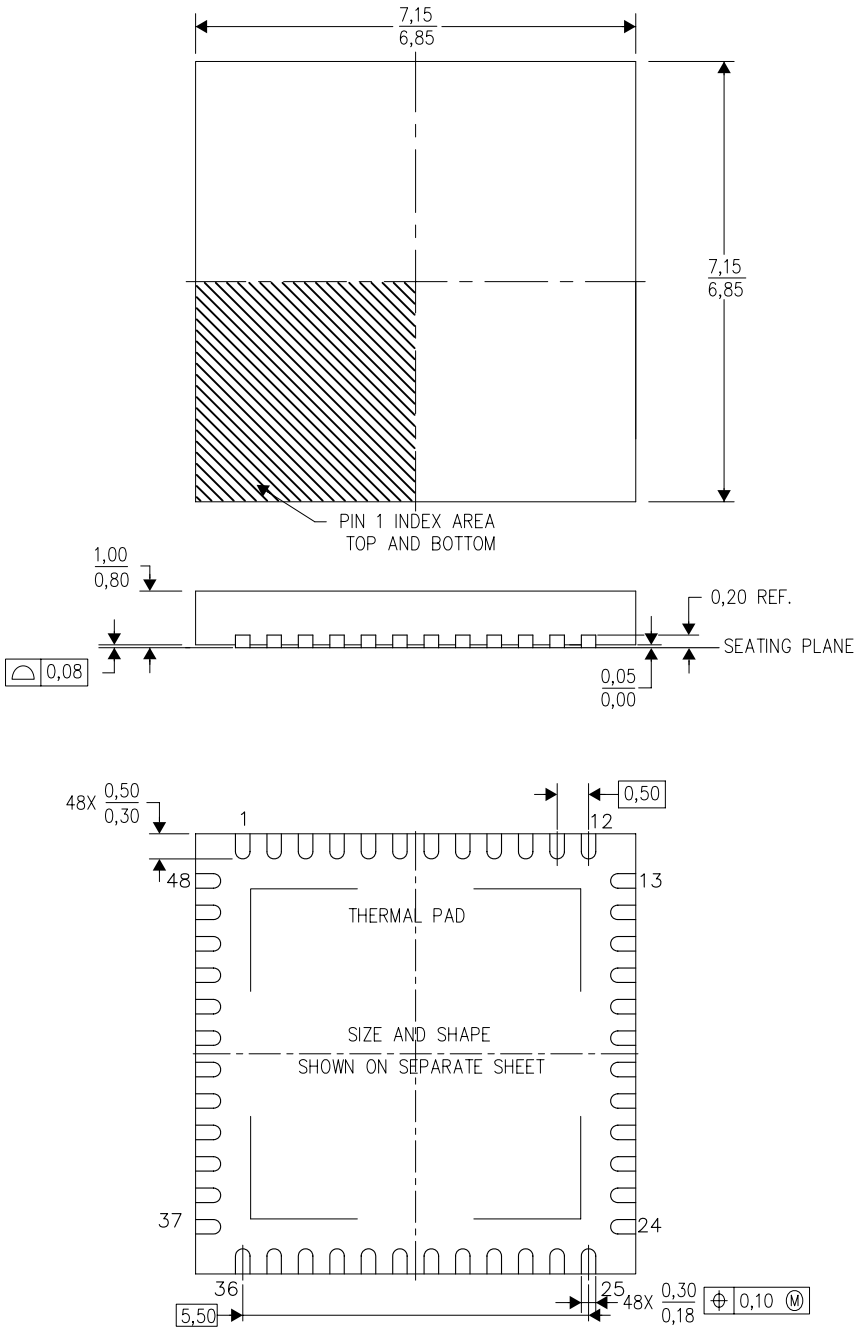
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

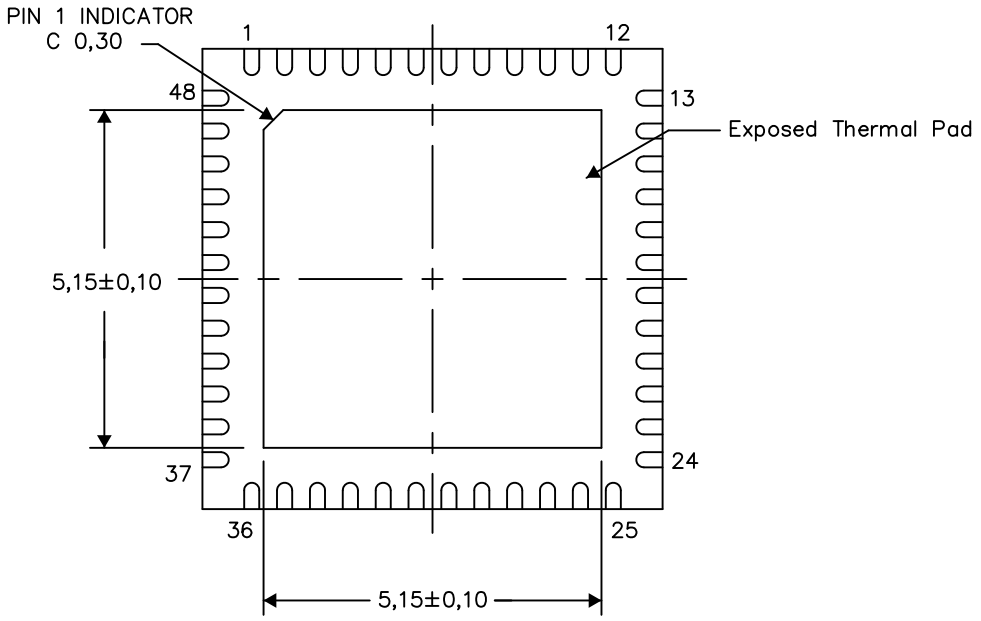
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



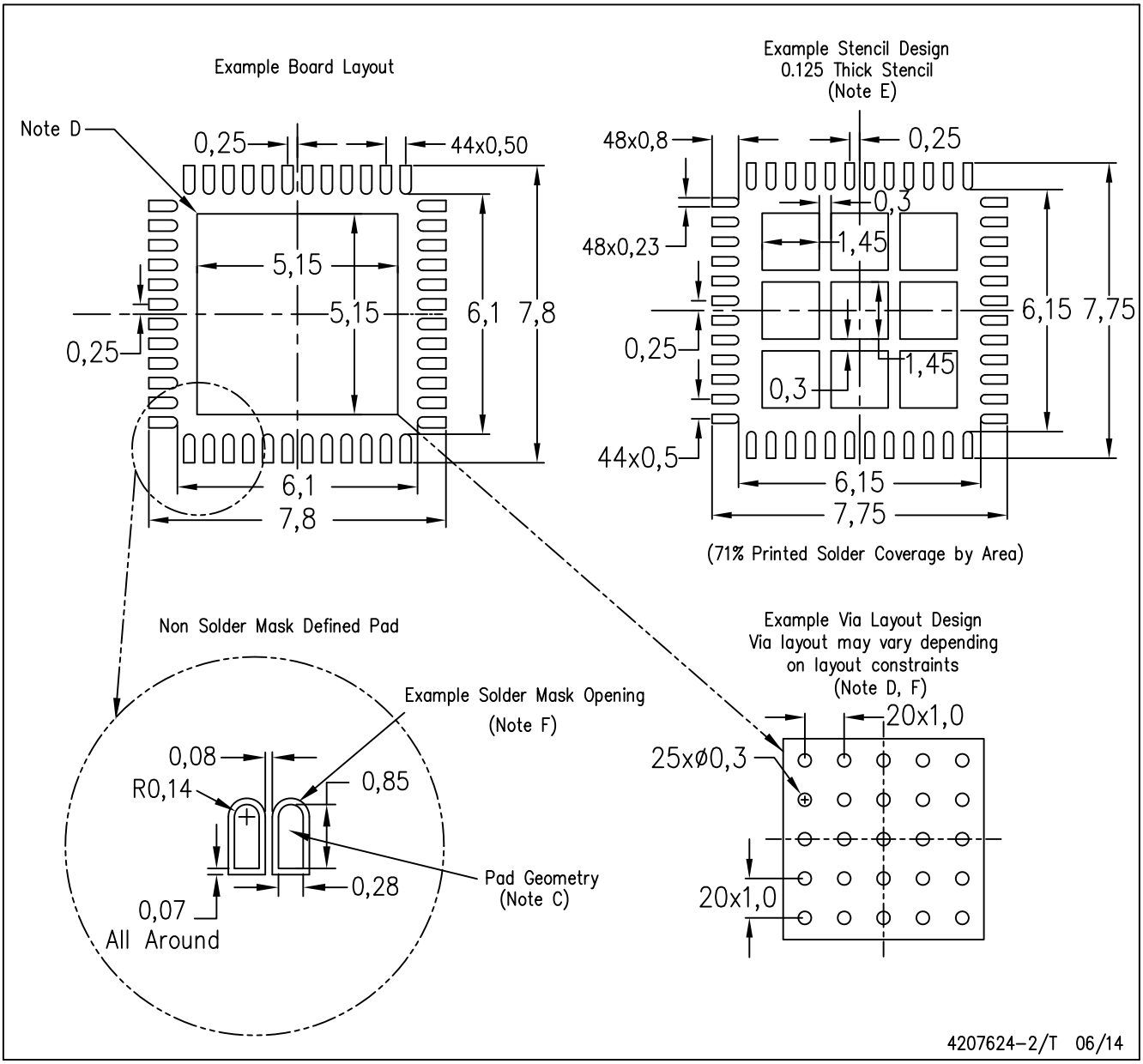
Bottom View

Exposed Thermal Pad Dimensions

4206354–2/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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