

Smart High-Side Power Switch

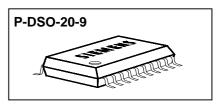
Two Channels: 2 x $60m\Omega$

Status Feedback

Product Summary

Operating Voltage	V _{bb(on)}	4.75.	41V
	Active channels	one	two parallel
On-state Resistance	R _{ON}	$60 \text{m}\Omega$	$30 m\Omega$
Nominal load current	I _{L(NOM)}	4.0A	6.0A
Current limitation	I _{L(SCr)}	17A	17A

Package



General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology.
- Fully protected by embedded protection functions

Applications

- µC compatible high-side power switch with diagnostic feedback for 5V, 12V and 24V grounded loads
- All types of resistive, inductive and capacitve loads
- Most suitable for loads with high inrush currents, so as lamps
- · Replaces electromechanical relays, fuses and discrete circuits

Basic Functions

- Very low standby current
- CMOS compatible input
- Improved electromagnetic compatibility (EMC)
- · Fast demagnetization of inductive loads
- Stable behaviour at undervoltage
- Wide operating voltage range
- Logic ground independent from load ground

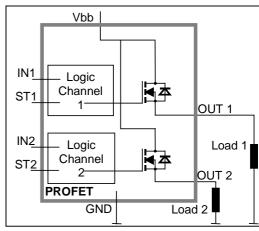
Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of V_{bb} protection
- Electrostatic discharge protection (ESD)

Diagnostic Function

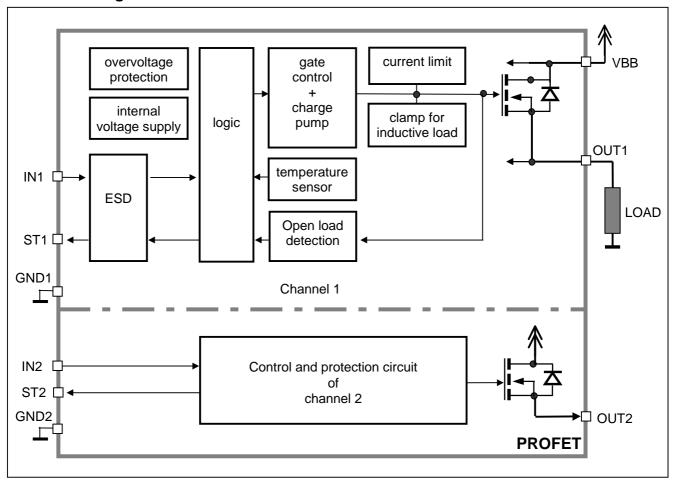
- Diagnostic feedback with open drain output
- Open load detection in ON-state
- Feedback of thermal shutdown in ON-state

Block Diagram





Functional diagram



Pin Definitions and Functions

Pin	Symbol	Function
1,10,	V_{bb}	Positive power supply voltage. Design the
11,12,		wiring for the simultaneous max. short circuit
15,16,		currents from channel 1 to 2 and also for low
19,20		thermal resistance
3	IN1	Input 1,2, activates channel 1,2 in case of
7	IN2	logic high signal
17,18	OUT1	Output 1,2, protected high-side power output
13,14	OUT2	of channel 1,2. Design the wiring for the max.
		short circuit current
4	ST1	Diagnostic feedback 1,2 of channel 1,2,
8	ST2	open drain, low on failure
2	GND1	Ground 1 of chip 1 (channel 1)
6	GND2	Ground 2 of chip 2 (channel 2)
5,9	N.C.	Not Connected

Pin configuration

(top view)		
V_{bb}	1 •	20	V_{bb}
GND1	2	19	V _{bb}
IN1	3	18	OUT1
ST1	4	17	OUT1
N.C.	5	16	V_{bb}
GND2	6	15	V _{bb}
IN2	7	14	OUT2
ST2	8	13	OUT2
N.C.	9	12	V_{bb}
V_{bb}	10	11	V _{bb}
			1



Maximum Ratings at $T_i = 25$ °C unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 4)	$V_{ m bb}$	43	V
Supply voltage for full short circuit protection $T_{j,\text{start}} = -40 \dots +150^{\circ}\text{C}$	$V_{ m bb}$	24	V
Load current (Short-circuit current, see page 5)	<i>I</i> ∟	self-limited	Α
Load dump protection ¹⁾ $V_{\text{LoadDump}} = V_{\text{A}} + V_{\text{S}}$, $V_{\text{A}} = 13.5 \text{ V}$ $R_{\text{I}}^{(2)} = 2 \Omega$, $t_{\text{d}} = 200 \text{ ms}$; IN = low or high, each channel loaded with $R_{\text{L}} = 8.0 \Omega$,	V _{Load dump} 3)	60	V
Operating temperature range	$T_{\rm j}$	-40+150	°C
Storage temperature range	T_{stg}	-55+150	
Power dissipation (DC) ⁴⁾ $T_a = 25$ °C:	P_{tot}	3.7	W
(all channels active) $T_a = 85$ °C:		1.9	
Maximal switchable inductance, single pulse $V_{bb} = 12V$, $T_{j,start} = 150^{\circ}C^{4}$,	7	10.0	
$I_L = 4.0 \text{ A}$, $E_{AS} = 220 \text{ mJ}$, 0Ω one channel:	Z_{L}	19.9	mH
$I_L = 6.0 \text{ A}, E_{AS} = 540 \text{ mJ}, 0\Omega$ two parallel channels:		22.3	
see diagrams on page 9	1		
Electrostatic discharge capability (ESD) IN: (Human Body Model) ST: out to all other pins shorted: acc. MIL-STD883D, method 3015.7 and ESD assn. std. S5.1-1993	V _{ESD}	1.0 4.0 8.0	kV
R=1.5kΩ; C=100pF	17	40 .40	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Input voltage (DC)	V_{IN}	-10 +16	V
Current through input pin (DC)	I _{IN}	±2.0	mA
Current through status pin (DC)	I _{ST}	±5.0	
see internal circuit diagram page 8			

Thermal Characteristics

Parameter and Conditions		Symbol	Values			Unit	
			min	typ	Max		
Thermal resistance junction - soldering point ^{4),5)}	each channel:	R			13.5	K/W	
,		$R_{\rm thjs}$			13.3	r\/vv	
junction - ambient4)	one channel active:	$R_{\rm thja}$		41			
	all channels active:			34			

¹⁾ Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a 150 Ω resistor for the GND connection is recommended.

 $^{^{2)}}$ R_{I} = internal resistance of the load dump test pulse generator

³⁾ V_{Load dump} is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

⁴⁾ Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70μm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 14

⁵⁾ Soldering point: upper side of solder edge of device pin 15. See page 14



Electrical Characteristics

Parameter and Conditions, each of the two channels	Symbol		Values		Unit
at $T_j = -40+150$ °C, $V_{bb} = 12$ V unless otherwise specified		min	typ	Max	-
Load Switching Capabilities and Characteristic	S				
On-state resistance (V_{bb} to OUT); $I_L = 2 \text{ A}, V_{bb} \ge 7V$					
each channel, $T_i = 25$ °C:	R _{ON}		50	60	mΩ
$T_{\rm j} = 150^{\circ}{\rm C}$			100	120	
two parallel channels, $T_i = 25$ °C: see diagram, page 10			25	30	
Nominal load current one channel active:	I _{L(NOM)}	3.6	4.0		Α
two parallel channels active:		5.5	6.0		
Device on PCB ⁶), $T_a = 85$ °C, $T_j \le 150$ °C					
Output current while GND disconnected or pulled up; Vbb = 30 V, VIN = 0,	/L(GNDhigh)			2	mA
see diagram page 8; (not tested specified by design)					
Turn-on time ⁷⁾ IN \int to 90% V_{OUT} :	<i>t</i> on	30	100	200	μs
Turn-off time IN \square to 10% V_{OUT} :	$t_{ m off}$	30	100	200	
$R_{\rm L}$ = 12 Ω					
Slew rate on 7)	d V/dt _{on}	0.1		1	V/μs
10 to 30% V_{OUT} , $R_{\text{L}} = 12 \Omega$:					
Slew rate off ⁷⁾ 70 to 40% V_{OUT} , $R_{\text{L}} = 12 \Omega$:	-dV/dt _{off}	0.1		1	V/µs

Operating randineters						
Operating voltage Tj=-40		$V_{ m bb(on)}$	4.75		41	V
	T _j =25150°C:				43	
Overvoltage protection ⁸⁾	<i>T</i> _j =-40°C:	$V_{\rm bb(AZ)}$	41			V
$I_{\rm bb} = 40 \text{ mA}$	$T_{\rm j}$ =25150°C:		43	47	52	
Standby current ⁹⁾	<i>T</i> _j =-40°C25°C:	I _{bb(off)}		10	18	μΑ
$V_{IN} = 0$; see diagram page 10	$T_{\rm j}$ =150°C:				50	
Leakage output current (included in Ibb(off))		I _{L(off)}		1	10	μΑ
VIN = 0						
Operating current ¹⁰⁾ , $V_{IN} = 5V$,						
$I_{\text{GND}} = I_{\text{GND1}} + I_{\text{GND2}},$	one channel on:	I _{GND}		0.8	1.5	mΑ
	two channels on:			1.6	3.0	

⁶⁾ Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm 2 (one layer, 70 μ m thick) copper area for $V_{\mbox{bb}}$ connection. PCB is vertical without blown air. See page 14

⁷⁾ See timing diagram on page 11.

⁸⁾ Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a 150 Ω resistor for the GND connection is recommended). See also Von(CL) in table of protection functions and circuit diagram on page 8.

Measured with load; for the whole device; all channels off

¹⁰⁾ Add I_{ST} , if $I_{ST} > 0$

BTS 728 L2

Parameter and Conditions, each of the two channels		Symbol	Values		Unit	
at T _j = -40+150°C, V_{bb} = 12 V unless oth	nerwise specified		min	typ	Max	
Protection Functions						
Current limit, (see timing diagrams, pag	je 12)					
	$T_j = -40$ °C:	I _{L(lim)}	21	28	36	Α
	<i>T</i> j =25°C:		17	22	31	
	$T_{j} = +150^{\circ}C$:		12	16	24	
Repetitive short circuit current limit,						
$T_{\rm j} = T_{\rm jt}$	each channel	I _{L(SCr)}		17		Α
two parallel channels				17		
(see timing diagrams, page 12)						
Initial short circuit shutdown time	$T_{\rm j,start}$ =25°C:	t _{off(SC)}		2.4		ms
(see timing diagrams on page 12)						
Output clamp (inductive load switch						V
at $VON(CL) = V_{bb} - VOUT$, $I_{L} = 40 \text{ mA}$	$T_{\rm j}$ =-40°C:	$V_{ON(CL)}$	41			
	=25°C150°C:		43	47	52	
Thermal overload trip temperature		T_{jt}	150			°C
Thermal hysteresis		$\Delta T_{\rm jt}$		10		K
Reverse Battery						
Reverse battery voltage 12)		-V _{bb}			32	V
Drain-source diode voltage ($V_{out} > V_{L} = -4.0 \text{ A}, T_{j} = +150 ^{\circ}\text{C}$	/bb)	-V _{ON}		600		mV

¹¹⁾ If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest V_{ON(CL)}

¹²⁾ Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 8).

BTS 728 L2

Parameter and Conditions, ea	ach of the two channels	Symbol		Values		Unit
at T _j = -40+150°C, V_{bb} = 12 V unles		- Cym.501	min			•
at 1) = -40+130 C, vpp = 12 v unie.	33 Otherwise specified		min	typ	Max	
Diagnostic Characteristics						
Open load detection current, (c	n-condition)					
	each channel	I _{L (OL)}	10		500	mΑ
		•		"	•	
. ,						
Input and Status Feedback ¹³				Ţ		
Input resistance		R_{I}	2.5	3.5	6	kΩ
(see circuit page 8)						
Input turn-on threshold voltage		$V_{IN(T+)}$	1.7		3.2	V
Input turn-off threshold voltage		$V_{IN(T-)}$	1.5			V
Input threshold hysteresis		$\Delta V_{\text{IN(T)}}$		0.5		V
Off state input current	$V_{IN} = 0.4 \text{ V}$:	I _{IN(off)}	1		50	μΑ
On state input current	$V_{IN} = 5 \text{ V}$:	I _{IN(on)}	20	50	90	μΑ
Delay time for status with open load after switch		t _{d(ST OL4)}	100	520	900	μs
off; (see diagram on page 13)						
Status output (open drain)						
- n n n	$I_{ST} = +1.6 \text{ mA}$:	$V_{\rm ST(high)}$	5.4	6.1		V
Zener limit voltage	ISI - TI.0 IIIA.	Y ST (High)	• • •	_		

 $^{^{\}rm 13)}\,$ If ground resistors ${\rm R}_{\rm GND}$ are used, add the voltage drop across these resistors.



Truth Table

Channel 1	Input 1	Output 1	Status 1
Channel 2	Input 2	Output 2	Status 2
	level	level	BTS 728L2
Normal	L	L	Н
operation	Н	Н	Н
Open load	L	Z	Н
	Н	Н	L
Overtem-	L	L	Н
perature	Н	L	L

L = "Low" Level

X = don't care

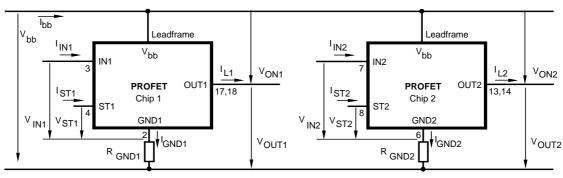
Z = high impedance, potential depends on external circuit

H = "High" Level S

Status signal valid after the time delay shown in the timing diagrams

Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor.

Terms

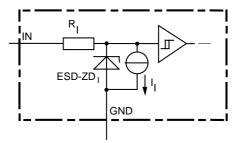


Leadframe (V_{bb}) is connected to pin 1,10,11,12,15,16,19,20

External R_{GND} optional; two resistors R_{GND1}, R_{GND2} = 150 Ω or a single resistor R_{GND} = 75 Ω for reverse battery protection up to the max. operating voltage.

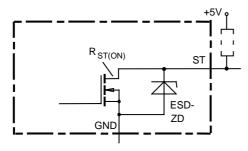
SIEMENS

Input circuit (ESD protection), IN1 or IN2



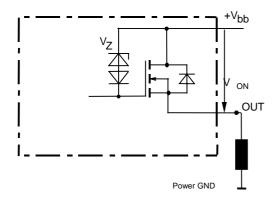
The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Status output, ST1 or ST2



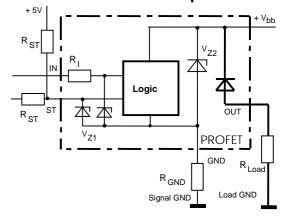
ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)}$ < 375 Ω at 1.6 mA. The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Inductive and overvoltage output clamp, OUT1 or OUT2



VON clamped to VON(CL) = 47 V typ.

Overvolt. and reverse batt. protection



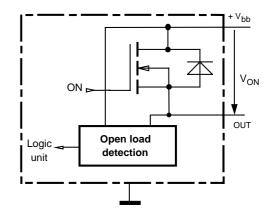
 V_{Z1} = 6.1 V typ., V_{Z2} = 47 V typ., R_{GND} = 150 Ω, R_{ST} = 15 kΩ, R_{I} = 3.5 kΩ typ.

In case of reverse battery the load current has to be limited by the load. Temperature protection is not active

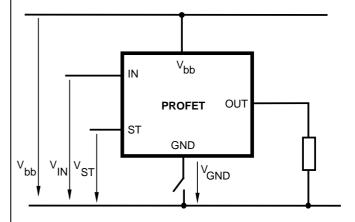
Open-load detection OUT1 or OUT2

ON-state diagnostic

Open load, if $V_{\text{ON}} < R_{\text{ON}} \cdot I_{\text{L(OL)}}$; IN high



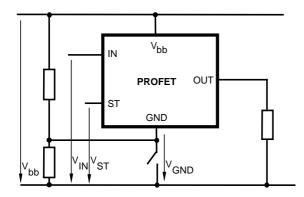
GND disconnect



Any kind of load. In case of IN = high is $V_{OUT} \approx V_{IN} - V_{IN}(T+)$. Due to $V_{GND} > 0$, no $V_{ST} = low$ signal available.

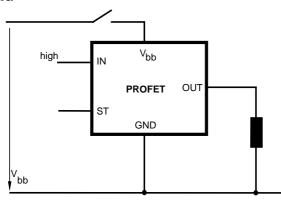


GND disconnect with GND pull up



Any kind of load. If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off Due to $V_{GND} > 0$, no $V_{ST} = low$ signal available.

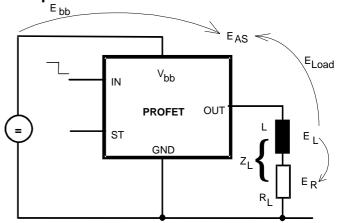
V_{bb} disconnect with energized inductive load



For inductive load currents up to the limits defined by Z_L (max. ratings and diagram on page 9) each switch is protected against loss of $V_{\mbox{bb}}$.

Consider at your PCB layout that in the case of Vbb disconnection with energized inductive load all the load current flows through the GND connection.

Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_{L} = \frac{1}{2} \cdot L \cdot I_{I}^{2}$$

While demagnetizing load inductance, the energy dissipated in PROFET is

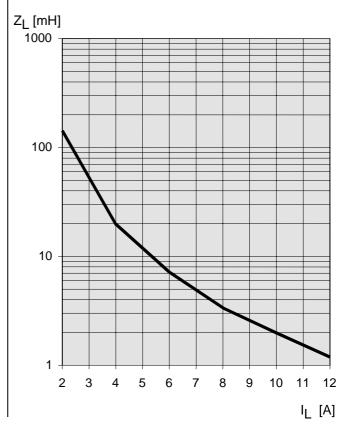
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t) dt$$

with an approximate solution for R $_L > 0\,\Omega$:

$$E_{\text{AS}} = \frac{I_{\text{L}} \cdot L}{2 \cdot R_{\text{L}}} (V_{\text{bb}} + |V_{\text{OUT(CL)}}|) \ ln \ (1 + \frac{I_{\text{L}} \cdot R_{\text{L}}}{|V_{\text{OUT(CL)}}|})$$

Maximum allowable load inductance for a single switch off (one channel)⁴⁾

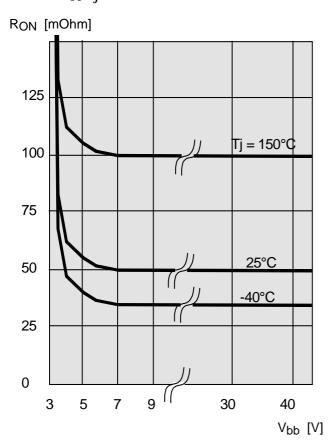
$$L = f(I_L)$$
; T_{j,start} = 150°C, V_{bb} = 12 V, R_L = 0 Ω





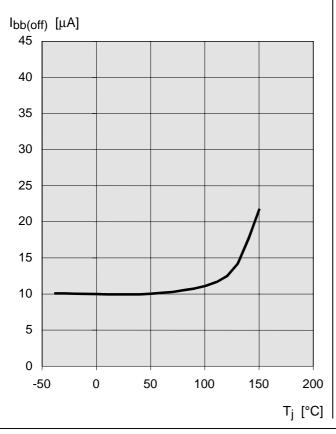
Typ. on-state resistance

 $R_{ON} = f(V_{bb}, T_j); I_L = 2 A, IN = high$



Typ. standby current

 $I_{bb(off)} = f(T_j); V_{bb} = 9...34 \text{ V}, \text{IN1,2} = \text{low}$



SIEMENS

Timing diagrams

Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

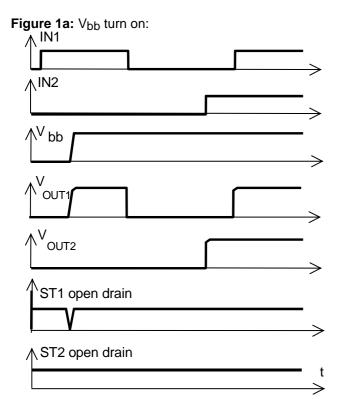


Figure 2a: Switching a resistive load, turn-on/off time and slew rate definition:

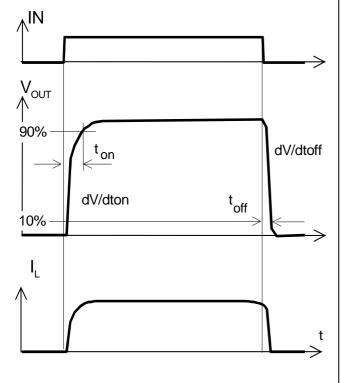
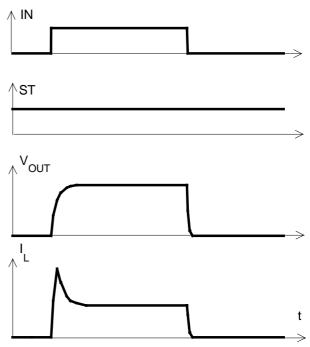
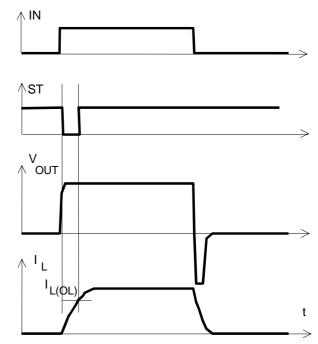


Figure 2b: Switching a lamp:



The initial peak current should be limited by the lamp and not by the current limit of the device.

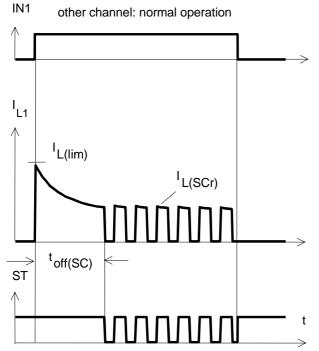
Figure 2c: Switching an inductive load



*) if the time constant of load is too large, open-load-status may occur

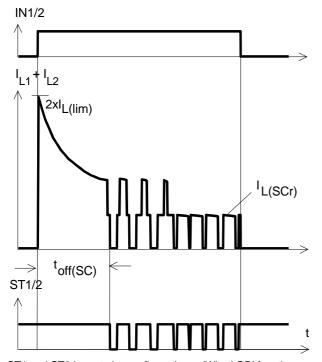
SIEMENS

Figure 3a: Turn on into short circuit: shut down by overtemperature, restart by cooling



Heating up of the chip may require several milliseconds, depending on external conditions

Figure 3b: Turn on into short circuit: shut down by overtemperature, restart by cooling (two parallel switched channels 1 and 2)



ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor.

Figure 4a: Overtemperature: Reset if $T_i < T_{it}$

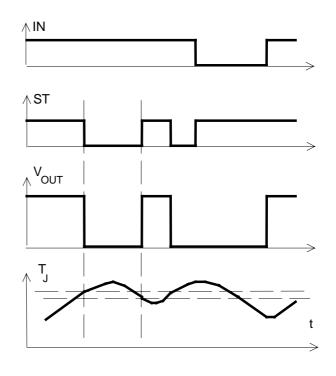


Figure 5a: Open load: detection in ON-state, open load occurs in on-state

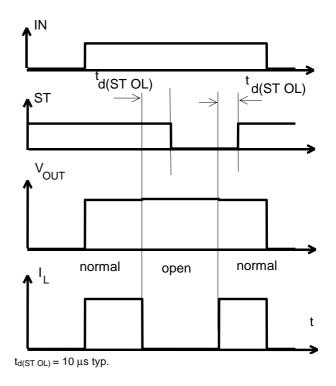
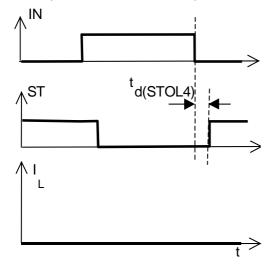




Figure 5b: Open load: turn on/off to open load



Package and Ordering Code

Standard: P-DSO-20-9

Sales Code	BTS 728 L2
Ordering Code	Q67060-S7014-A2

All dimensions in millimetres

0.35x45°
7.8-02

0.35x45°
7.8-02

0.35x45°
7.8-02

10.3±03

10.3±03

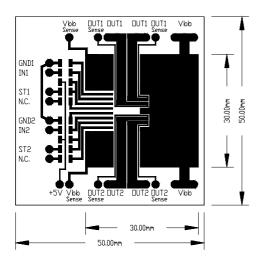
Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

Definition of soldering point with temperature T_s: upper side of solder edge of device pin 15.



Printed circuit board (FR4, 1.5mm thick, one layer $70\mu m$, $6cm^2$ active heatsink area) as a reference for max. power dissipation P_{tot} , nominal load current $I_{L(NOM)}$ and thermal resistance R_{thia}



Published by Siemens AG, Bereich Bauelemente, Vertrieb, Produkt-Information, Balanstraße 73, D-81541 München © Siemens AG 1999. All Rights Reserved

As far as patents or other rights of third parties are concerned, liability is only assumed for components per se, not for applications, processes and circuits implemented within components or assemblies. The information describes a type of component and shall not be considered as warranted characteristics. The characteristics for which SIEMENS grants a warranty will only be specified in the purchase contract. Terms of delivery and rights to change design reserved. For questions on technology, delivery and prices please contact the Offices of Semiconductor Group in Germany or the Siemens Companies and Representatives woldwide (see address list). Due to technical requirements components may contain dangerous substances. For information on the type in question please contact your nearest Siemens Office, Semiconductor Group. Siemens AG is an approved CECC manufacturer.

Packing: Please use the recycling operators known to you. We can also help you - get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport. For packing material that is returned to us unsorted or which we are not obliged to accept we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorised for such purpose! Critical components¹⁴⁾ of the Semiconductor Group of Siemens AG, may only be used in life supporting devices or systems¹⁵⁾ with the express written approval of the Semiconductor Group of Siemens AG.

¹⁴⁾ A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

Life support devices or systems are intended (a) to be implanted in the human body or (b) support and/or maintain and sustain and/or protect human life. If they fail, it is reasonably to assume that the health of the user or other persons may be endangered.