

# BTM7751G

TrilithIC

Automotive Power



Never stop thinking

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## 1 Overview

### Features

- Quad D-MOS switch driver
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Low  $R_{DS\ ON}$   
High side: 70 mΩ typ. @ 25°C, 180 mΩ max. @ 150°C  
Low side: 45 mΩ typ. @ 25°C, 105 mΩ max. @ 150°C
- Maximum peak current: typ. 14 A @ 25 °C
- Very low quiescent current: typ. 5 μA @ 25 °C
- Small outline, enhanced power PG-DSO-package
- Operates up to 40 V
- PWM frequencies up to 1 kHz
- Status flag diagnosis
- Short-circuit-protection
- Overtemperature shut down with hysteresis
- Internal clamp diodes
- Open load detection in Off-mode
- Under-voltage detection with hysteresis
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-28-22

### Description

The **BTM7751G** is part of the **TrilithIC** family containing three dies in one package: One double high-side switch and two low-side switches. The drains of these three vertical DMOS chips are mounted on separated lead frames. The sources are connected to individual pins, so the **BTM7751G** can be used in H-bridge- as well as in any other configuration. Both the double high-side and the two low-side switches of the **BTM7751G** are manufactured in SMART SIPMOS® technology which combines low  $R_{DS\ ON}$  vertical DMOS power stages with CMOS circuitry for control, protection and diagnosis.

Type	Package	Marking
BTM7751G	PG-DSO-28-22	BTM7751G

## 2 Pin Configuration

### 2.1 Pin Assignment

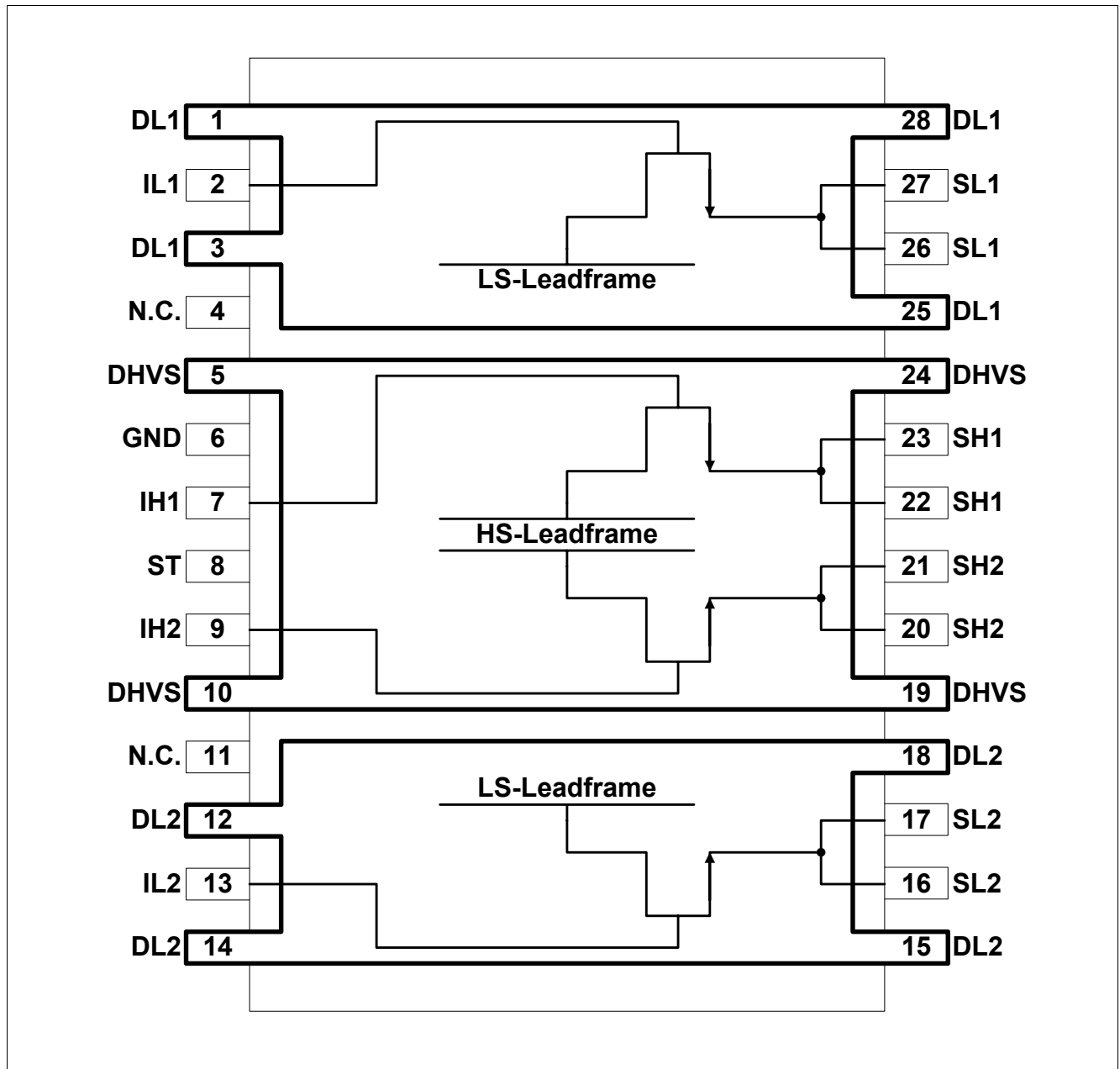


Figure 1 Pin Assignment BTM7751G (Top View)

**Table 1 Pin Definitions and Functions**

Pin No.	Symbol	Function
<b>1, 3, 25, 28</b>	<b>DL1</b>	<b>Drain of low-side switch1, lead frame 1 <sup>1)</sup></b>
2	IL1	Analog input of low-side switch1
4	N.C.	not connected
<b>5, 10, 19, 24</b>	<b>DHVS</b>	<b>Drain of high-side switches and power supply voltage, lead frame 2 <sup>1)</sup></b>
6	GND	Ground
7	IH1	Digital input of high-side switch1
8	ST	Status of high-side switches; open Drain output
9	IH2	Digital input of high-side switch2
11	N.C.	not connected
<b>12, 14, 15, 18</b>	<b>DL2</b>	<b>Drain of low-side switch2, lead frame 3 <sup>1)</sup></b>
13	IL2	Analog input of low-side switch2
<b>16,17</b>	<b>SL2</b>	<b>Source of low-side switch2</b>
<b>20,21</b>	<b>SH2</b>	<b>Source of high-side switch2</b>
<b>22,23</b>	<b>SH1</b>	<b>Source of high-side switch1</b>
<b>26,27</b>	<b>SL1</b>	<b>Source of low-side switch1</b>

1) To reduce the thermal resistance these pins are direct connected via metal bridges to the lead frame.

Pins written in **bold type** need power wiring.

The schematic diagram illustrates the internal architecture and pin connections of the DRV8835 motor driver. Key components and connections include:

- Power Supply:** A 12V supply ( $V_S = 12V$ ) is connected to pins 5, 10, 19, and 24 (DHVS). It includes a series resistor  $I_S$ , a 470nF capacitor ( $C_S$ ), and a 100μF capacitor ( $C_L$ ).
- Input Pins:**
  - ST (8):** Stop pin, connected to  $I_{STLK}$  and  $I_{ST}$ .
  - IH1 (7) and IH2 (9):** High-side input pins for channel 1 and 2, connected to  $I_{IH1}$  and  $I_{IH2}$ .
  - IL1 (2) and IL2 (13):** Low-side input pins for channel 1 and 2, connected to  $I_{IL1}$  and  $I_{IL2}$ .
  - Ground (6):** Connected to  $GND$ ,  $I_{GND}$ , and  $I_{LKCL}$ .
- Internal Blocks:**
  - Diagnosis and Biasing and Protection:** Central control blocks.
  - Gate Driver:** Four gate drivers (two for high-side, two for low-side) driving the MOSFETs.
  - Protection:** Blocks for fault detection and protection.
- Output Pins:**
  - SH1 (22, 23) and SH2 (20, 21):** High-side output pins, connected to  $I_{SH1}$ ,  $I_{SH2}$ ,  $I_{DLK1}$ , and  $I_{DLK2}$ .
  - SL1 (26, 27) and SL2 (16, 17):** Low-side output pins, connected to  $I_{SL1}$  and  $I_{SL2}$ .
  - DL1 (1, 3, 25, 28) and DL2 (12, 14, 15, 18):** Diode/Low-side output pins, connected to  $I_{DL1}$  and  $I_{DL2}$ .
- Other Signals:**
  - V<sub>ST</sub>, V<sub>STL</sub>, V<sub>STZ</sub>, V<sub>IH1</sub>, V<sub>IH2</sub>, V<sub>IL1</sub>, V<sub>IL th 1</sub>, V<sub>IL2</sub>, V<sub>IL th 2</sub>:** Various voltage signals and thresholds.
  - V<sub>DSH1</sub>, V<sub>DSH2</sub>, -V<sub>FH1</sub>, -V<sub>FH2</sub>:** Drain-source and forward voltage signals for high-side MOSFETs.
  - V<sub>DSL1</sub>, V<sub>DSL2</sub>, -V<sub>FL1</sub>, -V<sub>FL2</sub>:** Drain-source and forward voltage signals for low-side MOSFETs.
  - V<sub>UVON</sub>, V<sub>UVOFF</sub>:** Undervoltage lockout signals.

HS-Source-Current	Named during Short Circuit	Named during Leakage-Cond.
$I_{SH1.2}$	$I_{SCP\ H}$	$I_{DL\ LK}$

### 3 Block Diagram

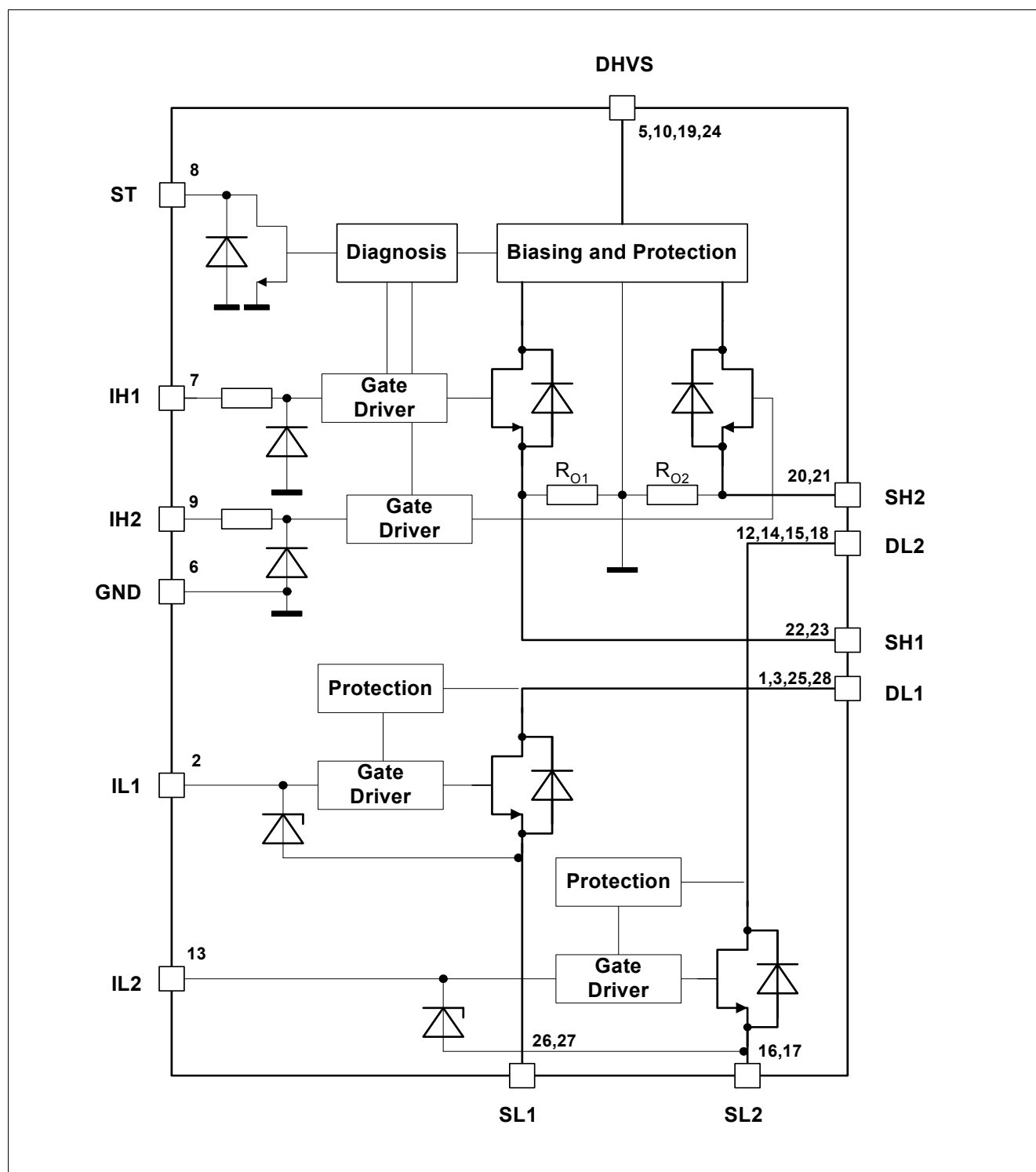


Figure 3 Block Diagram BTM7751G

## 4 Circuit Description

### 4.1 Input Circuit

The control inputs IH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages. The inputs are protected by ESD clamp-diodes. The inputs IL1 and IL2 are connected to the internal gate-driving units of the N-channel vertical power-MOS-FETs.

### 4.2 Output Stages

The output stages consist of an low  $R_{\text{DS(on)}}$  Power-MOS H-bridge. In H-bridge configuration, the D-MOS body diodes can be used for freewheeling when communicating inductive loads. If the high-side switches are used as single switches, positive and negative voltage spikes which occur when driving inductive loads are limited by integrated power clamp diodes.

### 4.3 Short Circuit Protection

The outputs are protected against

- output short circuit to ground
- output short circuit to the supply voltage, and
- overload (load short circuit).

An internal OP-Amp controls the Drain-Source-Voltage by comparing the DS-Voltage-Drop with an internal reference voltage. Above this trip point the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

### 4.4 Overtemperature Protection

The high-side and the low-side switches also incorporate an over temperature protection circuit with hysteresis which switches off the output transistors. In the case of the high-side switches, the status output is set to low.

### 4.5 Undervoltage Lockout

When  $V_S$  reaches the switch-on voltage  $V_{\text{UVON}}$  the IC becomes active with a hysteresis. The High-Side output transistors are switched off if the supply voltage  $V_S$  drops below the switch off value  $V_{\text{UVOFF}}$ .

### 4.6 Open Load Detection

The open load detection of the BTM7751G works in OFF condition and is based on a voltage measurement at the source of the high side switch. In order to use the open load detection SH2 has to be connected to Vcc via a pull up resistor. Because this pull up resistor would connect the bridge output to the  $\mu\text{C}$  supply it needs to be disconnected whenever the high side switch is on. This can be done by a transistor as shown in the application example ([Figure 4 “Application Example BTM7751G” on Page 15](#)). To check for open load:

- Set IH1 = IH2 = LOW (both high side switches off)
- Set IL2 = LOW, IL1 = HIGH (only low side switch 1 is on)
- Connect Rol (open load pull up) to 5V via transistor

If the load is connected properly it will pull down the voltage at SH2 to a value close to 0V.

If the load is disconnected the resistor will pull the voltage at SH2 to value close to Vcc.

If the voltage at SH2 is higher than the open load detection voltage  $V_{\text{OUT(OL)}}$  then ST will be pulled down.

## 4.7 Status Flag

The status flag output is an open drain output with zener-diode which requires a pull-up resistor, as shown in the application circuit in [Figure 4 “Application Example BTM7751G” on Page 15](#). Various errors as listed in the table “Diagnosis” are reported by switching the open drain output ST to low.

**Table 3 Truth table and Diagnosis (valid only for the High-Side-Switches)**

Flag	IH1	IH2	SH1	SH2	ST	Remarks
	Inputs		Outputs			
Normal operation; identical with functional truth table	0	0	L	L	1	stand-by mode
	0	1	L	H	1	switch2 active
	1	0	H	L	1	switch1 active
	1	1	H	H	1	both switches active
Open load at high-side switch 1	0	X	Z	X	0	detected
	1	X	H	X	1	
Open load at high-side switch 2	X	0	X	Z	0	detected
	X	1	X	H	1	
Overtemperature high-side switch1	0	X	L	X	1	
	1	X	L	X	0	detected
Overtemperature high-side switch2	X	0	X	L	1	
	X	1	X	L	0	detected
Overtemperature both high-side switches	0	0	L	L	1	
	X	1	L	L	0	detected
	1	X	L	L	0	detected
Under voltage	X	X	L	L	1	not detected

Inputs:

0 = Logic LOW

1 = Logic HIGH

X = don't care

Outputs:

Z = Output in tristate condition

L = Output in sink condition

H = Output in source condition

X = Voltage level undefined

Status:

1 = No error

0 = Error

## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings<sup>1)</sup>

– 40 °C <  $T_j$  < 150 °C

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
High-Side-Switches (Pins DHVS, IH1,2 and SH1,2)						
5.1.1	Supply voltage	$V_S$	− 0.3	42	V	−
5.1.2	Supply voltage for full short circuit protection	$V_{S(SCP)}$	−	28	V	
5.1.3	HS-drain current <sup>2)</sup>	$I_S$	− 7	<sup>3)</sup>	A	$T_A = 25^{\circ}\text{C}; t_p < 100 \text{ ms}$
5.1.4	HS-input current	$I_{IH}$	− 5	5	mA	Pin IH1 and IH2
5.1.5	HS-input voltage	$V_{IH}$	− 10	16	V	Pin IH1 and IH2
Status Output ST						
5.1.6	Status pull up voltage	$V_{ST}$	− 0.3	5.4	V	
5.1.7	Status Output current	$I_{ST}$	− 5	5	mA	Pin ST
5.1.8	Low-Side-Switches (Pins DL1,2, IL1,2 and SL1,2)					
5.1.9	Drain-Source-Clamp voltage	$V_{DSL}$	42	−	V	$V_{IL} = 0 \text{ V}; I_D \leq 1 \text{ mA}$
5.1.10	Supply voltage for short circuit protection	$V_{DSL(SCP)}$	−	30	V	$V_{IL} = 5 \text{ V}$
5.1.11			−	20	V	$V_{IL} = 10 \text{ V}$
5.1.12	LS-drain current <sup>2)</sup>	$I_{DL}$	− 7	<sup>3)</sup>	A	$T_A = 25^{\circ}\text{C}; t_p < 100 \text{ ms}$
5.1.13	LS-input voltage	$V_{IL}$	− 0.3	10	V	−
Temperatures						
5.1.14	Junction temperature	$T_j$	− 40	150	°C	−
5.1.15	Storage temperature	$T_{stg}$	− 55	150	°C	−
ESD Protection <sup>4)</sup>						
5.1.16	Input LS-Switch	$V_{ESD}$	−	2	kV	
5.1.17	Input HS-Switch	$V_{ESD}$	−	1	kV	
5.1.18	Status HS-Switch	$V_{ESD}$	−	2	kV	
5.1.19	Output LS and HS-Switch	$V_{ESD}$	−	8	kV	all other pins connected to Ground

1) Not subject to production test; specified by design

2) Single pulse

3) Internally limited

4) ESD susceptibility HBM according to EIA/JESD22-A114-B (1.5kΩ, 100pF)

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 5.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
5.2.20	Supply voltage	$V_S$	$V_{UVOFF}$	42	V	After $V_S$ rising above $V_{UVON}$
5.2.21	Input voltage HS	$V_{IH}$	- 0.3	15	V	–
5.2.22	Input voltage LS	$V_{IL}$	- 0.3	10	V	–
5.2.23	Status output current	$I_{ST}$	0	2	mA	–
5.2.24	Junction temperature	$T_j$	- 40	150	°C	–

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table*

## 5.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.25	LS-junction to soldering point <sup>1)</sup>	$R_{thJSP}$	–	–	20	K/W	measured to pin 3 or 12
5.3.26	HS-junction to soldering point <sup>1)</sup>	$R_{thJSP}$	–	–	20	K/W	measured to pin 19
5.3.27	Junction to Ambient <sup>1)</sup> $R_{thJA} = T_{j(HS)} / (P_{(HS)} + P_{(LS)})$	$R_{thJA}$	–	36	–	K/W	<sup>2)</sup>

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

## 5.4 Electrical Characteristics

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$ ;  $-40 \text{ °C} < T_j < 150 \text{ °C}$ ;  $8 \text{ V} < V_S < 18 \text{ V}$

unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Current Consumption HS-switch							
5.4.28	Quiescent current	$I_S$	–	5	9	μA	I <sub>H1</sub> = I <sub>H2</sub> = 0 V $T_J$ = 25 °C
			–	–	13	μA	I <sub>H1</sub> = I <sub>H2</sub> = 0 V
5.4.29	Supply current; one HS-switch active	$I_S$	–	2.1	4.3	mA	I <sub>H1</sub> or I <sub>H2</sub> = 5 V $V_S$ = 12 V
5.4.30	Supply current; both HS-switches active	$I_S$	–	4.3	8.6	mA	I <sub>H1</sub> and I <sub>H2</sub> = 5 V $V_S$ = 12 V
5.4.31	Leakage current of high-side switch	$I_{SH\ LK}$	–	–	6	μA	$V_{IH} = V_{SH} = 0\ V$ $V_S = 12\ V$
5.4.32	Leakage current through logic GND in free wheeling condition	$I_{LKCL} = I_{FH} + I_{SH}$	–	–	10	mA	$I_{FH} = 3\ A$ $V_S = 12\ V$
Current Consumption LS-switch							
5.4.33	Input current	$I_{IL}$	–	8	30	μA	$V_{IL} = 5\ V$ ; normal operation
			–	160	300	μA	$V_{IL} = 5\ V$ ; failure mode
5.4.34	Leakage current of low-side switch	$I_{DL\ LK}$	–	2	10	μA	$V_{IL} = 0\ V$ $V_{DSL} = 18\ V$
Under Voltage Lockout HS-switch							
5.4.35	Switch-ON voltage	$V_{UVON}$	–	–	4.8	V	$V_S$ increasing
5.4.36	Switch-OFF voltage	$V_{UVOFF}$	1.8	–	3.5	V	$V_S$ decreasing
5.4.37	Switch ON/OFF hysteresis	$V_{UVHY}$	–	1	–	V	$V_{UVON} - V_{UVOFF}$
Output stages							
5.4.38	Inverse diode of high-side switch; Forward-voltage	$V_{FH}$	–	0.8	1.2	V	$I_{FH} = 3\ A$
5.4.39	Inverse diode of low-side switch; Forward-voltage	$V_{FL}$	–	0.8	1.2	V	$I_{FL} = 3\ A$
5.4.40	Static drain-source on-resistance of high-side switch	$R_{DS\ ON\ H}$	–	70	–	mΩ	$I_{SH} = 1\ A$ ; $V_S = 12\ V$ $T_J = 25\ ^\circ C$
			–	125	180	mΩ	$I_{SH} = 1\ A$ ; $V_S = 12\ V$ $T_J = 150\ ^\circ C$
5.4.41	Static drain-source on-resistance of low-side switch	$R_{DS\ ON\ L}$	–	45	–	mΩ	$I_{SL} = 1\ A$ ; $V_{IL} = 5\ V$ $T_J = 25\ ^\circ C$
			–	75	105	mΩ	$I_{SL} = 1\ A$ ; $V_{IL} = 5\ V$ $T_J = 150\ ^\circ C$

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ;  $8 \text{ V} < V_s < 18 \text{ V}$   
unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Short Circuit of high-side switch to GND							
5.4.42	Initial peak SC current $t_{\text{del}} = 100 \mu\text{s}$ ; $V_{\text{S}} = 12 \text{ V}$ ; $V_{\text{DSH}} = 12\text{V}$	$I_{\text{SCP H}}$	15	19	23	A	$T_{\text{j}} = -40 \text{ }^{\circ}\text{C}$
			–	14	–	A	$T_{\text{j}} = +25 \text{ }^{\circ}\text{C}$
			8	10	13	A	$T_{\text{j}} = +150 \text{ }^{\circ}\text{C}$
Short Circuit of high-side switch to $V_{\text{s}}$							
5.4.43	Output pull-down-resistor	$R_{\text{O}}$	8	15	35	k $\Omega$	$V_{\text{DSL}} = 3 \text{ V}$
Short Circuit of low-side switch to $V_{\text{s}}$							
5.4.44	Initial peak SC current $V_{\text{DSL}} = 12\text{V}$ ; $V_{\text{IL}} = 5\text{V}$ ; $t_{\text{del}} = 250 \mu\text{s}$	$I_{\text{SCP L}}$	23	28	34	A	$T_{\text{j}} = -40 \text{ }^{\circ}\text{C}$
			–	22	–	A	$T_{\text{j}} = 25 \text{ }^{\circ}\text{C}$
			11.5	14	18	A	$T_{\text{j}} = 150 \text{ }^{\circ}\text{C}$
Thermal Shutdown <sup>1)</sup>							
5.4.45	Thermal shutdown junction temperature	$T_{\text{jSD}}$	155	180	190	$^{\circ}\text{C}$	–
5.4.46	Thermal switch-on junction temperature	$T_{\text{jSO}}$	150	170	180	$^{\circ}\text{C}$	–
5.4.47	Temperature hysteresis	$\Delta T$	–	10	–	$^{\circ}\text{C}$	$\Delta T = T_{\text{jSD}} - T_{\text{jSO}}$
Status Flag Output ST of high-side switch							
5.4.48	Low output voltage	$V_{\text{ST L}}$	–	0.2	0.6	V	$I_{\text{ST}} = 1.6 \text{ mA}$
5.4.49	Leakage current	$I_{\text{ST LK}}$	–	–	10	$\mu\text{A}$	$V_{\text{ST}} = 5 \text{ V}$
5.4.50	Zener-limit-voltage	$V_{\text{ST Z}}$	5.4	–	–	V	$I_{\text{ST}} = 1.6 \text{ mA}$
Open load detection in Off condition							
5.4.51	Open load detection voltage	$V_{\text{OUT(OL)}}$	1.8	2.8	4	V	
5.4.52	Status change after neg. input slope with OL	$t_{\text{d(OL)}}$	–	–	500	$\mu\text{s}$	$V_{\text{s}} = 12 \text{ V}$

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0 \text{ A}$ ;  $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ ;  $8 \text{ V} < V_S < 18 \text{ V}$   
unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		

#### Switching times of high-side switch<sup>1)</sup>

5.4.53	Turn-ON-time to 90% $V_{SH}$	$t_{ON}$	–	85	180	$\mu\text{s}$	$R_{Load} = 12 \Omega$ $V_S = 12 \text{ V}$
5.4.54	Turn-OFF-time to 10% $V_{SH}$	$t_{OFF}$	–	80	180	$\mu\text{s}$	
5.4.55	Slew rate on 10 to 30% $V_{SH}$	$dV/dt_{ON}$	–	–	1.2	$\text{V}/\mu\text{s}$	
5.4.56	Slew rate off 70 to 40% $V_{SH}$	$-dV/dt_{OFF}$	–	–	1.6	$\text{V}/\mu\text{s}$	

#### Switching times of low-side switch<sup>1)</sup>

5.4.57	Turn-ON-time to 10% $V_{DL}$	$t_{ON}$	–	60	150	$\mu\text{s}$	$R_{Load} = 10 \Omega$ $V_S = 12 \text{ V}$ $V_{IL} = 0 \text{ to } 5 \text{ V}$
5.4.58	Turn-OFF-time to 90% $V_{DL}$	$t_{OFF}$	–	60	150	$\mu\text{s}$	
5.4.59	Slew rate on 70 to 50% $V_{DL}$	$-dV/dt_{ON}$	–	1	1.5	$\text{V}/\mu\text{s}$	$R_{Load} = 4.7 \Omega$ $V_S = 12 \text{ V}$ $V_{IL} = 0 \text{ to } 5 \text{ V}$
5.4.60	Slew rate off 50 to 70% $V_{DL}$	$dV/dt_{OFF}$	–	1	1.5	$\text{V}/\mu\text{s}$	

#### Control Inputs of high-side switches IH 1, 2

5.4.61	H-input voltage	$V_{IH \text{ High}}$	–	–	2.5	$\text{V}$	–
5.4.62	L-input voltage	$V_{IH \text{ Low}}$	1	–	–	$\text{V}$	–
5.4.63	Input voltage hysteresis	$V_{IH \text{ HY}}$	–	0.3	–	$\text{V}$	–
5.4.64	H-input current	$I_{IH \text{ High}}$	15	30	60	$\mu\text{A}$	$V_{IH} = 5 \text{ V}$
5.4.65	L-input current	$I_{IH \text{ Low}}$	5	–	20	$\mu\text{A}$	$V_{IH} = 0.4 \text{ V}$
5.4.66	Input series resistance	$R_I$	2.7	4	5.5	$\text{k}\Omega$	–
5.4.67	Zener limit voltage	$V_{IH \text{ Z}}$	5.4	–	–	$\text{V}$	$I_{IH} = 1.6 \text{ mA}$

#### Control Inputs IL1, 2

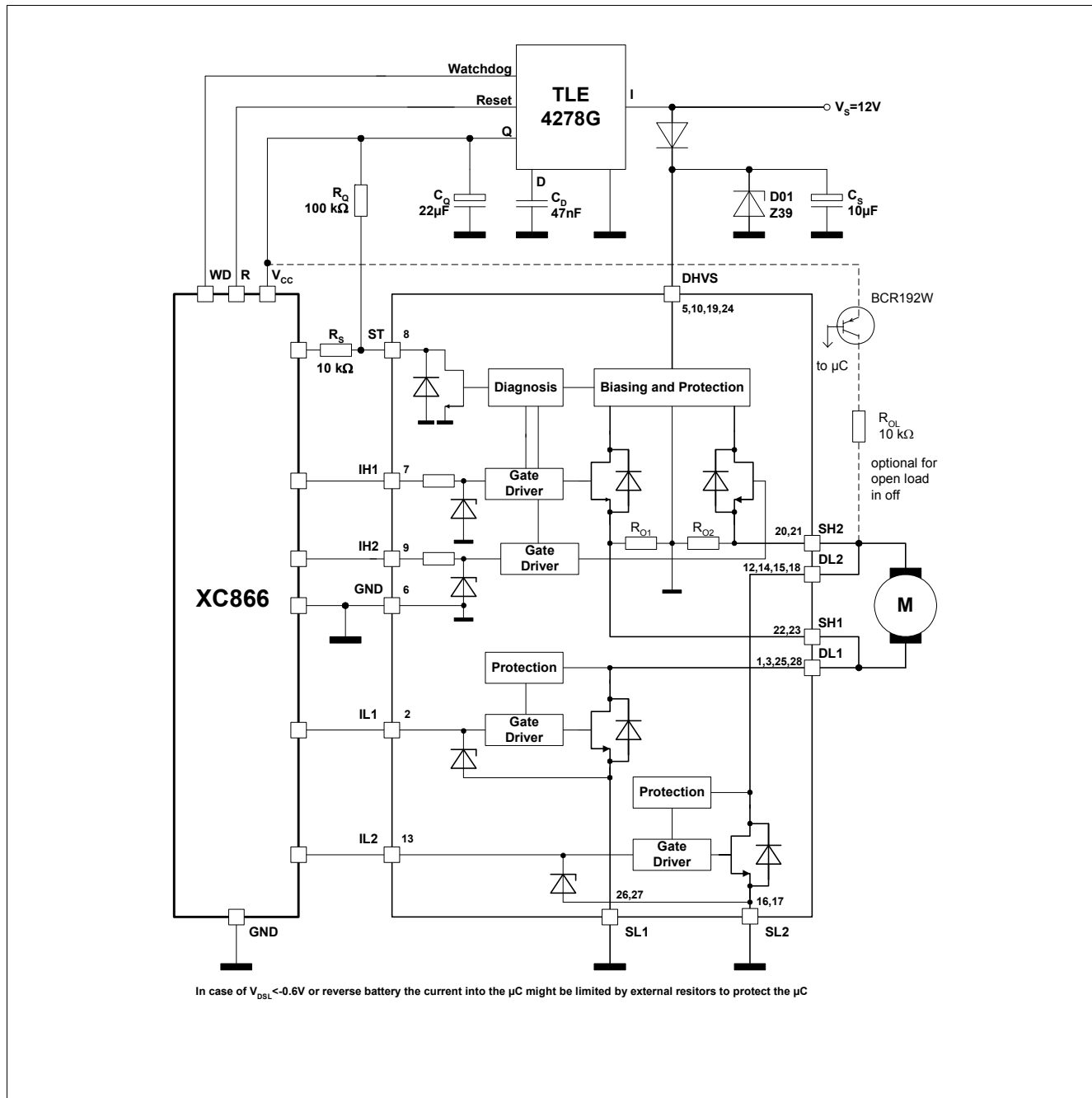
5.4.68	Gate-threshold-voltage	$V_{IL \text{ th}}$	0.9	1.7	2.2	$\text{V}$	$I_{DL} = 2 \text{ mA}$
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1) Not subject to production test; specified by design

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specified mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25^\circ\text{C}$  and the given supply voltage.*

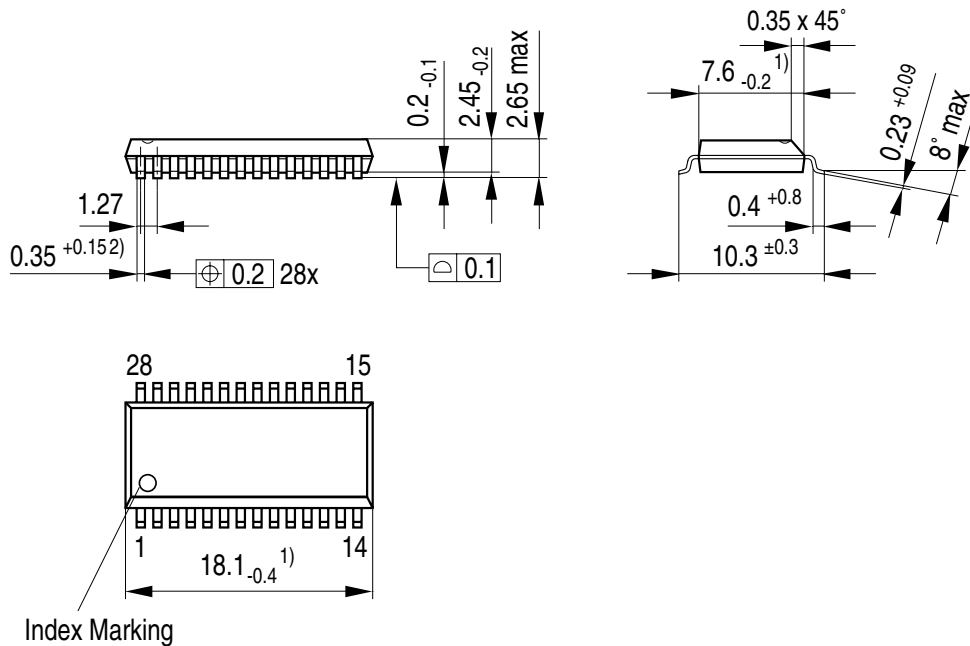
## 6 Application Information

*Note: The following simplified application examples are given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application*



**Figure 4 Application Example BTM7751G**

## 7 Package Outlines



- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

GPS05123

**Figure 5 PG-DSO-28-22 (Plastic Transistor Single Outline Package)**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:

<http://www.infineon.com/packages>.

Dimensions in mm

## 8 Revision History

Rev.	Date	Changes
1.0	2008-06-27	Initial Version

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