

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT428 (DPAK) surface mountable plastic package intended for use in applications requiring high bidirectional blocking voltage capability, high surge current capability and high thermal cycling performance.

2. Features and benefits

- Good bidirectional blocking voltage capability
- High surge current capability
- High thermal cycling performance
- Sensitive gate
- Surface mountable package

3. Applications

- Ignition circuits
- Motor control
- Protection circuits
- Voltage regulation

4. Quick reference data

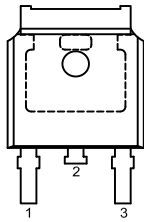
Table 1. Quick reference data

[illegible]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 335\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; $R_{GK} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 13		200	1000	-	V/ μs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 DPAK (SOT428)	 <i>sym037</i>
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT151S-500L	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	500	V
V_{RRM}	repetitive peak reverse voltage		-	500	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 103\text{ }^{\circ}\text{C}$; Fig. 1	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 103\text{ }^{\circ}\text{C}$; Fig. 2 ; Fig. 3	-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	120	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	-	132	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	72	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 10\text{ mA}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$

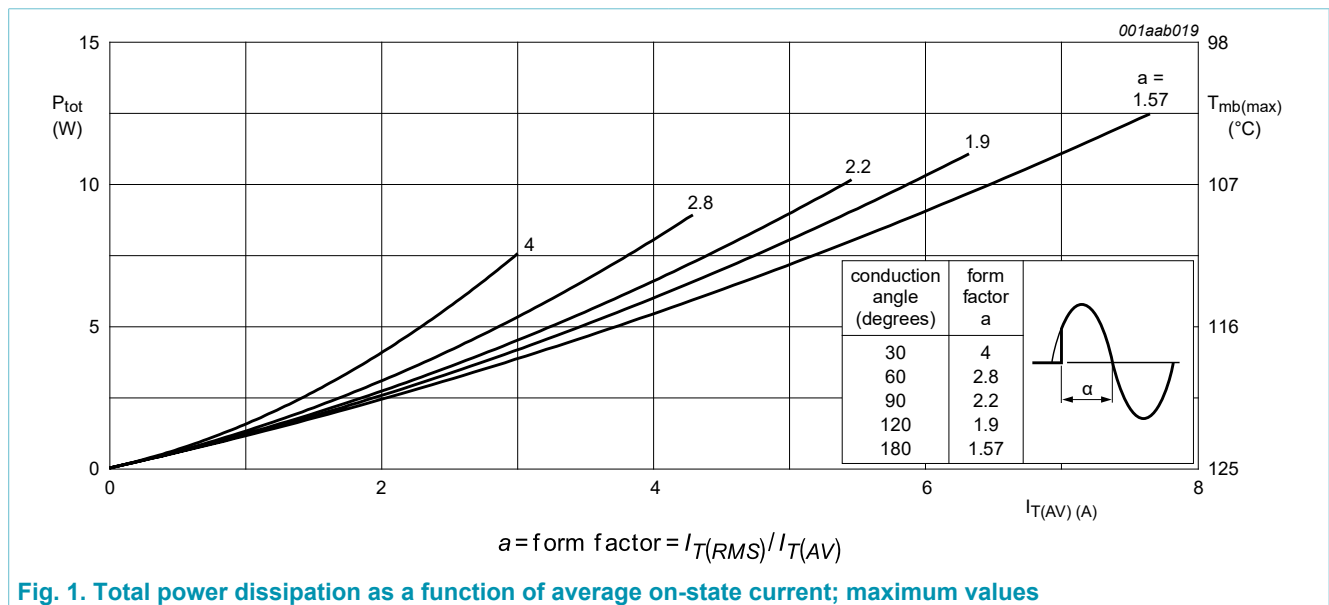


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

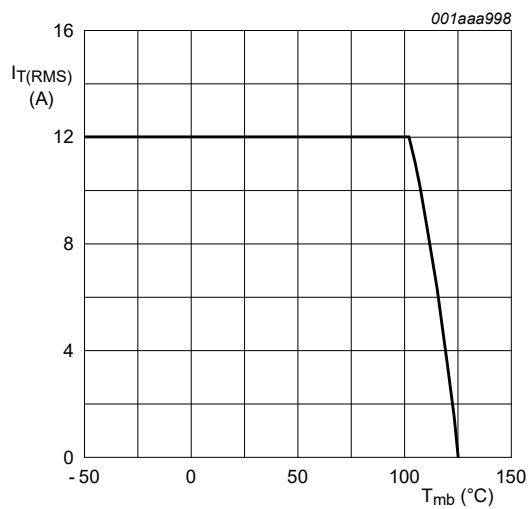
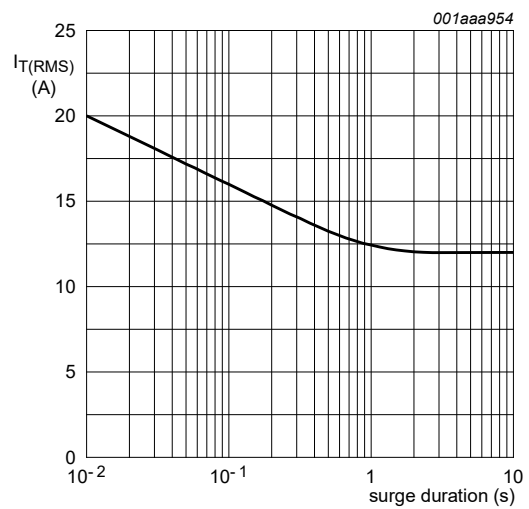
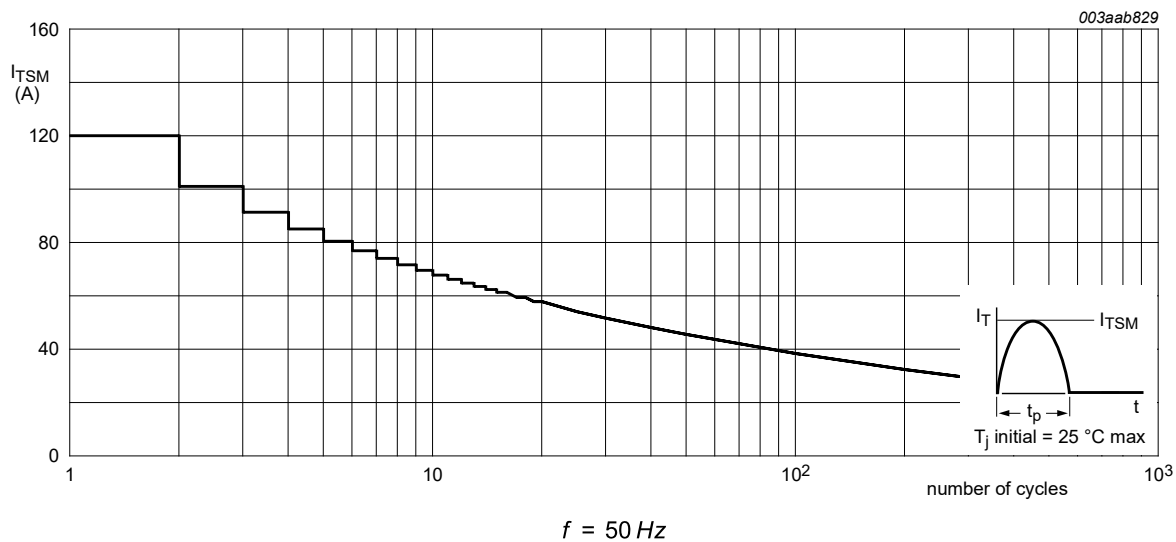


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



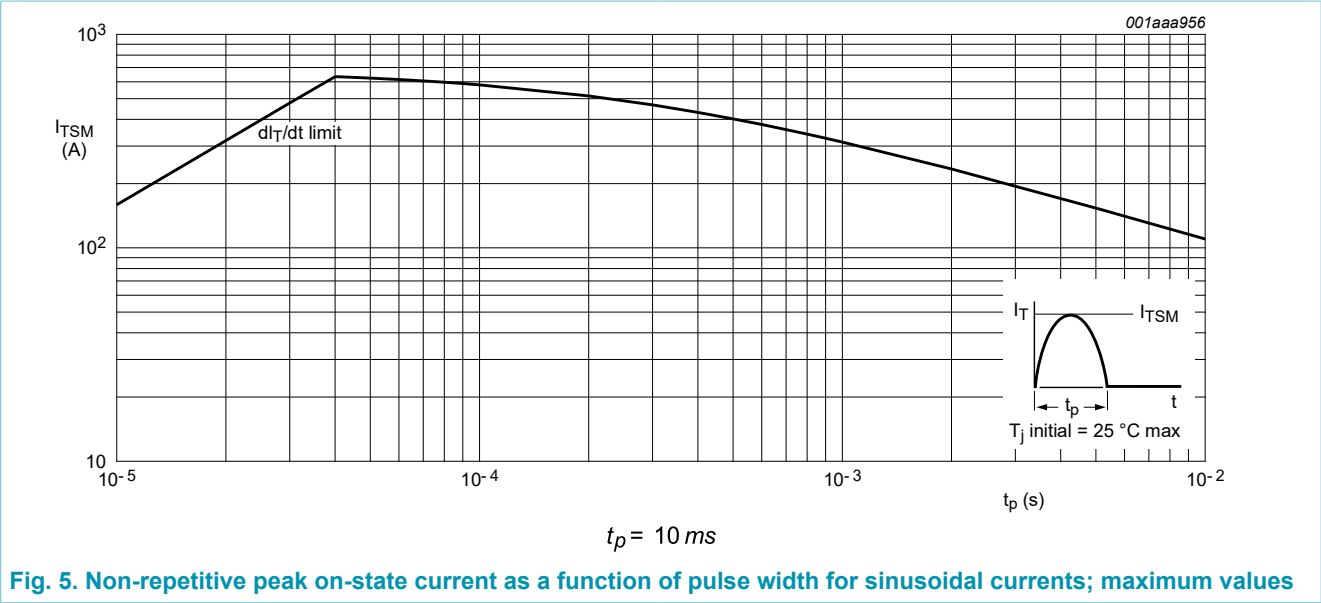
$f = 50 \text{ Hz}$; $T_{mb} = 103 \text{ °C}$

Fig. 3. RMS on-state current as a function of surge duration; maximum values



$f = 50 \text{ Hz}$

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	1.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	mounted on an FR4 printed-circuit board;; Fig. 7		-	75	-	K/W

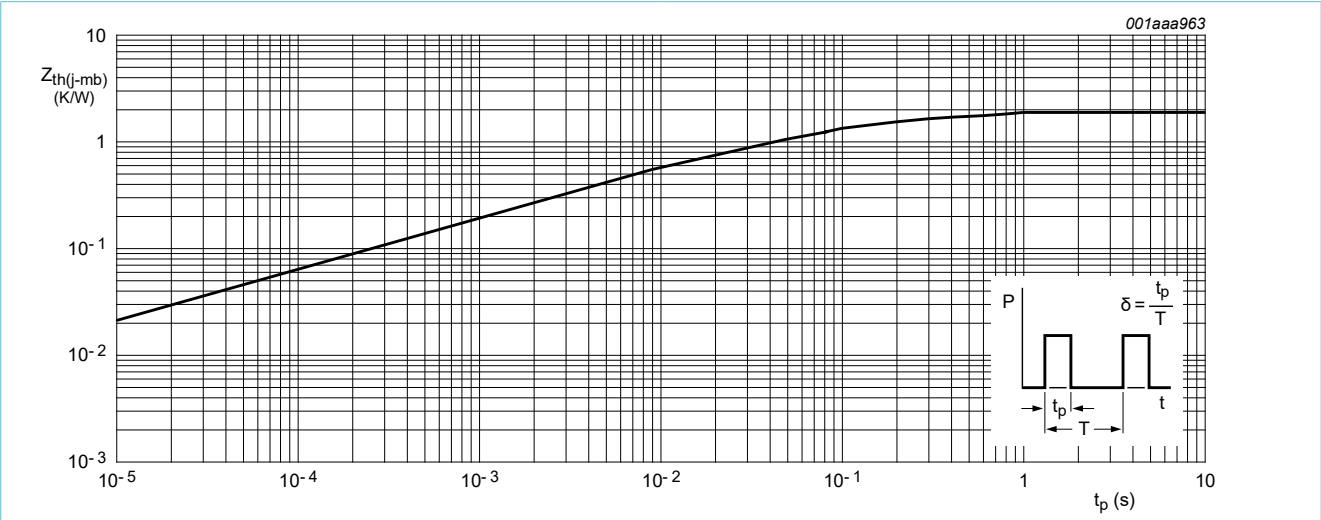


Fig. 6. Transient thermal impedance from junction to mounting base as as function of pulse width

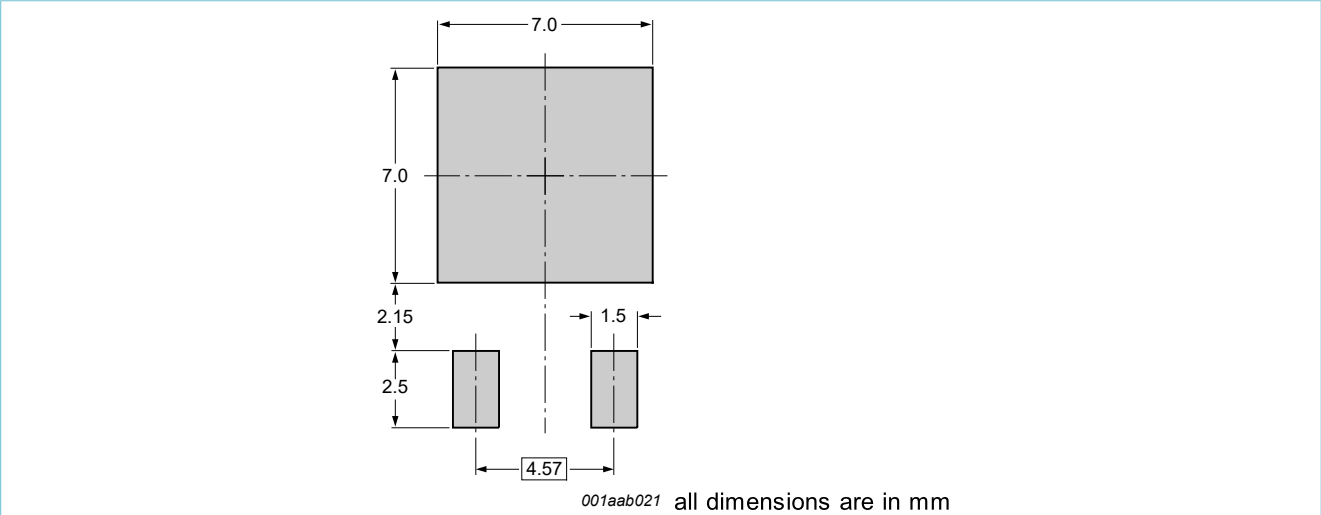


Fig. 7. Minimum footprint SOT428

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	2	5	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	10	40	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	7	20	mA
V_T	on-state voltage	$I_T = 23\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	1.4	1.75	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12	-	0.6	1.5	V
		$V_D = 500\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 12	0.25	0.4	-	V
I_D	off-state current	$V_D = 500\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
I_R	reverse current	$V_R = 500\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 335\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 13	200	1000	-	V/ μs
		$V_{DM} = 335\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 13	50	130	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 40\text{ A}$; $V_D = 500\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu\text{s}$; $T_j = 25\text{ }^\circ\text{C}$	-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 335\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{TM} = 20\text{ A}$; $V_R = 25\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 50\text{ V}/\mu\text{s}$; $R_{GK(EXT)} = 100\text{ }\Omega$; ($V_{DM} = 67\%$ of V_{DRM})	-	70	-	μs

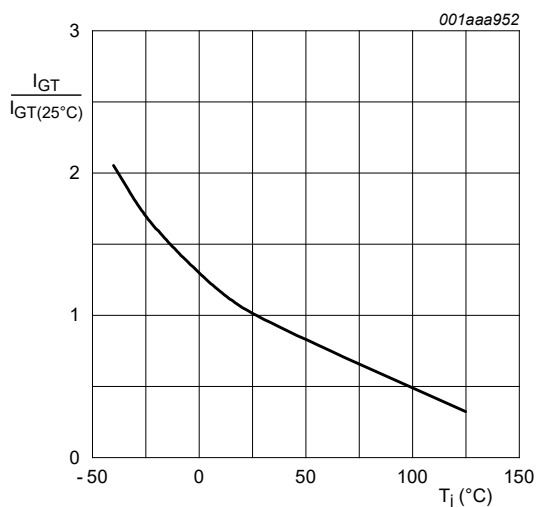


Fig. 8. Normalized gate trigger current as a function of junction temperature

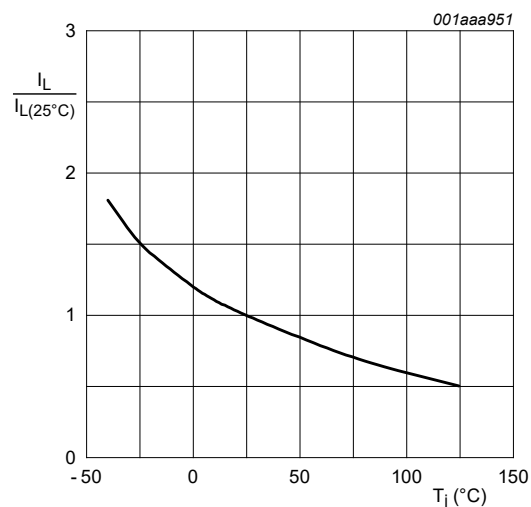


Fig. 9. Normalized latching current as a function of junction temperature

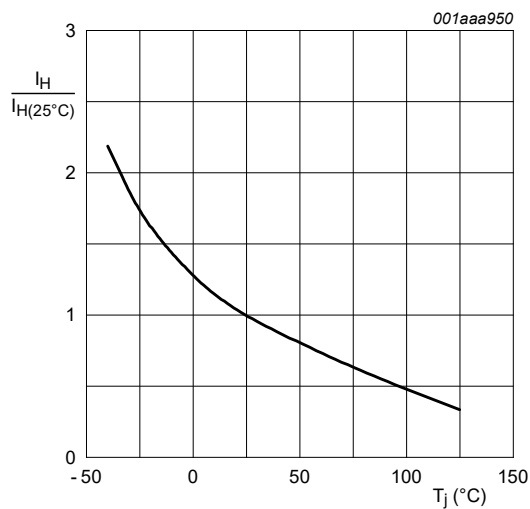
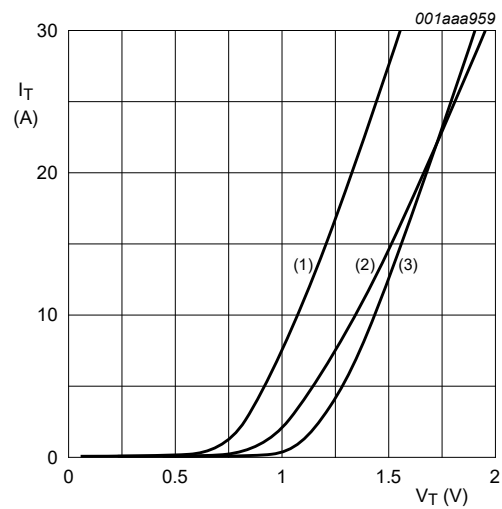


Fig. 10. Normalized holding current as a function of junction temperature



$V_o = 1.06 \text{ V}; R_s = 0.0304 \text{ } \Omega$
(1) $T_j = 125 \text{ } ^{\circ}\text{C}$; typical values
(2) $T_j = 125 \text{ } ^{\circ}\text{C}$; maximum values
(3) $T_j = 25 \text{ } ^{\circ}\text{C}$; maximum values

Fig. 11. On-state current as a function of on-state voltage

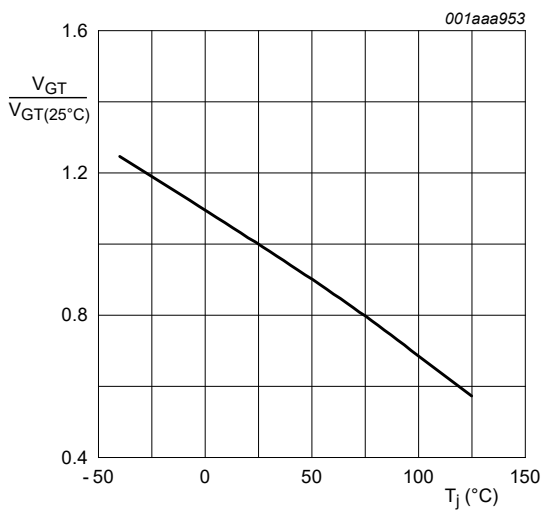
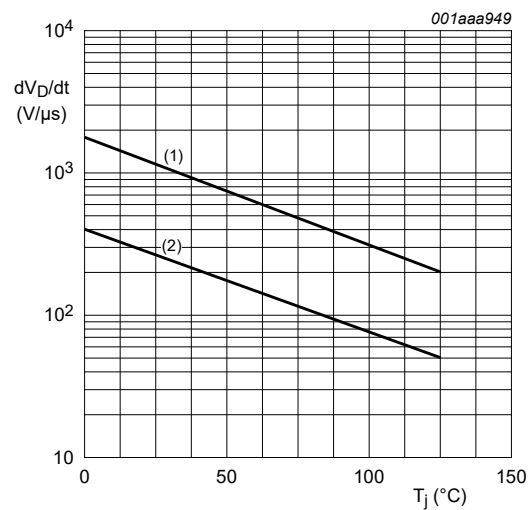


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



(1) $R_{GK} = 100 \text{ } \Omega$;
(2) gate open circuit

Fig. 13. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

10. Package outline

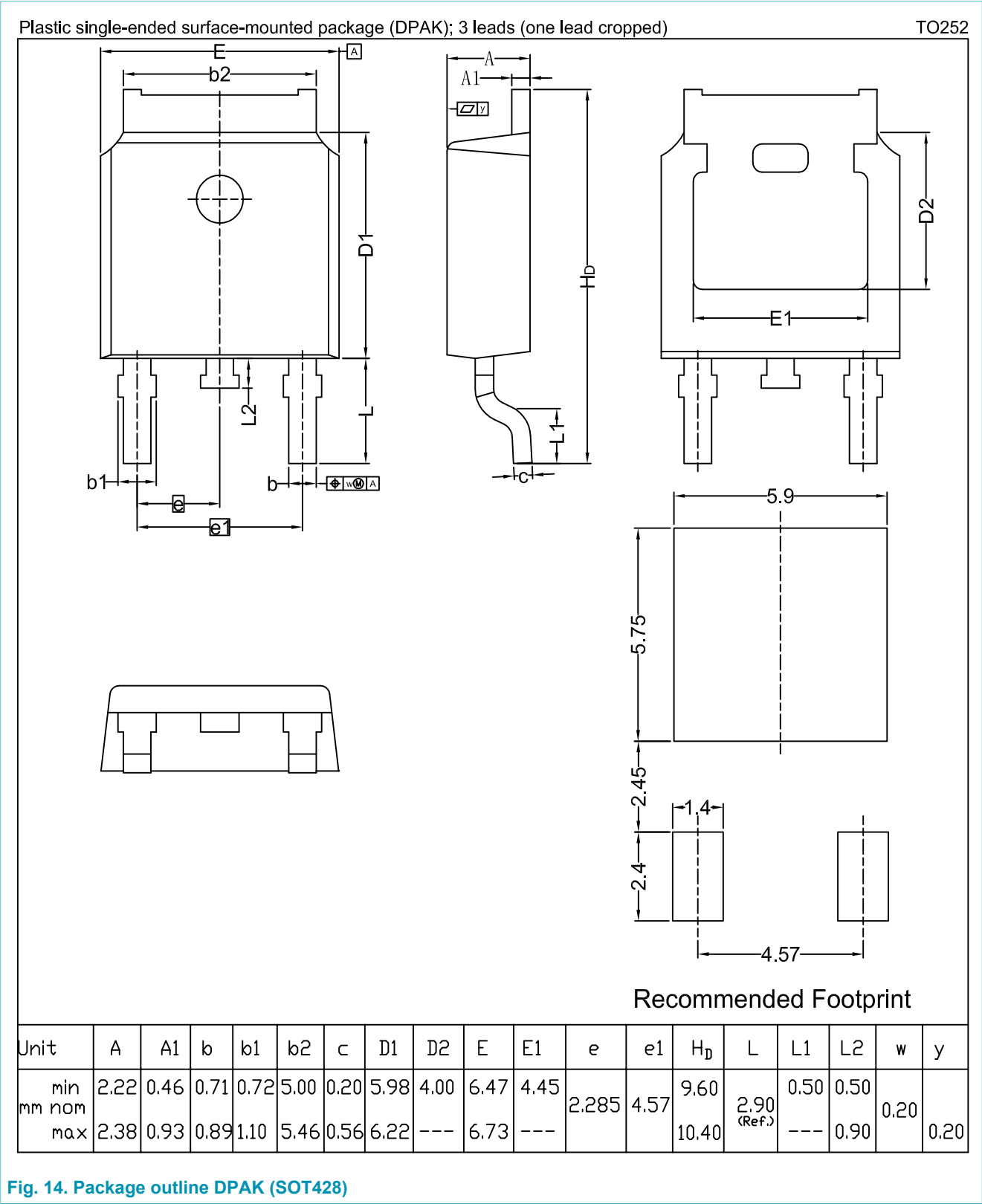


Fig. 14. Package outline DPAK (SOT428)

11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 11 June 2018