Never stop thinking

n-Channel Power MOSFET

OptiMOS™
BSZ018NE2LS

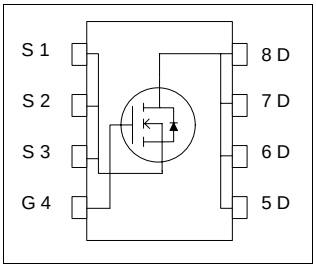
Data Sheet

2.0, 2011-03-29
Final

Industrial & Multimarket

1 Description

OptiMOS™25V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 25V the best choice for the demanding requirements of voltage regulator solutions in Servers, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space, efficiency and cost. OptiMOS™ products are designed to meet and exceed the energy efficiency and power density requirements of the sharpened next generation voltage regulation standards in computing applications.



Features

- Optimized for high performance buck converters
- 100% avalanche tested
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- Very low FOM_{QOSS} for High Frequency SMPS
- Low FOM_{SW} for High Frequency SMPS
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Qualified according to JEDEC[1)] for target applications
- Superior thermal resistance
- N-channel
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Applications

- On board power for server
- Power managment for high performance computing
- Synchronous rectification
- High power density point of load converters

Table 1 Key Performance Parameters

Parameter	Value	Unit		Related Links
V_{DS}	25	V		IFX OptiMOS webpage
$R_{DS(on),max}$	1.8	mΩ		IFX OptiMOS product brief
I_D	40	A		IFX OptiMOS spice models
Q_{OSS}	21	nC		IFX Design tools
$Q_{g\cdot typ}$	39			

Type	Package	Marking
BSZ018NE2LS	PG-TSDSON-8 (fused leads)	018NE2L

1) J-STD20 and JESD22

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	40	A	V_{GS}=10 V, T_C=25 °C
		-	-	40		V_{GS}=10 V, T_C=100 °C
		-	-	40		V_{GS}=4.5 V, T_C=25 °C
		-	-	40		V_{GS}=4.5 V, T_C=100 °C
		-	-	23		V_{GS}=4.5 V, T_A=25 °C, R_{thJA}=60 K/W
Pulsed drain current[1]	$I_{D,pulse}$	-	-	160		T_C=25 °C
Avalanche current, single pulse[2]	I_{AS}	-	-	20		
Avalanche energy, single pulse	E_{AS}	-	-	150	mJ	I_D=20 A,R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P_{tot}	-	-	69	W	T_C=25 °C
		-	-	2.1		T_A=25 °C, R_{thJA}=60 K/W
Operating and storage temperature	T_j,T_{stg}	-55	-	150	°C	
IEC climatic category; DIN IEC 68-1		55/150/56				

1) See figure 3 for more detailed information

2) See figure 13 for more detailed information

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.8	K/W	
Device on PCB	R_{thJA}	-	-	60		6 cm^2 cooling area[1]

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air

4 Electrical characteristics

Electrical characteristics, at Tj=25 °C, unless otherwise specified.

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	V_{GS}=0 V, I_D=1.0 mA
Gate threshold voltage	$V_{GS(th)}$	1	-	2.2		V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C
		-	10	100		V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.9	2.4	mΩ	V_{GS}=4.5 V, I_D=30 A
		-	1.5	1.8		V_{GS}=10 V, I_D=30 A
Gate resistance	R_G	-	0.8	-	Ω	
Transconductance	g_{fs}	70	140	-	S	$\|V_{DS}\|>2\|I_D\|_{RDS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2800	-	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Output capacitance	C_{oss}	-	1000	-		
Reverse transfer capacitance	C_{rss}	-	110	-		
Turn-on delay time	$t_{d(on)}$	-	5.5	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, R_G= 1.6 Ω
Rise time	t_r	-	4.4	-		
Turn-off delay time	$t_{d(off)}$	-	26	-		
Fall time	t_f	-	3.4	-		

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7	-	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	4.5	-		
Gate to drain charge	Q_{gd}	-	4.3	-		
Switching charge	Q_{sw}	-	6.7	-		
Gate charge total	Q_g	-	18.6	-		
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	
Gate charge total	Q_g	-	39	-	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 10V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	16.2	-		V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge	Q_{oss}	-	21	-		V_{DD}=12V, V_{GS}=0 V

1) See figure 16 for gate charge parameter definition

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	40	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	160		
Diode forward voltage	V_{SD}	-	0.8	1	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	20	-	nC	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs

5 Electrical characteristics diagrams

Table 8

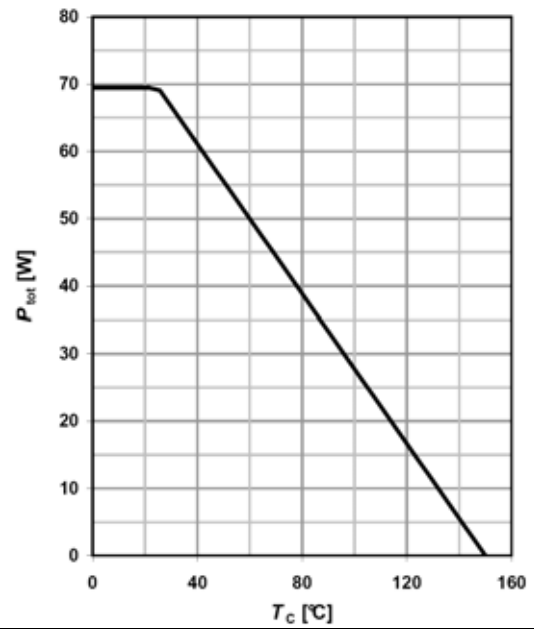
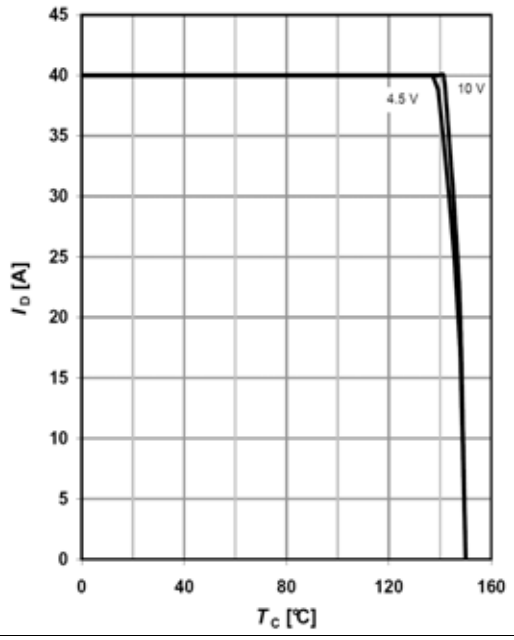
1 Power dissipation	2 Drain current
	
$P_{tot} = f(T_C)$	$I_D=f(T_C)$; parameter:V_{GS}

Table 9

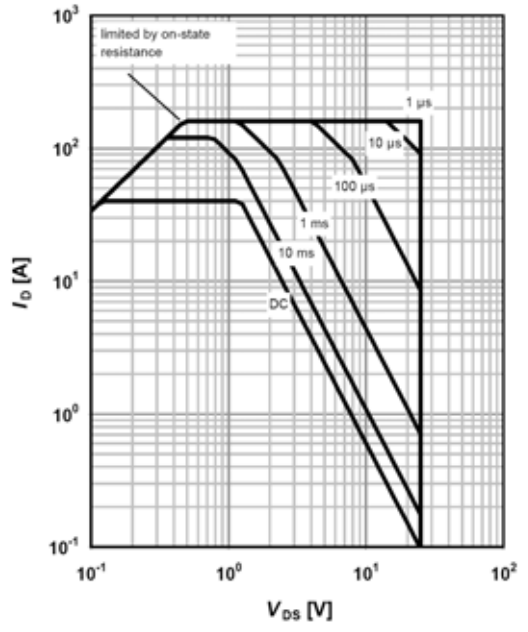
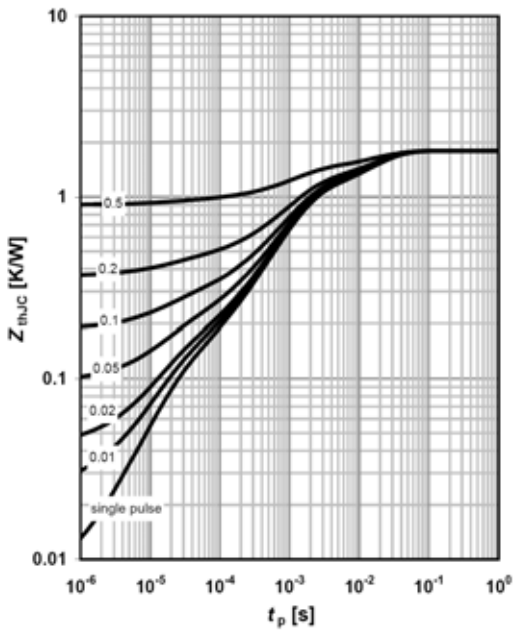
3 Safe operating area T_C=25 °C	4 Max. transient thermal impedance
	
I_D=f(V_{DS}); T_j=25 °C; D=0; parameter: T_p	$Z_{(thJC)}$=f(t_p); parameter: D=t_p/T

Table 10

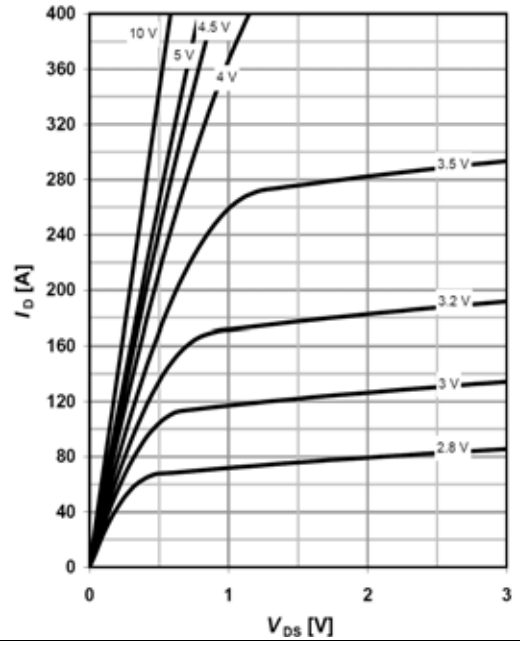
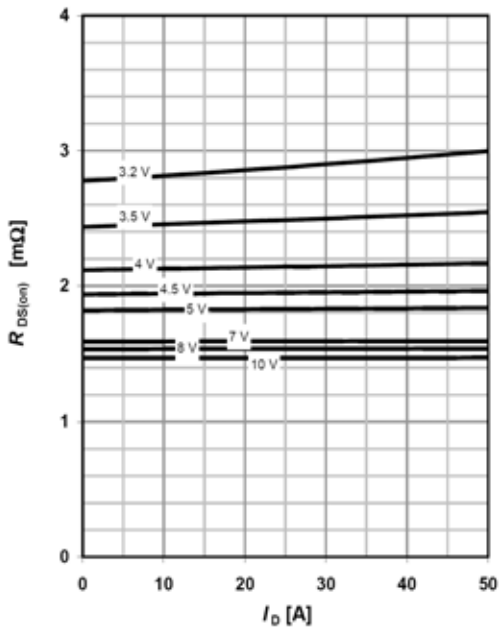
5 Typ. output characteristics T_C=25 °C	6 Typ. drain-source on-state resistance
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Table 11

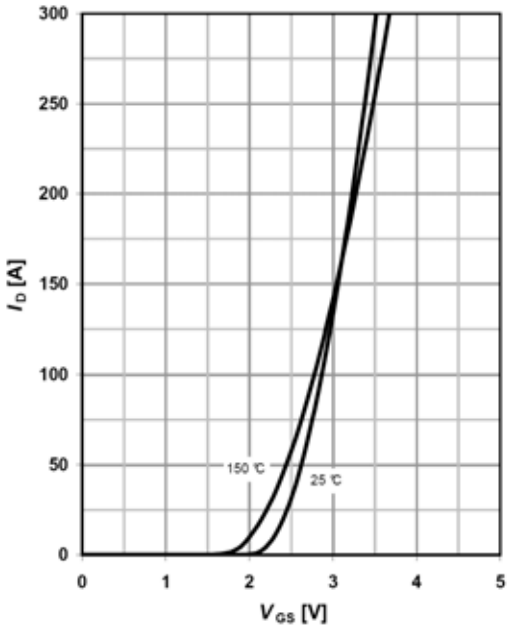
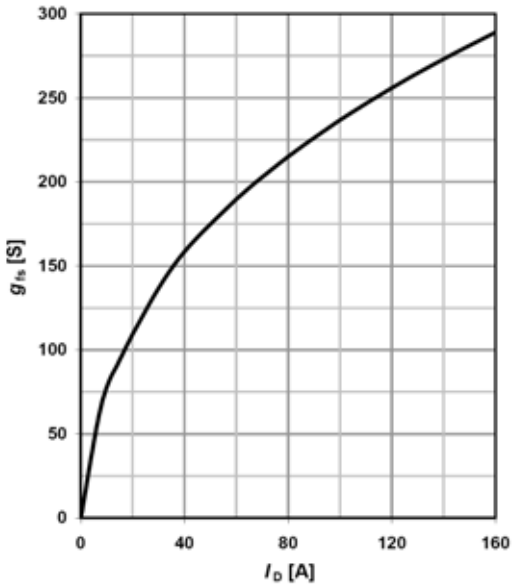
7 Typ. transfer characteristics	8 Typ. forward transconductance
	
I_D=f(VGS); |V_{DS}|>2|I_D|$R_{DS(on)max}$	g_{fs}=f(I_D); T_j=25 °C

Table 12

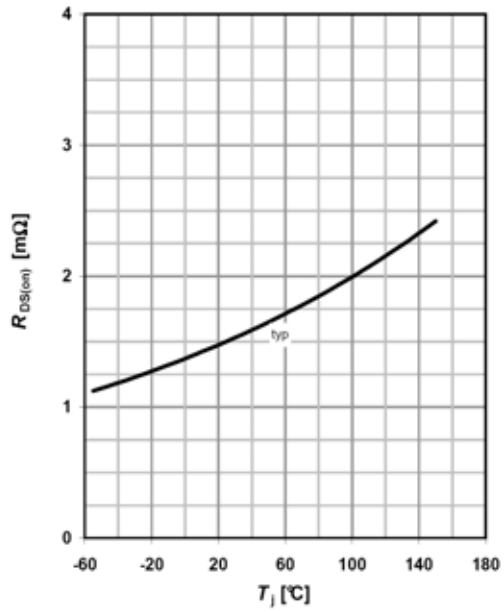
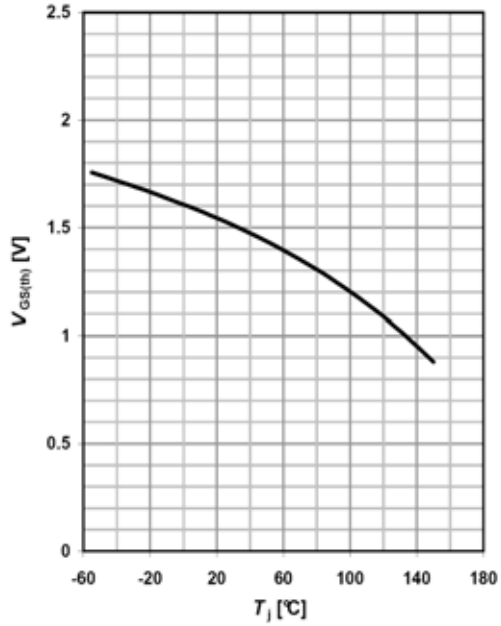
9 Drain-source on-state resistance	10 Typ. gate threshold voltage
	
$R_{DS(on)}=f(T_j)$; I_D=30 A; V_{GS}=10 V	$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; I_D=250 µA

Table 13

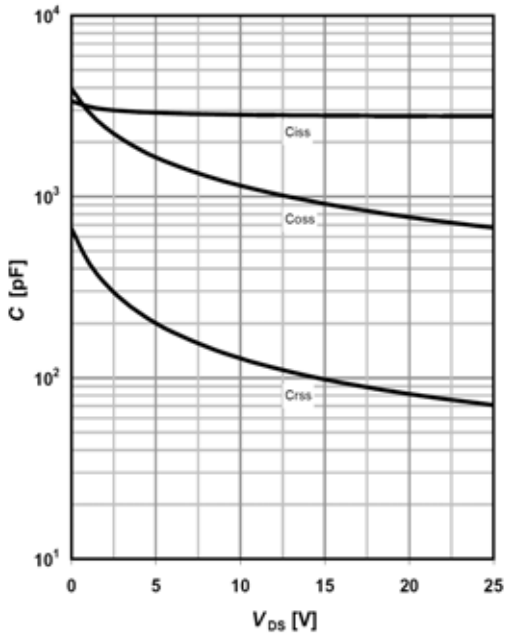
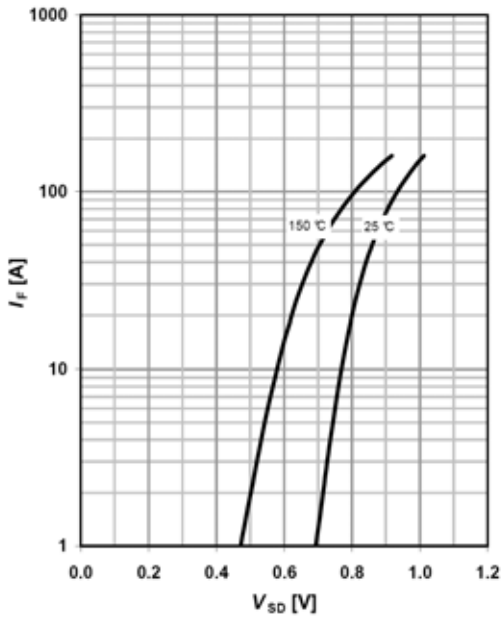
11 Typ. capacitances	12 Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	$I_F=f(V_{SD})$; parameter: T_j

Table 14

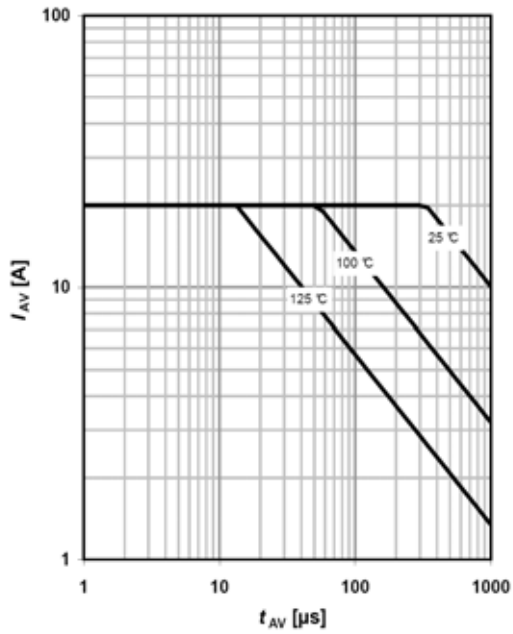
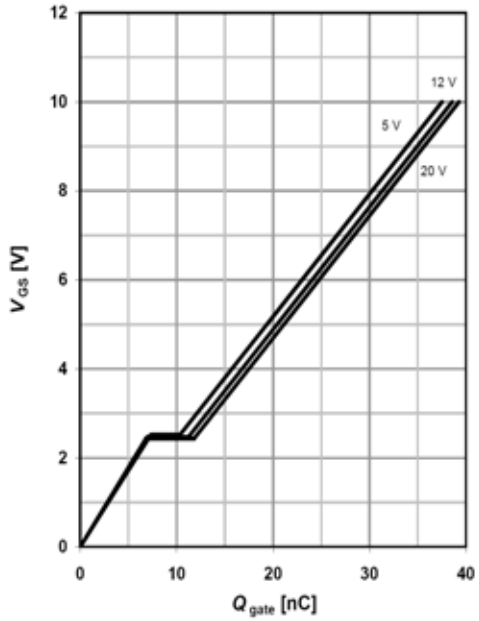
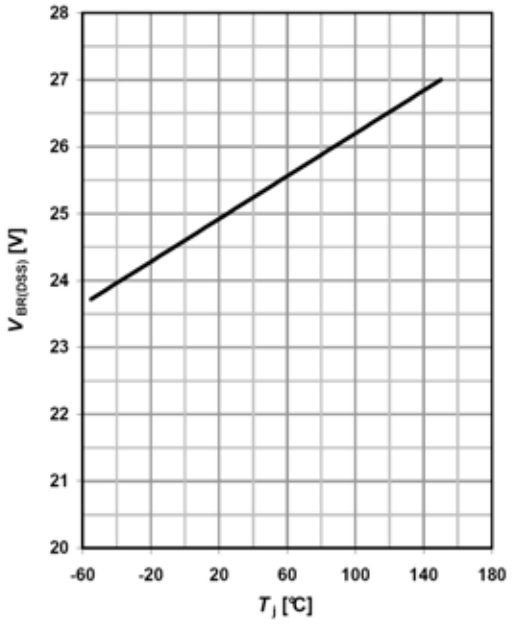
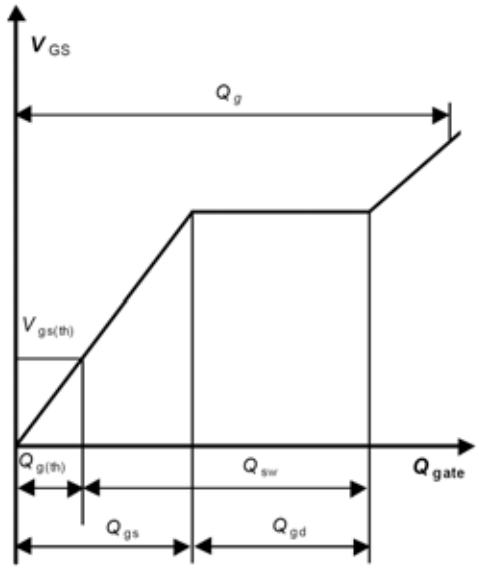
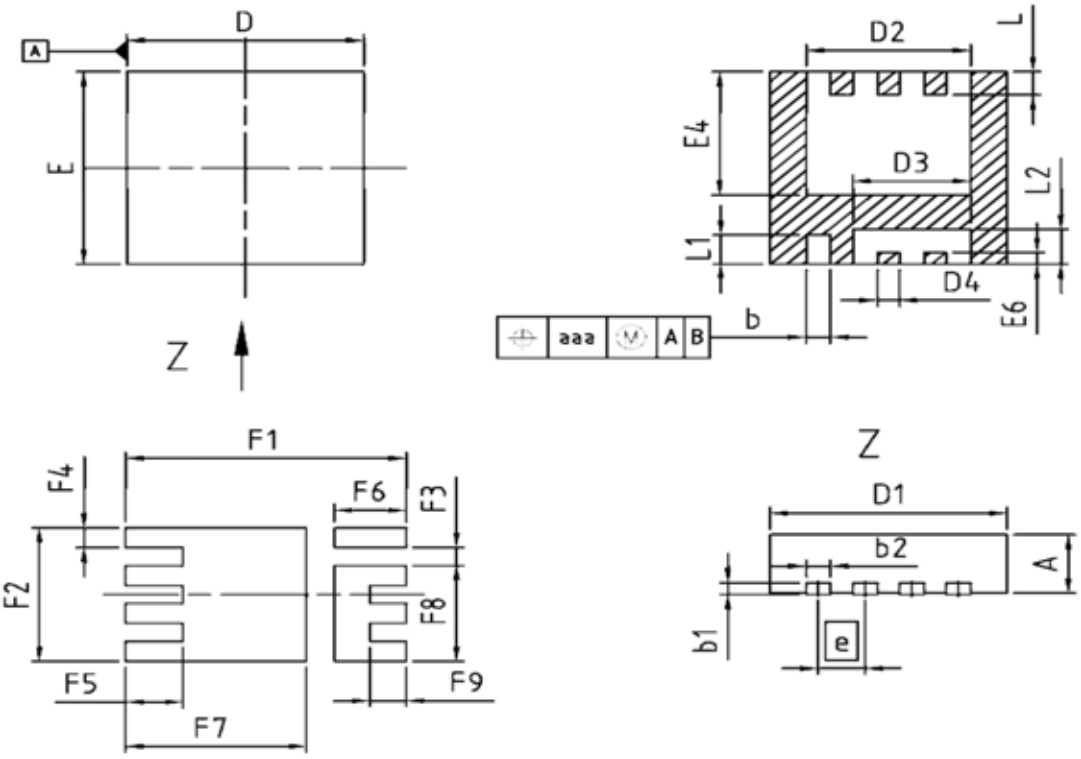
13 Avalanche characteristics	14 Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$	V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Table 15

15 Drain-source breakdown voltage	16 Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	

6 Package outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.24	0.44	0.009	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.19	2.39	0.086	0.094
D3	1.54	1.74	0.061	0.069
D4	0.21	0.41	0.008	0.016
E	3.20	3.40	0.126	0.134
E4	2.01	2.21	0.079	0.087
E6	0.10	0.30	0.004	0.012
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.30	0.51	0.012	0.020
L1	0.40	0.70	0.016	0.028
L2	0.50	0.70	0.020	0.028
aaa	0.25		0.010	
F1	3.90		0.154	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.80		0.031	
F6	1.00		0.039	
F7	2.51		0.099	
F8	1.64		0.065	
F9	0.50		0.020	

DOCUMENT NO.
Z8B00158553

SCALE
0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
27-12-2010

REVISION
02

Figure 1 Outlines PG-TSDSON-8 (fused leads), dimensions in mm/inches

7 Revision History

Revision History: 2011-03-29, 2.0

Previous Revision:

Revision	Subjects (major changes since last revision)
0.1	Release of target data sheet
2.0	Release Final version

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to: **erratum@infineon.com**

Edition 2011-03-29

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.