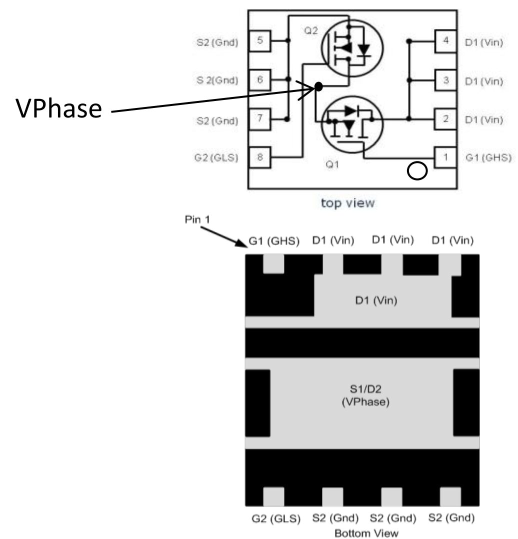
*Opti*MOS™ Power-MOSFET

Features

- Dual N-channel OptiMOS™ MOSFET
- Optimized for clean switching
- 100% avalanche tested
- Superior thermal resistance
- Optimized for high performance Buck converter
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	5	mΩ
I_D	40	A
Q_{OSS}	8.6	nC
Q_G(0V..10V)	13	nC



Type	Package	Marking
BSC0925ND	PG-TISON-8	0925ND

Maximum ratings, at T_j=25 °C, unless otherwise specified[2]

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	40	A
		V_{GS}=4.5 V, T_A=25 °C[3]	15	
		V_{GS}=4.5 V, T_A=70 °C[3]	12	
		V_{GS}=10 V, T_A=25 °C[4]	11	
Pulsed drain current[5]	$I_{D,pulse}$	T_C=25 °C	160	
Avalanche energy, single pulse	E_{AS}	I_D=20 A, R_{GS}=25 Ω	14	mJ
Gate source voltage	V_{GS}		±20	V

[1] J-STD20 and JESD22

[2] One transistor active

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[4] Device mounted on a minimum pad (one layer, 70 µm thick). One transistor active

[5] See figure 3 for more detailed information.

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	30	W
		T_A=25 °C, R_{thJA}=50 K/W[3)]	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

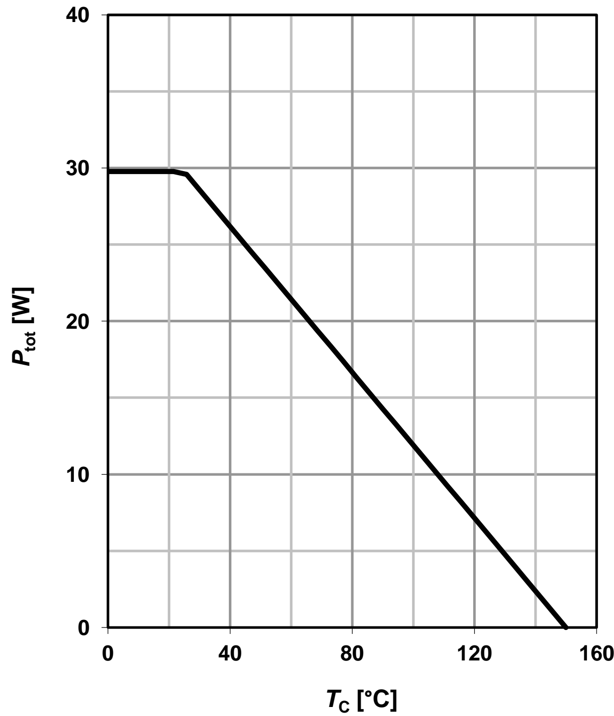
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	4.2	K/W
		top	-	-	20	
Device on PCB	R_{thJA}	6 cm^2 cooling area[3)]	-	-	50	
		minimum footprint[4)]	-	-	125	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1.2	-	2.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=20 A	-	5.6	7	mΩ
		V_{GS}=10 V, I_D=20 A	-	4.2	5	
Gate resistance	R_G		1.3	2.6	5.2	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A	38	77	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	870	1157	pF
Output capacitance	C_{oss}		-	330	439	
Reverse transfer capacitance	C_{rss}		-	49	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω	-	4.7	-	ns
Rise time	t_r		-	3.8	-	
Turn-off delay time	$t_{d(off)}$		-	17	-	
Fall time	t_f		-	3.0	-	
Gate Charge Characteristics[6)]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	2.4	3.2	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.4	-	
Gate to drain charge	Q_{gd}		-	2.2	2.9	
Switching charge	Q_{sw}		-	3.2	-	
Gate charge total	Q_g		-	6.7	8.9	
Gate plateau voltage	$V_{plateau}$		-	2.8	-	V
Gate charge total	Q_g	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V	-	13	17	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	5.4	-	
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	8.6	11	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	30	A
Diode pulse current	$I_{S,pulse}$		-	-	120	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=20 A, T_j=25 °C	-	0.87	1	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	5	-	nC

[6)] See figure 16 for gate charge parameter definition

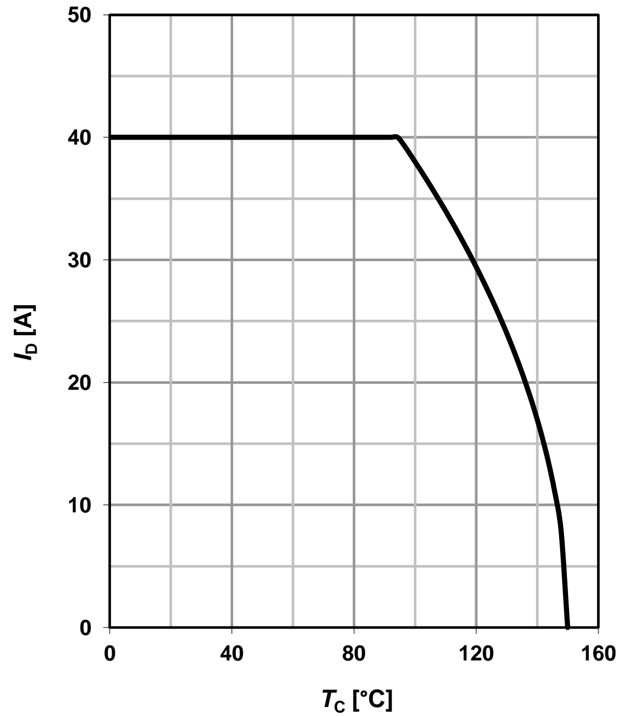
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

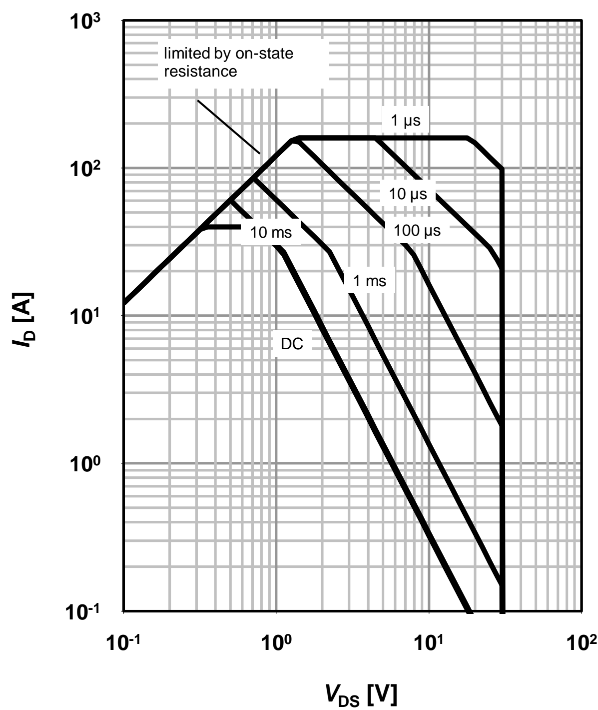
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

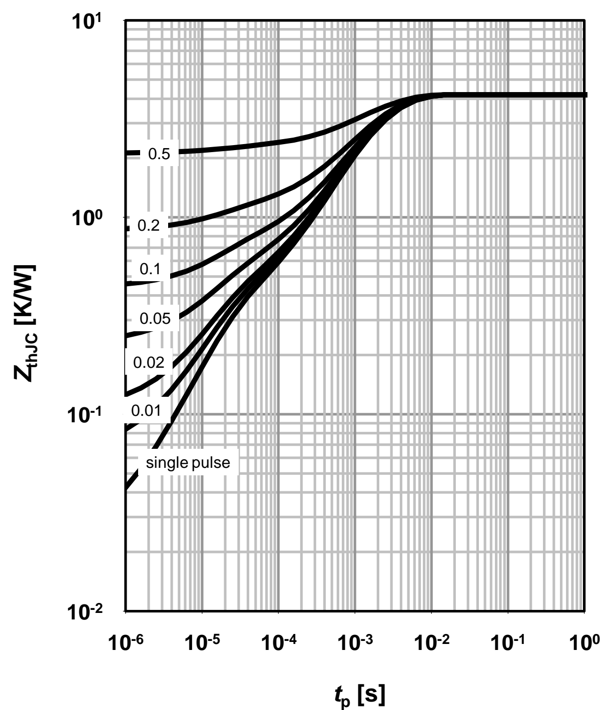
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

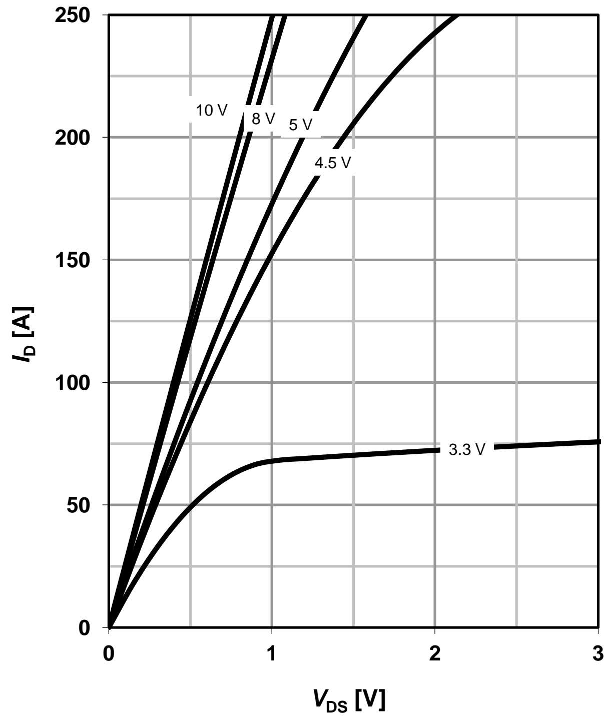
parameter: D=t_p/T



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

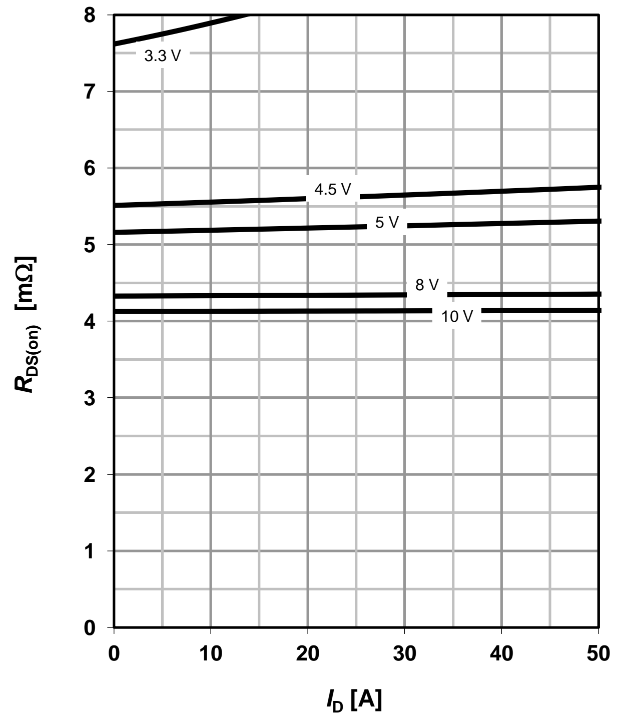
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

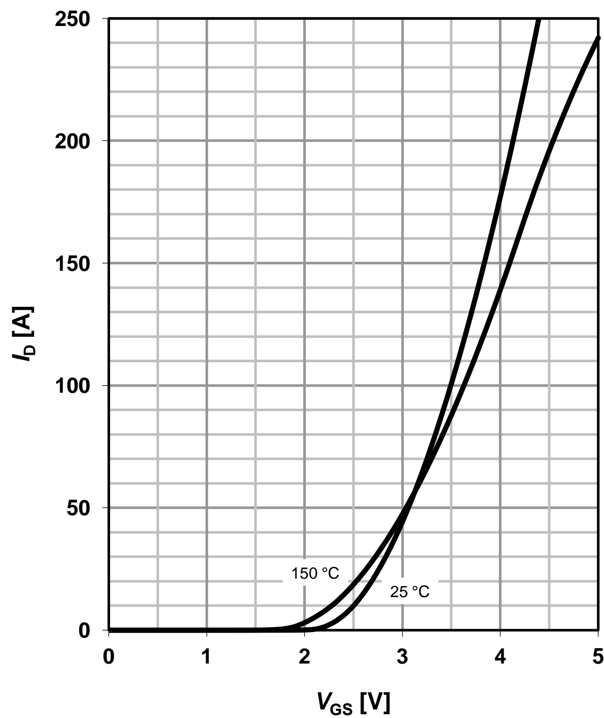
parameter: V_{GS}



7 Typ. transfer characteristics

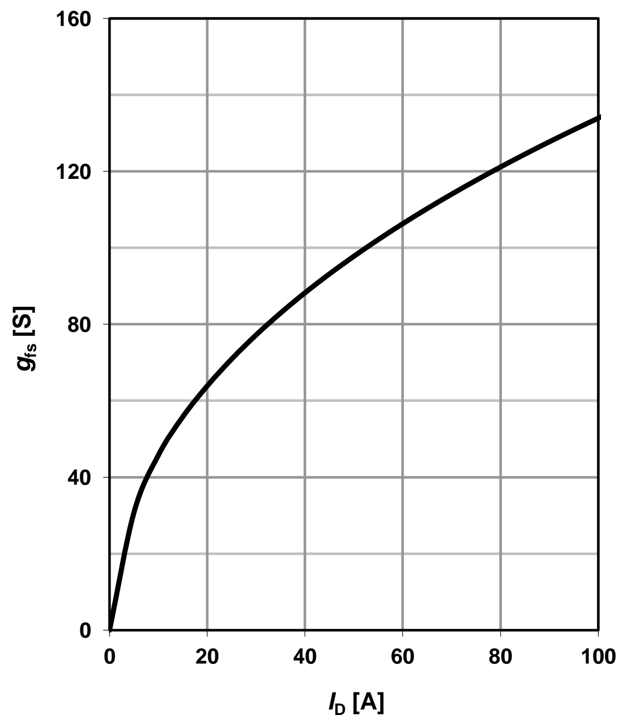
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



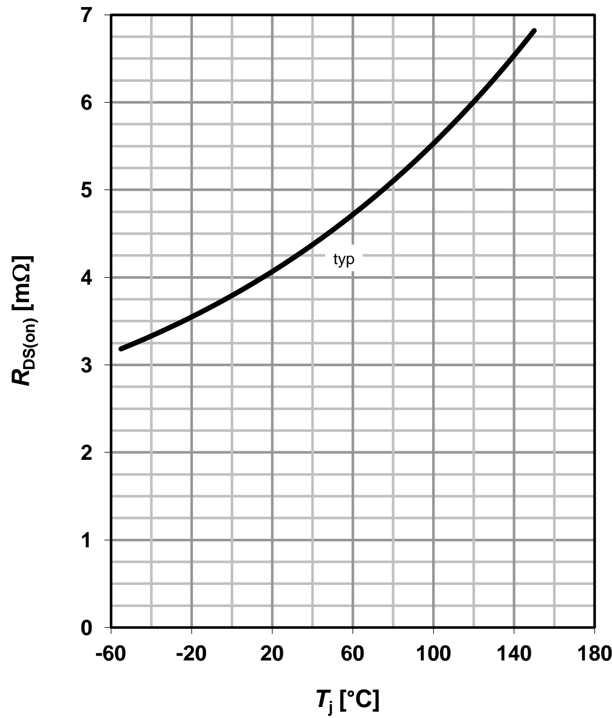
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



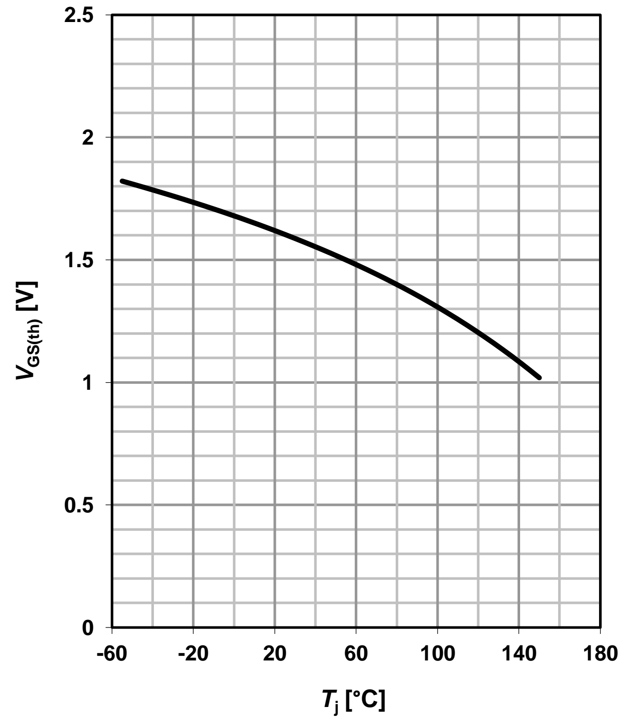
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V



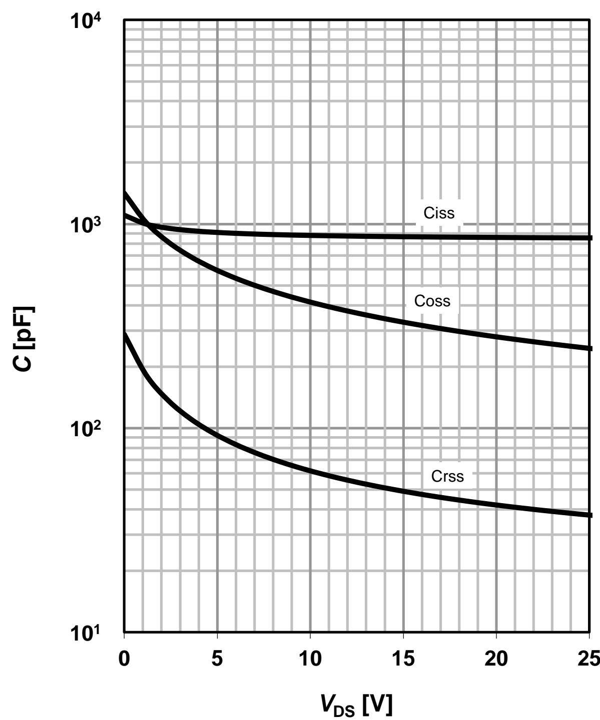
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA



11 Typ. capacitances

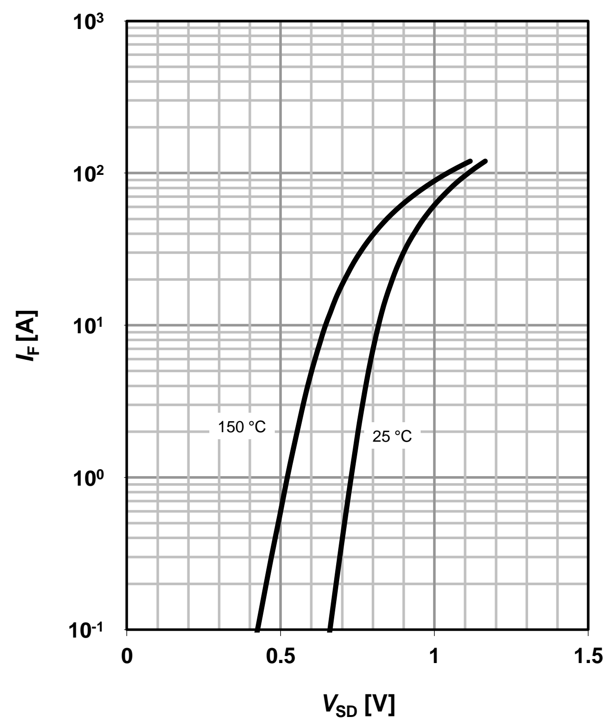
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

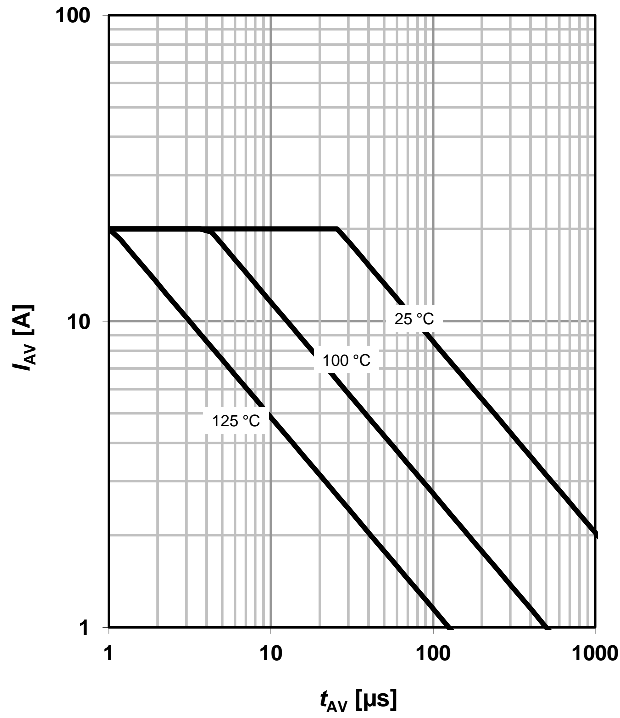
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

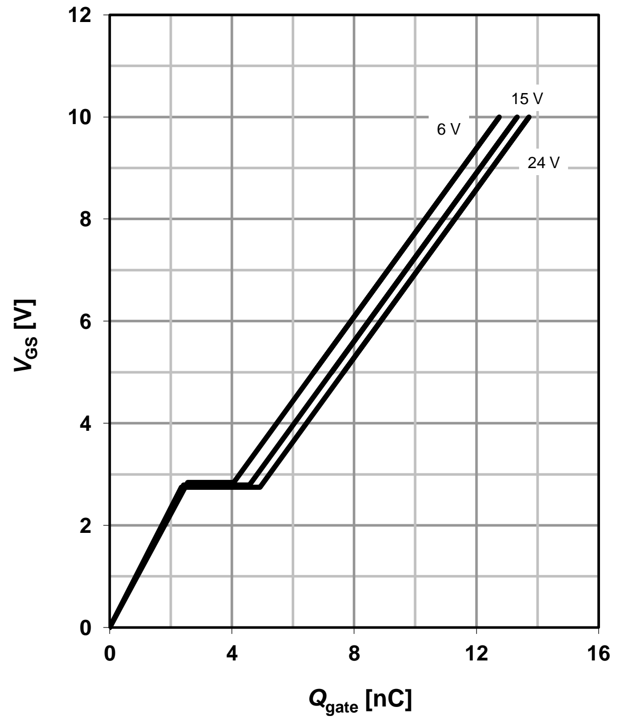
parameter: $T_{j(start)}$



14 Typ. gate charge

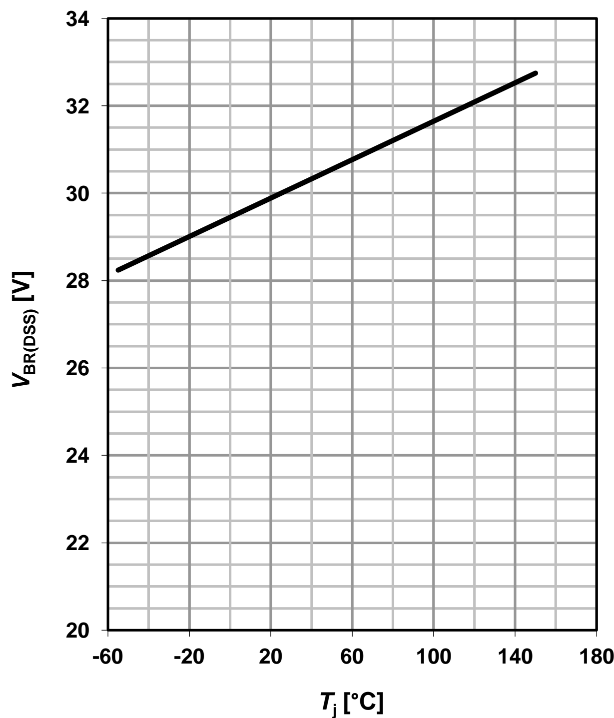
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

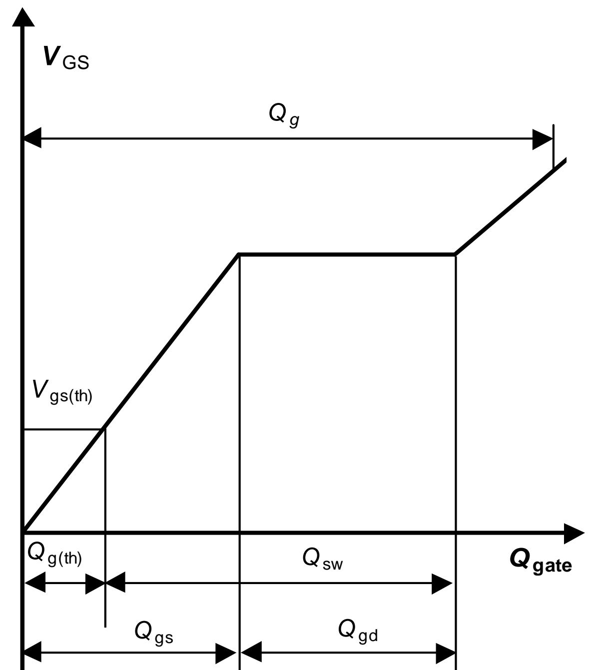


15 Drain-source breakdown voltage

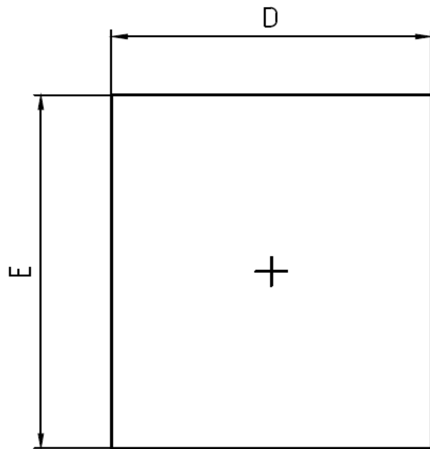
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

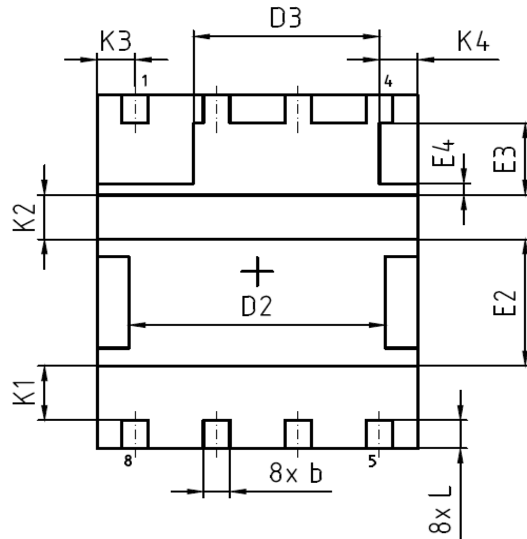


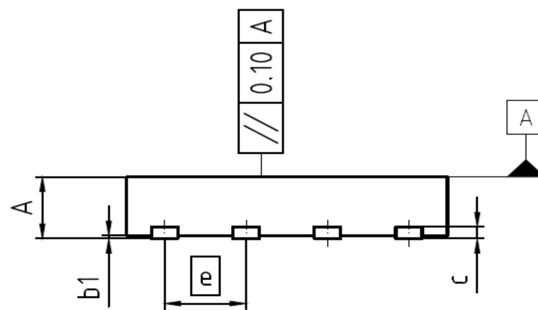
16 Gate charge waveforms



Package Outline **PG-TISON**







DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	**0.90**	**1.15**	**0.035**	**0.045**
b	**0.31**	**0.51**	**0.012**	**0.020**
b1	**0.00**	**0.05**	**0.000**	**0.002**
c	**0.10**	**0.30**	**0.004**	**0.012**
D	**4.90**	**5.10**	**0.193**	**0.201**
D2	**3.90**	**4.10**	**0.154**	**0.161**
D3	**2.80**	**3.00**	**0.110**	**0.118**
E	**5.90**	**6.10**	**0.232**	**0.240**
E2	**2.05**	**2.25**	**0.081**	**0.089**
E3	**1.12**	**1.32**	**0.044**	**0.052**
E4	**0.10**	**0.30**	**0.004**	**0.012**
e	**1.27 (BSC)**		**0.05 (BSC)**	
N	**8**		**8**	
L	**0.38**	**0.58**	**0.015**	**0.023**
K1	**0.82**	**1.02**	**0.032**	**0.040**
K2	**0.65**	**0.85**	**0.026**	**0.033**
K3 = K4	**0.50**	**0.70**	**0.019**	**0.027**

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SCALE
0 2.5 5mm

EUROPEAN PROJECTION

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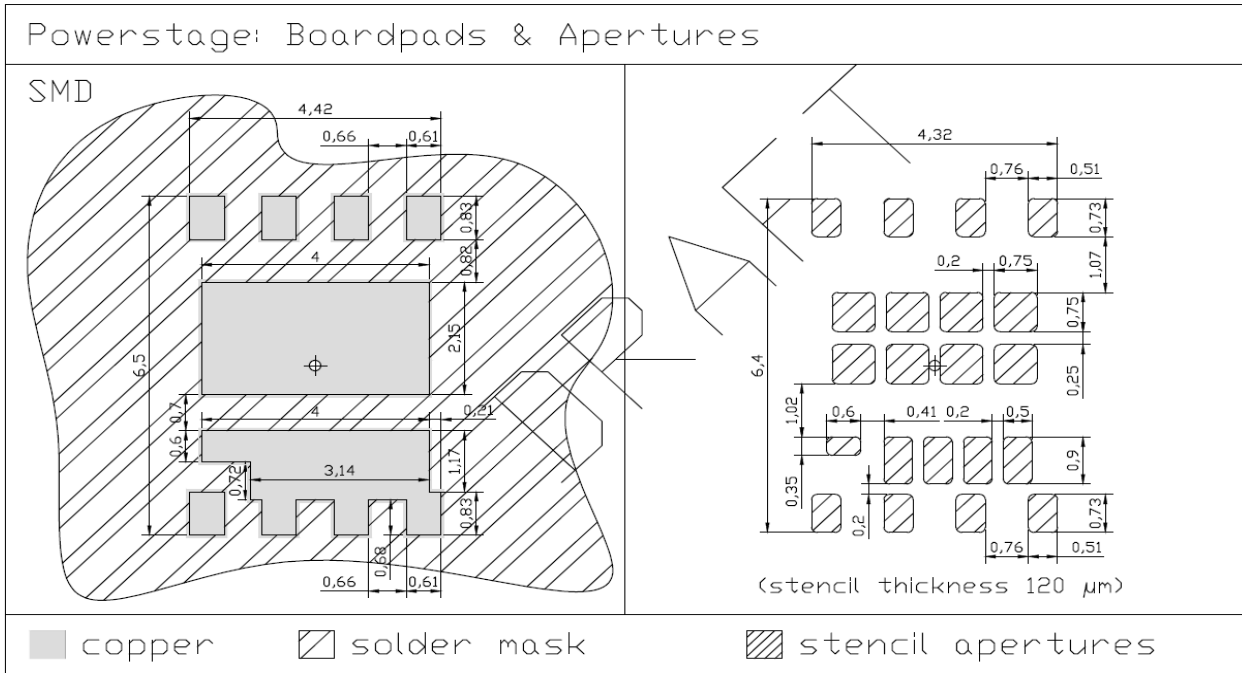
PG-TISON



Dimensions in mm

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