# bq25606 Standalone 3.0-A, Single Cell Battery Charger With 40V Over Voltage Protection Controller

## 1 Features

- High-Efficiency, 1.5-MHz, Synchronous Switch-Mode Buck Charger
  - 92% Charge Efficiency at 2 A from 5-V Input
  - Optimized for USB Voltage Input (5 V)
- Supports USB On-The-Go (OTG)
  - Boost Converter With Up to 1.2-A Output
  - 92% Boost Efficiency at 1-A Output
  - Accurate Constant Current (CC) Limit
  - Soft-Start Up To 500-µF Capacitive Load
  - Output Short Circuit Protection
- Single Input to Support USB Input and High Voltage Adapters
  - Support 3.9-V to 13.5-V Input Voltage Range With 20-V Absolute Maximum Input Voltage Rating
  - Maximum Power Tracking by Input Voltage Limit Up to 4.6 V (VINDPM)
  - VINDPM Threshold Automatically Tracks Battery Voltage
  - Auto Detect USB SDP, DCP and Non-Standard Adaptors
- 200nS Fast Turn-Off of Optional External OVPFET Standing Input Voltage Up to 40V
- High Battery Discharge Efficiency With 19.5-mΩ Battery Discharge MOSFET
- Narrow VDC (NVDC) Power Path Management
  - Instant-On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- 58-µA Low Battery Leakage Current with System Voltage Standby
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±6% at 1.2-A and 1.8-A Charge Current Regulation
  - ±5% at 0.5-A, 1.2-A and 1.8-A Input Current Regulation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown
  - Input UVLO and Overvoltage Protection

## 2 Applications

- EPOS, Portable Speakers, E-Cigarette
- Portable Internet Devices and Accessory

## 3 Description

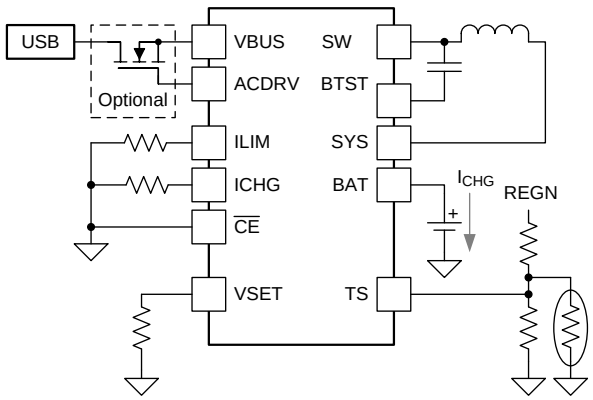
The bq25606 device is a highly-integrated standalone 3.0-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| bq25606 | VQFN (24) | 4.00 mm × 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents



## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| May 2017 | * | Initial release. |


Copyright © 2017, Texas Instruments Incorporated

## 5 Description (continued)

The bq25606 is a highly-integrated standalone 3.0-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of standalone chargers and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. Its input voltage and current regulation deliver maximum charging power to battery. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant high voltage adapter. The device sets default input current limit based on the built-in USB interface. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. When the device built-in USB interface identifies the input adaptor is unknown, the device's input current limit is determined by the ILIM pin setting resistor value. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5.15 V on VBUS with constant current limit up to 1.2-A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5 V minimum system voltage. With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This Supplement Mode prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It senses the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit and the battery voltage is higher than recharge threshold. If the fully charged battery falls below the recharge threshold, the charger automatically starts another charging cycle.

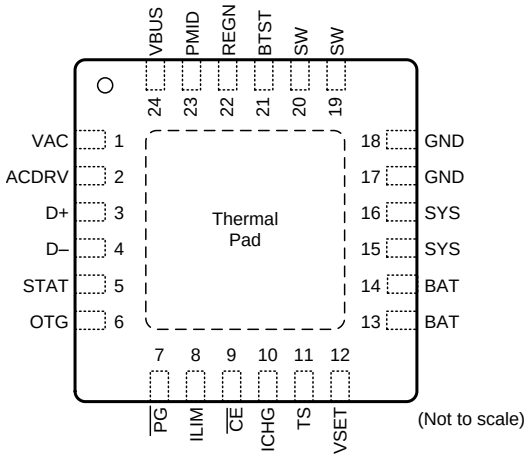
The charger provides various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer and overvoltage and overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds 110°C. The STAT output reports the charging status and any fault conditions.

The device family is available in 24-pin, 4 mm x 4 mm QFN package.

Copyright © 2017, Texas Instruments Incorporated

# 6 Pin Configuration and Functions

**bq25606 WQFN Package**
**24-Pin WQFN**
**Top View**




| Terminal | | I/O | Description |
|---|---|---|---|
| Name | No. | | |
| ACDRV | 2 | AO | Charge pump output to drive external N-channel MOSFET (OVPFET). ACDRV voltage is 11 V above VBUS when VAC voltage is below ACOV threshold and above $V_{VAC\_PRESENT}$. If external OVP is not used, leave this pin floating. |
| BAT | 13 | P | Battery connection point to the positive terminal of the battery pack. The internal current sensing resistor is connected between SYS and BAT. Connect a 10 µF closely to the BAT pin. |
| | 14 | | |
| BTST | 21 | P | PWM high side driver positive supply. internally, the BTST is connected to the cathode of the boost-strap diode. Connect the 0.047-µF bootstrap capacitor from SW to BTST. |
| $\overline{CE}$ | 9 | DI | Charge enable pin. When this pin is driven low, battery charging is enabled. |
| D+ | 3 | AIO | Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors |
| D– | 4 | AIO | Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors |
| GND | 17 | — | Power ground and signal ground |
| | 18 | | |
| ICHG | 10 | AI | $I_{CHG}$ pin sets the charge current limit. A resistor is connected from $I_{CHG}$ pin to ground to set charge current limit as $I_{CHG} = K_{ICHG}/R_{ICHG}$. The acceptable range for charge current is 300 mA – 3000 mA. |
| ILIM | 8 | AI | ILIM sets the input current limit. A resistor is connected from ILIM pin to ground to set the input current limit as IINDPM = $K_{ILIM}/R_{ILIM}$. The acceptable range for ILIM current is 500 mA - 3200 mA.<br>The resistor based input current limit is effective only when the input adapter is detected as unknown. Otherwise, the input current limit is determined by D+/D– detection outcome. |
| OTG | 6 | DI | Boost mode enable pin. When this pin is pulled HIGH, OTG is enabled. OTG cannot be floating. |
| $\overline{PG}$ | 7 | DO | Open drain active low power good indicator. Connect to the pull up rail through 10 kΩ resistor. LOW indicates a good input if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and input current limit is above 30 mA. |
| PMID | 23 | P | Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put a 10 -µF ceramic capacitor between PMID and GND. |
| REGN | 22 | P | PWM low side driver positive supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. |


Copyright © 2017, Texas Instruments Incorporated

**(continued)**

| Terminal | | I/O | Description |
|---|---|---|---|
| Name | No. | | |
| STAT | 5 | DO | Open-drain interrupt output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status.<br>Charge in progress: LOW<br>Charge complete or charger in SLEEP mode: HIGH<br>Charge suspend (fault response): BlinK at 1Hz |
| SW | 19 | P | Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047-μF bootstrap capacitor from SW to BTST. |
| | 20 | | |
| SYS | 15 | P | Converter output connection point. The internal current sensing resistor is connected between SYS and BAT. Connect a 20 μF capacitor close to the SYS pin. |
| | 16 | | |
| TS | 11 | AI | Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin voltage is out of range. Recommend 103AT-2 thermistor. |
| VAC | 1 | AI | Input voltage sensing. When VAC voltage is below ACOV threshold and above UVLO, external OVPFET turns on. If exteral OVP is not used, This pin must be shorted to VBUS pin. |
| VBUS | 24 | P | Charger input voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-uF ceramic capacitor from VBUS to GND and place it as close as possible to IC. |
| VSET | 12 | AI | VSET pin sets default battery charge voltage in bq25606. Program battery regulation voltage with a resistor pull-down from VSET to GND.<br>$R_{PD}$ > 50kΩ (float pin) = 4.208 V<br>$R_{PD}$ < 500Ω (short to GND) = 4.352 V<br>5kΩ < $R_{PD}$ < 25kΩ = 4.400 V |
| Thermal Pad | | P | Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane. |

Copyright © 2017, Texas Instruments Incorporated

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | Min | MAX | UNIT |
|---|---|---|---|---|
| Voltage Range (with respect to GND) | VAC | –2 | 40 | V |
| | ACDRV | –0.3 | 40 | V |
| Voltage Range (with respect to GND) | VBUS (converter not switching)(2) | –2 | 22 | V |
| Voltage Range (with respect to GND) | BTST, PMID (converter not switching)(2) | –0.3 | 22 | V |
| Voltage Range (with respect to GND) | SW | –2 | 16 | V |
| Voltage Range (with respect to GND) | BTST to SW | –0.3 | 7 | V |
| Voltage Range (with respect to GND) | D+, D– | –0.3 | 7 | V |
| Voltage Range (with respect to GND) | REGN, TS, $\overline{CE}$, $\overline{PG}$, BAT, SYS (converter not switching) | –0.3 | 7 | V |
| Output Sink current | STAT | | 6 | mA |
| Voltage Range (with respect to GND) | VSET, ILIM, ICHG, OTG | –0.3 | 7 | V |
| Voltage Range (with respect to GND) | PGND to GND (QFN package only) | –0.3 | 0.3 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) VBUS is specified up to 22 V for a maximum of 1 hour at room temperature

## 7.2 Recommended Operating Conditions

| | | Min | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{BUS}$ | Input voltage | 3.9 | | 13.5(1) | V |
| $I_{in}$ | Input current (VBUS) | | | 3.25 | A |
| $I_{SYSOP}$ | Output current (SW) | | | 3.0 | A |
| $V_{BATOP}$ | Battery voltage | | | 4.4 | V |
| $I_{BATOP}$ | Fast charging current | | | 3.0 | A |
| $I_{BATOP}$ | Discharging current (continuous) | | | 6 | A |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum voltage rating on either the BTST or SW pins. A tight layout minimizes switching noise.

## 7.3 Thermal information

| THERMAL METRIC | | bq25606 RGE (VQFN) 24 Pins | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 31.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 27 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 9.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 9.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.8 | °C/W |


Copyright © 2017, Texas Instruments Incorporated

## 7.4 Timing Requirements

| Parameter | | Additional Information | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VBUS/BAT POWER UP** | | | | | | |
| $t_{ACOV}$ | VAC OVP reaction time | VAC rising above ACOV threshold to turn off Q2 | | 200 | | ns |
| $t_{DEB}$ | VAC debounce time (time before ACDRV pulling high) | VAC rising above $V_{VAC\_PRESENT}$ threshold to ACDRV pulling high | | 15 | | ms |
| $t_{BADSRC}$ | Bad adapter detection duration | | | 30 | | ms |
| **BATTERY CHARGER** | | | | | | |
| $t_{TERM\_DGL}$ | Deglitch time for charge termination | | | 250 | | ms |
| $t_{RECHG\_DGL}$ | Deglitch time for recharge | | | 250 | | ms |
| $t_{SYSOVLD\_DGL}$ | System over-current deglitch time to turn off Q4 | | | 100 | | µs |
| $t_{BATOVP}$ | Battery over-voltage deglitch time to disable charge | | | 1 | | µs |
| $t_{SAFETY}$ | Typical Charge Safety Timer Range | | 8 | 10 | 12 | hr |

## 7.5 Electrical Characteristics

$V_{VAC\_PRESENT} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J$ = –40°C to 125°C and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **QUIESCENT CURRENTS** | | | | | | |
| $I_{BAT}$ | Battery discharge current (BAT, SW, SYS) in buck mode | $V_{BAT}$ = 4.5 V, $V_{BUS} < V_{AC\text{-}UVLOZ}$, leakage between BAT and VBUS, $T_J$< 85°C | | | 5 | µA |
| $I_{BAT}$ | Battery discharge current (BAT, SW, SYS) | $V_{BAT}$ = 4.5 V, No VBUS, $T_J$ < 85°C | | 58 | 85 | µA |
| $I_{VBUS}$ | Input supply current (VBUS) in buck mode | $V_{VBUS}$ = 12 V, $V_{VBUS} > V_{VBAT}$, converter not switching | | 1.5 | 3 | mA |
| $I_{VBUS}$ | Input supply current (VBUS) in buck mode | $V_{VBUS} >$ VUVLO, $V_{VBUS} > V_{VBAT}$, converter switching, VBAT = 3.8V, ISYS = 0A | | 3 | | mA |
| $I_{BOOST}$ | Battery discharge current in boost mode | $V_{BAT}$ = 4.2 V, boost mode, $I_{VBUS}$ = 0 A, converter switching | | 3 | | mA |
| **VBUS, VAC AND BAT PIN POWER-UP** | | | | | | |
| $V_{BUS\_OP}$ | VBUS operating range | $V_{VBUS}$ rising | 3.9 | | 13.5 | V |
| $V_{VAC\_PRESENT}$ | OVPFET turn-on threshold | $V_{VAC}$ rising | 3.36 | 3.65 | 3.97 | V |
| $V_{VAC\_PRESENT\_HYS}$ | | $V_{VAC}$ falling | | 300 | | mV |
| $V_{SLEEP}$ | Sleep mode falling threshold | ($V_{VAC}$–$V_{VBAT}$ ), $V_{BUSMIN\_FALL} \le V_{BAT} \le V_{REG}$, VAC falling | 37 | 76 | 126 | mV |
| $V_{SLEEPZ}$ | Sleep mode rising threshold | ($V_{VAC}$–$V_{VBAT}$ ), $V_{BUSMIN\_FALL} \le V_{BAT} \le V_{REG}$, VAC rising | 130 | 220 | 350 | mV |
| $V_{VAC\_OV\_RISE}$ | VAC Overvoltage rising threshold | VAC rising | 13.5 | 14.28 | 14.91 | V |
| $V_{VAC\_OV\_HYS}$ | VAC Overvoltage hysteresis | VAC falling | | 520 | | mV |
| $V_{BAT\_DPL\_FALL}$ | Battery depletion falling threshold (Q4 turn-off threshold) | $V_{BAT}$ falling | 2.15 | | 2.6 | V |
| $V_{BAT\_DPL\_RISE}$ | Battery Depletion rising threshold (Q4 turn-on threshold) | $V_{BAT}$ rising | 2.35 | | 2.82 | V |
| $V_{BAT\_DPL\_HYST}$ | Battery Depletion rising hysteresis | $V_{BAT}$ rising | | 180 | | mV |
| $V_{BUSMIN\_FALL}$ | Bad adapter detection falling threshold | $V_{BUS}$ falling | 3.65 | 3.8 | 3.93 | V |
| $V_{BUSMIN\_HYST}$ | Bad adapter detection hysteresis | | | 200 | | mV |
| $I_{BADSRC}$ | Bad adapter detection current source | Sink current from VBUS to GND | | 30 | | mA |
| **POWER-PATH** | | | | | | |

Copyright © 2017, Texas Instruments Incorporated

## Electrical Characteristics (continued)

$V_{VAC\_PRESENT} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J$ = –40°C to 125°C and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{SYS\_MIN}$ | System regulation voltage | $V_{VBAT} < V_{SYS\_MIN\ =\ 3.5V}$, charge enabled or disabled | 3.5 | 3.68 | | V |
| $V_{SYS}$ | System regulation voltage | $I_{SYS}$ = 0 A, $V_{VBAT} > V_{SYSMIN}$, charge disabled | | $V_{BAT}$ + 50 mV | | V |
| $R_{ON(RBFET)}$ | Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1 | -40°C≤ $T_A$ ≤ 125°C | | 45 | | mΩ |
| $R_{ON(HSFET)}$ | Top switching MOSFET on-resistance between PMID and SW - Q2 | $V_{REGN}$ = 5 V , -40°C≤ $T_A$ ≤ 125°C | | 62 | | mΩ |
| $R_{ON(LSFET)}$ | Bottom switching MOSFET on-resistance between SW and GND - Q3 | $V_{REGN}$ = 5 V , -40°C≤ $T_A$ ≤ 125°C | | 70 | | mΩ |
| $V_{FWD}$ | BATFET forward voltage in supplement mode | | | 30 | | mV |
| $R_{ON(BAT-SYS)}$ | SYS-BAT MOSFET on-resistance | QFN package, Measured from BAT to SYS, $V_{BAT}$ = 4.2V, $T_J$ = 25°C | | 19.5 | 24 | mΩ |
| $R_{ON(BAT-SYS)}$ | SYS-BAT MOSFET on-resistance | QFN package, Measured from BAT to SYS, $V_{BAT}$ = 4.2V, $T_J$ = –40 - 125°C | | 19.5 | 30 | mΩ |
| **BATTERY CHARGER** | | | | | | |
| $V_{BATREG}$ | Charge voltage | $R_{VSET}$ > 50 kΩ, –40 ≤ $T_J$ ≤ 85°C | 4.187 | 4.208 | 4.229 | V |
| | | $R_{VSET}$ < 500 Ω, –40 ≤ $T_J$ ≤ 85°C | 4.330 | 4.352 | 4.374 | V |
| | | $R_{VSET}$ = 10 kΩ, –40 ≤ $T_J$ ≤ 85°C | 4.378 | 4.4 | 4.422 | V |
| $V_{BATREG\_ACC}$ | Charge voltage setting accuracy | $V_{BAT}$ = 4.208 V or $V_{BAT}$ = 4.352 V, –40 ≤ $T_J$ ≤ 85°C | –0.5% | | 0.5% | |
| $I_{CHG\_REG\_RANGE}$ | Charge current regulation range | | 0 | | 3000 | mA |
| $I_{CHG\_REG}$ | Charge current regulation | $R_{ICHG}$ = 1100 Ω, $V_{VBAT}$ = 3.1 V or $V_{VBAT}$ = 3.8 V | 516 | 615 | 715 | mA |
| $I_{CHG\_REG\_ACC}$ | Charge current regulation accuracy | $R_{ICHG}$ = 1100 Ω, $V_{VBAT}$ = 3.1 V or $V_{VBAT}$ = 3.8 V | -16% | | 16% | |
| $I_{CHG\_REG}$ | Charge current regulation | $R_{ICHG}$ = 562 Ω, $V_{VBAT}$ = 3.1 V or $V_{VBAT}$ = 3.8 V | 1.14 | 1.218 | 1.28 | A |
| $I_{CHG\_REG}$ | Charge current regulation accuracy | $R_{ICHG}$ = 562 Ω, $V_{BAT}$ = 3.1 V or $V_{BAT}$ = 3.8 V | -6% | | 6% | |
| $I_{CHG\_REG}$ | Charge current regulation | $R_{ICHG}$ = 372 Ω, $V_{VBAT}$ = 3.1 V or $V_{VBAT}$ = 3.8 V | 1.715 | 1.813 | 1.89 | A |
| $I_{CHG\_REG\_ACC}$ | Charge current regulation accuracy | $R_{ICHG}$ = 372 Ω, $V_{VBAT}$ = 3.1 V or $V_{VBAT}$ = 3.8 V | -5% | | 5% | |
| $K_{ICHG}$ | Charge current regulation setting ratio | $R_{ICHG}$ = 372 Ω, 562 Ω $V_{VBAT}$ = 3.1 V or $V_{VBAT}$ = 3.8 V | 639 | 677 | 715 | A×Ω |
| $K_{ICHG\_ACC}$ | Charge current regulation setting ratio accuracy | $R_{ICHG}$ = 372Ω, 562 Ω $V_{VBAT}$ = 3.1 V or $V_{VBAT}$ = 3.8 V | -6% | | 6% | |
| $V_{BATLOWV\_FALL}$ | Battery LOWV falling threshold | Fast charge to precharge | 2.67 | 2.8 | 2.87 | V |
| $V_{BATLOWV\_RISE}$ | Battery LOWV rising threshold | Pre-charge to fast charge | 3.0 | 3.1 | 3.24 | V |
| $I_{PRECHG}$ | Precharge current regulation | $R_{ICHG}$ = 1100 Ω, $V_{VBAT}$ = 2.6 V, $I_{PRECHG}$ = 5% of $I_{CHG}$ = 615mA | 21 | | 38 | mA |
| $I_{PRECHG\_ACC}$ | Precharge current regulation accuracy | Percentage of $I_{CHG}$,$R_{ICHG}$ = 1100 Ω, $V_{VBAT}$ = 2.6 V, $I_{CHG}$ = 615mA | 3.4% | | 6.2% | |
| $I_{PRECHG}$ | Precharge current regulation | $R_{ICHG}$ = 562 Ω, $V_{VBAT}$ = 2.6 V, $I_{PRECHG}$ = 5% of $I_{CHG}$ = 1.218A | 48 | | 67 | mA |
| $I_{PRECHG\_ACC}$ | Precharge current regulation accuracy | Percentage of $I_{CHG}$,$R_{ICHG}$ = 562 Ω, V1330 = 2.6 V, $I_{CHG}$ = 1.218A | 3.9% | | 5.5% | |


Copyright © 2017, Texas Instruments Incorporated

## Electrical Characteristics (continued)

$V_{VAC\_PRESENT} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J$ = –40°C to 125°C and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{PRECHG}$ | Precharge current regulation | $R_{ICHG}$ = 372 Ω, $V_{VBAT}$ = 2.6 V, $I_{PRECHG}$ = 5% of $I_{CHG}$ = 1.813A | 76 | | 97 | mA |
| $I_{PRECHG\_ACC}$ | Precharge current regulation accuracy | Percentage of $I_{CHG}$,$R_{ICHG}$ = 372 Ω, $V_{VBAT}$ = 2.6 V, $I_{CHG}$ = 1.813A | 4.1% | | 5.4% | |
| $I_{TERM}$ | Termination current regulation | $R_{ICHG}$ = 562 Ω, $V_{VBAT}$ = 4.35V, $_{CHG}$ = 1.218A | 26 | | 100 | mA |
| $I_{TERM\_ACC}$ | Termination current regulation accuracy | Percentage of $I_{CHG}$, $R_{ICHG}$ = 562 Ω, $V_{VBAT}$ = 4.35 V, $I_{CHG}$ = 1.218 A | 2.1% | | 8.3% | |
| $I_{TERM}$ | Termination current regulation | $R_{ICHG}$ = 372 Ω, $V_{VBAT}$ = 4.35 V, $I_{CHG}$ = 1.813 A | 56 | 100 | 126 | mA |
| $I_{TERM\_ACC}$ | Termination current regulation accuracy | Percentage of $I_{CHG}$, $R_{ICHG}$ = 372 Ω, $V_{VBAT}$ = 4.35 V, $I_{CHG}$ = 1.813 A | 3.0% | | 7.0% | |
| $V_{SHORT}$ | Battery short voltage | $V_{VBAT}$ falling | 1.85 | 2 | 2.15 | V |
| $V_{SHORTZ}$ | Battery short voltage | $V_{VBAT}$ rising | 2.05 | 2.25 | 2.35 | V |
| $I_{SHORT}$ | Battery short current | $V_{VBAT} < V_{SHORTZ}$ | 70 | 90 | 110 | mA |
| $V_{RECHG}$ | Recharge Threshold below $V_{BAT\_REG}$ | $V_{BAT}$ falling | 87 | 121 | 156 | mV |
| $I_{SYSLOAD}$ | System discharge load current | $V_{SYS}$ = 4.2 V | | 30 | | mA |
| **INPUT VOLTAGE AND CURRENT REGULATION** | | | | | | |
| $V_{DPM\_VBAT}$ | Input voltage regulation limit | $V_{VBAT}$ < 4.1 V ($V_{VBAT}$= 3.6 V) | 4.171 | 4.3 | 4.429 | V |
| $V_{DPM\_VBAT\_ACC}$ | Input voltage regulation accuracy | $V_{VBAT}$ < 4.1 V ($V_{VBAT}$ = 3.6 V) | –3% | | 3% | |
| $I_{INDPM}$ | USB input current regulation limit | $V_{VBUS}$ = 5 V, USB500 charge port detected by DPDM , –40 ≤ $T_J$ ≤ 85°C | 448 | | 500 | mA |
| $I_{INDPM}$ | Input current regulation limit | $R_{ILIM}$ = 910 Ω, unknown adaptor detected by DPDM , –40 ≤ $T_J$ ≤ 85°C | 505 | 526 | 550 | mA |
| $I_{INDPM}$ | Input current regulation limit accuracy | $R_{ILIM}$ = 374 Ω, unknown adaptor detected by DPDM , –40 ≤ $T_J$ ≤ 85°C | 1220 | 1276 | 1330 | mA |
| $I_{INDPM}$ | Input current regulation limit | $R_{ILIM}$ = 265 Ω, unknown adaptor detected by DPDM , –40 ≤ $T_J$ ≤ 85°C | 1.73 | 1.8 | 1.871 | A |
| $I_{INDPM\_ACC}$ | Input current regulation limit accuracy | $R_{ILIM}$ = 265 Ω, 374 Ω, 910 Ω, unknown adaptor detected by DPDM , –40 ≤ $T_J$ ≤ 85°C | –5% | | 5% | |
| $K_{ILIM}$ | Input current setting ratio, $I_{LIM}$ = $K_{ILIM}$ / $R_{ILIM}$ | $R_{ILIM}$ = 910 Ω, 374 Ω, 265 Ω, unknown adaptor detected by DPDM, –40 ≤ $T_J$ ≤ 85°C | 459 | 478 | 500 | A×Ω |
| $K_{ILIM\_ACC}$ | Input current setting ratio, $I_{LIM}$ = $K_{ILIM}$ / $R_{ILIM}$ | $R_{ILIM}$ = 910 Ω, 374 Ω, 265 Ω, unknown adaptor detected by DPDM, –40 ≤ $T_J$ ≤ 85°C | –5% | | 5% | |
| $I_{IN\_START}$ | Input current limit during system start-up sequence | | | 200 | | mA |
| **BAT PIN OVERVOLTAGE PROTECTION** | | | | | | |
| $V_{BATOVP\_RISE}$ | Battery overvoltage threshold | $V_{BAT}$ rising, as percentage of $V_{BAT\_REG}$ | 103% | 104% | 105% | |
| $V_{BATOVP\_FALL}$ | Battery overvoltage threshold | $V_{BAT}$ falling, as percentage of $V_{BAT\_REG}$ | 101% | 102% | 103% | |

Copyright © 2017, Texas Instruments Incorporated

## Electrical Characteristics (continued)

$V_{VAC\_PRESENT}$ < $V_{VAC}$ < $V_{VAC\_OV}$ and $V_{VAC}$ > $V_{BAT}$ + $V_{SLEEP}$, $T_J$ = –40°C to 125°C and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **THERMAL REGULATION AND THERMAL SHUTDOWN** | | | | | | |
| $T_{JUNCTION\_REG}$ | Junction Temperature Regulation Threshold | | | 110 | | °C |
| $T_{SHUT}$ | Thermal Shutdown Rising Temperature | Temperature Increasing | | 160 | | °C |
| $T_{SHUT\_HYST}$ | Thermal Shutdown Hysteresis | | | 30 | | °C |
| **JEITA Thermistor Comparator (BUCK MODE)** | | | | | | |
| $V_{T1}$ | T1 (0°C) threshold, Charge suspended T1 below this temperature. | Charger suspends charge. As Percentage to $V_{REGN}$ | 72.4% | 73.3% | 74.2% | |
| $V_{T1}$ | Falling | As Percentage to $V_{REGN}$ | 69% | 71.5% | 74% | |
| $V_{T2}$ | T2 (10°C) threshold, Charge back to $I_{CHG}$/2 and 4.2 V below this temperature | As percentage of $V_{REGN}$ | 67.2% | 68% | 69% | |
| $V_{T2}$ | Falling | As Percentage to $V_{REGN}$ | 66% | 66.8% | 67.7% | |
| $V_{T3}$ | T3 (45°C) threshold, charge back to ICHG and 4.05V above this temperature. | Charger suspends charge. As Percentage to $V_{REGN}$ | 43.8% | 44.7% | 45.8% | |
| $V_{T3}$ | Falling | As Percentage to $V_{REGN}$ | 45.1% | 45.7% | 46.2% | |
| $V_{T5}$ | T5 (60°C) threshold, charge suspended above this temperature. | As Percentage to $V_{REGN}$ | 33.7% | 34.2% | 35.1% | |
| $V_{T5}$ | Falling | As Percentage to $V_{REGN}$ | 34.5% | 35.3% | 36.2% | |
| **COLD OR HOT THERMISTER COMPARATOR (BOOST MODE)** | | | | | | |
| $V_{BCOLD}$ | Cold Temperature Threshold, TS pin Voltage Rising Threshold | As Percentage to $V_{REGN}$ (Approx. –20°C w/ 103AT), –20°C ≤ $T_J$≤ 125°C | 79.5% | 80% | 80.5% | |
| $V_{BCOLD}$ | Falling | –20°C ≤ $T_J$≤ 125°C | 78.5% | 79% | 79.5% | |
| $V_{BHOT}$ | Hot Temperature Threshold, TS pin Voltage falling Threshold | As Percentage to $V_{REGN}$ (Approx. 60°C w/ 103AT), –20°C ≤ $T_J$≤ 125°C | 30.2% | 31.2% | 32.2% | |
| $V_{BHOT}$ | Rising | –20°C ≤ $T_J$≤ 125°C | 33.8% | 34.4% | 34.9% | |


Copyright © 2017, Texas Instruments Incorporated

## Electrical Characteristics (continued)

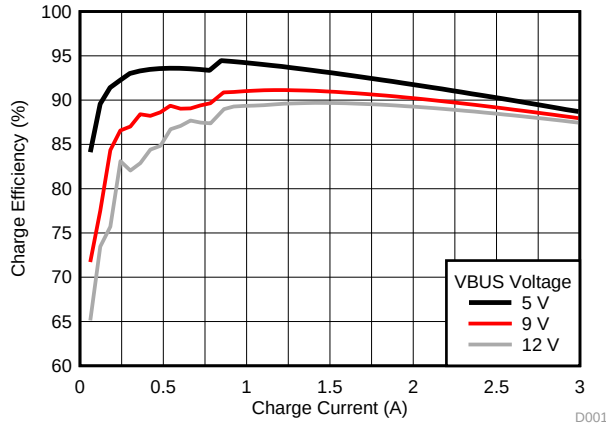
$V_{VAC\_PRESENT} < V_{VAC} < V_{VAC\_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J$ = –40°C to 125°C and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)** | | | | | | |
| $I_{HSFET\_OCP}$ | HSFET cycle-by-cycle over-current threshold | | 5.2 | | 8.0 | A |
| $I_{BATFET\_OCP}$ | System over load threshold | | 6.0 | | | A |
| **PWM** | | | | | | |
| $f_{SW}$ | PWM switching frequency | Oscillator frequency, buck mode | 1320 | 1500 | 1680 | kHz |
| | | Oscillator frequency, boost mode | 1170 | 1412 | 1500 | kHz |
| $D_{MAX}$ | Maximum PWM duty cycle(1) | | | 97% | | |
| **BOOST MODE OPERATION** | | | | | | |
| $V_{OTG\_REG}$ | Boost mode regulation voltage | $V_{VBAT}$ = 3.8 V, $I_{(PMID)}$ = 0 A | 4.972 | 5.126 | 5.280 | V |
| $V_{OTG\_REG\_ACC}$ | Boost mode regulation voltage accuracy | $V_{VBAT}$ = 3.8 V, $I_{(PMID)}$ = 0 A | -3 | | 3 | % |
| $V_{BATLOWV\_OTG}$ | Battery voltage exiting boost mode | $V_{VBAT}$ falling | 2.6 | 2.8 | 2.9 | V |
| | Battery voltage entering boost mode | $V_{VBAT}$ rising | 2.9 | 3.0 | 3.15 | V |
| $I_{OTG}$ | OTG mode output current limit | | 1.2 | 1.4 | 1.6 | A |
| $V_{OTG\_OVP}$ | OTG overvoltage threshold | Rising threshold | 5.55 | 5.8 | 6.15 | V |
| **REGN LDO** | | | | | | |
| $V_{REGN}$ | REGN LDO output voltage | $V_{VBUS}$ = 9 V, $I_{REGN}$ = 40 mA | 5.6 | 6 | 6.65 | V |
| $V_{REGN}$ | REGN LDO output voltage | $V_{VBUS}$ = 5 V, $I_{REGN}$ = 20 mA | 4.6 | 4.7 | 4.9 | V |
| **LOGIC I/O PIN CHARACTERISTICS ($\overline{CE}$, PSEL, SCL, SDA,, $\overline{INT}$)** | | | | | | |
| $V_{ILO}$ | Input low threshold $\overline{CE}$ | | | | 0.4 | V |
| $V_{IH}$ | Input high threshold $\overline{CE}$ | | 1.3 | | | V |
| $I_{BIAS}$ | High-level leakage current $\overline{CE}$ | Pull up rail 1.8 V | | | 1 | µA |
| $V_{ILO}$ | Input low threshold OTG | | | | 0.4 | V |
| $V_{IH}$ | Input high threshold OTG | | 1.3 | | | V |
| $I_{BIAS}$ | High-level leakage current OTG | Pull up rail 1.8 V | | | 1 | µA |
| **LOGIC I/O PIN CHARACTERISTICS ($\overline{PG}$, STAT)** | | | | | | |
| $V_{OL}$ | Low-level output voltage | | | | 0.4 | V |
| D+/D– DETECTION | | | | | | |
| $V_{D+\_1P2}$ | D+ Threshold for Non-standard adapter (combined V1P2_VTH_LO and V1P2_VTH_HI) | | 1.05 | | 1.35 | V |
| $I_{D+\_LKG}$ | Leakage current into D+ | HiZ | -1 | | 1 | µA |
| $V_{D-\_600MVSRC}$ | Voltage source (600 mV) | | 500 | 600 | 700 | mV |
| $I_{D-\_100UAISNK}$ | D– current sink (100 µA) | $V_{D-}$ = 500 mV, | 50 | 100 | 150 | µA |
| $R_{D-\_19K}$ | D– resistor to ground (19 kΩ) | $V_{D-}$ = 500 mV, | 14.25 | | 24.8 | kΩ |
| $V_{D-\_0P325}$ | D– comparator threshold for primary detection | D– pin Rising | 250 | | 400 | mV |
| $V_{D-\_2P8}$ | D– Threshold for non-standard adapter (combined V2P8_VTH_LO and V2P8_VTH_HI) | | 2.55 | | 2.85 | V |
| $V_{D-\_2P0}$ | D– Comparator threshold for non-standard adapter (For non-standard – same as bq2589x) | | 1.85 | | 2.15 | V |
| $V_{D-\_1P2}$ | D– Threshold for non-standard adapter (combined V1P2_VTH_LO and V1P2_VTH_HI) | | 1.05 | | 1.35 | V |
| $I_{D-\_LKG}$ | Leakage current into D– | HiZ | -1 | | 1 | µA |

(1) Specified by design. Not production tested.

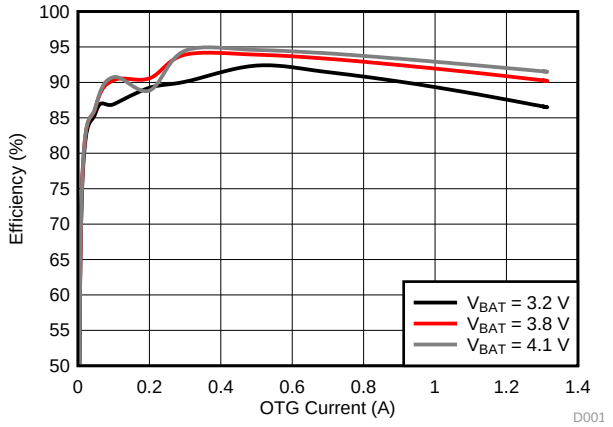
Copyright © 2017, Texas Instruments Incorporated

## 7.6 Typical Characteristics



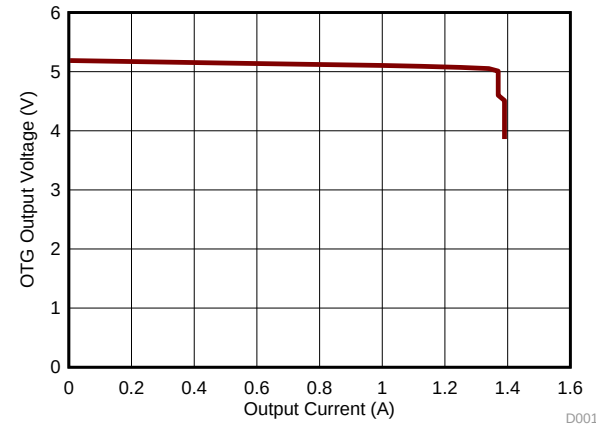

$f_{SW}$ = 1.5 MHz Inductor DCR = 18 mΩ
$V_{BAT}$ = 3.8 V

**Figure 1. Charge Efficiency vs. Charge Current**




$V_{OTG}$ = 5.15 V inductor DCR = 18 mΩ

**Figure 2. Efficiency vs. OTG Current**




0 A ≤ $I_{OTG}$ ≤1.37 A $V_{OTG}$ = 5.15 V
$V_{VBAT}$ = 3.8 V

**Figure 3. OTG Output Voltage vs. Output Current**

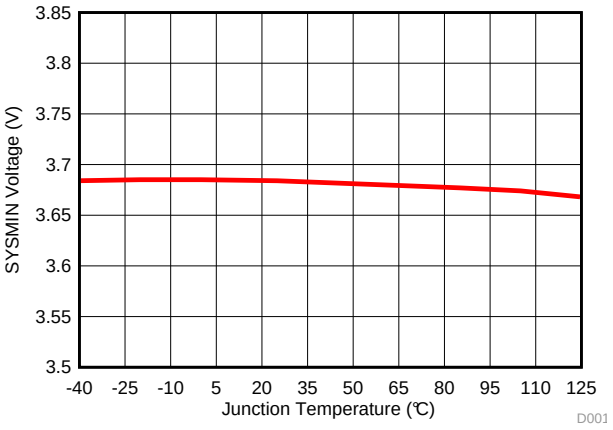



**Figure 4. SYSMIN Voltage vs. Junction Temperature**

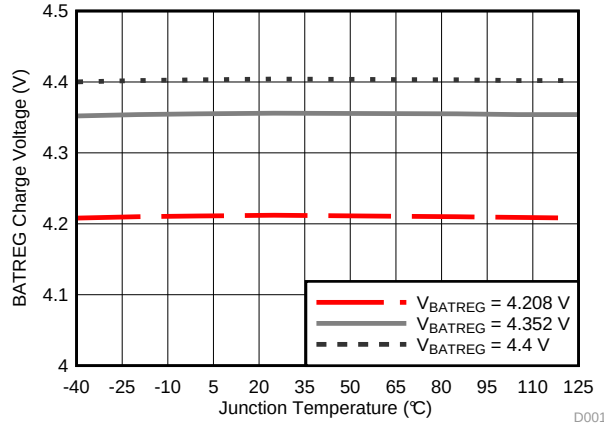
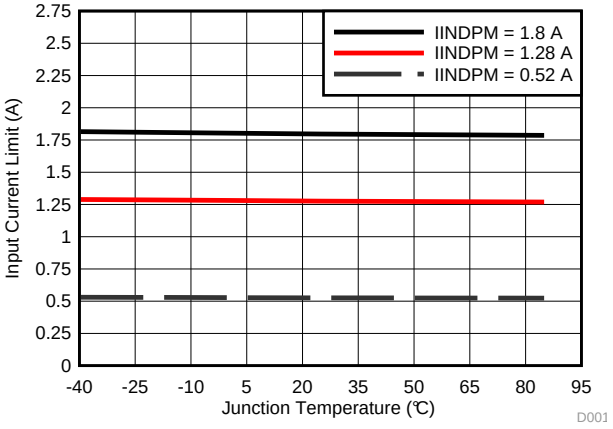



**Figure 5. BATREG Charge Voltage vs. Junction Temperature**

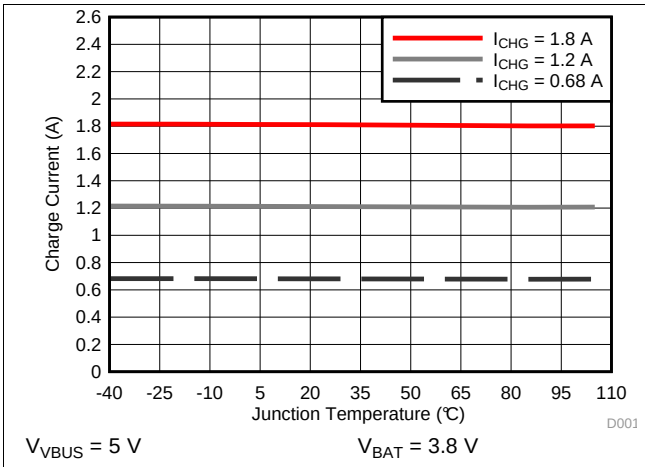



$V_{VBUS}$ = 5 V

**Figure 6. Input Current Limit vs. Junction Temperature**

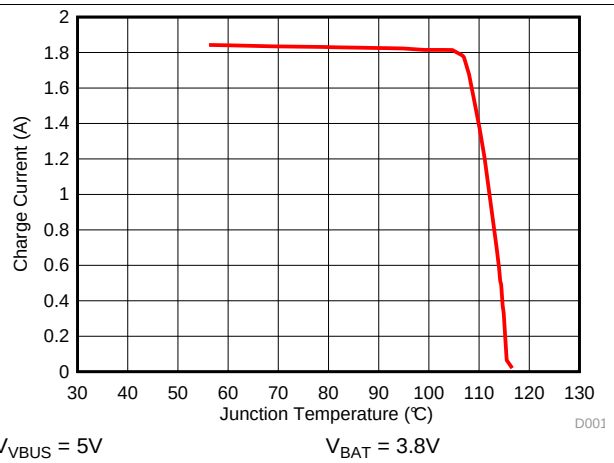

Copyright © 2017, Texas Instruments Incorporated

## Typical Characteristics (continued)



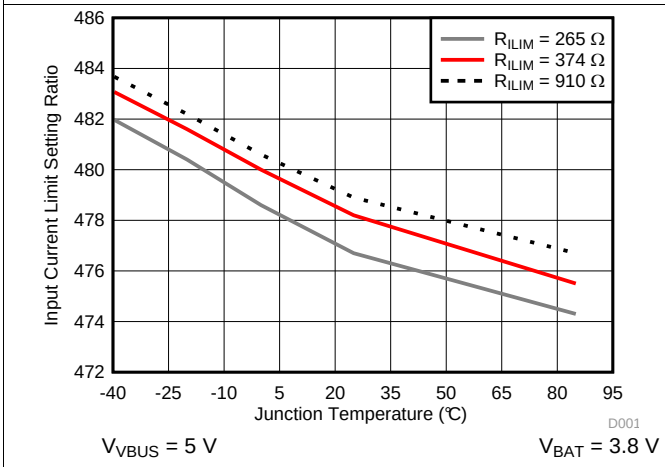

$V_{VBUS}$ = 5 V $V_{BAT}$ = 3.8 V

**Figure 7. Charge Current vs. Junction Temperature**



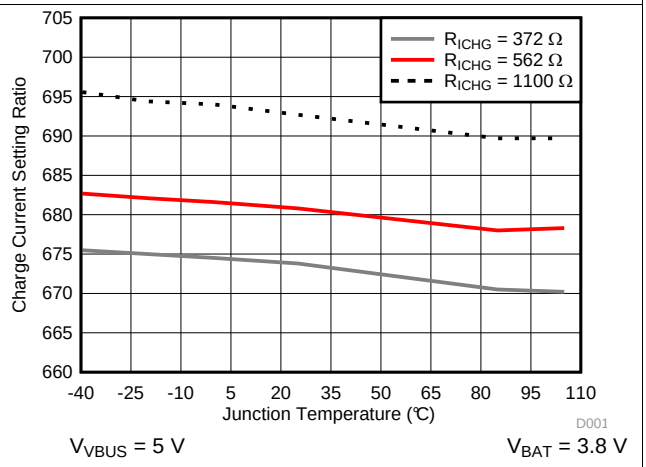

$V_{VBUS}$ = 5V $V_{BAT}$ = 3.8V

**Figure 8. Charge Current vs. Junction Temperature**




$V_{VBUS}$ = 5 V $V_{BAT}$ = 3.8 V

**Figure 9. Input Current Limit Setting Ratio vs. Junction Temperature**




$V_{VBUS}$ = 5 V $V_{BAT}$ = 3.8 V

**Figure 10. Charge Current Setting Ratio vs. Junction Temperature**

Copyright © 2017, Texas Instruments Incorporated

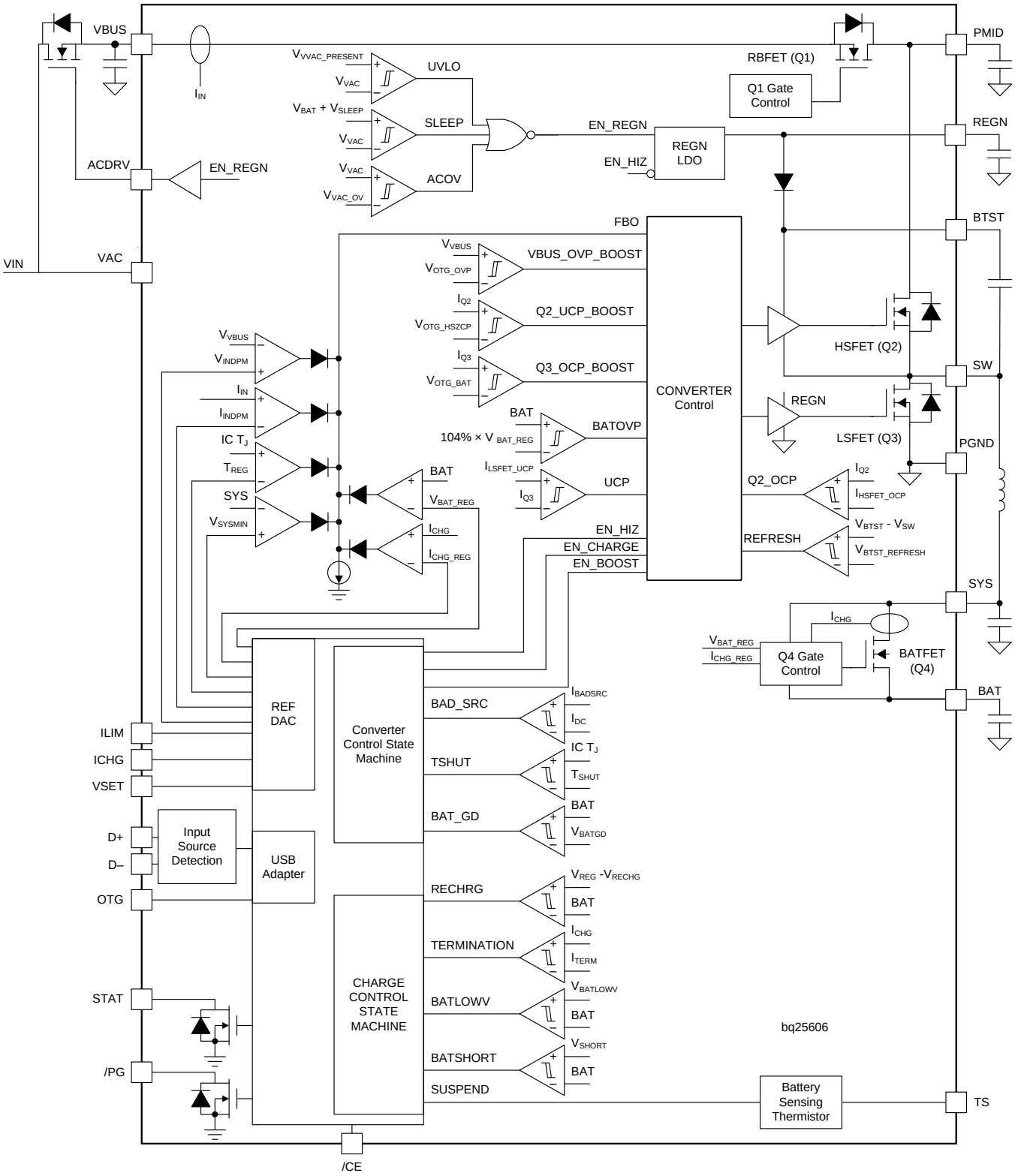
# 8 Detailed Description

## 8.1 Overview

The bq25606 device is a highly integrated 3.0-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.


Copyright © 2017, Texas Instruments Incorporated

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$), the BATFET turns on and connects battery to system. The REGN stays off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (*Supplement Mode*). When the system is overloaded or shorted ($I_{BAT} > I_{BATFET\_OCP}$), the device turns off BATFET immediately until the input source plugs in again.

### 8.3.2 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power Up OVPFET
2. Power Up REGN LDO
3. Poor Source Qualification
4. *IInput Source Type Detection is* based on D+/D– to set input current limit (IINDPM) .
5. Input Voltage Limit Threshold Setting (VINDPM threshold)
6. Converter Power-up

#### *8.3.2.1 Power Up OVPFET*

The external OVPFET provides an additional layer of voltage protection for the device. The external OVPFET is enabled when all the below conditions are valid.

- VAC above $V_{VAC\_PRESENT}$
- VAC below $V_{BAT} + V_{SLEEP}$ in boost mode
- VAC below $V_{VAC\_OV}$
- After $t_{DEB}$ (15ms nom.) delay is completed

If one of the above conditions is not valid, the device is in high impedance state (HIZ) with REGN LDO off. The device draws less current ($I_{VBUS\_HIZ}$) from VBUS during a HIZ state. The battery powers the system when the device is in a HIZ state.

As shown in Figure 11, $V_{VAC\_PRESENT(rising)} < V_{VAC} < V_{VAC\_OV(rising)}$ must be valid before ACDRV goes high.

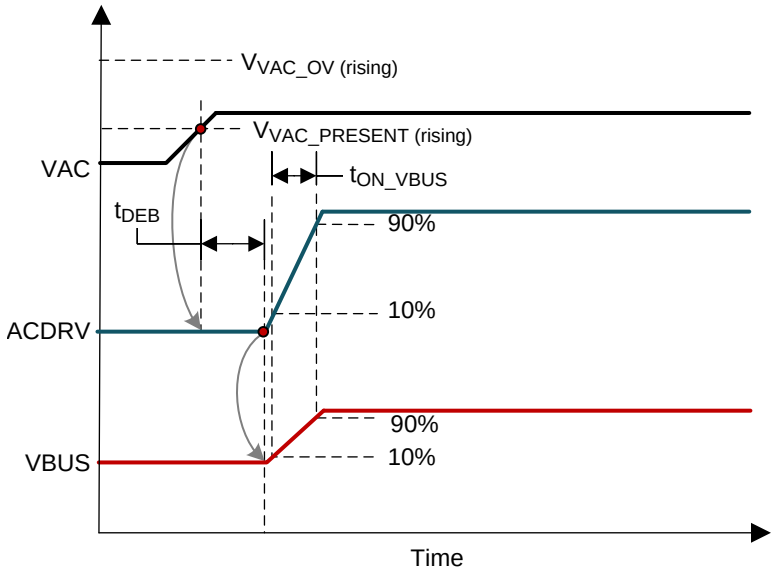



**Figure 11. OVPFET Startup Control**


Copyright © 2017, Texas Instruments Incorporated

## Feature Description (continued)

### 8.3.2.2 Power Up REGN Regulation

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- $V_{VAC}$ above $V_{VAC\_PRESENT}$
- $V_{VAC}$ above $V_{BAT}$ + $V_{SLEEPZ}$ in buck mode or VBUS below $V_{BAT}$ + $V_{SLEEP}$ in boost mode
- After 220-ms delay is completed

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than IVBUS_HIZ from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

### 8.3.2.3 Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

- VAC voltage below $V_{VAC\_OV}$
- VBUS voltage above $V_{VBUSMIN}$ when pulling $I_{BADSRC}$ (typical 30 mA)

If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

### 8.3.2.4 Input Source Type Detection

After the REGN LDO is powered, the device runs input source detection through D+/D– lines. The bq25606 follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/ DCP) and non-standard adapter through USB D+/D– lines. The bq25606 sets input current limit through D+/D- detection and ILIM pins.

#### 8.3.2.4.1 D+/D– detection sets input current limit in limit.bq25606

The bq25606 contains a D+/D– based input source detection to set the input current limit at VBUS plug-in. The D+/D– detection includes standard USB BC1.2 and non-standard adapter. When input source is plugged in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the non-standard adapter detection is applied to set the input current input current limit. The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the D+/D– pins. If an adapter is detected as DCP, the input current limit is 2.4 A. If an adapter is detected as unknown, the input current limit is set by ILIM pin.

**Table 1. Non-Standard Adapter Detection**

| Non-Standard Adapter | D+ Threshold | D– Threshold | Input Current Limit (A) |
|---|---|---|---|
| Divider 1 | $V_{D+}$ within $V_{2P7\_VTH}$ | $V_{D–}$ within $V_{2P0\_VTH}$ | 2.1 |
| Divider 2 | $V_{D+}$ within $V_{1P2\_VTH}$ | $V_{D–}$ within $V_{1P2\_VTH}$ | 2 |
| Divider 3 | $V_{D+}$ within $V_{2P0\_VTH}$ | $V_{D–}$ within $V_{2P7\_VTH}$ | 1 |
| Divider 4 | $V_{D+}$ within $V_{2P7\_VTH}$ | $V_{D–}$ within $V_{2P7\_VTH}$ | 2.4 |

**Table 2. Input Current Limit Setting from D+/D– Detection**

| D+/D– Detection | Input Current Limit (IINLIM) |
|---|---|
| USB SDP (USB500) | 500 mA |
| USB DCP | 2.4 A |
| Divider 3 | 1 A |
| Divider 1 | 2.1 A |
| Divider 4 | 2.4 A |
| Divider 2 | 2 A |
| Unknown 5-V Adapter | Set by ILIM pin |

Copyright © 2017, Texas Instruments Incorporated

#### 8.3.2.5 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device's VINDPM is set at 4.3V. The device supports dynamic VINDPM tracking which tracks the battery voltage. The device's VINDPM tracks battery voltage with 200mV offset such that when VBAT + 200mV is greater than 4.3V, the VINDPM value is automatically adjusted to VBAT + 200mV.

#### 8.3.2.6 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current is limited to is to 200 mA. After the system rises above 2.2 V, the device limits input current to the value set by ILIM pin.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to PFM control at light load or when battery is below minimum system voltage setting or charging is disabled.

### 8.3.3 Boost Mode Operation From Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The maximum output current is up to 1.2 A. The boost operation can be enabled if the conditions are valid:

1. BAT above $V_{OTG\_BAT}$
2. VBUS less than BAT+$V_{SLEEP}$ (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH)
4. Voltage at TS (thermistor) pin is within acceptable range ($V_{BHOT} < V_{TS} < V_{BCOLD}$)
5. After 30-ms delay from boost mode enable

During boost mode, the VBUS output is 5.15 V and the output current can reach up to 1.2 A. The boost output is maintained when BAT is above $V_{OTG\_BAT}$ threshold.

When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot.

### 8.3.4 Standalone Power Management

### 8.3.5 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

### 8.3.6 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3.0-A charge current for high capacity tablet battery. The 19.5-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

#### 8.3.6.1 Autonomous Charging Cycle

With battery charging is enabled ($\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle. The device default charging parameters are listed in Table 3.

**Table 3. Charging Parameter Default Setting**

| Default Mode | bq25606 |
|---|---|
| Charging voltage | VSET controlled |
| Charging current | $I_{CHG}$ controlled |
| Pre-charge current | 5% of ICHG |
| Termination current | 5% of ICHG |


Copyright © 2017, Texas Instruments Incorporated

**Table 3. Charging Parameter Default Setting (continued)**

| Default Mode | bq25606 |
|---|---|
| Temperature profile | JEITA |
| Safety timer | 10 hours |

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled ($\overline{CE}$ is low)
- No thermistor fault on TS
- No safety timer fault

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold , the device automatically starts a new charging cycle. After the charge is done, toggle $\overline{CE}$ pin can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking).

#### *8.3.6.2 Charging Termination*

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage *Supplement Mode*.

#### *8.3.6.3 Thermistor Qualification*

The charger device provides a single thermistor input for battery temperature monitor.

#### *8.3.6.4 JEITA Guideline Compliance During Charging Mode*

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), the charge current is reduced to 20% of programmed fast charge current. At warm temperature (T3-T5), the charge voltage is reduced to 4.1 V.

1The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VREG or 4.1V (configured by JEITA_VSET). The current setting at cool temperature (T1-T2) can be further reduced to 20% of fast charge current (JEITA_ISET).

Copyright © 2017, Texas Instruments Incorporated

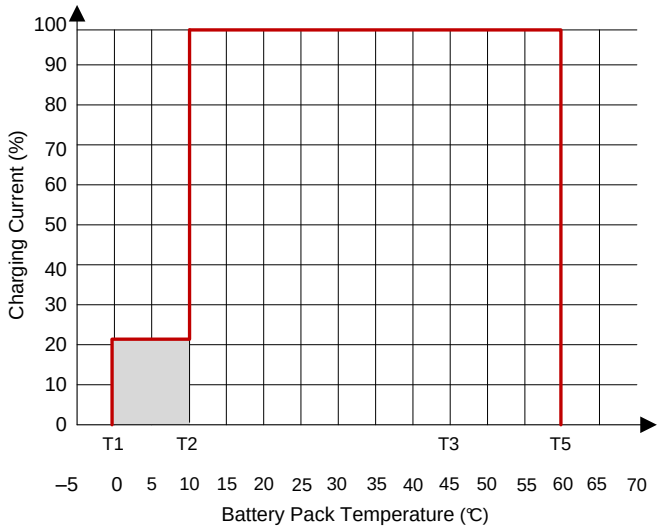



**Figure 12. JEITA Profile: Charging Current**

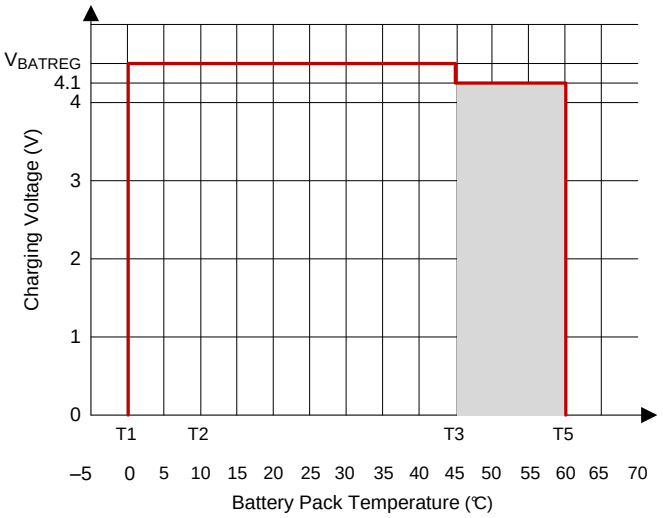



**Figure 13. JEITA Profile: Charging Voltage**

Equation 1 through Equation 2 describe updates to the resistor bias network.

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{VT1} - 1\right)} \quad (1)$$

$$RT1 = \frac{\left(\left(\frac{V_{REGN}}{VT1}\right) - 1\right)}{\left(\frac{1}{RT2}\right) + \left(\frac{1}{RTH_{COLD}}\right)} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

- $RTH_{COLD}$ = 27.28 KΩ
- $RTH_{HOT}$ = 3.02 KΩ
- RT1 = 5.23 KΩ
- RT2 = 30.9 KΩ

### 8.3.6.5 Boost Mode Thermistor Monitor during Battery Discharge Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the VBCOLD to VBHOTthresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended.

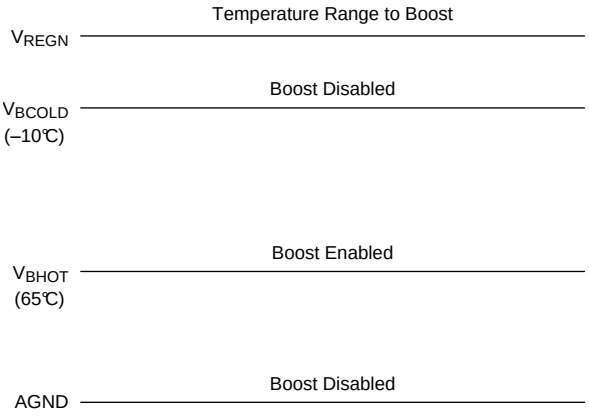



**Figure 14. TS Pin Thermistor Sense Threshold in Boost Mode**


Copyright © 2017, Texas Instruments Incorporated

### 8.3.6.6 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below $V_{BATLOWV}$ threshold and 10 hours when the battery is higher than $V_{BATLOWV}$ threshold.

During input voltage, current, JEITA cool or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation throughout the whole charging cycle, the safety timer will expire in 20 hours.

During the fault, timer is suspended. Once the fault goes away, fault resumes. If user stops the current charging cycle, and start again, timer gets reset.

### 8.3.6.7 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_Min bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the VDS of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage..

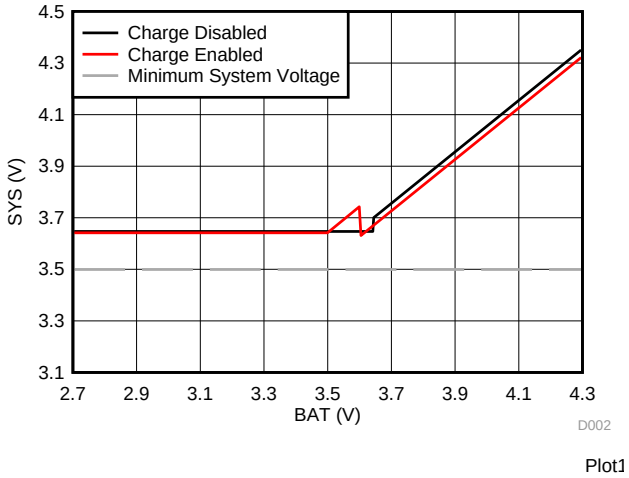



**Figure 15. System Voltage vs Battery Voltage**

### 8.3.6.8 Dynamic Power management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IIDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

Figure 16 shows the DPM response with 9-V/1.2-A adapter, 3.2-V battery, 2.8-A charge current and 3.5-V minimum system voltage setting.

Copyright © 2017, Texas Instruments Incorporated

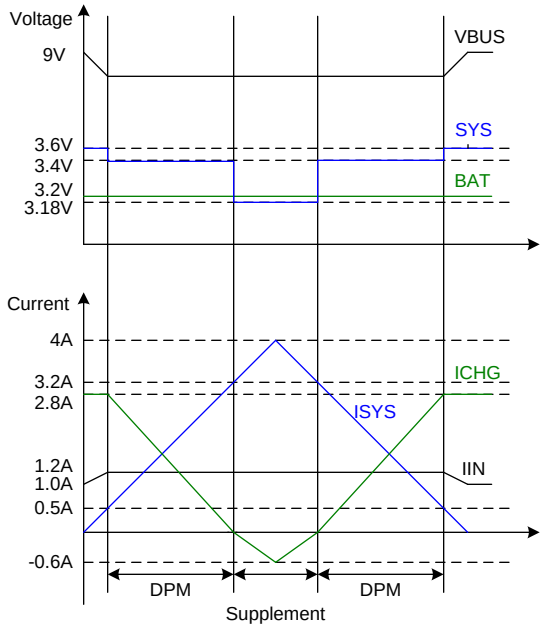



**Figure 16. DPM Response**

### *8.3.6.9 Supplement Mode*

When the system voltage falls 180 mV (VBAT > VSYSMin) or 45 mV (VBAT < VSYSMin) below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce RDSON until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. Figure 17 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

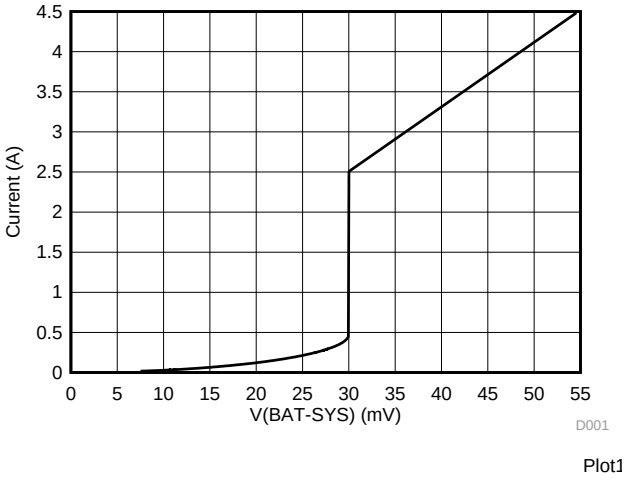



**Figure 17. BAFET V-I Curve**

## 8.3.7 Status Outputs ($\overline{PG}$, STAT)

### *8.3.7.1 Power Good indicator ($\overline{PG}$ Pin)*

The $\overline{PG}$ pin goes LOW to indicate a good input source when:


Copyright © 2017, Texas Instruments Incorporated

- VBUS above $V_{VBUS\_UVLO}$
- VBUS above battery (not in sleep)
- VBUS below $V_{VAC\_OV}$ threshold
- VBUS above $V_{VBUSMin}$ (typical 3.8 V) when $I_{BADSRC}$ (typical 30 mA) current is applied (not a poor source)
- Completed *input Source Type Detection*

#### *8.3.7.2 Charging Status indicator (STAT)*

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED.

**Table 4. STAT Pin State**

| CHARGING STATE | STAT INDICATOR |
|---|---|
| Charging in progress (including recharge) | LOW |
| Charging complete | HIGH |
| Sleep mode, charge disable | HIGH |
| Charge suspend (input overvoltage, TS fault, timer fault or system overvoltage)<br>Boost Mode suspend (due to TS fault) | Blinking at 1 Hz |

### 8.3.8 Protections

#### *8.3.8.1 Input Current Limit*

The device's ILIM pin is to program maximum input current when D+/D- detection identifies an unknown adaptor plugged in. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

#### *8.3.8.2 Voltage and Current Monitoring in Converter Operation*

The device closely monitors the input and system voltage, as well as internal FET currents for safe buck and boost mode operation.

##### 8.3.8.2.1 Voltage and Current Monitoring in Buck Mode

###### *8.3.8.2.1.1 Input Overvoltage (ACOV)*

If VAC exceeds $V_{VAC\_OV}$ , the OVPFET turns off in 200ns to protect VBUS. In the meantiem, HSFET stops switching immediately.

###### *8.3.8.2.1.2 System Overvoltage Protection (SYSOVP)*

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above minimum system regulation voltage when the system is regulate at $V_{SYSMIN}$. Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger provides 30 mA discharge current to bring down the system voltage.

#### *8.3.8.3 Voltage and Current Monitoring in Boost Mode*

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

##### 8.3.8.3.1 VBUS Soft Start

When the boost function is enabled, the device soft-starts boost mode to avoid inrush current.

##### 8.3.8.3.2 VBUS Output Protection

The device monitors boost output voltage and other conditions to provide output short circuit and overvoltage protection. The Boost build in accurate constant current regulation to allow OTG to adaptive to various types of load. If short circuit is detected on VBUS, the Boost turns off and retry 7 times. If retries are not successful, OTG is disabled.

Copyright © 2017, Texas Instruments Incorporated

#### 8.3.8.3.3 Boost Mode Overvoltage Protection

When the VBUS voltage rises above regulation target and exceeds VOTG_OVP, the device stop switching.

### *8.3.8.4 Thermal Regulation and Thermal Shutdown*

#### 8.3.8.4.1 Thermal Protection in Buck Mode

The bq25606 monitors the internal junction temperature $T_J$ to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate.

#### 8.3.8.4.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds $T_{SHUT}$ (160ºC), the boost mode is disabled and BATFET is turned off. When IC junction temperature is below $T_{SHUT}$(160ºC) - $T_{SHUT\_HYS}$ (30ºC), the BATFET is enabled automatically to allow system to restore .

### *8.3.8.5 Battery Protection*

#### 8.3.8.5.1 Battery overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging.

#### 8.3.8.5.2 Battery Over-Discharge Protection

When battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge latch-off, an input source plug-in is required at VBUS. The battery is charged with $I_{SHORT}$ (typically 100 mA) current when the VBAT < VSHORT, or precharge current as set by 5% of ICHG when the battery voltage is between $V_{SHORTZ}$ and $V_{BAT\_LOWV}$.

#### 8.3.8.5.3 System Over-Current Protection

When the system is shorted or significantly overloaded (IBAT > IBATOP) and the current exceeds BATFET overcurrent limit, the BATFET latches off. The BATFET latch can be reset with VBUS plug-in.

## 9 Application and Implementation

**NOTE**

information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application information

A typical application consists of the device configured as a stand-alone power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

External OVPFET is optional. When external OVP is not used, short the VBUS and VAC pins and allow ACDRV pin to float (as shown in Figure 19)


Copyright © 2017, Texas Instruments Incorporated

## 9.2 Typical Application Diagram

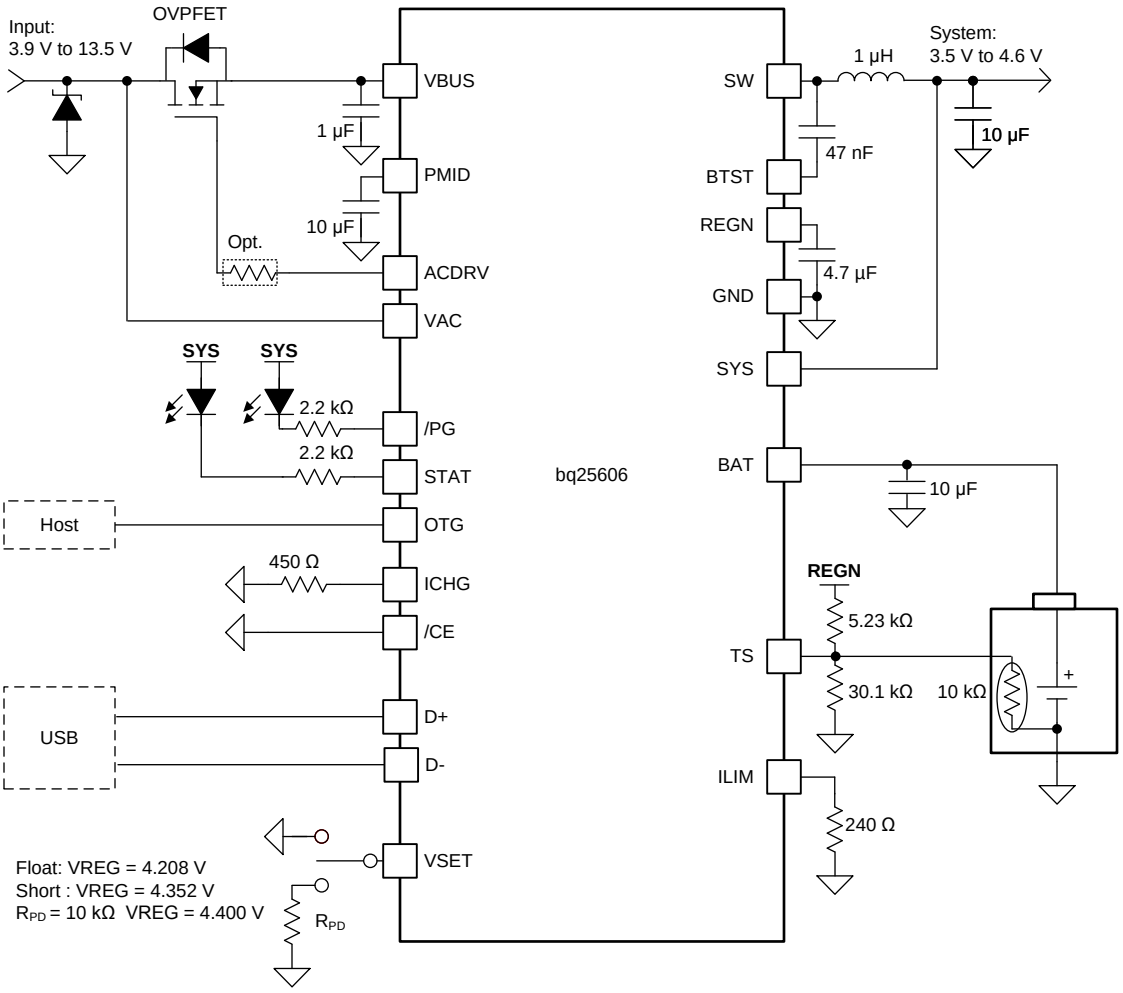



**Figure 18. bq25606 Application With OVPFET**

## Typical Application Diagram (continued)

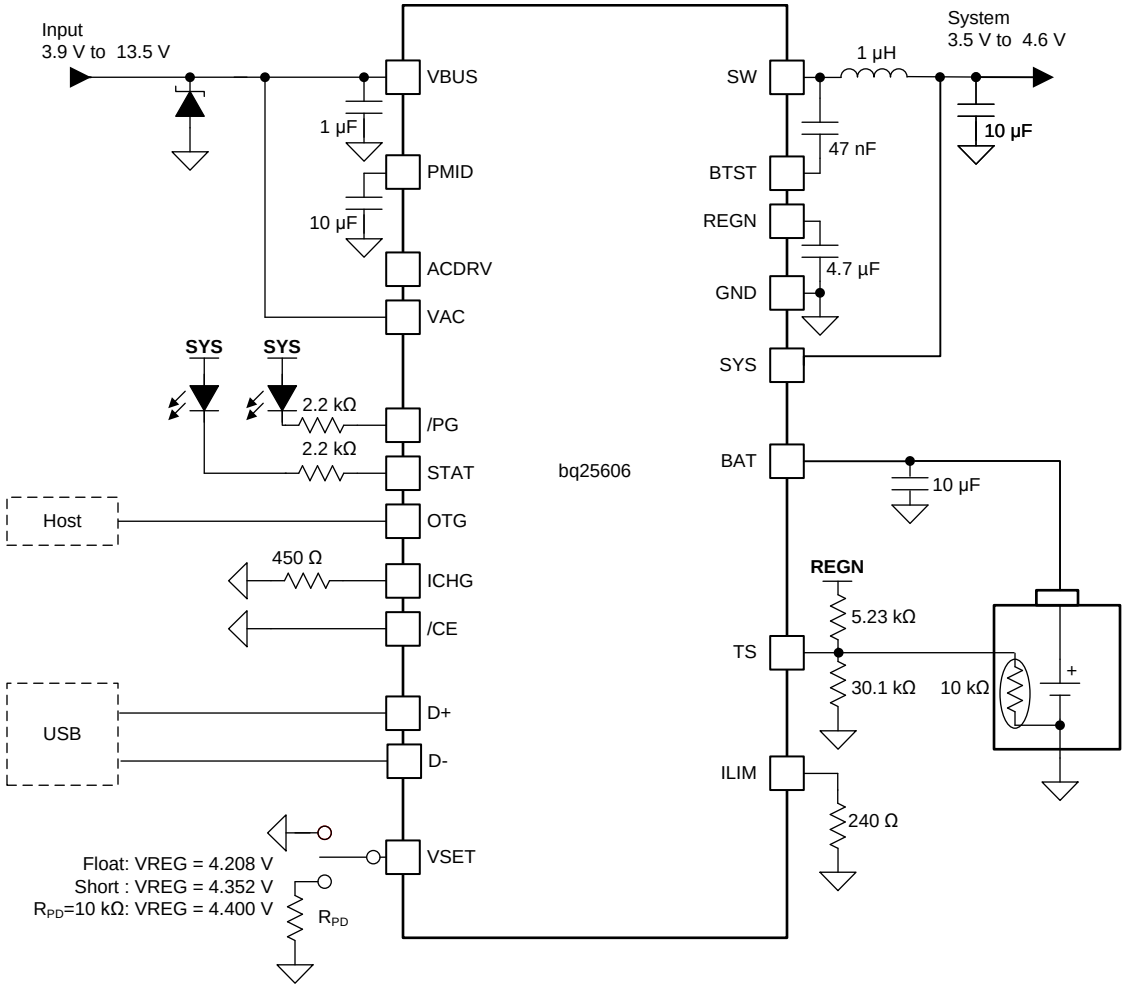



**Figure 19. bq25606 Application Without OVPFET**

### 9.2.1 Design Requirements

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 inductor Selection*

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current ($I_{CHG}$) plus half the ripple current ($I_{RIPPLE}$):

$$I_{SAT} \geq I_{CHG} + (1/2)\ I_{RIPPLE} \quad (4)$$

The inductor ripple current depends on the input voltage ($V_{VBUS}$), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency ($f_S$) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \quad (5)$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.


Copyright © 2017, Texas Instruments Incorporated

## Typical Application Diagram (continued)

### 9.2.2.2 input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current $I_{Cin}$ occurs where the duty cycle is closest to 50% and can be estimated using Equation 6.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (6)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15 V input voltage. Capacitance of 22-μF is suggested for typical of 3A charging current.

### 9.2.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. Equation 7 shows the output capacitor RMS current $I_{COUT}$ calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (7)$$

The output capacitor voltage ripple can be calculated as follows:

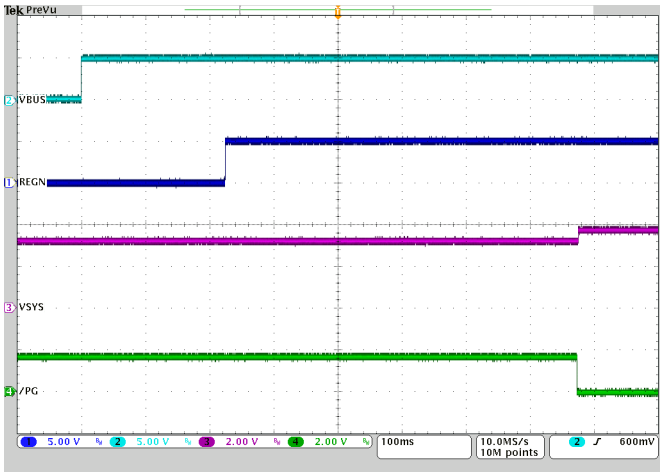
$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation optimized for >20μF ceramic output capacitance. The preferred ceramic capacitor is 10V rating, X7R or X5R.

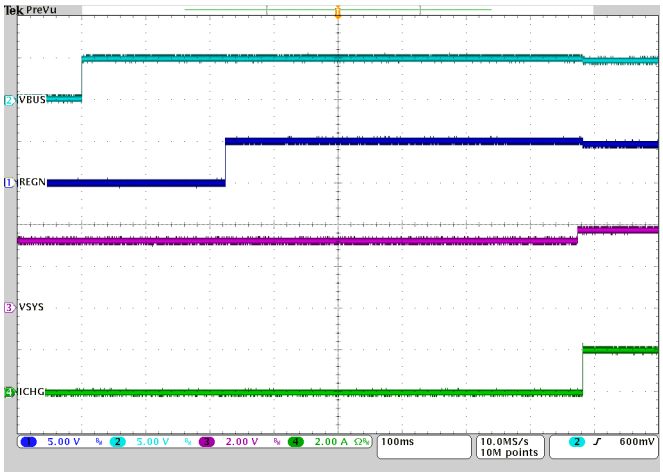
Copyright © 2017, Texas Instruments Incorporated

## 9.3 Application Curves



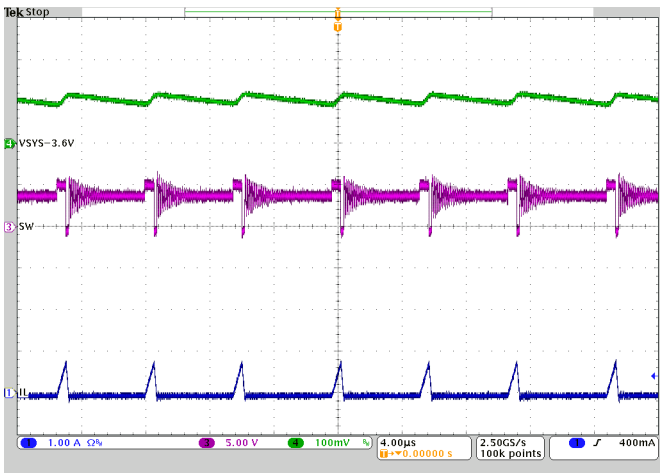

$V_{VBUS}$ = 5 V $V_{VBAT}$ = 3.2 V

**Figure 20. Power-Up with Charge Disabled**



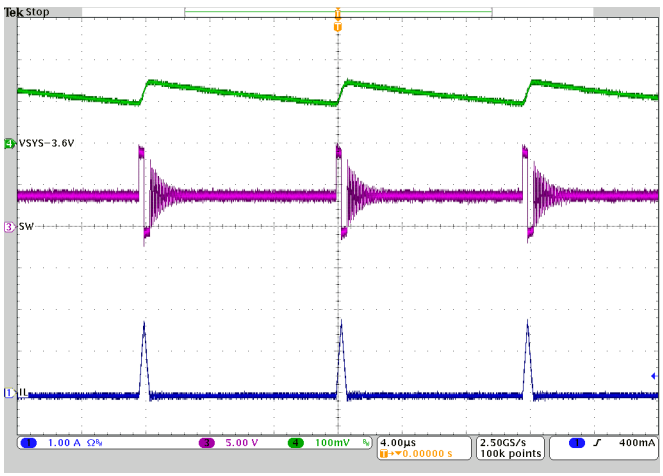

$V_{VBUS}$ = 5 V $V_{VBAT}$ = 3.2 V
$I_{CHG}$ = 2 A

**Figure 21. Power-Up with Charge Enabled**




$V_{VBUS}$ = 5 V
$I_{SYS}$ = 50 mA Charge Disabled

**Figure 22. PFM Switching in Buck Mode**

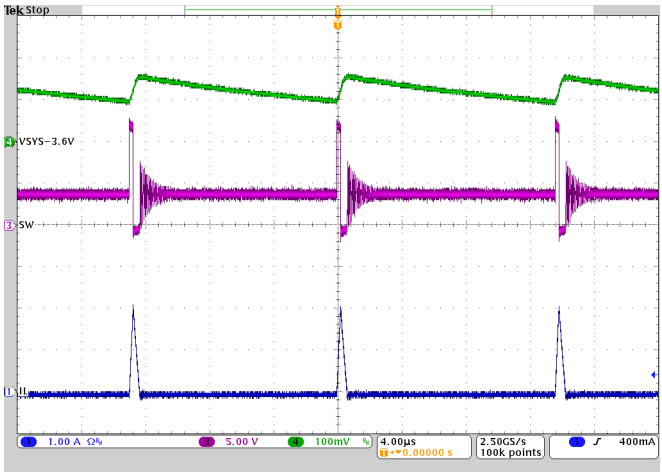



$V_{VBUS}$ = 9 V
$I_{SYS}$ = 50 mA Charge Disabled

**Figure 23. PFM Switching in Buck Mode**

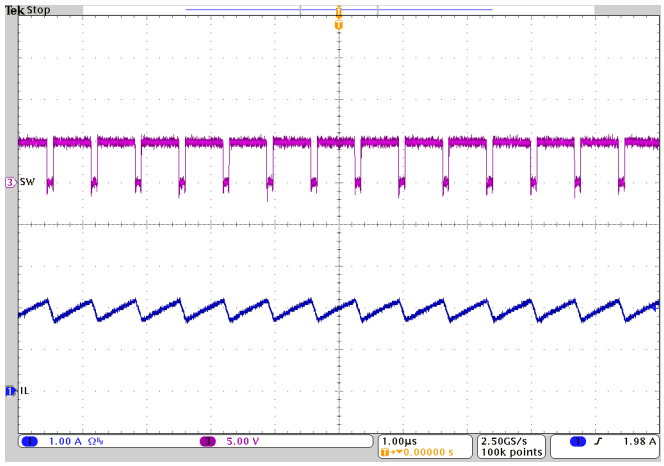

Copyright © 2017, Texas Instruments Incorporated

## Application Curves (continued)



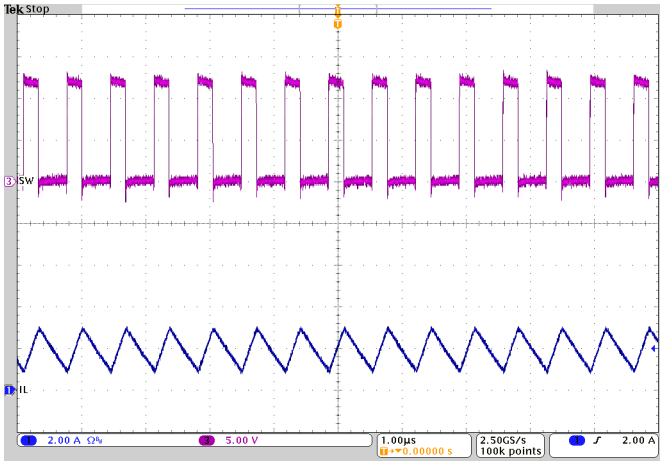

$V_{VBUS}$ = 12 V
$I_{SYS}$ = 50 mA
Charge Disabled

**Figure 24. PFM Switching in Buck Mode**



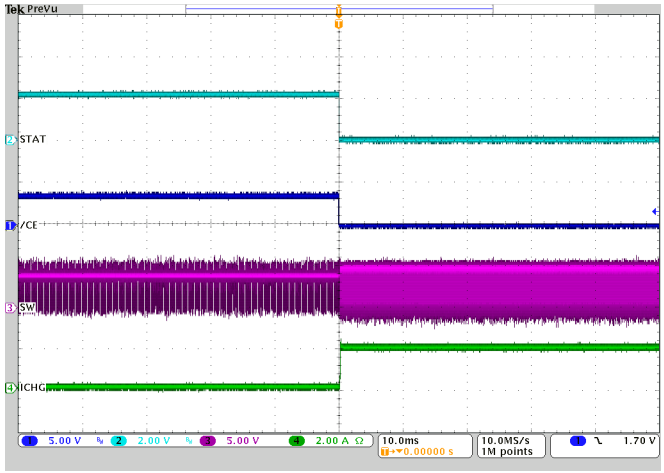

$V_{VBUS}$ = 5 V
$I_{CHG}$ = 2 A
$V_{VBAT}$ = 3.8 V

**Figure 25. PWM Switching in Buck Mode**




$V_{VBUS}$ = 12 V
$I_{CHG}$ = 2 A
$V_{VBAT}$ = 3.8 V

**Figure 26. PWM Switching in Buck mode**

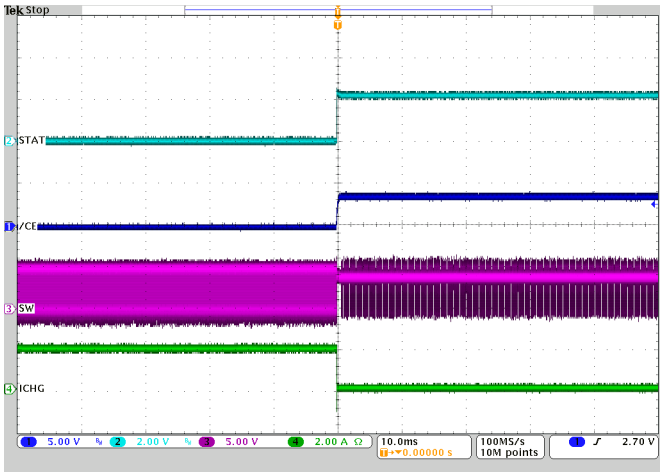



$V_{VBUS}$ = 5 V
$I_{CHG}$ = 2 A
$V_{VBAT}$ = 3.2 V

**Figure 27. Charge Enable**

Copyright © 2017, Texas Instruments Incorporated

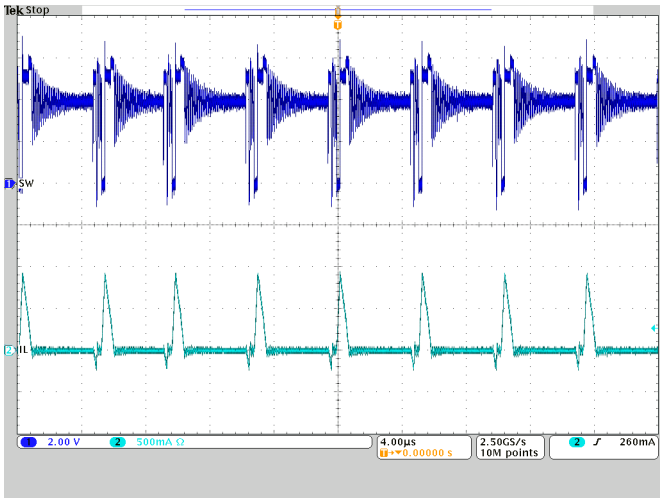
## Application Curves (continued)




$V_{VBUS}$ = 5 V $V_{VBAT}$ = 3.2 V

$I_{CHG}$ = 2 A

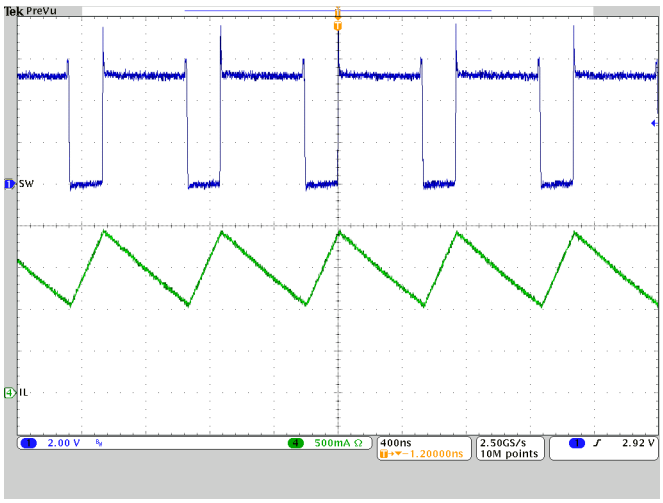
**Figure 28. Charge Disable**




$V_{VBAT}$ = 4 V

$I_{LOAD}$= 50 mA PFM Enabled

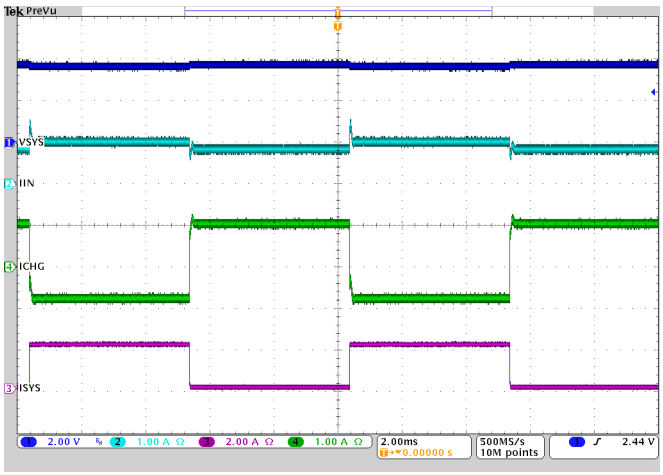
**Figure 29. OTG Switching**




$V_{VBAT}$ = 4 V

$I_{LOAD}$= 1 A PFM Enabled

**Figure 30. OTG Switching**




$V_{VBUS}$ = 5 V $I_{INDPM}$ = 1 A

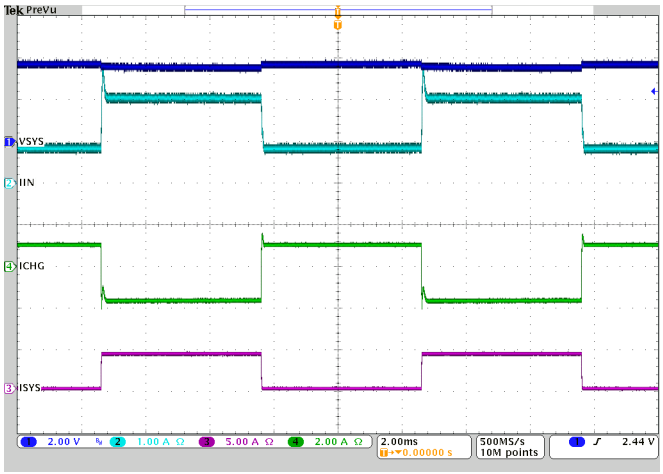
$I_{SYS}$ from 0 A to 2 A $I_{CHG}$ = 1 A

$V_{BAT}$ = 3.7 V

**Figure 31. System Load Transient**

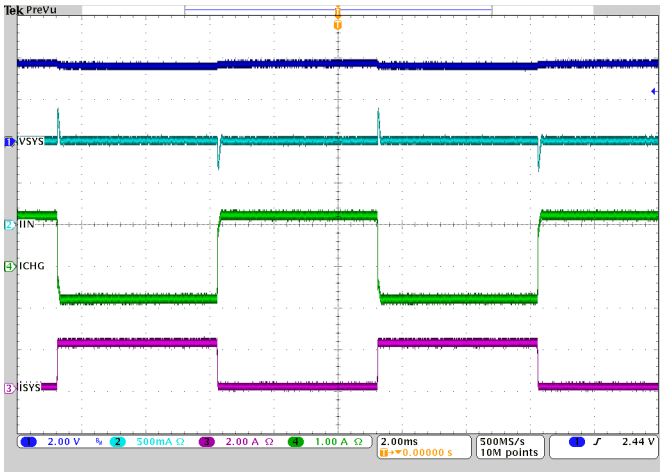

Copyright © 2017, Texas Instruments Incorporated

## Application Curves (continued)



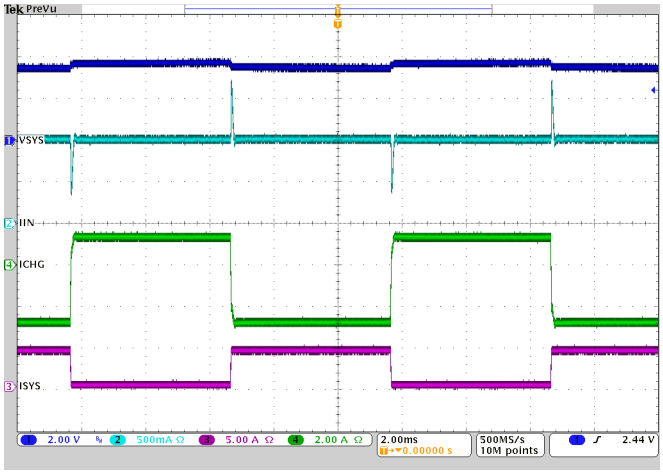

$V_{VBUS}$ = 5 V
$I_{SYS}$ from 0 A to 4 A
$V_{BAT}$ = 3.7 V
$I_{INDPM}$ = 2 A
$I_{CHG}$ = 1 A

**Figure 32. System Load Transient**



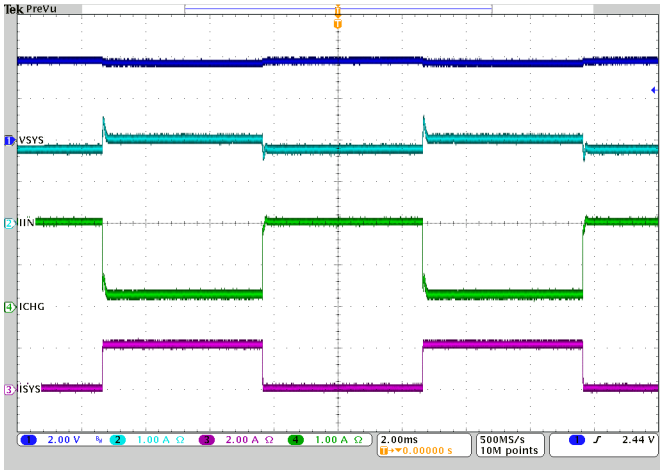

$V_{VBUS}$ = 5 V
$I_{SYS}$ from 0 A to 2 A
$V_{BAT}$ = 3.7 V
$I_{INDPM}$ = 1 A
$I_{CHG}$ = 2 A

**Figure 33. System Load Transient**




$V_{VBUS}$ = 5 V
$I_{SYS}$ from 0 A to 4 A
$V_{BAT}$ = 3.7 V
$I_{INDPM}$ = 1 A
$I_{CHG}$ = 2 A

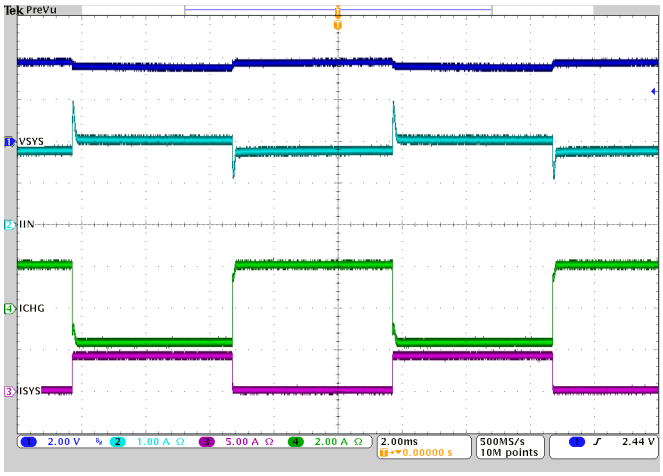
**Figure 34. System Load Transient**




$V_{VBUS}$ = 5 V
$I_{SYS}$ from 0 A to 2 A
$V_{BAT}$ = 3.7 V
$I_{INDPM}$ = 2 A
$I_{CHG}$ = 2 A

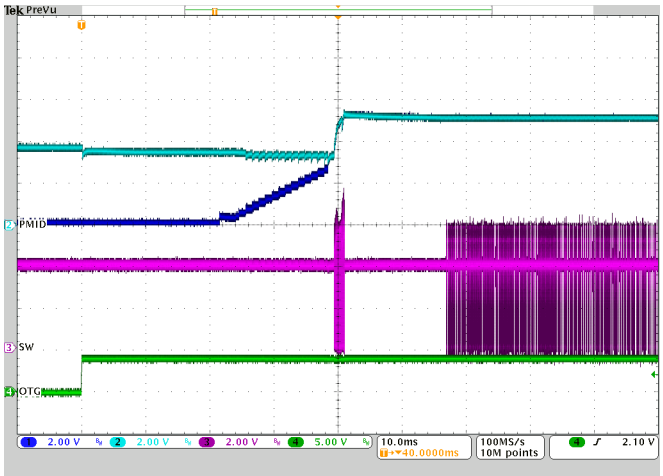
**Figure 35. System Load Transient**

## Application Curves (continued)




$V_{VBUS}$ = 5 V
$I_{SYS}$ from 0 A to 4 A
$V_{BAT}$ = 3.7 V
$I_{INDPM}$ = 2 A
$I_{CHG}$ = 2 A

**Figure 36. System Load Transient**




$V_{BAT}$ = 3.8 V
$C_{LOAD}$ = 470 µF

**Figure 37. OTG Start-Up**


Copyright © 2017, Texas Instruments Incorporated

## 10 Power Supply Recommendations

in order to provide an output voltage on SYS, the bq25606 device requires a power supply between 3.9 V and 14.2 V input with at least 100-mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

Copyright © 2017, Texas Instruments Incorporated

# 11 Layout

## 11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 38) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.

See the EVM user's guide SLUUBL3 for the recommended component placement with trace and via locations. For the VQFN information, refer to SCBA017 and SLUA271.

## 11.2 Layout Example

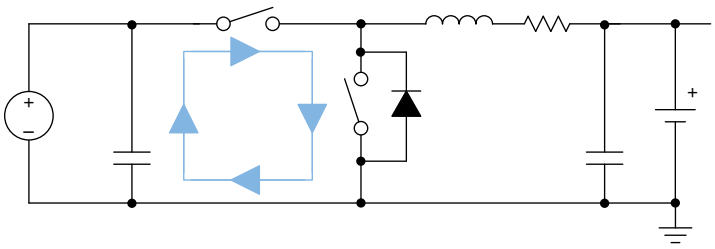


**Figure 38. High Frequency Current Path**


Copyright © 2017, Texas Instruments Incorporated

## Layout Example (continued)

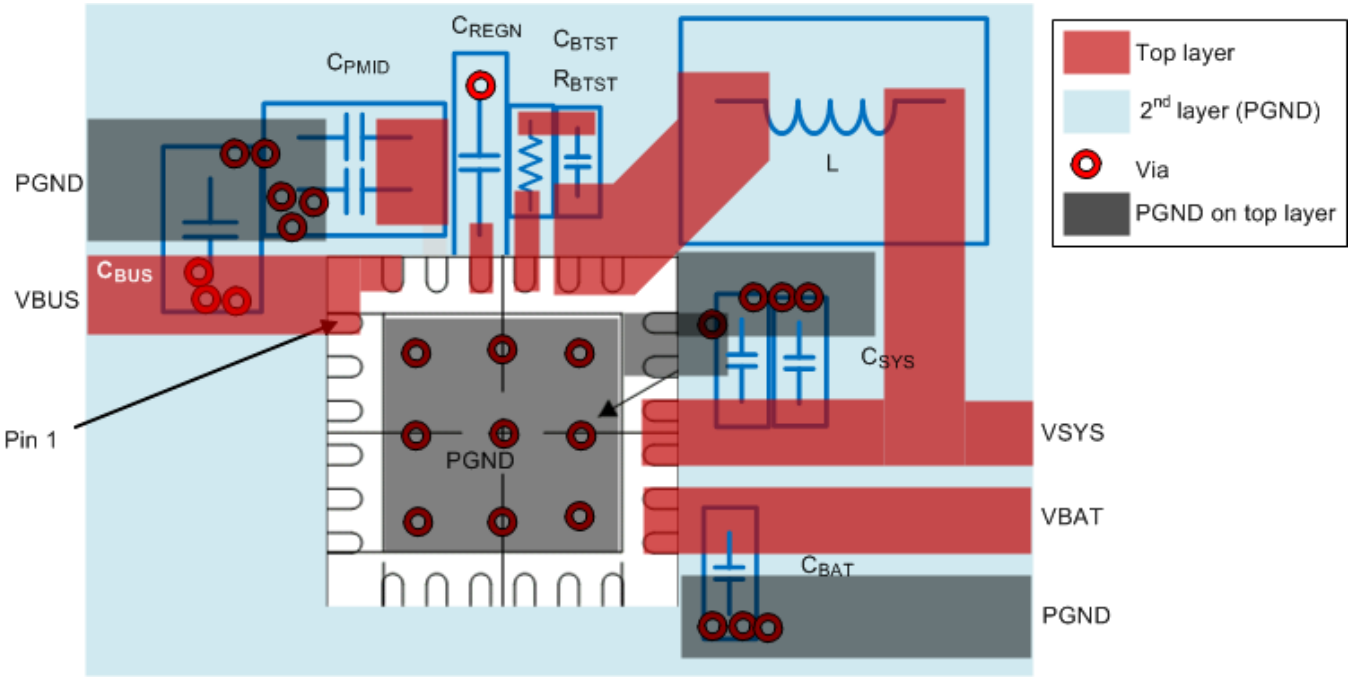



**Figure 39. Layout Example**

# 12 Device and Documentation Support

## 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.2 Trademarks

E2E is a trademark of Texas Instruments.

## 12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.


Copyright © 2017, Texas Instruments Incorporated

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2017, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ25606RGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ25606 | Samples |
| BQ25606RGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ25606 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

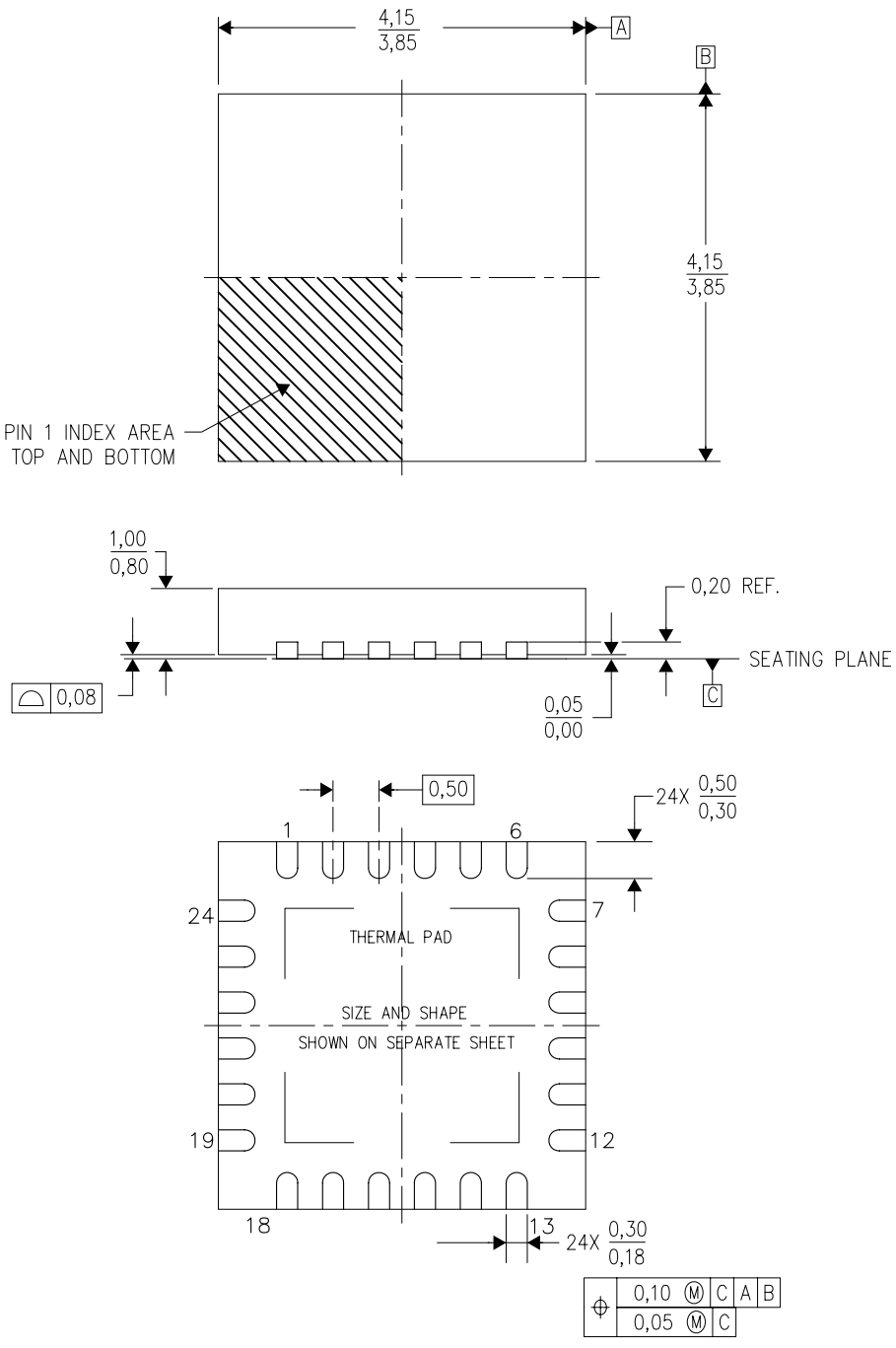
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

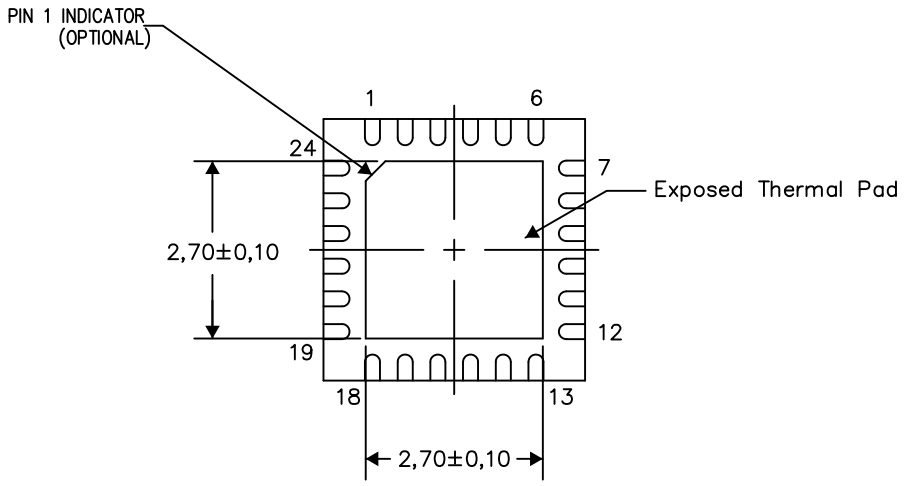
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



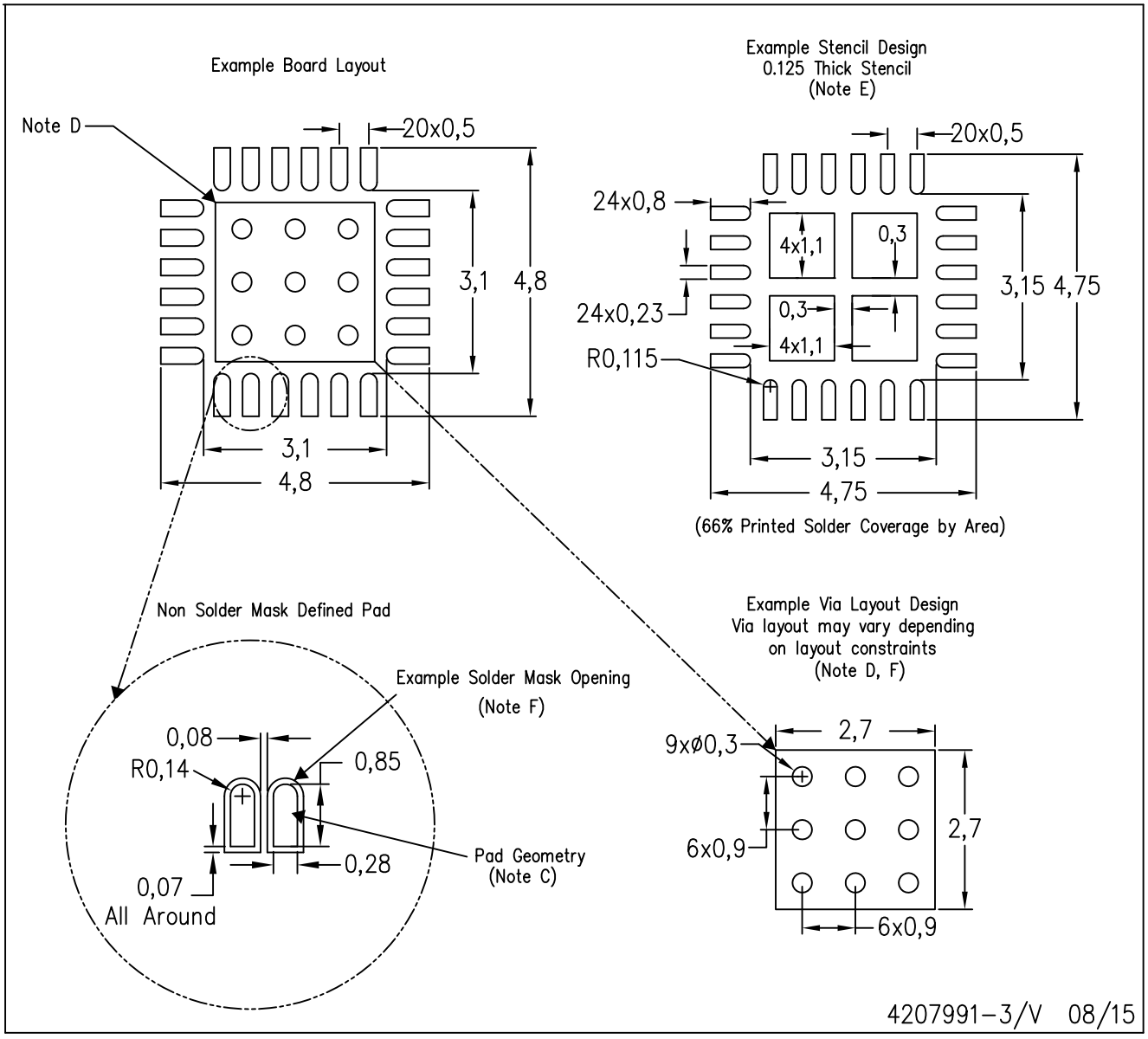

Bottom View

Exposed Thermal Pad Dimensions

4206344–5/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated