# BGT60TR13C

## 60 GHz Radar Sensor

## Datasheet V2.4.6

### Features

- 60 GHz radar sensor for FMCW operation
- 5.5 GHz bandwidth
- Antenna-in-package (6.5 x 5.0 x 0.9 $mm^3$)
- Digital interface for chip configuration and radar data acquistion
- Optimized power modes for low-power operation
- Integrated state machine for independent operation

### Potential applications

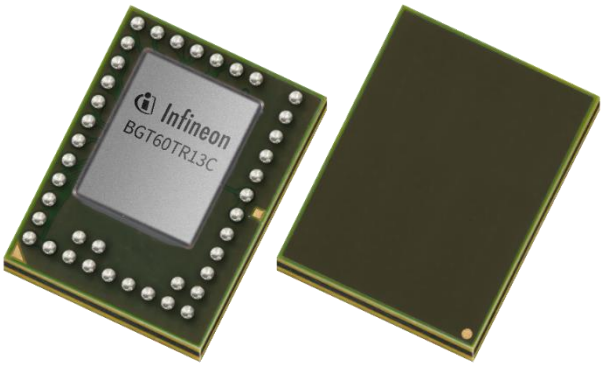
- Radar frontend for gesture sensing
- High resolution FMCW radars
- Short range sensing operations
- Hidden sensing applications behind radome

### Product validation

Packaged device qualified according to JEDEC 20/22.

### Description

The BGT60TR13C, a 60 GHz radar sensor with antenna in package, enables ultra-wide bandwidth FMCW operation in a small package. Sensor configuration and data acquisition are enabled with a digital interface and the integrated state machine enables independent data acquisition with power mode optimization for lowest power consumption.



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# 1 Introduction

New smart sensors for gesture recognition can be based on radar systems, in special case, FMCW radars. Those systems can comprise several blocks: Radio Frequency (RF) front-end, Analog Base Band (ABB), Analog to Digital Converter (ADC), Phase Locked Loop (PLL), memory (FIFO e.g.), Serial Peripheral Interface (SPI) and Antennas. Smart sensors require a high level of integration, thus, the components listed above should be integrated in a single chip solution. BGT60TR13C offers this level of integration in a single chipset.

## 1.1 Product Overview

The core functionality of BGT60TR13C is to transmit frequency modulated continuous wave (FMCW) signal via one of the transmitter channel (TX) and receive the echo signals from the target object on the three receiving channels (RX). Each receiver path includes a baseband filtering, a VGA, as well as an ADC. The digitized output is stored in a FIFO. The data are transferred to an external host, microcontroller unit (MCU) or application processor (AP), to run radar signal processing. A typical implementation of a sensor system consists of two main blocks only (see Figure 1):

- BGT60TR13C handles the RF signals and provides the sampled IF signals
- Application Processor which captures and processes the radar signals

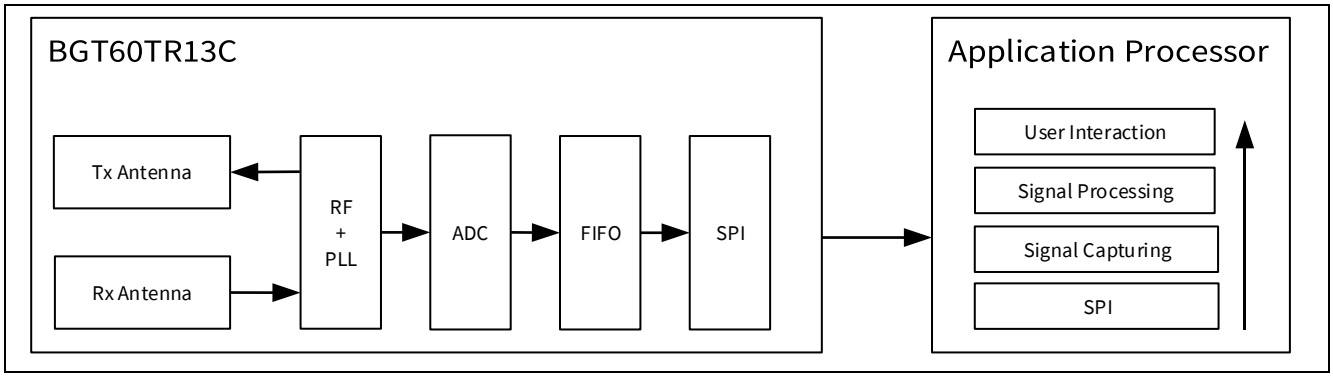


**Figure 1 Data flow in the complete radar sensor system**

## 1.2 Potential Applications

The chipset has been designed to address mainly the following potential applications:

- Radar frontend for gesture sensing
- High resolution FMCW radars
- Short range sensing operations
- Hidden sensing applications behind radome

# Introduction

## 1.3 BGT60TR13C Bare Die Block Diagram

BGT60TR13C block diagram is presented in Figure 2.

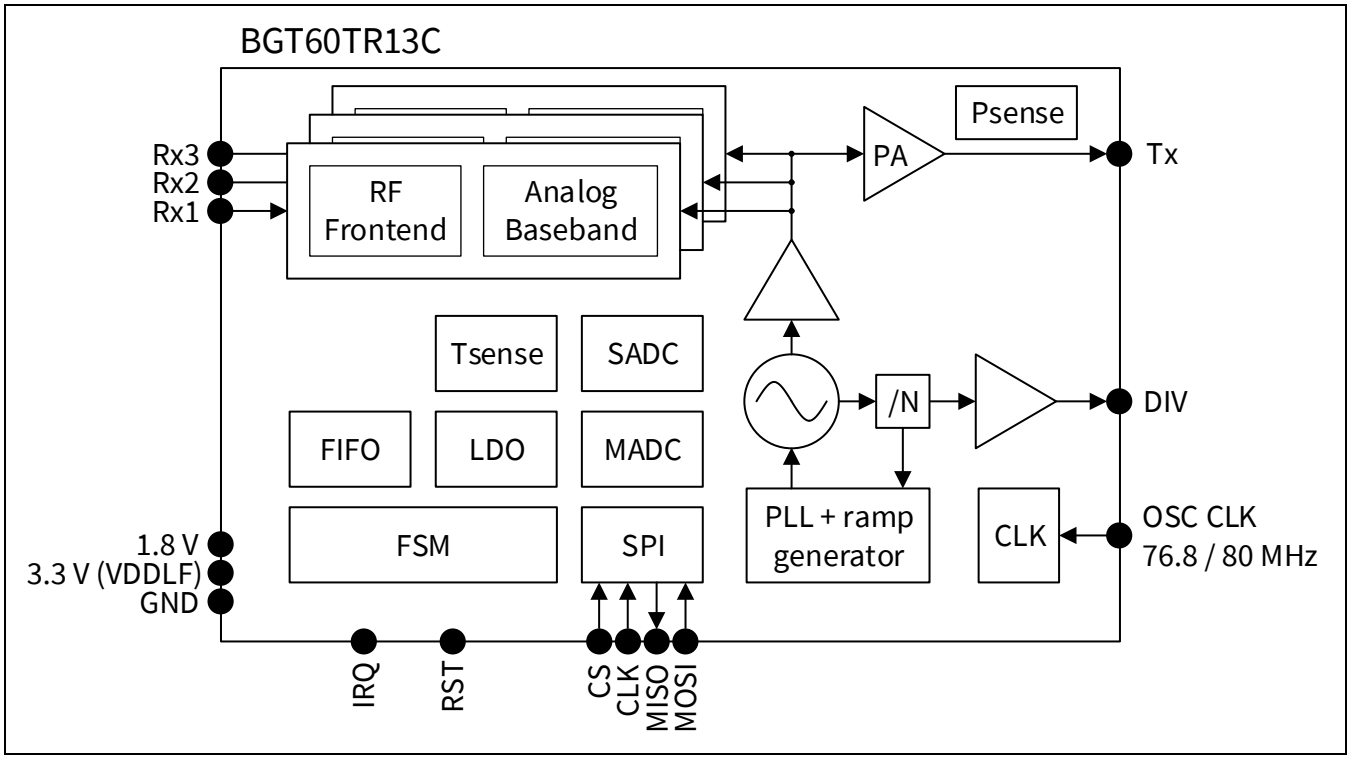


**Figure 2 BGT60TR13C Bare die block diagram**

**Feature List:**

- Single supply voltage level of 1.8 V for both, digital and analog domains
- Integrated LDOs from 1.8 V to 1.5 V to supply the digital domain
- RF-Frontend at 60 GHz covering frequencies from 58.0 to 63.5 GHz with one TX and three RX channels
- Baseband chain consisting of high pass filter, low noise voltage gain amplifier (VGA), and antialiasing filters
- Three ADC channels with 12 bits resolution and up to 4 MSps sampling rate to sample the RX-IF channels
- Integrated RF-PLL, timers, counters, and FSM to run set of frames in standalone mode (no communication with AP required except first trigger and raw data transfer)
- Full duplex FIFO structure as data buffer ( 196 kbit = 8192 words x 24 bits )
- Linear Feedback Shift Register (LFSR) test pattern generator on chip for data transfer check
- 8 to 10 bits sensor ADC for power and temperature measurement
- Standard SPI mode for configuration and status register read accesses
- Dedicated power modes for power reduction
- An external 80 MHz reference oscillator is used as a system clock source
- BITE (Built in test equipment) for EOL test in production at Infineon to verify RF performance
- Fabricated with BiCMOS Infineon process technology
- Housed in a laminate package
- Antennas integrated in the redistribution layers of the package

# Introduction

## 1.4 BGT60TR13C Pin Definition and Function

The following Figure 3 shows the bottom view of BGT60TR13C laminate package with the pin and antenna number assignment.

The function of each pin is described in Table 1 (See also Table 2 andTable 3).

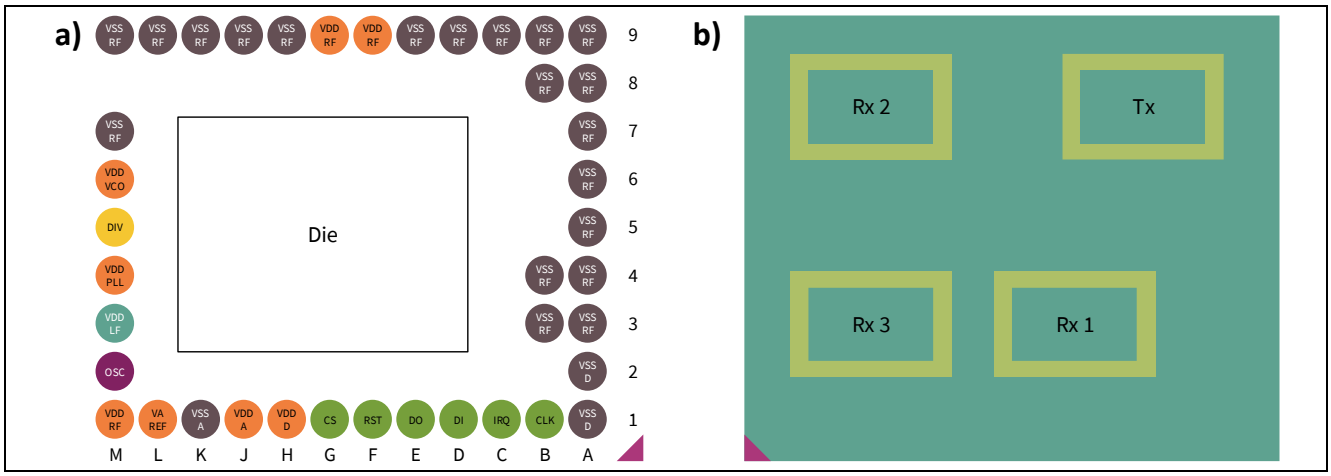


**Figure 3 BGT60TR13C pin out in bottom view (a) and antenna numbers assignment in top view (b)**

**Table 1 Ball and Antenna Definition**

| **Ball** | **Function** |
|---|---|
| A1, A2 | VSSD |
| B1 | CLK |
| C1 | IRQ |
| D1 | DI |
| E1 | DO |
| F1 | DIO3 |
| G1 | CS_N |
| H1 | VDDD |
| J1 | VDDA |
| K1 | VSSA |
| L1 | VAREF |
| M1, F9, G9 | VDDRF |
| M2 | OSC_CLK |
| M3 | VDDLF |
| M4 | VDDPLL |
| M5 | DIV_TEST |
| M6 | VDDVCO |
| M7, M9, L9, K9, J9, H9, E9, D9, C9, B9, B8, A9, A8, A7, A6, A5, B4, A4, B3, A3 | VSSRF |
| **Antenna** | **Function** |
| Tx1 | Transmitter |
| Rx1 | Receiver ch1 |
| Rx2 | Receiver ch2 |

**Table 1 Ball and Antenna Definition**

| Ball | Function |
|---|---|
| Rx3 | Receiver ch3 |

### 1.4.1 IO and Supply Pins

The following Table 2 gives an overview on the input/output pins of BGT60TR13C.

**Table 2 BGT60TR13C Input/Output Pins**

| Symbol | Type | Domain | Description | Domain |
|---|---|---|---|---|
| DIV_TEST | $A_{OUT}$ | VDDRF | VCO divided by 16 output | Analog-RF |
| OSC_CLK | $A_{IN}$ | VDDRF | 80 MHz (e.g.) Xtal input | Analog-RF |
| CLK | $D_{IN}$ | VDDD | SPI CLK input | SPI |
| IRQ | $D_{OUT}$ | VDDD | Interrupt output | Control FSM |
| CS_N | $D_{IN}$ | VDDD | SPI chip select input, active low | SPI |
| DI | $D_{IN}$ | VDDD | SPI signal from the host output | SPI |
| DO | $D_{OUT}$ | VDDD | SPI signal to the host input | SPI |
| DIO3 | $D_{IN}$ / $D_{OUT}$ | VDDD | HW reset pin | SPI |

The power supply pins are described in Table 3.

**Table 3 BGT60TR13C Supply Pins**

| Symbol | Type | Domain | Description | Domain |
|---|---|---|---|---|
| VDDD | $V_{IN}$ | 1.8 V | Digital supply voltage | Digital |
| VDDA | $V_{IN}$ | 1.8 V | Analog supply voltage | ADC |
| VAREF | $V_{OUT}$ | 1.2 V | Positive reference voltage output; for bypass cap | ADC |
| VDDVCO | $V_{IN}$ | 1.8 V | Analog supply voltage to the VCO | Analog-RF |
| VDDRF | $V_{IN}$ | 1.8 V | Analog supply voltage | Analog-RF |
| VDDLF | $V_{IN}$ | 3.3V | Analog supply voltage for the level shifter for the PLL loop filter | Analog-RF |
| VDDPLL | $V_{IN}$ | 1.8 V | Analog supply voltage to the PLL | Analog-RF |
| VSSRF | GNDA | 0 V | Analog ground connection | Analog-RF |
| VSSA | GNDA | 0 V | Analog ground connection | ADC |
| VSSD | GNDD | 0 V | Digital ground connection | Digital |

**Abbreviations:**

$V_{IN}$ … supply voltage input pin

$D_{IN}$ … digital input pin

$D_{OUT}$ … digital output pin

$V_{OUT}$ … supply voltage output pin

$A_{OUT}$ … analog output pin

## Introduction

$A_{IN}$ … analog input pin

GNDA … analog ground connection

GNDD … digital ground connection

## 1.5 BGT60TR13C Functional Block Diagram

BGT60TR13C consists of some main functional blocks:

- **Antenna** built in package, see Figure 31
- **RF Frontend** consisting of 3ch Rx, 1ch Tx, LO generation, and divider by 4/5
- **ABB**, analog baseband consisting of high pass filter (HPF), VGA, anti-aliasing filter (AAF)
- **PLL**, 3rd order sigma-delta based to perform FMCW ramp
- **MADC**, 3ch 12 bits differential SAR ADCs interfaced to the ABB via a driver and to the FIFO via a mux, see paragraph **Error! Reference source not found.**
- **SADC**, 8 to 10 bits single-ended SAR ADC used to sense the sensor data
- **FIFO**, 196 kbit= 8192 words x 24 bits
- **Register banks**, 127 registers, see paragraph 3
- **SPI**, up to 50 MHz clock in standard mode
- **FSM**, finite state machine which manage the complete chip
- Clock wise, two domains can be identified:
    - 80 MHz system clock (SYS_CLK) domain for PLL, MADC, SADC, and FIFO
    - 50 MHz (e.g.) SPI clock

The main FSM syncs those two domains.

## Introduction

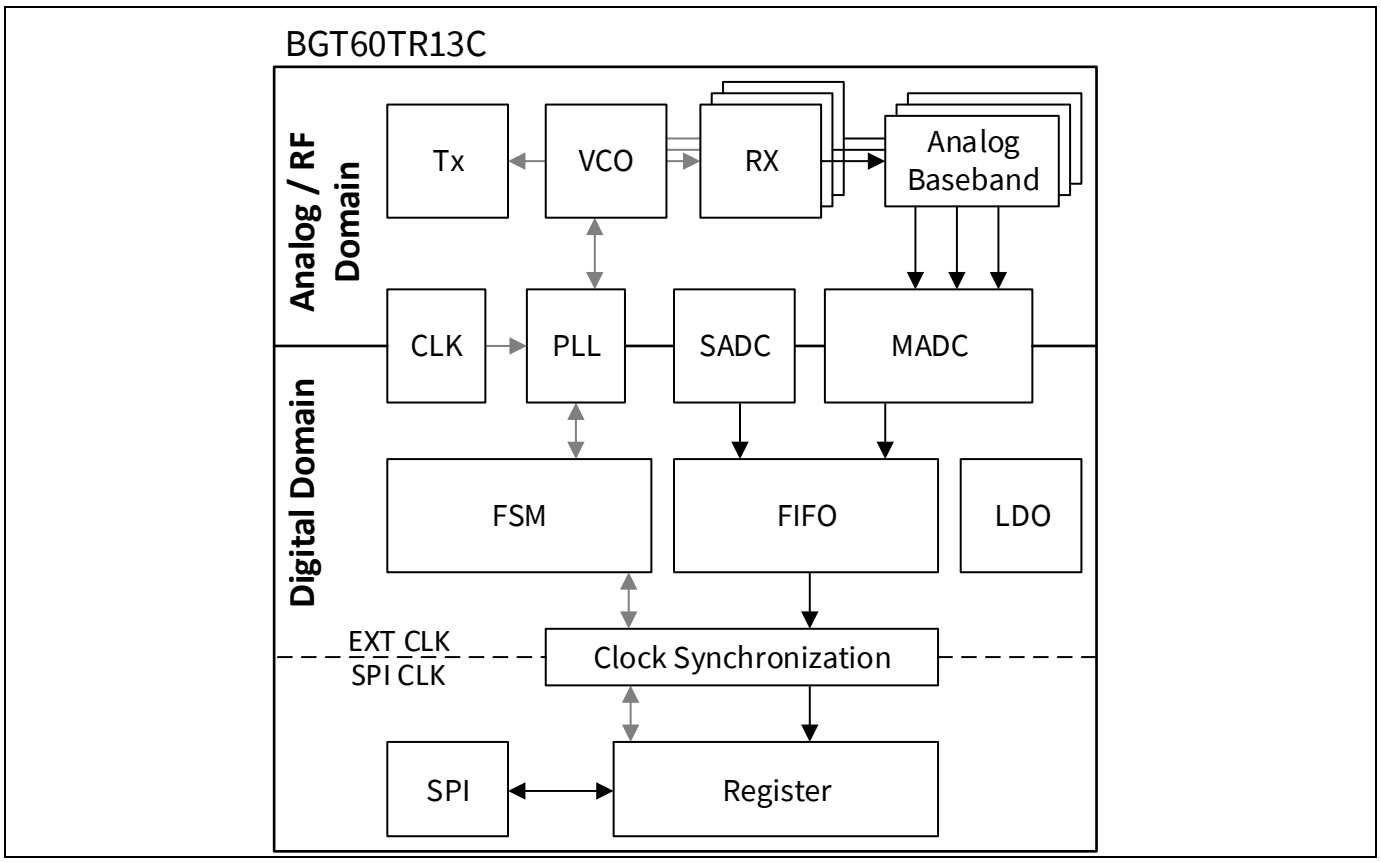


**Figure 4 BGT60TR13C functional overview**

# 2 General Product Specification

The reference for all specified data is the Infineon application board, available on request.

## 2.1 Absolute Maximum Ratings

**Table 4** **Absolute Maximum Ratings $T_b$= -40°C to 105°C,** all voltages with respect to ground, positive current flowing into pin (unless otherwise specified). Parameters not subject to production test

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Supply Voltage | VDDD | V | -0.3 | | +2 | |
| Supply Voltage | VDDA | V | -0.3 | | +2 | |
| Supply Voltage | VDDRF | V | -0.3 | | +2 | |
| Supply Voltage | VDDVCO | V | -0.3 | | +2 | |
| Supply Voltage | VDDPLL | V | -0.3 | | +2 | |
| Supply Voltage | VDDLF | V | -0.3 | | +3.7 | |
| DC Voltage at all I/O Pins | $V_{I/O}$ | V | -0.3 | | VDD+0.3 | Not exceeding 2V |
| RF Input Power Level | PRF | dBm | | | +10 | At the Rx input-port |
| Junction Temperature | Tj | °C | -40 | | +125 | |
| Storage Temperature | Tstg | °C | -40 | | +150 | |

***Warning: Stresses above the maximum values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and lifetime. Functionality of the device might not be given under these conditions.***

## 2.2 Range of Functionality

**Table 5** **Range of Functionality,** VDDD= 1.71 to 1.89 V, Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Supply Voltage | VDDD | V | 1.71 | 1.8 | 1.89 | Noise on each supply domain should not exceed the level of 20µVpp in the frequency range 20kHz-700kHz[1)] |
| Supply Voltage | VDDA | V | 1.71 | 1.8 | 1.89 | |
| Supply Voltage | VDDRF | V | 1.71 | 1.8 | 1.89 | |
| Supply Voltage | VDDVCO | V | 1.71 | 1.8 | 1.89 | |
| Supply Voltage | VDDPLL | V | 1.71 | 1.8 | 1.89 | |
| Supply Voltage | VDDLF | V | 2.5 | 3.3 | 3.63 | |
| Chip Backside Temperature | Tb | °C | -20 | | 70 | Measured with the on chip temperature sensor |
| Frequency Range | $f_{RF}$ | GHz | 58.0 | | 63.5 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| System Reference Frequency | $f_{SYS\_CLK}$ | MHz | 75 | 80 | 85 | 1.8 V CMOS clock; 78 MHz not allowed |
| Duty cycle of $f_{SYS\_CLK}$ | $f_{DUTSYS}$ | % | 45 | 50 | 55 | |
| Rise and Fall Time of $f_{SYS\_CLK}$ | $t_{RS,FS,SYS}$ | ns | | | 6 | |
| Phase Jitter of $f_{SYS\_CLK}$ | $J_{PHSYS}$ | ps | | 1 | | BW: 12kHz to 20MHz |

1) This value will guarantee no artifact/false target in the Range-Doppler map when it is calculated with a minimum of 8 chirps.

## 2.3 Current Consumption

**Table 6 Overall Current Consumption,** VDD (all except LF)= 1.71 to 1.89 and Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep[1)] | $Idd_{ds}$ | mA | 0.05 | 0.12 | 0.555[5)] | |
| Idd Idle[2)] | $Idd_{idle}$ | mA | 0.05 | 2.8 | 5 | |
| Idd Init0, 3Rx+ 1Tx | $Idd_{int0}$ | mA | 136 | 175 | 205 | |
| Idd Init1, 3Rx+ 1Tx[3)] | $Idd_{int1}$ | mA | 141 | 185 | 215 | |
| Idd Active, 3Rx + 1Tx[4)] | $Idd_{act}$ | mA | 160 | 201 | 230 | |

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

5) The value at max refers to the max temperature, +70°C, and the max supply, 1.89 V

**Table 7 VDDD Domain Current Consumption,** VDD (any except LF)= 1.71 to 1.89 and Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep[1)] | $DIdd_{ds}$ | mA | 0.05 | 0.1 | 0.48[5)] | |
| Idd Idle[2)] | $DIdd_{idle}$ | mA | 1.5 | 2.5 | 3.5 | |
| Idd Init0, 3Rx+ 1Tx | $DIdd_{int0}$ | mA | 2 | 3 | 4 | |
| Idd Init1, 3Rx+ 1Tx[3)] | $DIdd_{int1}$ | mA | 3 | 4 | 5 | |
| Idd Active, 3Rx + 1Tx[4)] | $DIdd_{act}$ | mA | 3 | 4 | 5 | |

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, FIFO in low power mode, DAC Tx set to #31 for an output power of +5dBm

5) The value at max refers to the max temperature, +70°C, and the max supply, 1.89 V

**Table 8 VDDA Domain Current Consumption,** VDD (any except LF)= 1.71 to 1.89 and Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep[1] | $AIdd_{ds}$ | mA | 0 | 0.005 | 0.01 | |
| Idd Idle[2] | $AIdd_{idle}$ | mA | 0.01 | 0.2 | 0.3 | |
| Idd Init0, 3Rx+ 1Tx | $AIdd_{int0}$ | mA | 0.5 | 1.6 | 3 | |
| Idd Init1, 3Rx+ 1Tx[3] | $AIdd_{int1}$ | mA | 0.5 | 1.6 | 3 | |
| Idd Active, 3Rx + 1Tx[4] | $AIdd_{act}$ | mA | 0.5 | 1.6 | 3 | |

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

**Table 9 VDDPLL Domain Current Consumption,** VDD (any except LF)= 1.71 to 1.89 and Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep[1] | $PLLIdd_{ds}$ | mA | 0 | 0.005 | 0.01 | |
| Idd Idle[2] | $PLLIdd_{idle}$ | mA | 0 | 0.005 | 0.01 | |
| Idd Init0, 3Rx+ 1Tx | $PLLIdd_{int0}$ | mA | 0.6 | 0.9 | 1.2 | |
| Idd Init1, 3Rx+ 1Tx[3] | $PLLIdd_{int1}$ | mA | 5 | 8 | 10 | |
| Idd Active, 3Rx + 1Tx[4] | $PLLIdd_{act}$ | mA | 5 | 8 | 10 | |

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

**Table 10 VDDLF Domain Current Consumption,** VDD (any except LF)= 1.71 to 1.89 and Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep[1] | $LFIdd_{ds}$ | mA | 0 | 0.005 | 0.01 | |
| Idd Idle[2] | $LFIdd_{idle}$ | mA | 0 | 0.005 | 0.01 | |
| Idd Init0, 3Rx+ 1Tx | $LFIdd_{int0}$ | mA | 0.2 | 0.45 | 0.5 | |
| Idd Init1, 3Rx+ 1Tx[3] | $LFIdd_{int1}$ | mA | 0.2 | 0.45 | 0.5 | |
| Idd Active, 3Rx + 1Tx[4] | $LFIdd_{act}$ | mA | 0.2 | 0.45 | 0.5 | |

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

**Table 11 VDDRF + VDDVCO Domain Current Consumption,** VDD (any except LF)= 1.71 to 1.89 and Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep[1)] | $RFIdd_{ds}$ | mA | 0 | 0.02 | 0.045 | |
| Idd Idle[2)] | $RFIdd_{idle}$ | mA | 0 | 0.02 | 0.045 | |
| Idd Init0, 3Rx+ 1Tx | $RFIdd_{int0}$ | mA | 133 | 170 | 196 | |
| Idd Init1, 3Rx+ 1Tx[3)] | $RFIdd_{int1}$ | mA | 133 | 170 | 196 | |
| Idd Active, 3Rx + 1Tx[4)] | $RFIdd_{act}$ | mA | 151 | 187 | 212 | |

1) All registers in reset mode, 80 MHz clock path disabled

2) MADC band-gap running

3) Idd for the rest of interchirp similar to Init1

4) Device set in radar mode, DAC Tx set to #31

## 2.4 ESD Integrity

**Table 12 ESD Integrity,** VDD(any)= 1.71 to 1.89 V, Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| ESD robustness, HBM<br>All pins | $V_{ESD-HBM}$ | V | -2000 | | +2000 | According to JS-001 (R = 1.5 kΩ, C = 100 pF) |
| ESD robustness, CDM<br>All pins except M2 | $V_{ESD-CDM}$ | V | -500 | | +500 | According to JS-002 |
| ESD robustness, CDM<br>Pin M2 | $V_{ESD-CDM, M2}$ | V | -250 | | +250 | According to JS-002 |

CDM: Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

HBM: Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C=100 pF).

## 2.5 Thermal Resistance

**Table 13 Thermal Resistance,** VDD(any)= 1.71 to 1.89 V, Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Package Rth | $R_{th}$ | K/W | | 35 | | Chip backside to ambient temperature |

## 2.6 Product Validation

Qualified for potential applications listed in section 1.2 based on the test conditions in the relevant tests of JEDEC20/22.

# 3 BGT60TR13C Registers

An array of registers visible via the SPI is used to control and program the states of the different blocks inside the chip.

## 3.1 Register List

The registers are arranged in blocks of 24 bits each. Each block is identified by its unique address. The registers are accessed from the SPI module. The bit fields from each register are arranged in MSB first order.

**Table 14 The following table gives an overview on the BGT60TR13C registers.Register Overview / Address Table**

| Register Address | Register Name | Description | | |
|---|---|---|---|---|
| 0x00 | MAIN | Main register | | |
| 0x01 | ADC0 | MADC control register | | |
| 0x02 | CHIP_ID | Digital and RF version | | |
| 0x03 | STAT1 | Status register 1 | | |
| 0x04 | PACR1 | PLL analog control register 1 | | |
| 0x05 | PACR2 | PLL analog control register 2 | | |
| 0x06 | SFCTL | SPI and FIFO Control | | |
| 0x07 | SADC_CTRL | Sensor ADC ctrl reg | | |
| 0x08 | CSI_0 | Channel set idle mode 0 | | |
| 0x09 | CSI_1 | Channel set idle mode 1 | | |
| 0x0A | CSI_2 | Channel set idle mode 2 | | |
| 0x0B | CSCI | Channel set control idle mode | | |
| 0x0C | CSDS_0 | Channel set deep sleep mode 0 | | |
| 0x0D | CSDS_1 | Channel set deep sleep mode 1 | | |
| 0x0E | CSDS_2 | Channel set deep sleep mode 2 | | |
| 0x0F | CSCDS | Channel set control deep sleep mode | | |
| 0x10 | CSU1_0 | Channel set 1 (up) | | |
| 0x11 | CSU1_1 | Channel set 1 (up) | | |
| 0x12 | CSU1_2 | Channel set 1 (up) | | |
| 0x13 | CSD1_0 | Channel set 1 (down) | | |
| 0x14 | CSD1_1 | Channel set 1 (down) | | |
| 0x15 | CSD1_2 | Channel set 1 (down) | | |
| 0x16 | CSC1 | Channel set control 1 (up/dn) | | |
| 0x17 | CSU2_0 | Channel set 2 (up) | | |
| 0x18 | CSU2_1 | Channel set 2 (up) | | |
| 0x19 | CSU2_2 | Channel set 2 (up) | | |
| 0x1A | CSD2_0 | Channel set 2 (down) | | |
| 0x1B | CSD2_1 | Channel set 2 (down) | | |
| 0x1C | CSD2_2 | Channel set 2 (down) | | |

## BGT60TR13C Registers

| | | | | |
|---|---|---|---|---|
| 0x1D | CSC2 | Channel set control 2 (up/dn) | | |
| 0x1E | CSU3_0 | Channel set 3 (up) | | |
| 0x1F | CSU3_1 | Channel set 3 (up) | | |
| 0x20 | CSU3_2 | Channel set 3 (up) | | |
| 0x21 | CSD3_0 | Channel set 3 (down) | | |
| 0x22 | CSD3_1 | Channel set 3 (down) | | |
| 0x23 | CSD3_2 | Channel set 3 (down) | | |
| 0x24 | CSC3 | Channel set control 3 (up/dn) | | |
| 0x25 | CSU4_0 | Channel set 4 (up) | | |
| 0x26 | CSU4_1 | Channel set 4 (up) | | |
| 0x27 | CSU4_2 | Channel set 4 (up) | | |
| 0x28 | CSD4_0 | Channel set 4 (down) | | |
| 0x29 | CSD4_1 | Channel set 4 (down) | | |
| 0x2A | CSD4_2 | Channel set 4 (down) | | |
| 0x2B | CSC4 | Channel set control 4 (up/dn) | | |
| 0x2C | CCR0 | Chirp control register 0 | | |
| 0x2D | CCR1 | Chirp control register 1 | | |
| 0x2E | CCR2 | Chirp control register 2 | | |
| 0x2F | CCR3 | Chirp control register 3 | | |
| 0x30 | PLL1_0 | FSU1 – shape 1 | | |
| 0x31 | PLL1_1 | RSU1 – shape 1 | | |
| 0x32 | PLL1_2 | RTU1 – Shape 1 | | |
| 0x33 | PLL1_3 | AP1 – shape 1 | | |
| 0x34 | PLL1_4 | FSD1 – shape 1 | | |
| 0x35 | PLL1_5 | RSD1 – shape 1 | | |
| 0x36 | PLL1_6 | RTD1 – shape 1 | | |
| 0x37 | PLL1_7 | SCR – shape 1 | | |
| 0x38 | PLL2_0 | FSU1 – shape 2 | | |
| 0x39 | PLL2_1 | RSU1 – shape 2 | | |
| 0x3A | PLL2_2 | RTU1 – shape 2 | | |
| 0x3B | PLL2_3 | AP1 – shape 2 | | |
| 0x3C | PLL2_4 | FSD1 – shape 2 | | |
| 0x3D | PLL2_5 | RSD1 – shape 2 | | |
| 0x3E | PLL2_6 | RTD1 – shape 2 | | |
| Ox3F | PLL2_7 | SCR – shape 2 | | |
| 0x40 | PLL3_0 | FSU1 – shape 3 | | |
| 0x41 | PLL3_1 | RSU1 – shape 3 | | |
| 0x42 | PLL3_2 | RTU1 – shape 3 | | |
| 0x43 | PLL3_3 | AP1 – shape 3 | | |
| 0x44 | PLL3_4 | FSD1 – shape 3 | | |
| 0x45 | PLL3_5 | RSD1 – shape 3 | | |

## BGT60TR13C Registers

| | | | | |
|---|---|---|---|---|
| 0x46 | PLL3_6 | RTD1 – shape 3 | | |
| 0x47 | PLL3_7 | SCR – shape 3 | | |
| 0x48 | PLL4_0 | FSU1 – shape 4 | | |
| 0x49 | PLL4_1 | RSU1 – shape 4 | | |
| 0x4A | PLL4_2 | RTU1 – shape 4 | | |
| 0x4B | PLL4_3 | AP1 – shape 4 | | |
| 0x4C | PLL4_4 | FSD1 – shape 4 | | |
| 0x4D | PLL4_5 | RSD1 – shape 4 | | |
| 0x4E | PLL4_6 | RTD1 – shape 4 | | |
| 0x4F | PLL4_7 | SCR – shape 4 | | |
| 0x55 | RFT0 | RF test register 0 | | |
| 0x56 | RFT1 | RSVD | | |
| 0x59 | PLL_DFT0 | PLL DFT register 0 | | |
| 0x5D | STAT0 | Status register 0 | | |
| 0x5E | SADC_RESULT | Sensor ADC result register | | |
| 0x5F | FSTAT | FIFO status register | | |
| >= 0x60 | | FIFO access | | |

*Note: Reserved bits (RSVD) in the registers should not be modified. They should be kept in the default/reset state unless otherwise specified.*

### 3.1.1 Abbreviations

Access modes on the registers:

- R … Readable register or bit field
- W … Writeable register or bit field
- S … Status bit can be set to readable mode “R”
- RSVD … Reserved value which is not assigned at the moment

## 3.2 CHIP_ID

The register CHIP_ID provides information regarding the digital code version, the RF block version, and the antenna configuration (number of channels, position of the antennas e.g.).

It is used by the driver to configure the device properly according to the information above.

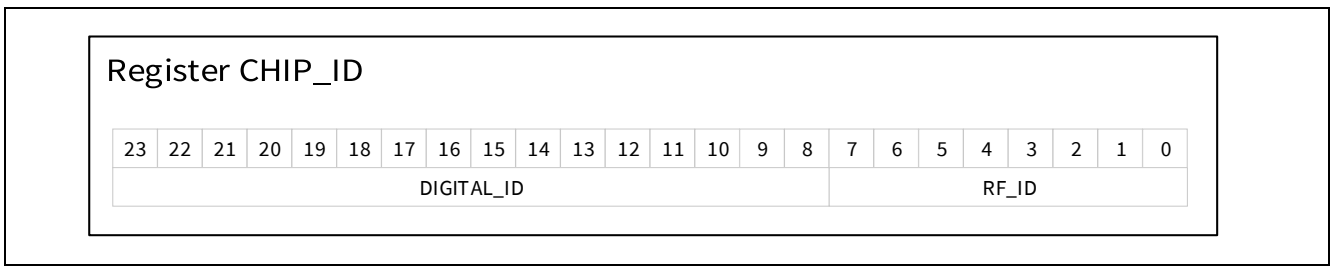


**Figure 5 CHIP_ID register**

**Table 15 CHIP_ID: Register Description**

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| DIGITAL_ID | 23:8 | R | $3_D$ | $3_D$ |
| RF_ID | 7:0 | R | $3_D$ … 1ch Tx, 3ch Rx | $3_D$ |

The Digital_ID as well as the RF_ID will be incremented according to the latest chip release/version.

## 3.3 STAT1 - Status Register1

The status register provides internal counter values for the actual number of frames and shapes. They are also provided to the data header. However it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 µs.

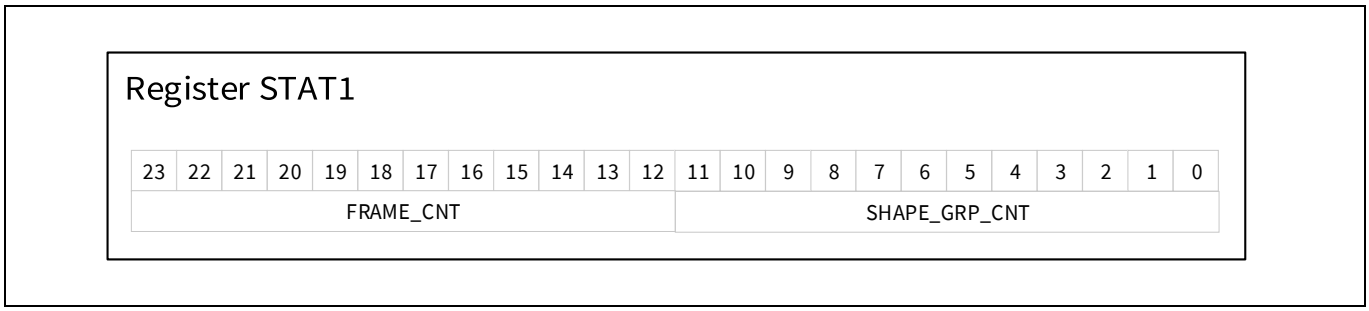


**Figure 6 STAT1: status register 1**

**Table 16 STAT1: Register Description**

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| FRAME_CNT | 23:12 | R | Frame counter value:<br>$0_D$ … Reset value / after max. value rollover<br>$4095_D$ … Max. value<br>Note:<br>This field is for debug only. | $0_D$ |
| SHAPE_GRP_CNT | 11:0 | R | Shape group counter counts the actual shape groups:<br>$0_D$ … Reset value / after max. value for SHAPE_GRP_CNT reached<br>$4095_D$ … Max. value | $0_D$ |

*Note:*

1. *A shape consists of an “Up Chirp” segment and a “Down Chirp” segment.*
2. *A sawtooth shape is generated by an “Up Chirp” and a “Fast Down Chirp”.*
3. *There is no data acquisition in the “Fast Down Chirp”.*

## 3.4 SFCTL – SPI and FIFO Control Register

This register is used to configure the SPI and FIFO.

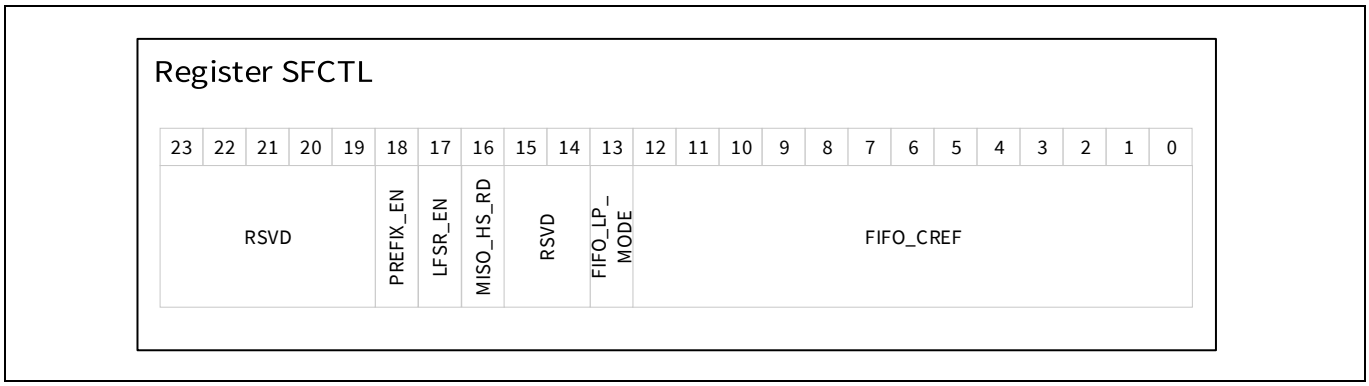


**Figure 7 SPI and FIFO Control Register**

**Table 17 SPI and FIFO Control: Register Description**

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| RSVD | 23:19 | RW | RSVD | $14_B$ |
| PREFIX_EN | 18 | RW | Enables the data header written into the FIFO prior to the sampling data of each chirp:<br>$0_B$… No prefix data header prior to chirp data<br>$1_B$… Prefix data header added prior to chirp data<br>(see section 4.1 for data header) | $0_B$ |
| LFSR_EN | 17 | RW | Enable LFSR register data generation:<br>$0_B$ … Normal data acquisition, LFSR reset<br>$1_B$ … LFSR data generation started<br>LFSR should be enabled after a FIFO reset to ensure an empty FIFO (see also 4.10). | $0_B$ |
| MISO_HS_RD | 16 | RW | $0_B$ … MISO data is sent with falling edge of SPI CLK<br>$1_B$ … MISO data is sent with rising edge ( ½ cycle earlier )<br><br>Note: HS_RD = $0_B$ can only be used for a SPI clock < 25 MHz. For HS-transfer please check the timing of the SPI Master and adjust settings accordingly.<br><br>The setting becomes active when the last bit of FSCTL is clocked out and it affects MISO immediately.<br>See also section 4.3.1. | $1_B$ |
| RSVD | 15:14 | RW | RSVD | $0_B$ |
| FIFO_LP_MODE | 13 | RW | FIFO power mode:<br>$0_B$ … FIFO permanently enabled<br>$1_B$ … FIFO activated dynamically | $0_B$ |
| FIFO_CREF | 12:0 | RW | FIFO compare reference: it defines the compare filling status for interrupt and CREF reporting | $0_D$ |

## BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| | | | When filling status is > FIFO_CREF an interrupt is issued:<br>$0_D$ … minimum value is 0, interrupt generated in case first sample is written into FIFO<br>$8191_D$ … maximum value in case FIFO is full with 8192 memory locations<br>eg. CREF = 0x1000 represents a 50% compare reference | |

## 3.5 STAT0 - Status Register 0

The status register STAT0 provides the actual value of some specific internal states. However it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 µs.

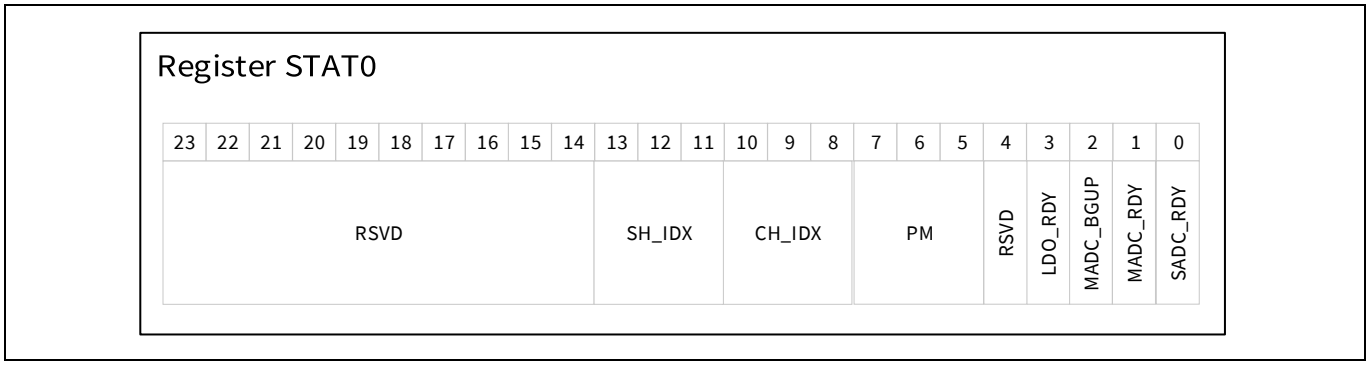


**Figure 8 STAT0: Control FSM Status Register**

**Table 18 STAT0: Register Description**

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| RSVD | 23:14 | R | RSVD | $0_D$ |
| SH_IDX | 13:11 | R | Actual chirp shape enabled by the FSM:<br>$0_D$ … PLLU1<br>$1_D$ … PLLD1<br>$2_D$ … PLLU2<br>$3_D$ … PLLD2<br>$4_D$ … PLLU3<br>$5_D$ … PLLD3<br>$6_D$ … PLLU4<br>$7_D$ … PLLD4 | $0_D$ |
| CH_IDX | 10:8 | R | Actual channel set enabled by the FSM:<br>$0_D$ … CSU1<br>$1_D$ … CSD1<br>$2_D$ … CSU2<br>$3_D$ … CSD2<br>$4_D$ … CSU3<br>$5_D$ … CSD3 | $0_D$ |

**Table 18 STAT0: Register Description**

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| | | | $6_D$ … CSU4<br>$7_D$ … CSD4 | |
| PM | 5:7 | R | Power Mode is the current power mode status of FSM:<br>$1_D$ … Active Mode<br>$2_D$ … Interchirp Mode<br>$3_D$ … Idle Mode<br>$5_D$ … Deep Sleep Mode<br>$0_D$,$4_D$,$6_D$,$7_D$ … RSVD | $5_D$ |
| RSVD | 4 | R | RSVD | $0_B$ |
| LDO_RDY | 3 | R | LDO output level, i.e. VDDC, above the threshold:<br>$0_B$ … LDO output level below threshold<br>$1_B$ … LDO output level above threshold, ready | $0_B$ |
| MADC_BGUP | 2 | R | MADC bandgap reference power up status:<br>$0_B$ … Status down<br>$1_B$ … Up and running | $0_B$ |
| MADC_RDY | 1 | R | MADC status:<br>$0_B$ … Status down<br>$1_B$ … Up and running | $0_B$ |
| SADC_RDY | 0 | R | SADC startup / calibration status:<br>$0_B$ … Status down<br>$1_B$ … Up and running | $0_B$ |

## 3.6 FSTAT - FIFO Status Register

The global status register FSTAT is used to monitor the FIFO. It should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 µs.

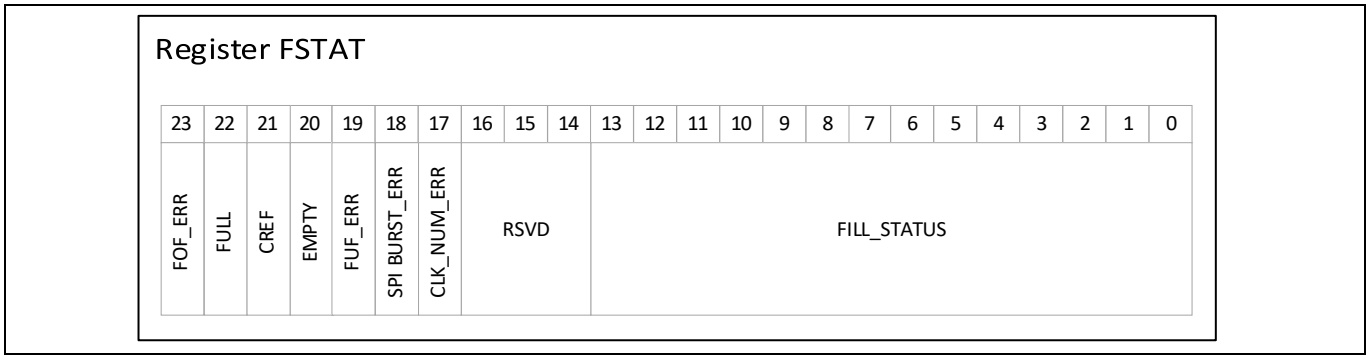


**Figure 9 FSTAT Register**

**Table 19 FSTAT: Register Description**

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| FOF_ERR | 23 | R | FIFO overflow error bit shows if more sample data are transferred to the FIFO than FIFO memory locations are | $0_B$ |

## BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| | | | available to store the data. The flag will be shown also in GSR0 as a part of FIFO over or underflow error bit FOU_ERR:<br>$0_B$ … No FIFO overflow<br>$1_B$ … FIFO had an overflow condition | |
| FULL | 22 | R | The FULL bit shows if the FIFO has fully filled up:<br>$0_B$ … FIFO is not full<br>$1_B$ … FIFO is full | $0_B$ |
| CREF | 21 | R | $0_B$ … FIFO filling status below CREF<br>$1_B$ … FIFO filling status is > CREF | $0_B$ |
| EMPTY | 20 | R | The FIFO empty bit EMPTY signals if the FIFO is empty:<br>$0_B$ … FIFO stores at least one sample<br>$1_B$ … FIFO is empty | $1_B$ |
| FUF_ERR | 19 | R | FIFO under flow error signals if the host was reading more sampling data from the FIFO than available. The flag will be shown also in GSR0 as a part of FIFO over or underflow error bit FOU_ERR:<br>$0_B$ … No error<br>$1_B$ … FIFO underflow occurred | $0_B$ |
| SPI BURST_ERR | 18 | R | In case of burst error this bit is set. Further details in the Note below and in 4.8:<br>$0_B$ … No error<br>$1_B$ … Burst error occurred. Bit will be reset after HW or SW reset condition.<br>See also section 4.8. | $0_B$ |
| CLK_NUM_ERR | 17 | R | Clock number error bit is set when SPI clocks do not fit the expected clock cycles. Further details in the Note below and in 4.8:<br>$0_B$ … No error<br>$1_B$ … Burst error occurred. Bit will be reset after HW or SW reset condition.<br>See also section 4.8. | $0_B$ |
| RSVD | 16:14 | R | Not used | $0_D$ |
| FILL_STATUS | 13:0 | R | FIFO filling status:<br>0x0 … FIFO empty<br>0x1000 … FIFO 50% filled<br>0x2000 … FIFO full<br>This bit field is for de-bugging only. It should not be evaluated while the MADC sampling and filing up the FIFO.<br>It can be evaluated when the FSM status is held, for example, after an FSM reset or in a specific power mode, Deep Sleep e.g. | $0_D$ |

*Note:*

*FOF/FUF will be cleared after these resets:*

## BGT60TR13C Registers

- FIFO reset
- SW reset
- HW reset

## 3.7 GSR0 - Global Status Register

The global status register GSR0 is related to SPI read/write monitoring.

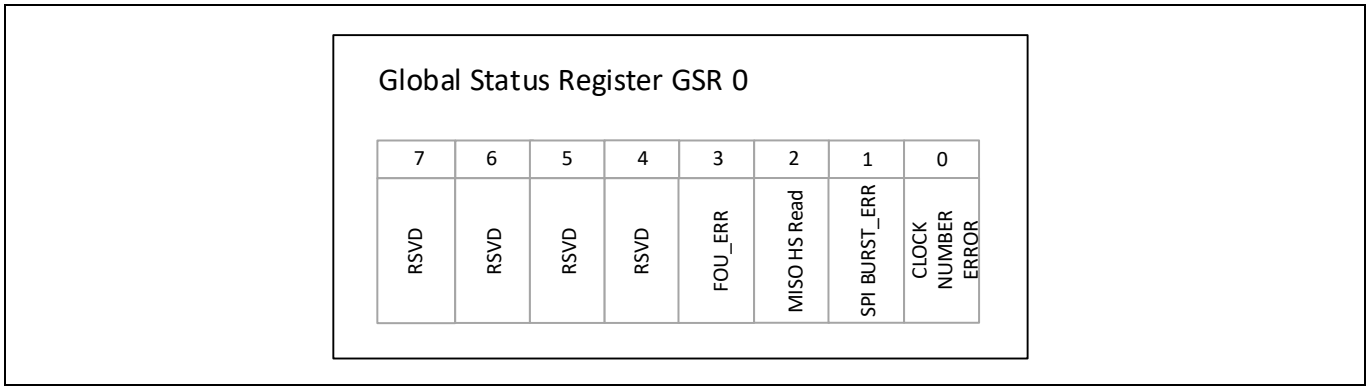


**Figure 10 GSR0 Register**

**Table 20 GSR0: Register Description**

| Symbol | Bits | Type | Description | RST |
|---|---|---|---|---|
| RSVD | 7 | R | Reserved | |
| RSVD | 6 | R | Reserved | |
| RSVD | 5 | R | Reserved | |
| RSVD | 4 | R | Reserved | |
| FOU_ERR | 3 | R | Shows if FIFO overflow or underflow condition occurred. The error will be cleared after the following resets: FIFO reset or SW reset or HW reset:<br>$1_B$ … Error condition occurred<br>$0_B$ … No error | $0_B$ |
| MISO HS Read | 2 | R | SPI: MISO high speed mode activated | $1_B$ |
| SPI BURST_ERR | 1 | R | SPI burst error, defined within the SPI spec (see section 4.8):<br>$0_B$ … No burst read/write error<br>$1_B$ … Burst error | $0_B$ |
| CLOCK NUMBER ERROR | 0 | R | Defined within the SPI spec:<br>$0_B$ … No clock number error<br>$1_B$ … Error condition occurred | $0_B$ |

# 4 Data Organization and SPI Interface

## 4.1 Data Header

The main FSM is capable of generating a data header to be attached to the actual radar raw data. The structure of the header is shown in Figure 11 and in Table 21. The data header can be disabled by controlling the bit SFCTL:PREFIX_EN (see section 3.4).

A sync-word is sent at the beginning of each acquisition to make the radar raw-data from each shape unique. This can be useful in case of broken communication with the application processor or in case of errors. Supposing the FIFO will generate a “FIFO overflow flag” the sync-word 0x000000 can be evaluated by the host controller and used to resync with the BGT60TR13C and discard the data received before this sync word (if header or sync-word not used then the controller should reset the FIFO, discarding the actual FIFO data). On “FIFO underflow flag”, the received data bits from the host are $111111111111_B$.

Following, the header includes also the frame counter and shape group counter, as well as the actual APU/APD value and temperature value.

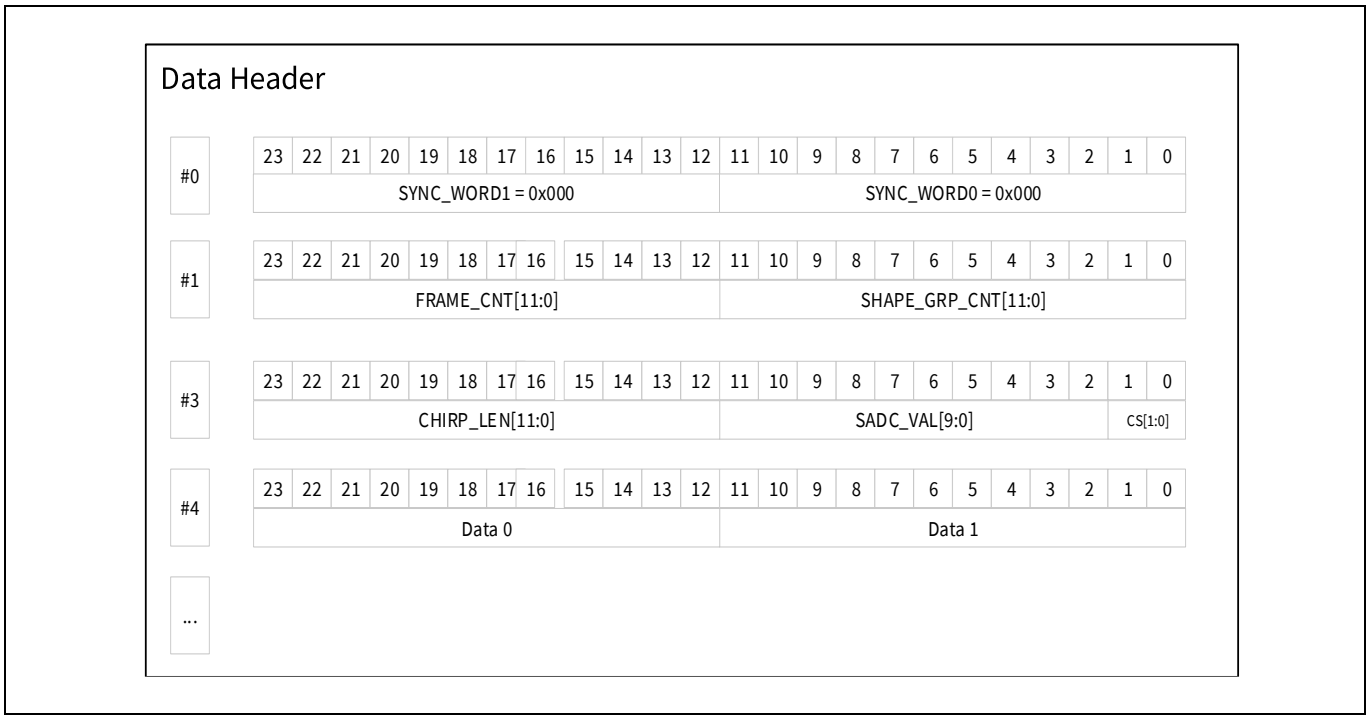


**Figure 11 Data header**

## Data Organization and SPI Interface

**Table 21 Data Header Description**

| Symbol | Reg | Bits | Description | RST |
|---|---|---|---|---|
| SYNC_WORD1 | #0 | 23:12 | The sync-word can be used to identify the start of a new chirp. In case the MADC will output also a sequence of 0x000000, to make the sync-word unique, the data from the MADC will be automatically changed to 0x001 before transferring it to the FIFO. | $0_D$ |
| SYNC_WORD0 | #0 | 11:0 | See SYNC_WORD1. | $0_D$ |
| FRAME_CNT | #1 | 23:12 | Same as STAT1:FRAME_CNT (see section 3.3). | $0_D$ |
| SHAPE_GRP_CNT | #1 | 11:0 | Same as STAT1:SHAPE_GRP_CNT (see section 3.3). | $0_D$ |
| CHIRP_LEN | #2 | 23:12 | Number of MADC samples inside the chirp (APU/APD value of related chirp). | $0_D$ |
| SADC_VAL | #2 | 11:2 | 10 bits of sensor ADC output data (eg. temperature). | $0_D$ |
| CS | #2 | 1:0 | Indicates the channel shape number to which the following sampling data belongs to. | |
| Data 0 | #3 | 23:12 | MSB data (see section 4.2). | |
| Data 1 | #3 | 11:0 | LSB data (see section 4.2). | |

## 4.2 FIFO and Dataflow

The memory in the BGT60TR13C is based on a FIFO. The FIFO consists of a circular shift register organized in 8192 words of 24 bits each. Three dataflow modes from MADC to the FIFO are supported by the FSM (see Figure 12):

- Mode 1: Only one ADC active (can be any ADC from 1 to 3)
  - Data from 1st sample, 12 bits, are temporarily stored in a buffer
  - When the 2nd sample, 12 bits, are available, both, 1st and 2nd, 24 bits, are stored into one data word
- Mode 2: Two ADCs active (can be any ADC from 1 to 3)
  - Data from active ADCs, 12+12 bits, are occupying one data word in the FIFO
- Mode 3: Three ADCs active
  - Data from first two channels are stored into a data word while data from third channel is buffered. On the consecutive trigger the buffered data and the one from first channel are stored in a data word while the data of the second channel is buffered. On the next trigger the buffered data plus the data from the third channel are stored in a third data word, etc.

## Data Organization and SPI Interface

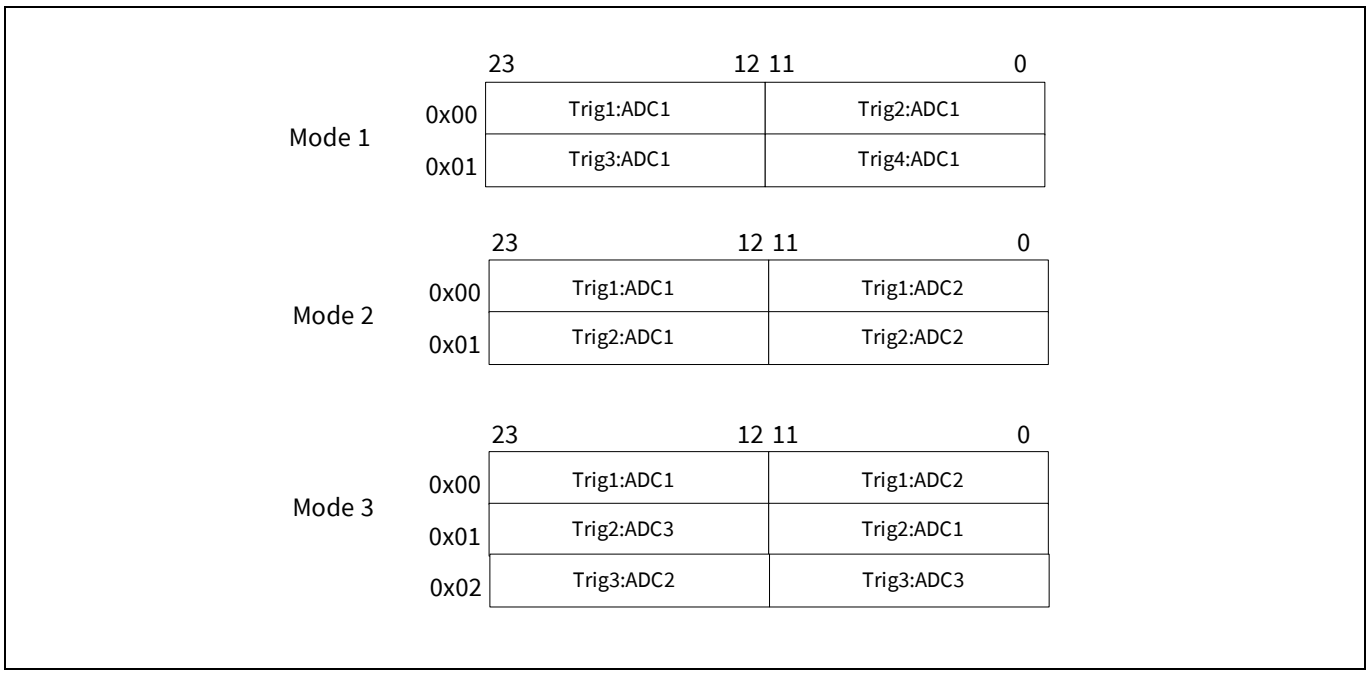


**Figure 12 FIFO organization**

Readout from the FIFO is done from the SPI block. Due to max frequency of SPI clock, 50 MHz, the readout rate from the FIFO is:

- 50 MHz / SPI Mode / 24 bit = 480 ns = 40 cycles (in the 80 MHz domain)

Readout from the FIFO should be executed from the host controller using memory address with correct data length. Data length can be derived from the data header or based on the “sync-word”.

*Note:*

*An illegal write to memory address space will lead to lost FIFO data!*

## 4.3 SPI – Serial Peripheral Interface Module

The SPI is the communication interface between the host and the BGT60TR13C. It enables the host to read from, or write to (program) the registers as well as reading from the FIFO.

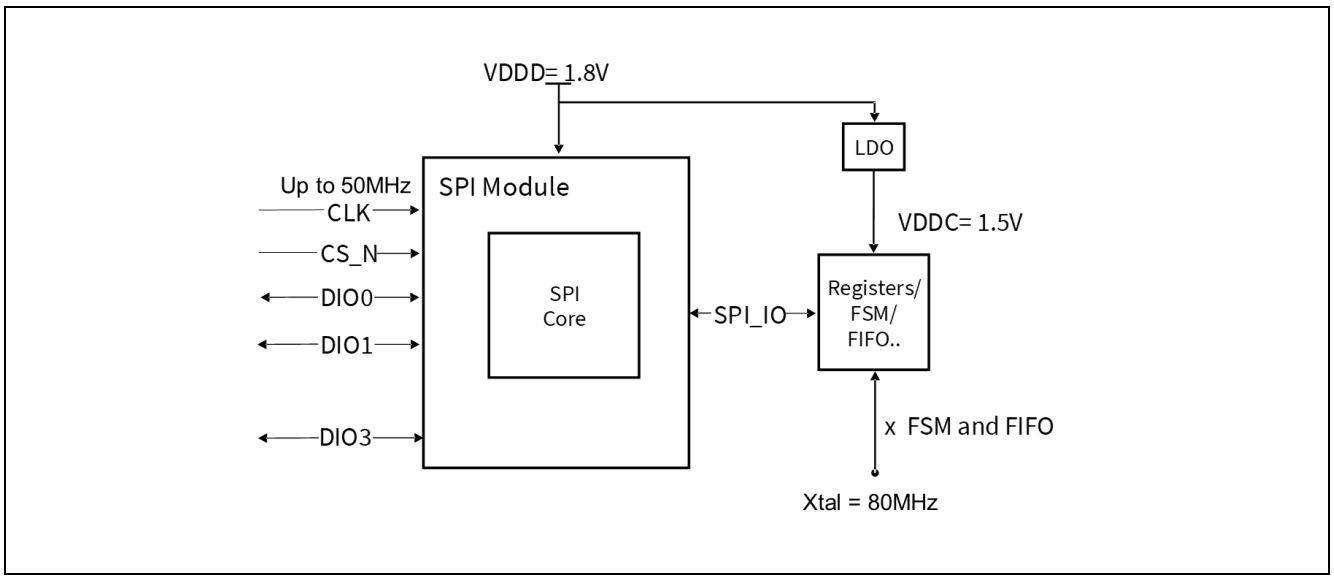


**Figure 13 SPI module**

## Data Organization and SPI Interface

BGT60TR13C device features four I/O pins for SPI communication and one for chip reset. DIO[x] pins are pulled up to logic high inside the pad.

- CS_N to be connected to SS of the SPI master
- CLK to be connected to CLK of the SPI master
- DIO0, DI to be connected to MOSI of the SPI master
- DIO1, DO to be connected to MISO of the SPI master
- DIO2 not available on BGT60TR13C
- DIO3 to be connected to reset

**Table 22 SPI Pins**

| Pin Name | Standard SPI Mode Function | Remarks |
|---|---|---|
| CS_N | CS_N | Chip select |
| CLK | CLK | SPI clock |
| DIO0 | DI | HiZ, biderectional |
| DIO1 | DO | HiZ, bidirectional |
| DIO2 | N.A. | Not available on BGT60TR13C |
| DIO3 | RESET | HiZ, bidirectional |

The SPI interface can be clocked up to 50MHz. To meet the timing requirements for higher SPI clock frequencies (e.g. > 25MHz) the BGT60TR13C device offers an additional high speed mode (SFCTL:MISO_HS_RD) which increase the timing budget on SPI master side by sending out data via DO with the rising edge instead of the falling edge of the CLK.

### 4.3.1 Standard SPI Timing

The timing diagram for normal SPI mode (SFCTL:MISO_HS_RD =0) is presented in Figure 14. A SPI transfer is started with a falling edge of chip select signal CS_N generated by the SPI master. At the same time the SPI master shall drive the level of the data input signal DI (master output, slave input) according to the first bit. Also with the falling edge of the chip select signal CS_N the SPI slave applies the level of the data output signal DO (master input, slave output) according to the first bit which shall be transferred to the SPI master, the level becomes stable after the period t(dS). The SPI master has to wait for the time t(L) before the clock signal CLK can be generated.

With the rising edge of CLK the SPI slave captures the level of DI. The SPI master must keep the DI level stable for t(mos) before and for t(moh) after the rising edge of CLK to ensure valid setup and hold time of the SPI slave. With the falling edge of CLK the SPI master shall set the level of DI according to the next bit the master wants to send.

The SPI master is supposed to read the level of DO with the rising edge of CLK. The SPI slave keeps the DO level stable for t(mis) before and for t(mih) after the rising edge of CLK. With the falling edge of CLK the SPI slave drives the level of DO according to the next bit, DO becomes stable after t(mih).

After the last bit has been transferred and CLK has gone to low level, the SPI master must set CS_N to high level to stop the transfer. The master must take care that the period between the last rising edge of CLK and the rising edge of CS_N is not shorter than t(T). Within the period t(dh) after the rising edge of CS_N the SPI slave drives DO to high impedance state again.

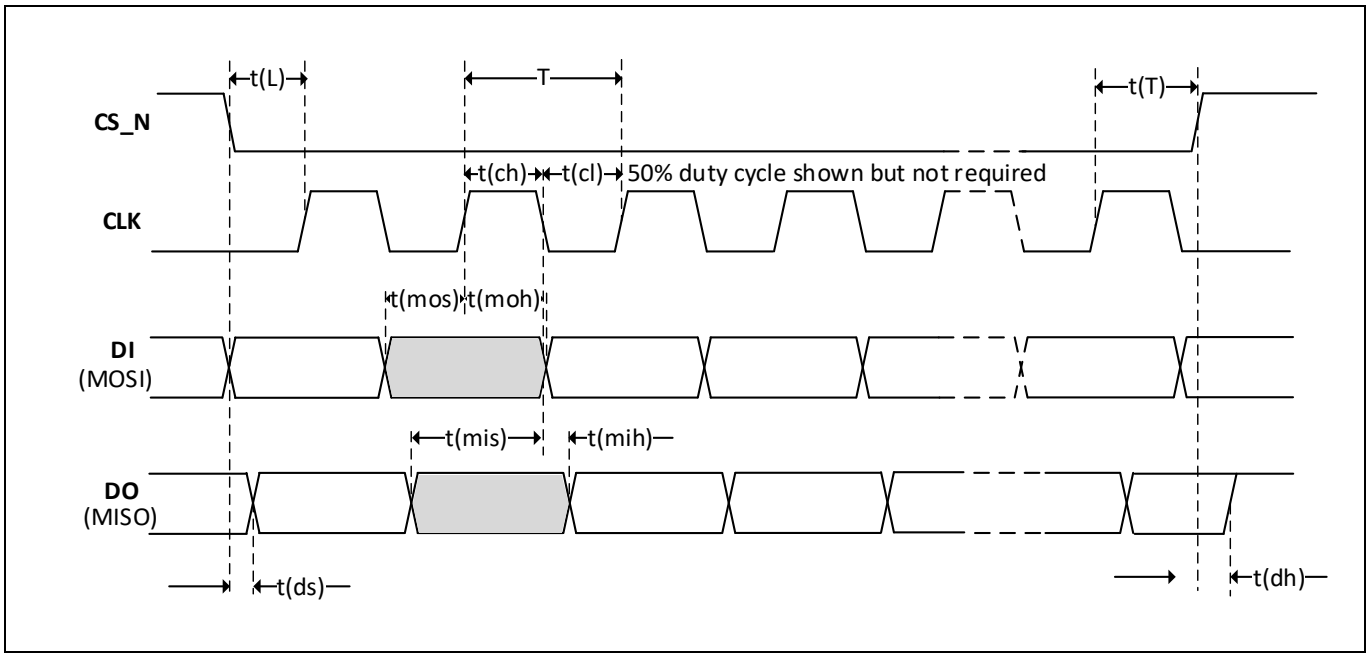


**Figure 14 SPI interface timing diagram for SFCTL:MISO_HS_RD = $0_b$**

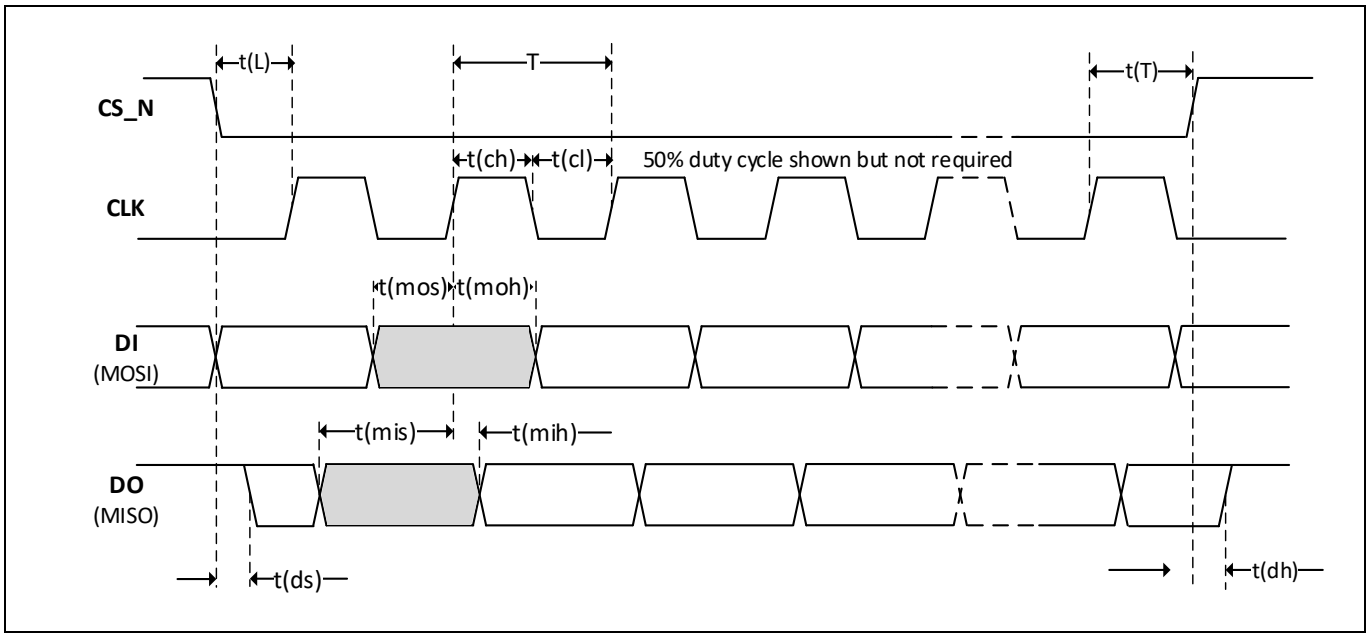


**Figure 15 SPI interface timing diagram for SFCTL:MISO_HS_RD = $1_b$**

BGT60TR13C can operate at SPI clock frequencies up to 50MHz, but the maximum achievable SPI clock frequency is limited by DI related setup and hold times of SPI master and SPI slave. If for example the SPI master requires a longer MISO setup time than t(mis), the SPI clock speed in normal SPI mode must be reduced. Alternatively BGT60TR13C can be switched to SPI high speed mode by setting SFCTL:MISO_HS_RD = $1_b$.

The timing diagram for high speed SPI mode is presented in Figure 15. In this mode the SPI master is still supposed to capture the level of DO with the rising edge of CLK. The SPI slave keeps the level of DO stable for t(mis) before the rising edge of CLK. The SPI slave keeps the level of DO stable for t(mih) after the rising edge of CLK, and then sets the level of DO according to the next bit which is send out.

## Data Organization and SPI Interface

**Table 23 SPI Timing Requirements,** VDDD= 1.71 to 1.89 V, Tb= -20 to +70°C

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| SPI clock period: 50MHz, with 1% clock jitter | T | ns | 20 | | | |
| Clock high | t(ch) | ns | 9.0 | | | |
| Clock low | t(cl) | ns | 9.0 | | | |
| Master output setup | t(mos) | ns | 5.0 | | | |
| Master output hold | t(moh) | ns | 5.0 | | | |
| Master input setup | t(mis) | ns | 5.0 | | | T=20ns (see Note 2) |
| Master input hold | t(mih) | ns | 1.0 | | | |
| Lead time before the first working clock edge occurs | t(L) | ns | 9.0 | | | |
| Tailing time after the last working clock edge | t(T) | ns | 1 | | | |
| Data setup time after the DO goes in low impedance state | t(ds) | ns | | | 5 | Guaranteed by design |
| Data hold time before DO goes in hi impedance state. | t(dh) | ns | | | 5 | Guaranteed by design |

*Note:*

1. *If SFCTL:MISO_HS_RD is not set properly then data read on MISO may not be correct.*
2. *t(mis) is specified for a maximum SPI clock frequency of 50MHz. This results in a maximum delay (time output valid) of T-t(mis) = 15ns between falling edge of CLK (for MISO_HS_RD=0) and DO level becoming valid. For MISO_HS_RD=1 it's the rising edgle of CLK. The timing is guaranteed for worst case condition: VDDD = 1.71 V, Tb=+70°C, output load of Cload = 50 pF.*

### 4.3.2 Logic Levels

The digital inputs and outputs are fully CMOS compatible (reported in Table 24). All IO input / output timings are based on 50% voltage reference levels (see Figure 16). I/O interfaces are shown in Figure 19, input pins, and Figure 20, output pins, which include internal pull-ups.

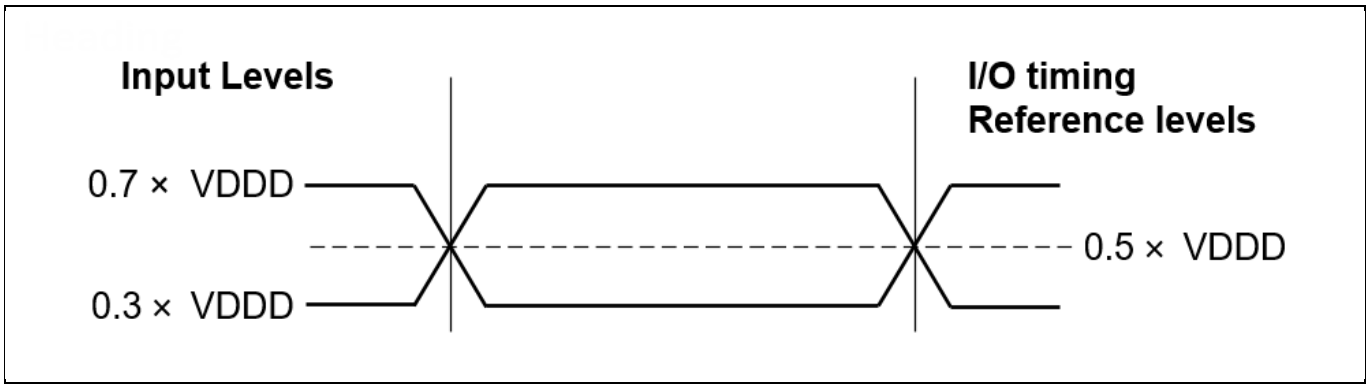


**Figure 16 AC timing input/output reference levels**

The input logic hysteresis prevents input buffers from oscillation. The minimum hysteresis range $V_{HYST}$ is in between the lower (0.3 × VDDD) and upper logic level (0.7 × VDDD) boundaries (see Figure 17). Above 0.7 × VDDD

## Data Organization and SPI Interface

the input signal is a logical '1' while below 0.3 × VDDD it is a logical '0' regardless of hysteresis. Due to temperature drifts and device variation the hysteresis range $V_{HYST}$ can be up to 0.7 × VDDD or down to 0.3 × VDDD but typically around 0.5 × VDDD. Parameters reported in Table 24 and Table 25.

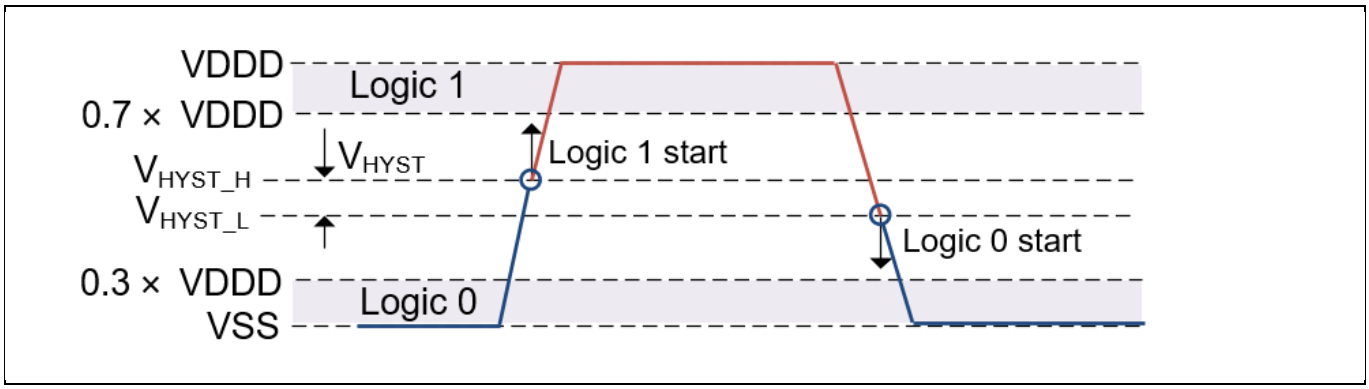


**Figure 17 Logic input levels and hysteresis**

The digital output pads have a fixed output pad strength that gives a specific slew-rate for rising signals, $dV_{TR}$, and falling signals, $dV_{TF}$ (see Figure 18). Minimum slew rates were simulated considering a total capacitive load of 15pF. Results reported in Table 24 and Table 25.

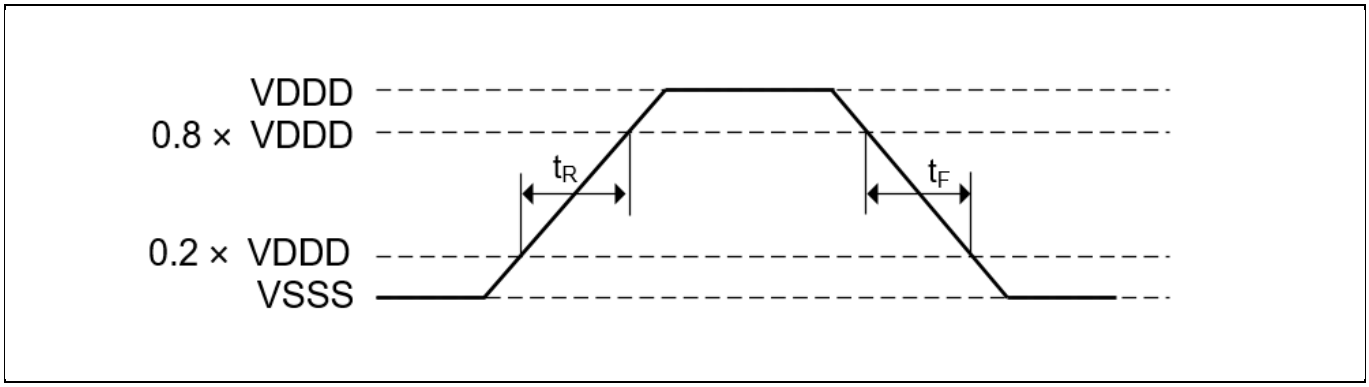


**Figure 18 Rise/Fall Time, Slew Rate specified between 0.2 × VDDD and 0.8 × VDDD**

## Data Organization and SPI Interface

**Table 24 Logical Levels for Pins CLK, CS_N, DI, DIO3** VDDD= 1.71 to 1.89 V, Tb= -20 to +70°C, ambient temperature not below -40°C; all voltages with respect to VSSD digital ground, positive current flowing into pin (unless otherwise specified)

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| LOW level | $V_{IN(L)}$ | V | 0 | | 0.3 × VDDD | |
| HIGH level | $V_{IN(H)}$ | V | 0.7 × VDDD | | VDDD | |
| Input current (0V < $V_{IN}$<VDDD) | $I_{IN}$ | µA | -150 | | 150 | |
| Input capacitance CLK/CS_N | $C_{IN}$ | pF | 1.8 | | | |
| Input capacitance DI/DIO3 | $C_{IN}$ | pF | 3.1 | | | |
| Minimum hysteresis voltage range between 0.3*VDDD and 0.7*VDDD | $V_{HYST}$ | V | 0.175 | | | $V_{HYST\_H}$ - $V_{HYST\_L}$ |
| Upper hysteresis signal level | $V_{HYST\_H}$ | V | | 0.5 × VDDD + $V_{HYST}$ / 2 | 0.7 × VDDD | |
| Lower hysteresis signal level | $V_{HYST\_L}$ | V | 0.3 × VDDD | 0.5 × VDDD - $V_{HYST}$ / 2 | | |
| Output pad slew rate for rising wave form | $dV_{TR}$ | V/ns | 0.32 | | | 0.2 × VDDD to 0.8 × VDDD |
| Output pad slew rate for falling wave form | $dV_{TF}$ | V/ns | 0.33 | | | 0.2 × VDDD to 0.8 × VDDD |

## Data Organization and SPI Interface

**Table 25 Logic Levels for Pins IRQ, DO, DIO3** VDDD= 1.71 to 1.89 V, Tb= -20 to +70°C, ambient temperature not below -40°C; all voltages with respect to VSSD digital ground, positive current flowing into pin (unless otherwise specified)

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| LOW level | $V_{OUT(L)}$ | V | 0 | | 0.3 × VDDD | |
| HIGH level | $V_{OUT(H)}$ | V | 0.7 × VDDD | | VDDD | |
| Output current (LOW) | $I_{OUT(L)}$ | mA | -5 | | | |
| Output current (HIGH) | $I_{OUT(H)}$ | mA | | | 5 | |
| Allowed load capacitance to provide maximum signal frequency on DO | $C_{LOAD}$ | pF | | | 15 | |
| Minimum hysteresis voltage range between 0.3*VDDD and 0.7*VDDD | $V_{HYST}$ | V | 0.175 | | | $V_{HYST\_H}$ - $V_{HYST\_L}$ |
| Upper hysteresis signal level | $V_{HYST\_H}$ | V | | 0.5 × VDDD + $V_{HYST}$ / 2 | 0.7 × VDDD | |
| Lower hysteresis signal level | $V_{HYST\_L}$ | V | 0.3 × VDDD | 0.5 × VDDD - $V_{HYST}$ / 2 | | |
| Output pad slew rate for rising wave form | $dV_{TR}$ | V/ns | 0.32 | | | 0.2 × VDDD to 0.8 × VDDD |
| Output pad slew rate for falling wave form | $dV_{TF}$ | V/ns | 0.33 | | | 0.2 × VDDD to 0.8 × VDDD |

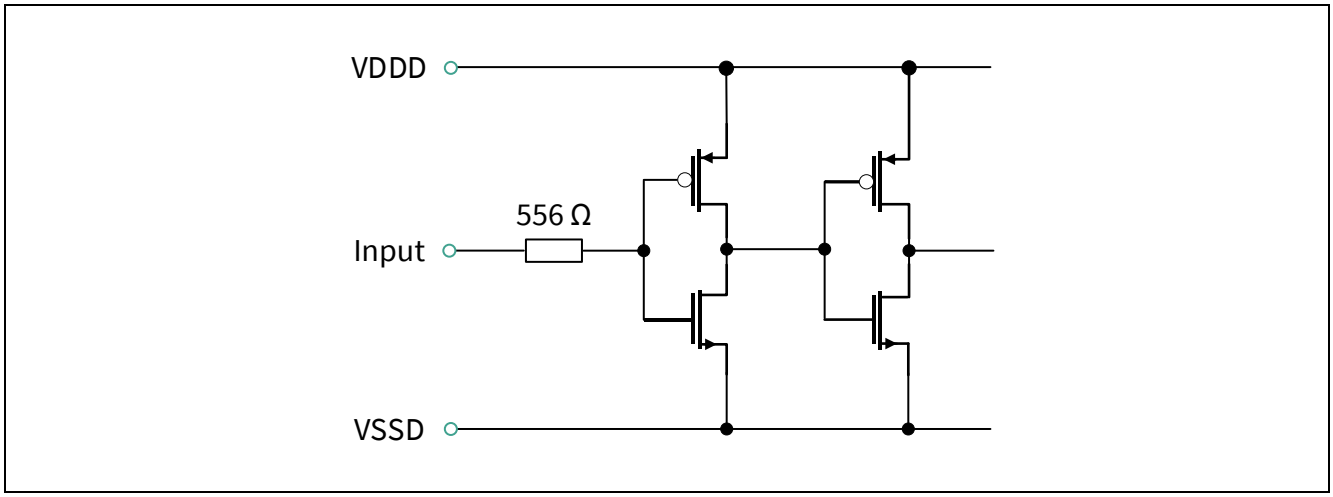


**Figure 19 Interface for input pins CLK, CS_N, DI, DIO3**

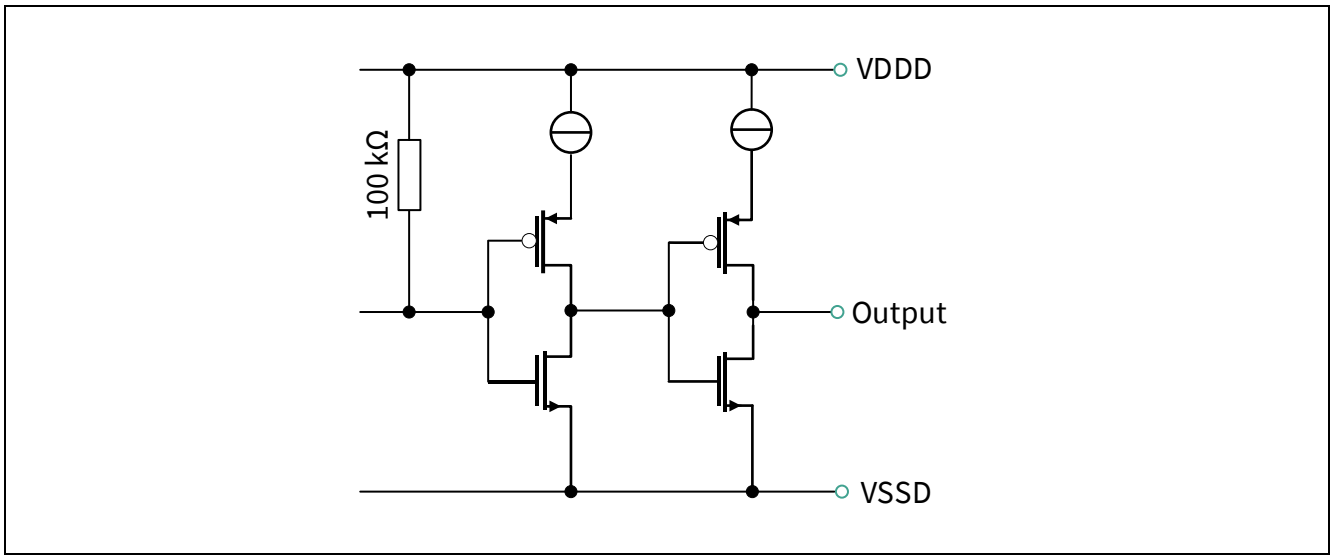


**Figure 20 Interface for output pins IRQ, DO, DIO3**

## 4.4 Overshoot and Undershoot Waveform Definition

During operation the applied signals and supply levels should not exceed absolute maximum DC levels specified in datasheet. Digital signals can have positive or negative overshoots due to inductive and/or capacitive loads. The following**Error! Reference source not found.** Table 26 reports the allowed overshoot timings and signal levels for all logic signals.

**Table 26 Overshoot and Undershoot Signal Levels**

| Spec | Symbol | Unit | Value | | | Condition |
|---|---|---|---|---|---|---|
| Parameter | | | Min | Typ | Max | |
| Maximum absolute overshoot voltage level | Vos | V | | | VDDD + 0.5 V | see Note: |
| Maximum absolute undershoot voltage level | Vus | V | | | VSS – 0.5 V | see Note:3 |

*Note:*

*Maximum pad current not exceeding ±5 mA (see also Table 25). No slew rate limitation existing on digital signals for overshoots / undershoots.*

## 4.5 IBIS Model

A BGT60TR13C IBIS Model is available under NDA upon reqest. It is based on timing simulations. In order to better reflect the real timing behavior, different pad models for input/output signals are used and summarized in Table 27. The driver strength for all pads are fix (PRG0=0).

**Table 27 IBIS Pad Types and Models** (see Ibis model)

| Pin | IBIS PAD Model |
|---|---|
| CSN | IN: MODEL_654_7345_110 |
| CLK | IN: MODEL_654_7345_110 |
| DIO0 / DI | IN: MODEL_8138_4982_52<br>OUT: MODEL_8138_4982_59 |

| Pin | IBIS PAD Model |
|---|---|
| DIO1 / DO | IN: MODEL_8138_4982_52<br>OUT: MODEL_8138_4982_59 |
| DIO2 | Not available on BGT60TR13C |
| DIO3 / Reset | IN: MODEL_8138_4982_52<br>OUT: MODEL_8138_4982_59 |
| IRQ | OUT: MODEL_8138_4982_55 |

## 4.6 SPI Functionality

Each word transferred over the SPI bus has a length of 1 command byte + 3 data Bytes. The communication is done bitwise. First the address is transferred with MSB first. The address is followed by the R/W-bit and then followed by the data which is sent MSB first, too. At the same time, while command byte is received, a freely from system level configurative global status register (8 bits, GSR0) is serial shifted out on DO (MSB first). On the following 24 clock cycles the selected register content is shifted out on DO, MSB first.
Depending on sent R/W-bit there are two different operation modes available, the write mode and the read mode. Every write mode is a read mode too.

**Write-Mode**
After the start condition the desired address is sent. The address is 7 bits long followed by a bit that is a data direction bit (read/write). A one indicates a write operation (see Figure 21).

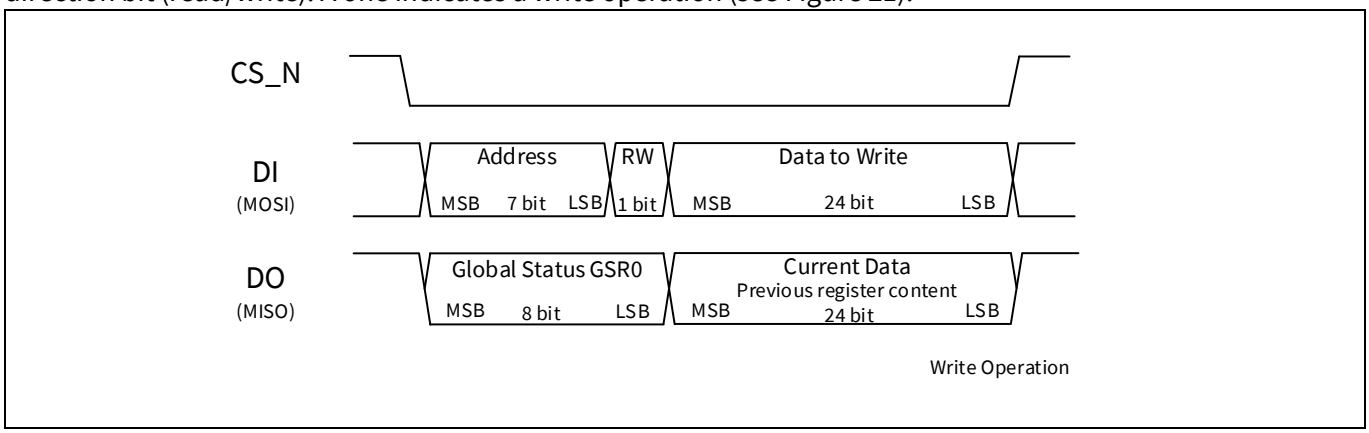


**Figure 21 SPI timing write mode**

**Read-Mode**
After the start condition, the desired address is sent like in the write operation. A zero of the R/W-bit indicates a read access. The data on DI after the command byte may contain any value. The DO behavior is the same as in write mode.

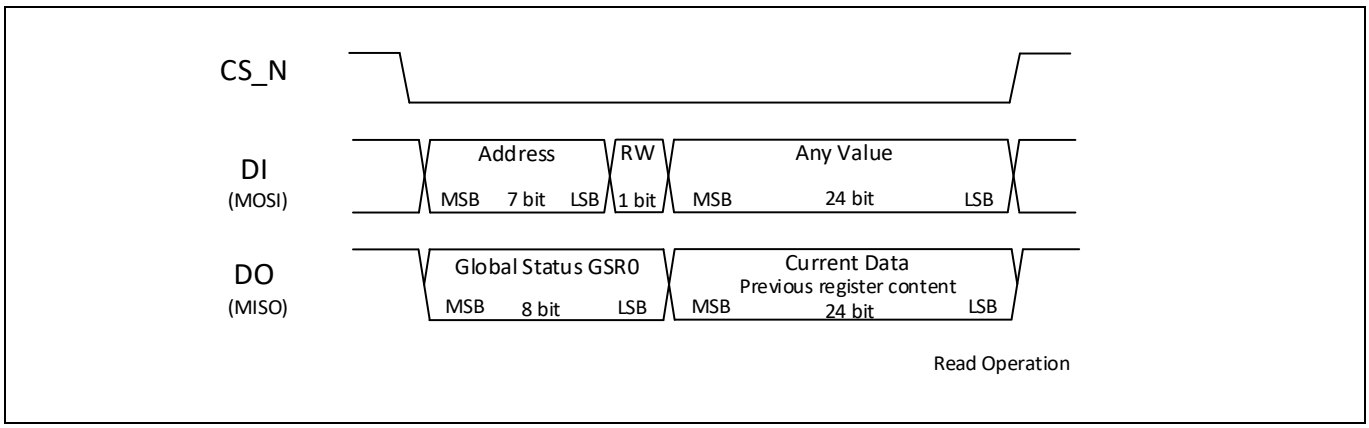


**Figure 22 SPI timing read mode**

## 4.7 SPI Burst Mode

The burst mode can be used to read or write out several registers or some data from the FIFO instead of reading just single registers or data. The burst mode command is sent by the host. The burst mode command consists of several bit fields and is shown in Figure 23.

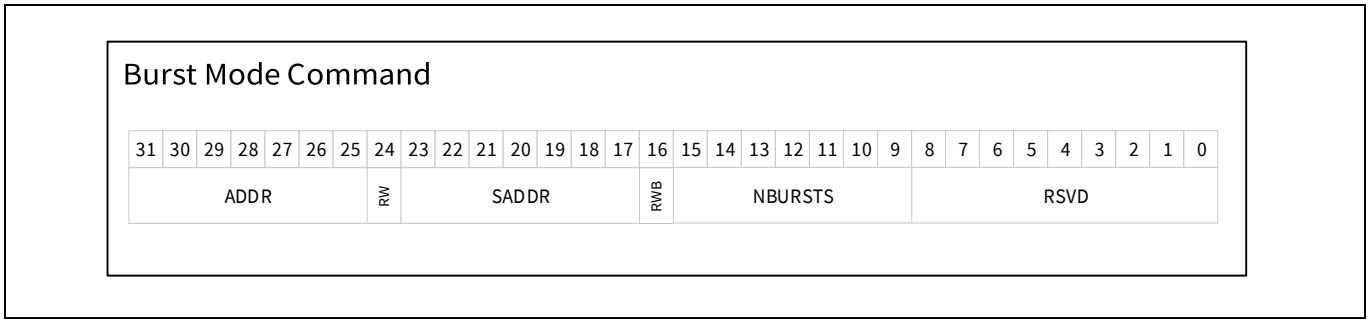


**Figure 23 Burst mode command**

The following Table 28 shows a detailed description on the burst mode command bit fields.

**Table 28 Burst Mode Command Bit Field Description**

| Bit field | Bit | Description | RST |
|---|---|---|---|
| ADDR | 31:25 | To enter the burst mode the following address is used:<br>0x7F … request the burst read/write. | |
| RW | 24 | Read/Write register access:<br>Fixed to $1_B$ … write to address 0x7F | |
| SADDR | 23:17 | Starting address where the burst starts processing:<br>< 0x60 Register access<br>== 0x60 FIFO access<br>> 0x60 Reserved<br>- Address is incremented automatically inside a burst. | |
| RWB | 16 | Burst read or write:<br>$0_B$ … Perform a read burst<br>$1_B$ … Perform a write burst, (writes to FIFO not supported) | |
| NBURSTS | 15:9 | Number of processed data blocks:<br>0x00… “unbounded” burst accesses | |

| Bit field | Bit | Description | RST |
|---|---|---|---|
| | | 0x01 to 0x7E … number of words to transfer | |

*Note:*

*A single data block is 24 bits width for both, the sampling memory and the registers.*

### Burst Mode Operation

After the start condition the 32 bits burst mode command is sent from the SPI master on DI. At the same time, the status register GSR0 (four $1_B$ bits + four status bits) followed by 24 padding bits set to 0B is shifted out on DO. After the command sequence is done, the register/FIFO data is shifted out to the SPI master on DO. In burst write mode, the register data to be written is shifted in from the SPI master (application processor e.g.).

### Burst Mode Read Sequence:

In the read sequence, the SPI master reads from the device.

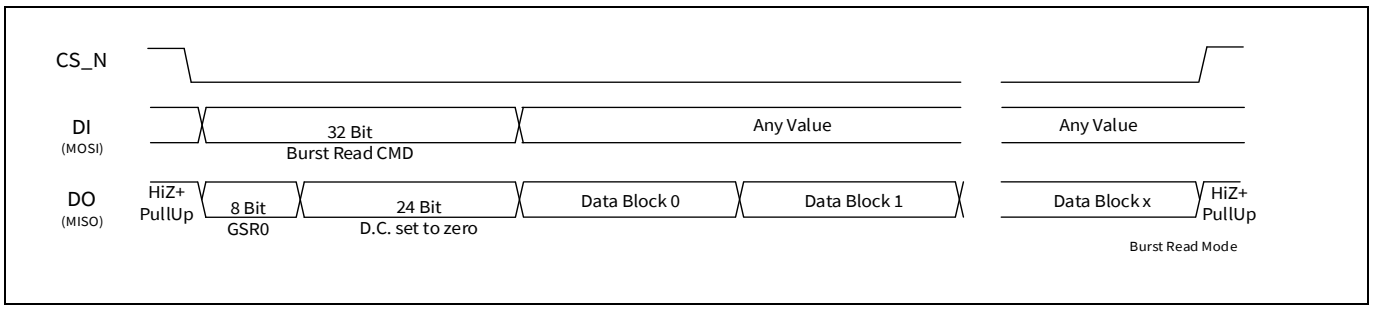


**Figure 24 Burst mode read sequence**

### Burst Mode Write Sequence:

In the burst write mode, the SPI master writes to the device.

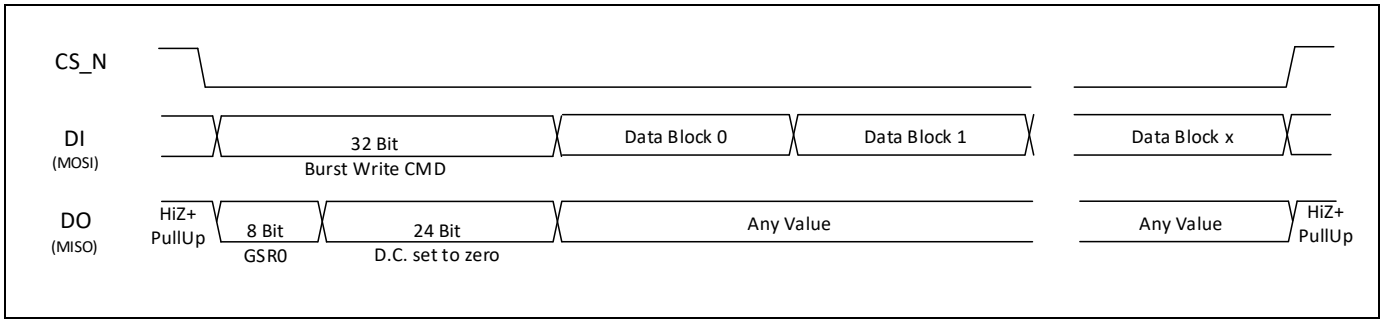


**Figure 25 Burst mode write sequence**

### Sampling Data Arrangements in Data Blocks

The data from the FIFO are streamed out during the burst read request, starting from the FIFO address zero. The 1st ADC is the ADC channel with the lowest channel number. As far as the sampling memory is organized in 24 bits and up to three ADC channels are selectable through the ADC channel selection bits, the data blocks are arranged as follows.

In case a single ADC is selected the data blocks are shown in Figure 26.

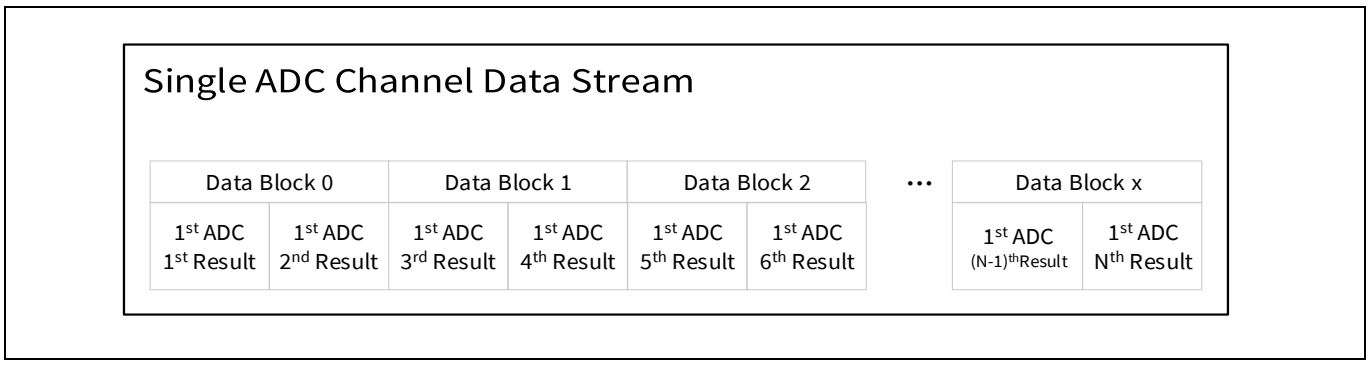


**Figure 26 Single ADC channel selected**

In case two ADCs are selected the data blocks are arranged as shown in Figure 27.

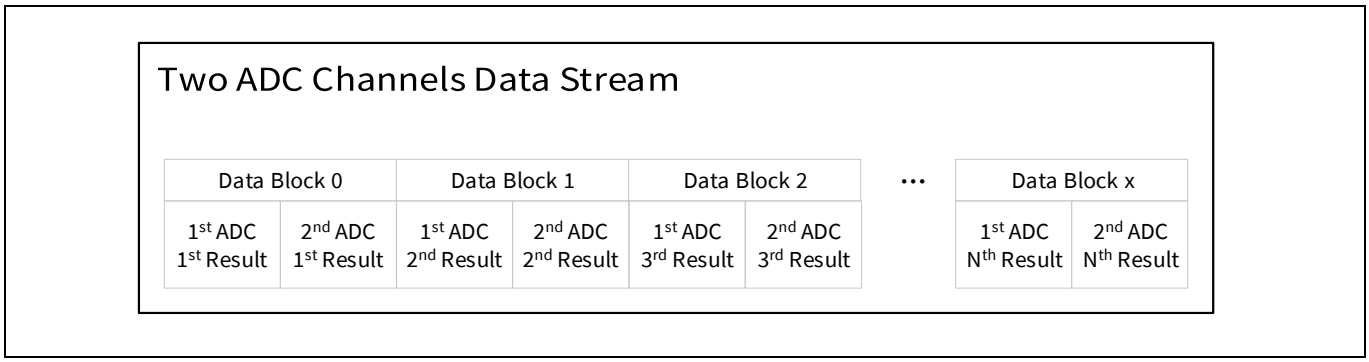


**Figure 27 Two ADC channels selected**

In case three ADCs are selected the data blocks are arranged as shown in Figure 28.

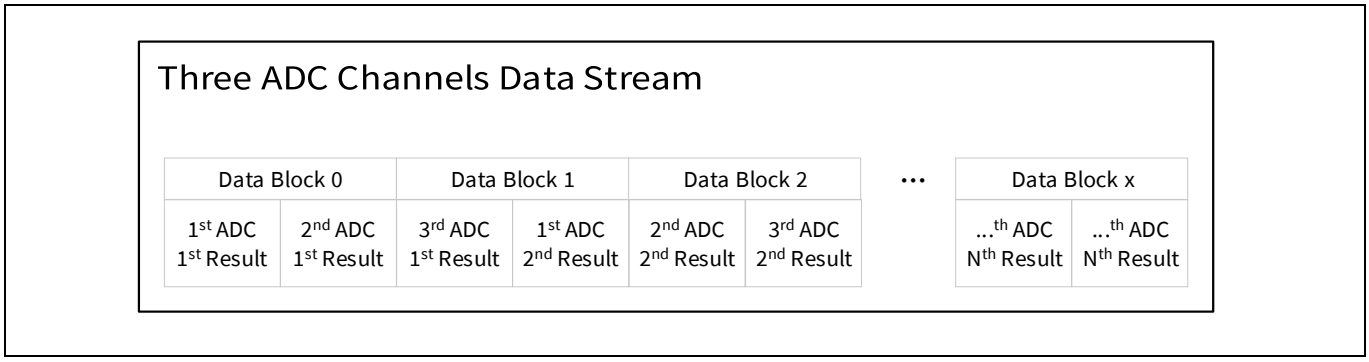


**Figure 28 Three ADC channels selected**

**Example: Burst Mode Read Sampling Memory Sequence**

The following burst mode command is sent from the host to initialize the burst mode to read from the FIFO an undefined number of sampling data:

BMCMD_RS = (ADDR = 0x7F, RW = 0x01, SADDR = 0x60, RWB = 0x0, NBURSTS = 0)

**REMARK:**

For each burst read request to the sampling memory, the sampling-memory address pointer is reset to the initial value. So that memory can be read out from the beginning until the application processor stops burst reading.

## Data Organization and SPI Interface

**Example: Burst Mode Read Registers Sequence**

The following burst mode command is sent from the host to initialize the burst mode to read out 10 registers starting from register address 3:

BMCMD_RR10 = (ADDR = 0x7F, RW = 0x01, SADDR = 0x3, RWB = 0x0, NBURSTS =10)

## 4.8 SPI Error Detection

SPI BURST_ERR and CLK_NUM_ERR (see also Table 19) will be cleared after these resets:

- SW reset
- HW reset

SPI BURST_ERR and CLK_NUM_ERR are reported in the global status bits of the next SPI transaction and latched as sticky bits in the FSTAT register.

In order to understand if the captured sample data are corrupted, the host can evaluate the bit field CLK_NUM_ERR and SPI BURST_ERR as reported in Table 29.

**Table 29 SPI BURST_ERR and CLK_NUM_ERR Definitions**

| Length Range | Transaction | SPI BURST_ERR | CLK_NUM_ERR | Behavior on read/write |
|---|---|---|---|---|
| 0 | Null command | $0_B$ | $0_B$ | Ignored |
| 1-31 | Short length error in single | $0_B$ | $1_B$ | Command ignored |
| >32 | Long length error in single | $0_B$ | $1_B$ | Extra bits ignored |
| 1-31 | Short length error in SPI burst header | $0_B$ | $1_B$ | Command ignored |
| <24xN | Missing whole data word in bounded burst | $1_B$ | $0_B$ | Available data words used |
| >24xN | Extra whole data word in bounded burst | $1_B$ | 0 | Extra data word(s) ignored |
| %24>0 | Misaligned bit-count for bounded burst | $1_B$ | $1_B$ | Extra bits ignored |
| %24>0 | Misaligned bit-count for infinite burst | $0_B$ | $1_B$ | Partial data word may be discarded |

*Note:*

- *Ignored write transaction means that no register (or memory) content is affected by the partial write command, or incomplete data word.*
- *Ignored read transaction means that the returned data is invalid, and for the FIFO no words are removed by the partial read command, or incomplete data word.*
- *Discarded read transaction means that the data is already read from the FIFO but only partially transferred; subsequent read pops next word from FIFO.*
- *Data from the FIFO may be discarded after a length error in the infinite burst (NBURST=0) occurs. The FIFO read has to happen, since at that stage the data is required to be shifted out, but if not all bits are shifted out the FIFO is already read and the partial data word may be discarded.*

# Data Organization and SPI Interface

## 4.9 Hardware Reset Sequence

The After power up, the chip is not in a default reset condition and requires a dedicated HW reset as described below. Only after the HW reset also other reset sequences can be triggered via SPI (e.g. SW, FIFO and FSM- reset). For such SPI triggered resets an external OSC_CLK (see Table 2) needs to be applied, while the HW reset does not require any external OSC_CLK.

HW Reset Sequence: While CS_N is = '$1_B$' DIO3 must perform a $1_B \rightarrow 0_B \rightarrow 1_B$ transition

The behavior is presented in Figure 29 with:

T_CS_BRES = 100 ns

T_RES = 100 ns

T_CS_ARES = 100 ns

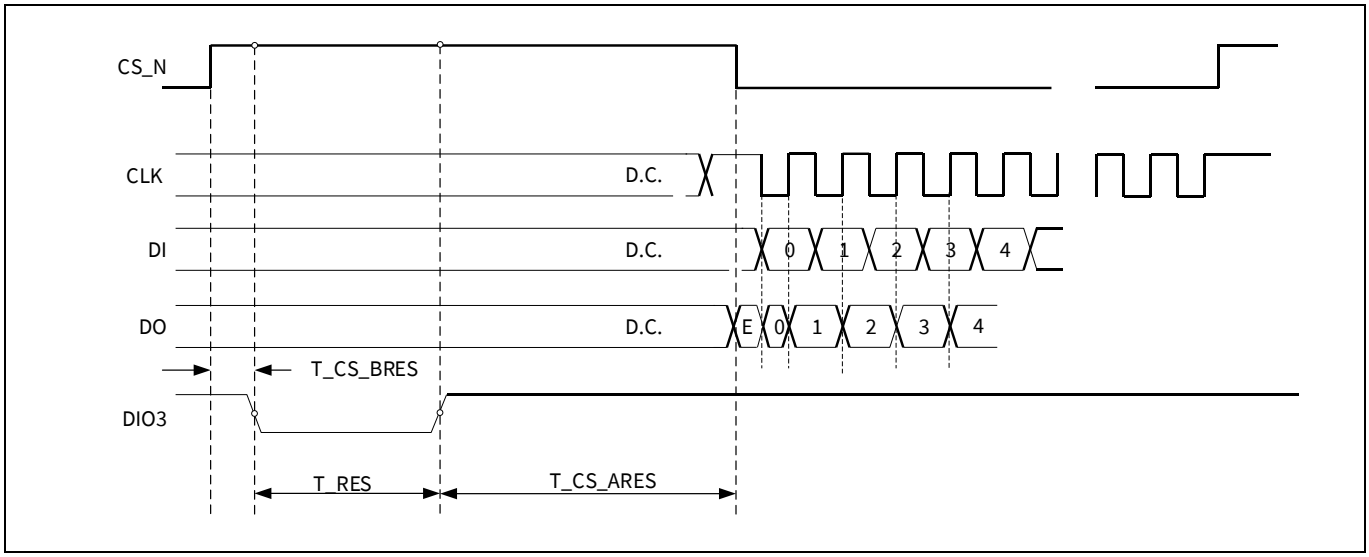


**Figure 29 Hardware reset Sequence**

## 4.10 Software Triggered Resets

Besides the hard reset, three reset sequences are supported and can be triggered in the ISO register. They are defined according to the following hierarchy:

Soft reset → FIFO reset → FSM reset

* **Software Reset**
  - Resets all registers to default state
  - Resets all internal counters (shape, frame e.g. )
  - Perform FIFO reset
  - Performs FSM reset
  - A delay of 100 ns after the SW_RESET is needed before the next SPI command is sent

* **FIFO Reset**
  - Reset the read and write pointers of the FIFO

- Array content will not be reset, but cannot be read out
- FIFO empty is signaled, filling status = 0
- Resets register FSTAT
- Performs an implicit FSM reset

* **FSM Reset**

- Resets FSM to deep sleep mode
- Resets FSM internal counters for channel/shape set and timers
- Resets STAT0 and STAT1 register
- Reset PLL ramp start signal
- Reset PA_ON
- Terminates frame (shape and frame counters incremented although maybe not complete)

## 4.11 IRQ Output

BGT60TR13C provides one interrupt pin output (IRQ). In default mode, the IRQ signal is used to monitor the filling level of the FIFO as described below.

**IRQ status definition:**

- IRQ is high after:
  - CS_N goes high and FSTAT:FILL_STATUS >= SFCTL:FIFO_CREF (see also 3.4 and 3.6).
- IRQ is low (as a consequence of):
  - CS_N goes high and FSTAT:FILL_STATUS < SFCTL:FIFO_CREF (see also 3.4 and 3.6).
  - or CS_N is active low

The following figure shows the IRQ signal in case of FIFO-burst reads.

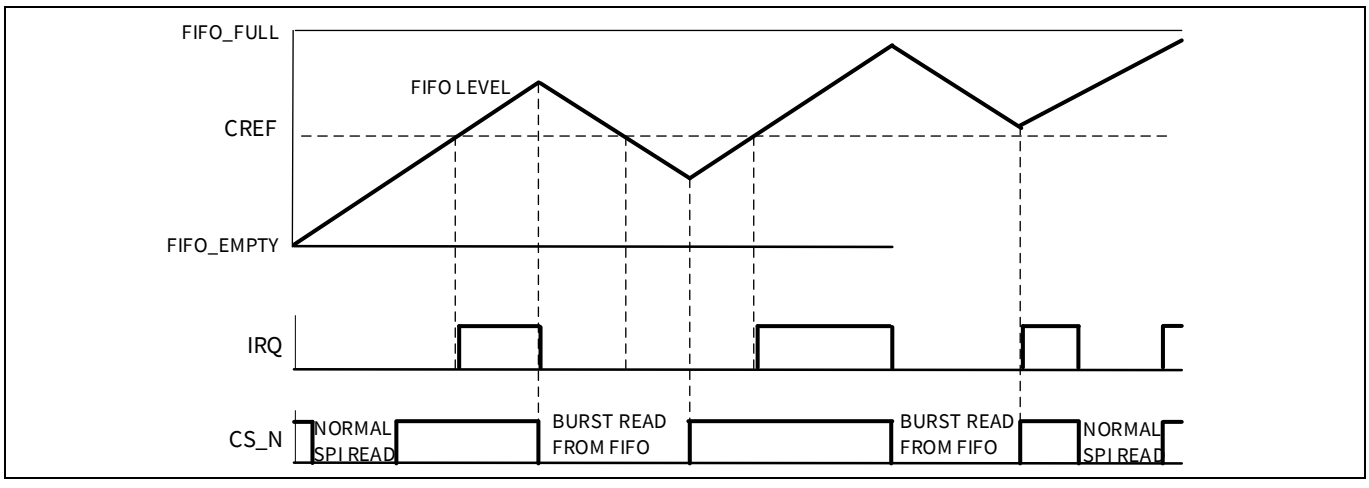


**Figure 30 IRQ status behavior during radar mode with FSM capturing data**

# 5 Package

The BGT60TR13C chipset is housed in a laminate package with solder balls of 300 µm diameter and a standoff of 240 µm. According to IPC/JEDEC's J-STD0, the moisture sensitivity level (MSL) is 3. Figure 31 shows the top view of BGT60TR13C package and its physical dimension. The bottom view is presented in Figure 32. The package size is 6.5 x 5 x 0.9 $mm^3$ with ball pitch of 500 µm. Package outline is reported on Figure 33. Package name: PG-VF2BGA40-1.

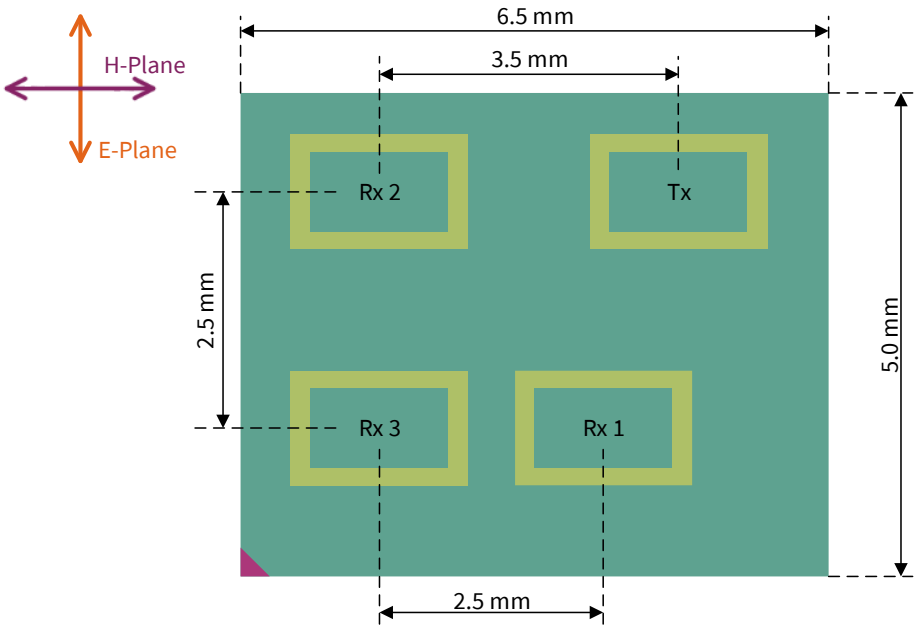


**Figure 31 Top view of BGT60TR13C**

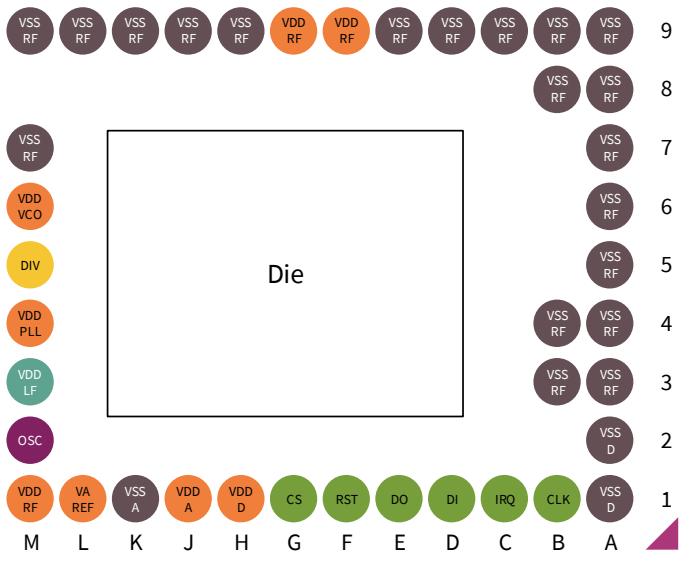


**Figure 32 Bottom view of BGT60TR13C**

# Package

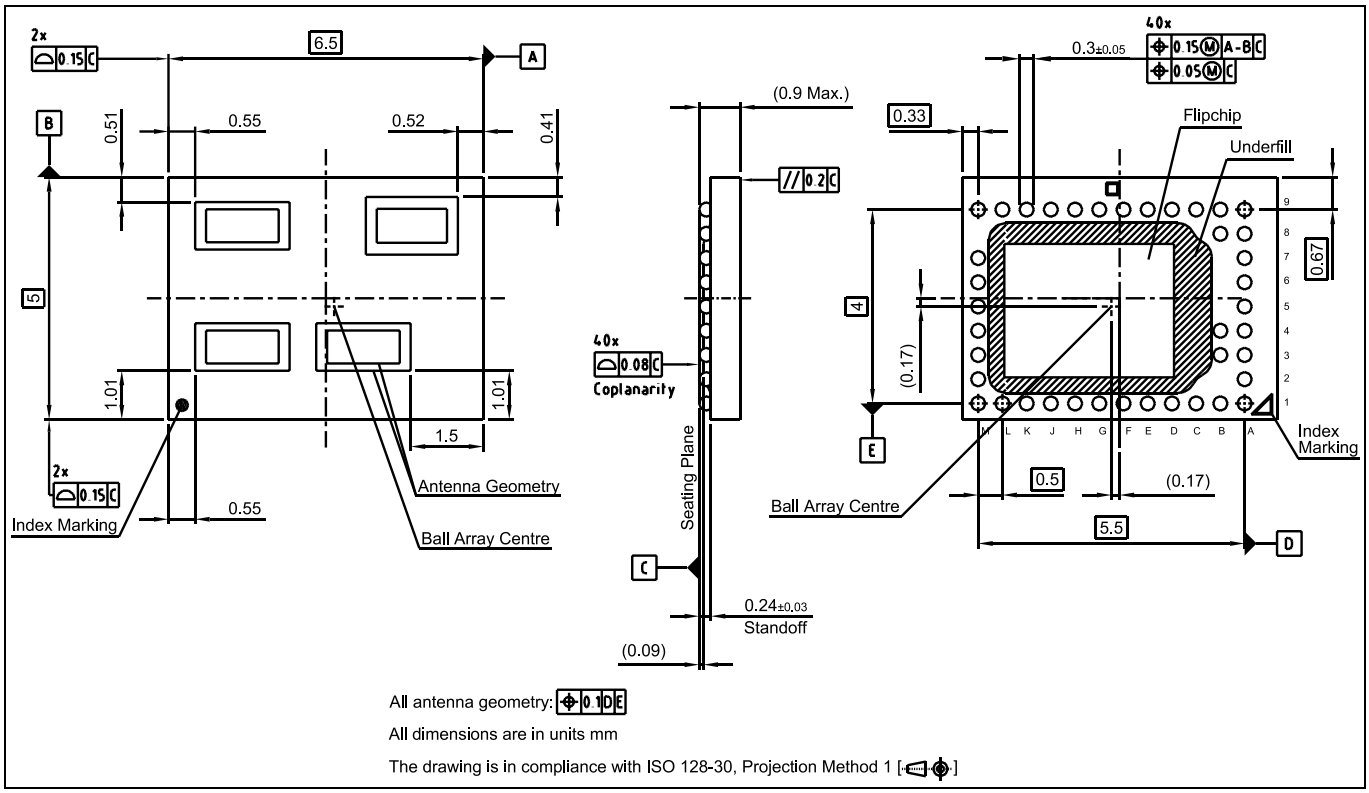


**Figure 33 Package outline PG-VF2BGA-40-1**

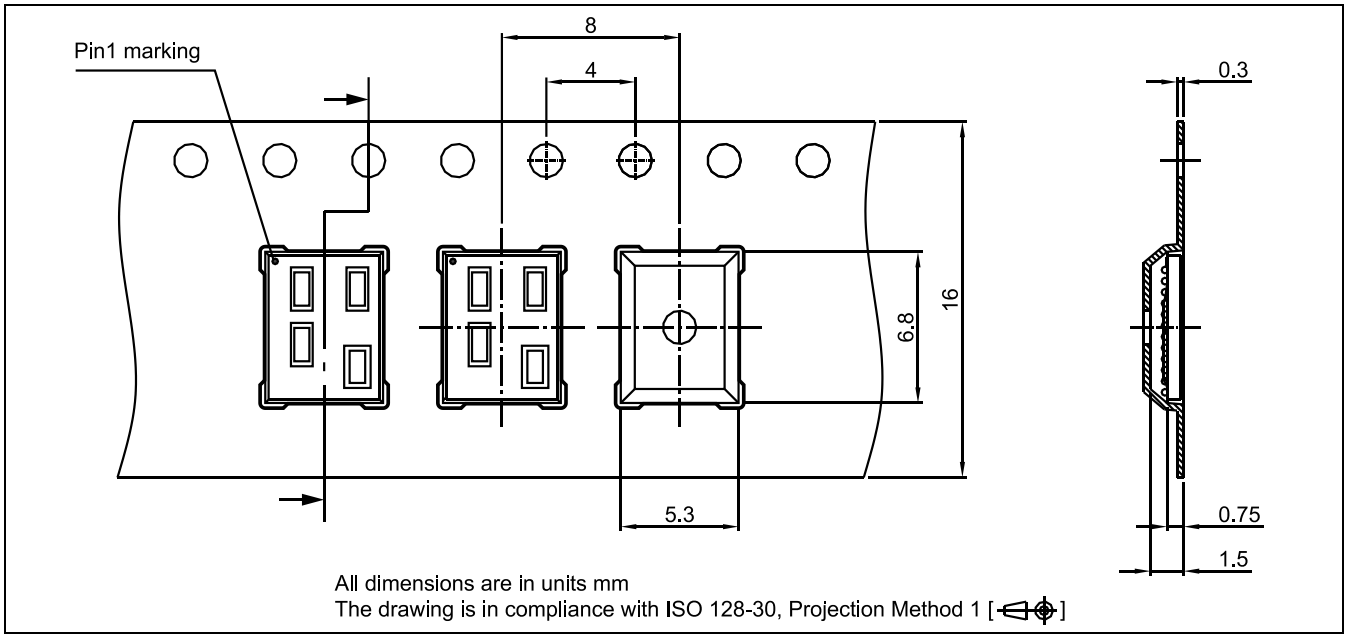


**Figure 34 Tape of PG-VF2BGA-40-1**

## Package

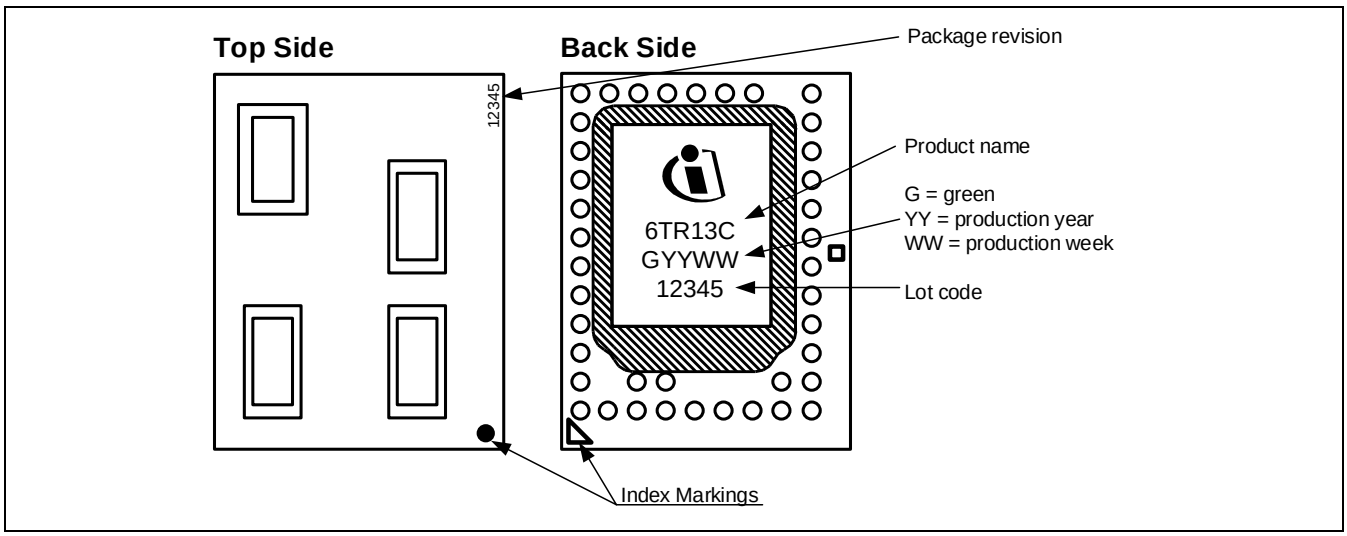


**Figure 35 Marking layout of PG-VF2BGA-40-1 (example)**

## 5.1 Built-in Antenna Specifications

Antenna performance reported in Table 30 are guaranteed by design. Typical antenna behavior is measured on Infineon reference board. Typical antenna beam plots are available in a specific application note and upon specific request.

**Table 30 Antennas In Package Specifications**

| Spec | Unit | Value | | | Condition |
|---|---|---|---|---|---|
| Parameter | | Min | Typ | Max | |
| RX_BW, TX_BW | GHz | 58.0 | | 63.5 | Antenna bandwidth |
| GTX | dBi | 2.0 | 3.5 | 5.0 | Antenna gain of a single TX antenna |
| GRX | dBi | 2.0 | 3.5 | 5.0 | Antenna gain of a single RX antenna |
| HPBW_RX_E | Deg | 50 | 65 | 80 | Half-power beam width of a single RX antenna in the E-plane direction |
| HPBW_RX_H | Deg | 20 | 35 | 50 | Half-power beam width of a single RX antenna in the H-plane direction. |
| HPBW_TX_E | Deg | 50 | 65 | 80 | Half-power beam width of a single TX antenna in the E-plane direction |
| HPBW_TX_H | Deg | 25 | 40 | 55 | Half-power beam width of a single TX antenna in the H-plane direction |
| D_RX_RX | mm | | 2.5 | | Center-to-center distance between RX antennas in X and Y direction |

# 6 Abbreviations

**Table 31 Abbreviations**

| Symbol | Description |
|---|---|
| AAF | Anti-aliasing filter |
| ADC | Analog to digital converter |
| AP | Application Processor |
| DAC | Digital to analog converter |
| ESD | Electrostatic discharge |
| FMCW | Frequency modulated continuous wave |
| HBM | Human body model (related to ESD) |
| CDM | Charge device model (related to ESD) |
| HPF | High pass filter |
| IC | Integrated circuit |
| LPF | Low pass filter |
| MCU | Microcontroller Unit |
| PLL | Phase locked loop integrated circuit |
| RF | Radio Frequency |
| RSVD | Reserved |
| RX | Receiver |
| SPI | Serial peripheral interface |
| TX | Transmitter |
| LDO | Low dropout voltage regulator |
| RST | Reset or Default setting |
| MSB | Most significant bit |
| LSB | Least significant bit |

# 7 Revision History

| Document version | Date of release | Description of changes |
|---|---|---|
| 2.4.6 | 2021-01-08 | First Version |

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