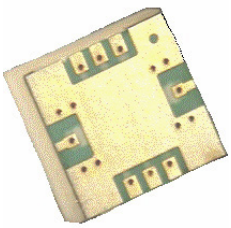
AMMP-6125

10-24 GHz x2 Frequency Multiplier

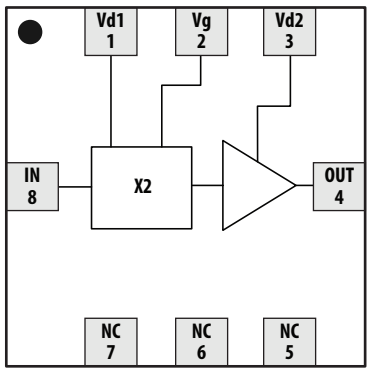
Data Sheet



Description

The AMMP-6125 is an easy-to-use surface mounted packaged integrated frequency multiplier (x2) that operates from 10 to 24 GHz output frequency. It has integrated amplification, matching, harmonic suppression, and bias networks. 15 dBc min. of harmonic rejection is delivered. The input/output are matched to 50 Ω and fully DC blocked. This MMIC is a cost effective alternative to hybrid (discrete-FET) amplifiers that require complex tuning and assembly process.

Functional Block Diagram



Pin	Function
1	Vd1
2	Vg
3	Vd2
4	RF_OUT
5	NC
6	NC
7	NC
8	RF_IN

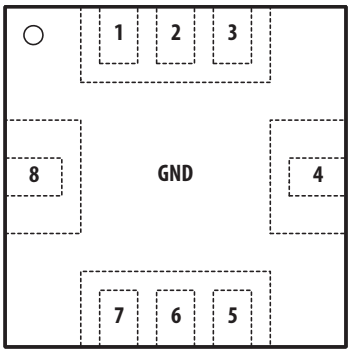
Features

- 5 x 5 mm surface mount package
- Wide frequency operation: 10-24 GHz (Output)
- 50 Ω Input and Output Match
- –40° C to +85° C operation
- Output Power of +21.5 dBm Typical
- Fo, 3xFo, 4Fo Rejection: 15 dBc min

Applications

- Microwave Radio Systems
- VSAT
- Satellite Up/Down Link
- Test Equipment

Package Diagram



TOP VIEW

Attention: Observe Precautions for handling electrostatic sensitive devices.
ESD Machine Model: 40V
ESD Human Body Model: 150V
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

ELECTRICAL SPECIFICATIONS

Table 1. Absolute Maximum Ratings

Parameter		Specifications			
Description		**Min.**	**Max.**	**Unit**	**Comments**
Drain Voltage	Vd1		5	V	
	Vd2		6	V	
Gate Voltage	Vg	-2.5	0	V	
CW Input Power			10	dBm	
MSL			MSL2		
Channel Temperature			150	°C	
Storage Temperature		-45	150	°C	

Table 2. Recommended Operating Range

Parameter			Specifications				
Description		**Pin**	**Min.**	**Typical**	**Max.**	**Unit**	**Comments**
Drain Voltage		Vd1		3.5	4.0	V	
		Vd2		5.0	5.5	V	
Gate Voltage		Vg	-1.4	-1.2	-1	V	
Frequency range		Input	5		12	GHz	
		Output	10		24	GHz	
Input Power			-6	0	+4	dBm	
Quiescent Current		I_{dsq1}		100		mA	Vd1 = 3.5 V
		I_{dsq2}		110		mA	Vd2 = 5 V
Thermal Resistance, θ_{ch-b}				26.4		°C/W	
Case Temperature			-40		+85	°C	
ESD	Human Body Model			150	V		
	Machine Model			40	V		

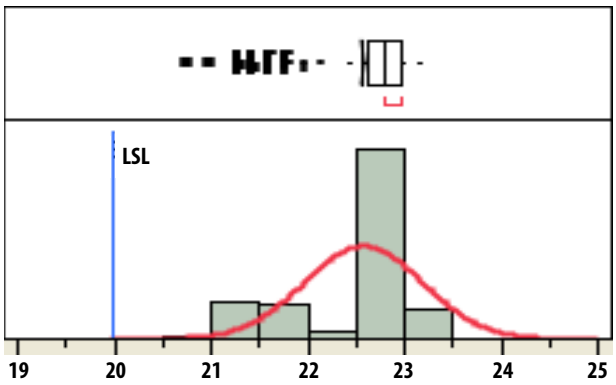
Table 3. RF Electrical Characteristics

All data measured on a Rogers 4003 demo board at Vd1 = 3.5 V, Vd2 = 5 V, Vg = -1.2 V, T_A = 25°C, Pin = 0 dBm and 50 Ω at all ports, unless otherwise specified.

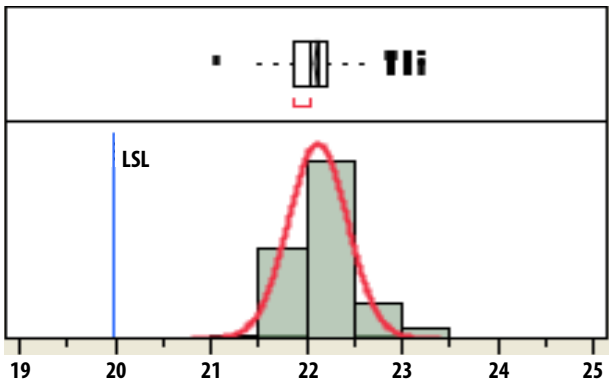
		Performance				
Parameter		**Min.**	**Typical**	**Max.**	**Unit**	**Comments**
Output Power	Freq = 10 GHz Freq = 17 GHz Freq = 24 GHz	20	22.8 22.1 21.5		dBm	
Fundamental Suppression	Freq = 5 GHz Freq = 8.5 GHz Freq = 12 GHz	15	21 25.9 29.5		dBc	f_{in} = 5, 8.5, 12 GHz
3rd Harmonic Suppression	Freq = 15 GHz Freq = 25.5 GHz Freq = 36 GHz	15	18.3 27.2 25.2		dBc	f_{in} = 5, 8.5, 12 GHz
4th Harmonic Suppression			15		dBc	
Input Return Loss			-12		dB	
Output Return Loss			-10		dB	
Drain Current	Id1		115		mA	P_{out} = 21 dBm
	Id2		145		mA	
Gate Current (Ig)			-5		µA	

Note:
1. Output Power, Fundamental Suppression and 3rd Harmonic Suppression measurement accuracy is subjected to the tolerance of ± 0.5 dBm, ± 1 dBc & ± 1 dBc respectively.

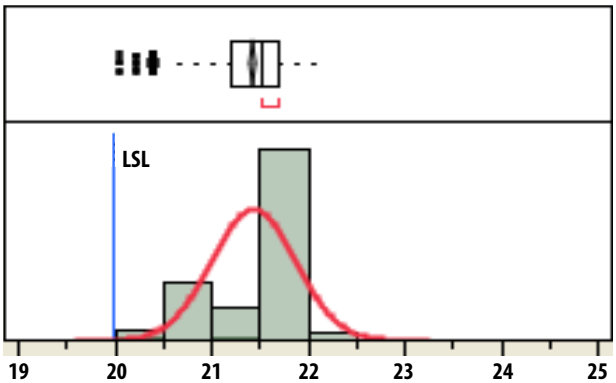
Product Consistency Distribution Charts at 5 GHz, 8.5 GHz and 12 GHz, Vd1 = 3.5 V, Vd2 = 5 V, Vg = -1.2 V (Sample size of 2,800 pieces)



Pout @ 10 GHz, Mean = 22.8 dBm, LSL = 20 dBm

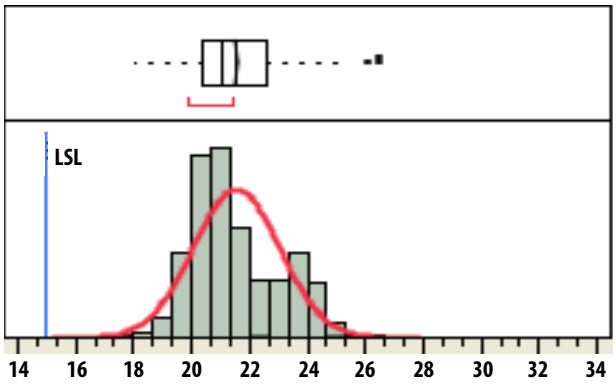


Pout @ 17 GHz, Mean = 22.1 dBm, LSL = 20 dBm

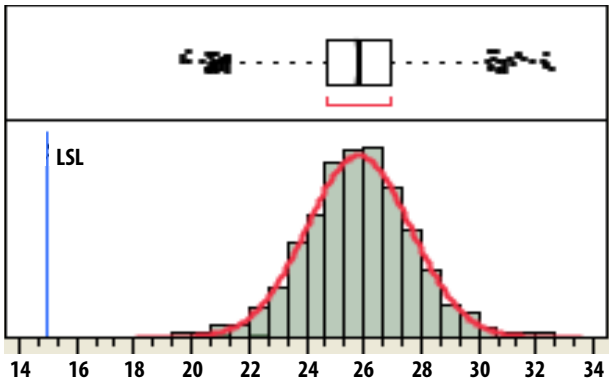


Pout @ 24 GHz, Mean = 21.5 dBm, LSL = 20 dBm

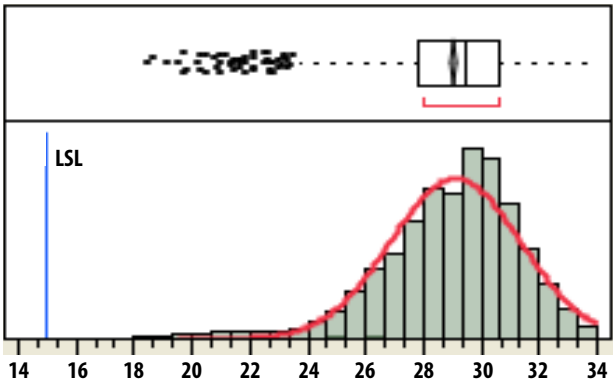
Product Consistency Distribution Charts at 5 GHz, 8.5 GHz and 12 GHz, Vd1 = 3.5 V, Vd2 = 5 V, Vg = -1.2 V (Sample size of 2,800 pieces) (Continued)



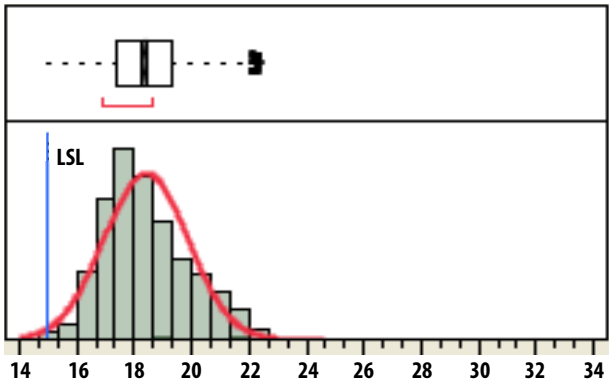
FS @ 5 GHz, Mean = 21 dBc, LSL = 15 dBc



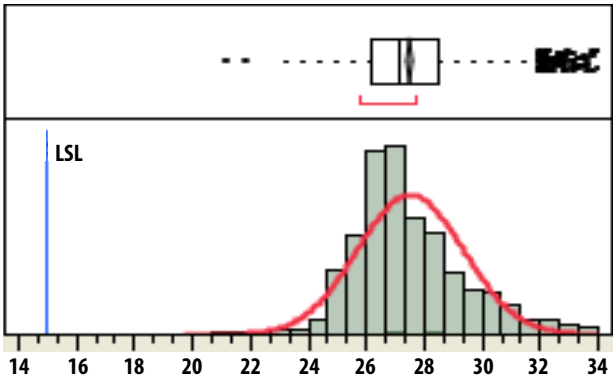
FS @ 8.5 GHz, Mean = 25.9 dBc, LSL = 15 dBc



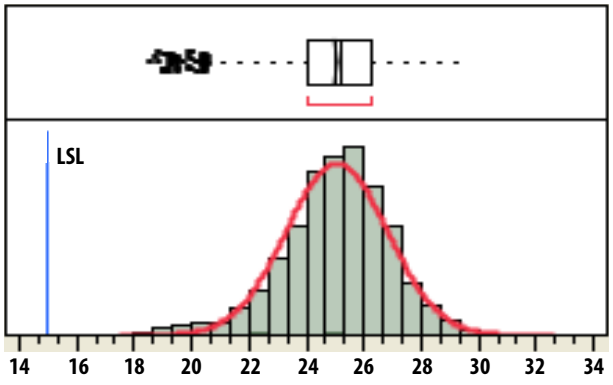
FS @ 12 GHz, Mean = 29.5 dBc, LSL = 15 dBc



Harmonics @ 15 GHz, Mean = 18.3 dBc, LSL = 15 dBc



Harmonics @ 25.5 GHz, Mean = 27.2 dBc, LSL = 15 dBc



Harmonics @ 36 GHz, Mean = 25.2 dBc, LSL = 15 dBc

Selected performance plots

All data measured on a Rogers 4003 demo board at Vd1 = 3.5 V, Vd2 = 5 V, Vg = -1.2 V, T_A = 25° C, Pin = 0 dBm and 50 Ω at all ports, unless otherwise specified.

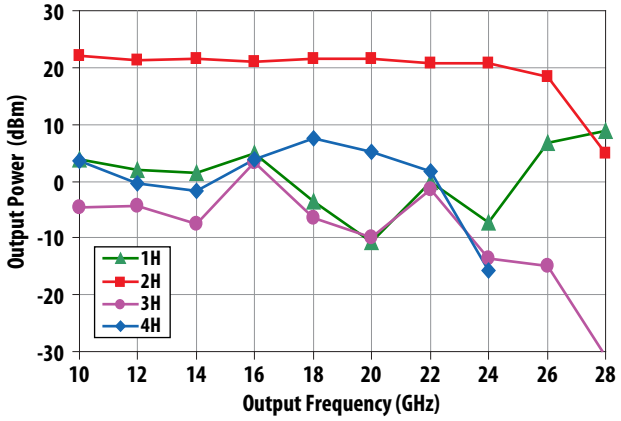


Figure 1. Output Power vs. Output Frequency @ Pin = 0 dBm

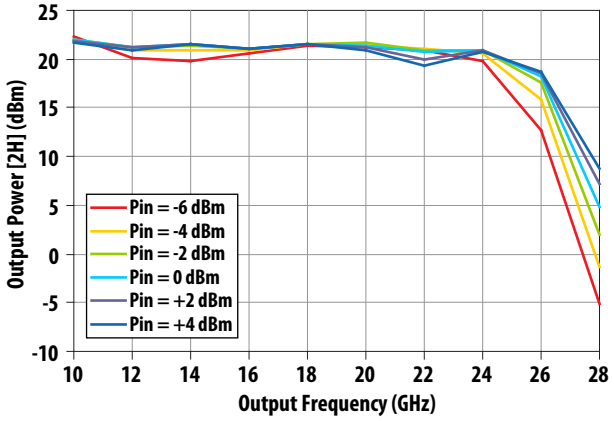


Figure 2. Output Power [2H] vs Output Frequency Over Pin

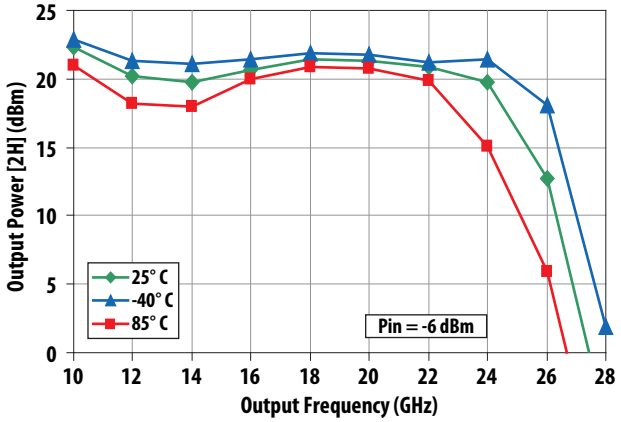


Figure 3. Output Power vs. Output Frequency @ Pin = -6 dBm over Temperature

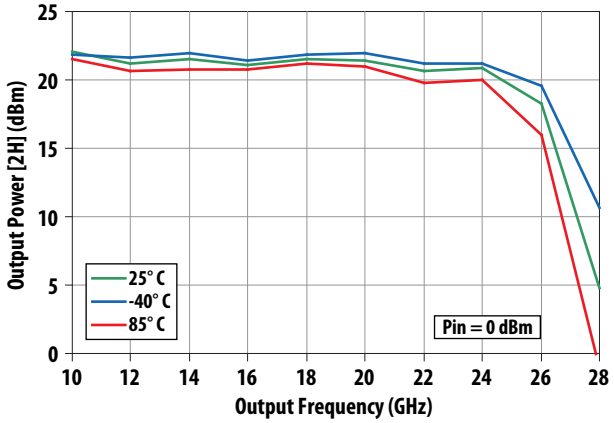


Figure 4. Output Power vs. Output Frequency @ Pin = 0 dBm over Temperature

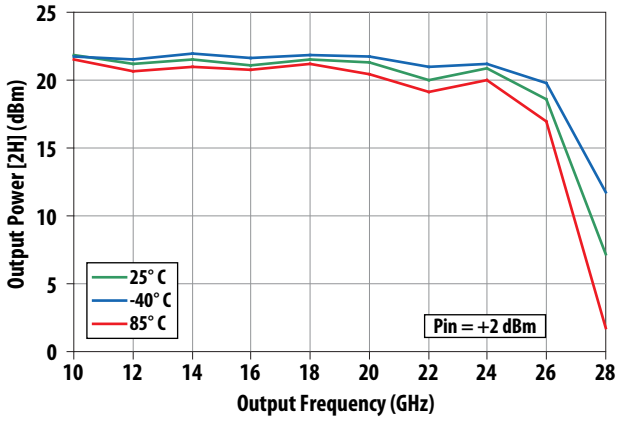


Figure 5. Output Power vs. Output Frequency @ Pin = +2 dBm over Temperature

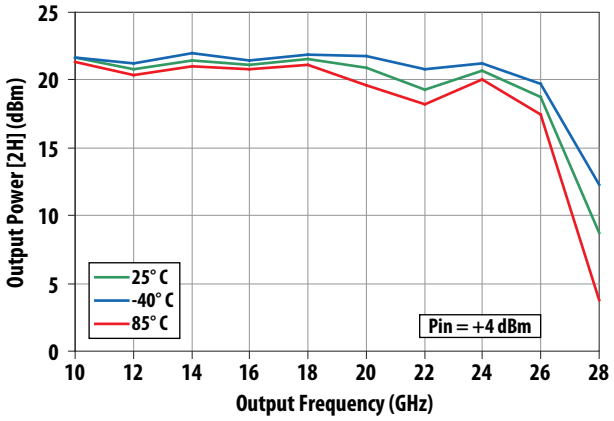


Figure 6. Output Power vs. Output Frequency @ Pin = +4 dBm over Temperature

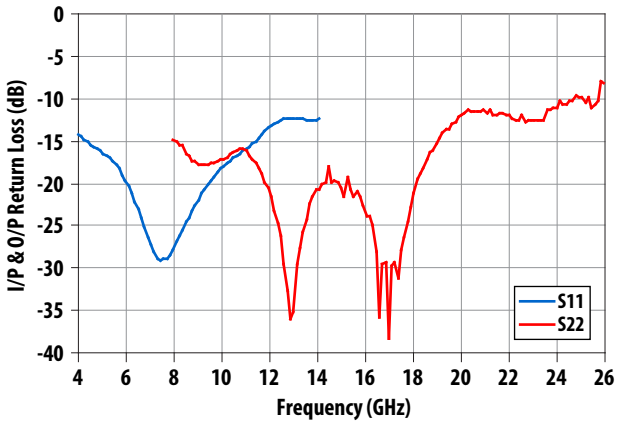


Figure 7. Input and Output Return Loss at Pin = 0 dBm

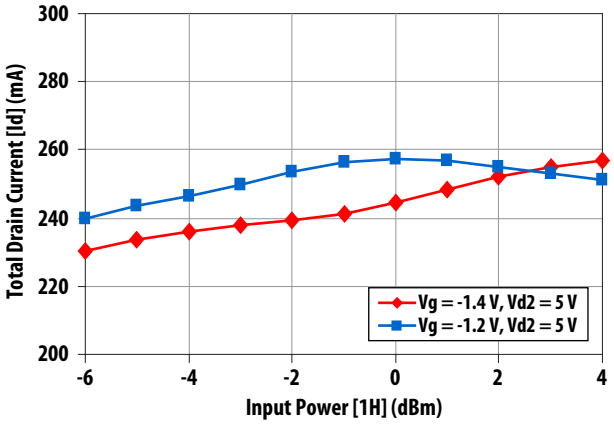


Figure 8. Total Drain Current vs. Pin

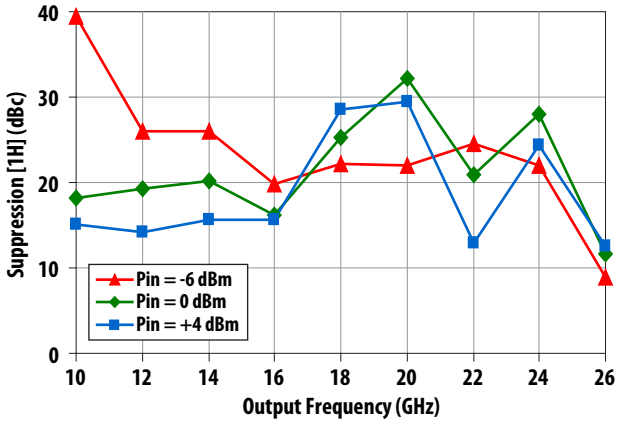


Figure 9. Fundamental [1H] Suppression vs Output Frequency at Variable Pin

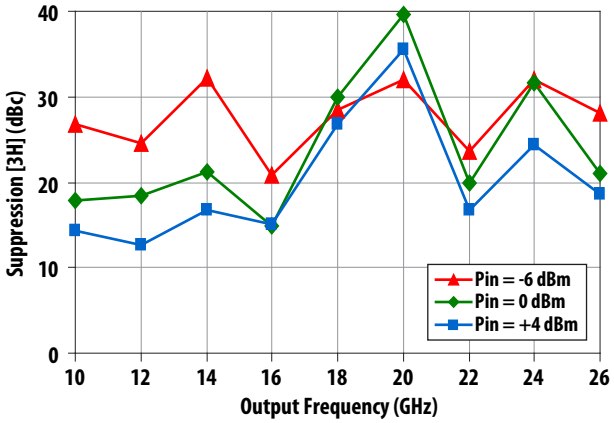


Figure 10. 3rd Harmonic [3H] Suppression vs Output Frequency at Variable Pin

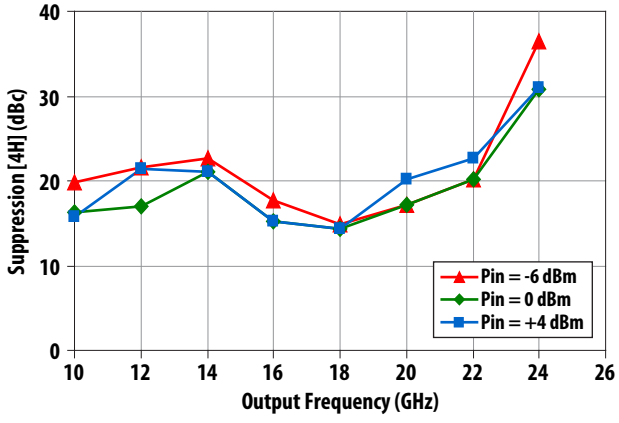


Figure 11. 4th Harmonic [4H] Suppression vs Output Frequency at Variable Pin

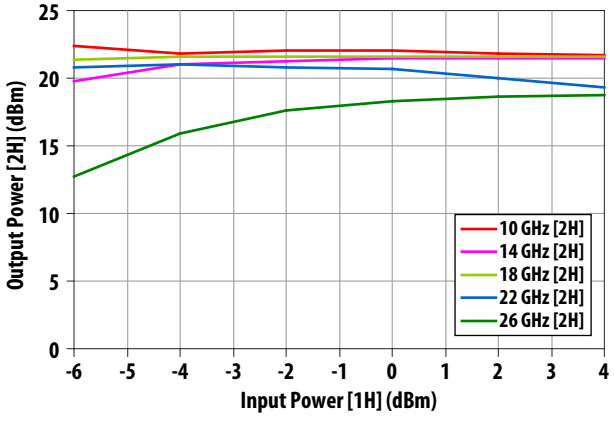


Figure 12. Output Power [2H] vs Pin at variable Output Frequency

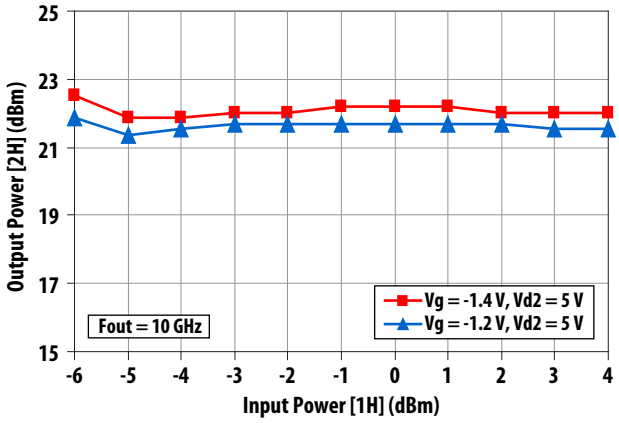


Figure 13. Output Power [2H] vs Input Power @ Fout = 10 GHz

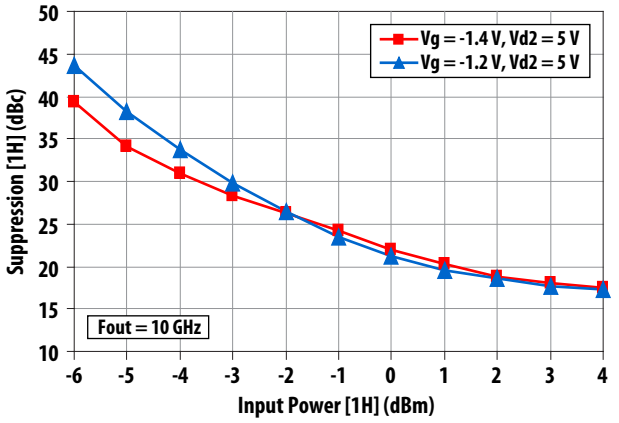


Figure 14. Fundamental Suppression [1H] vs Input Power @ Fout = 10 GHz

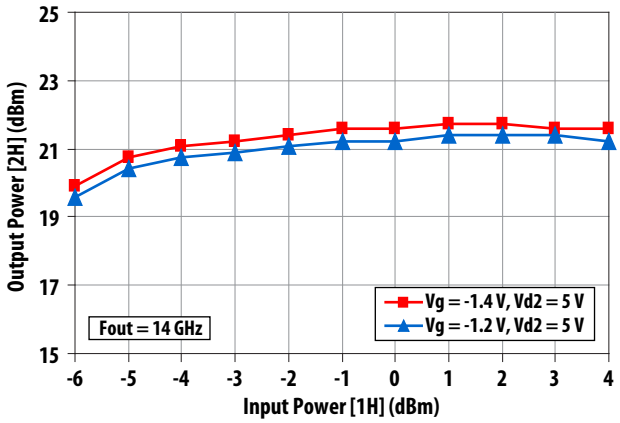


Figure 15. Output Power [2H] vs Input Power @ Fout = 14 GHz

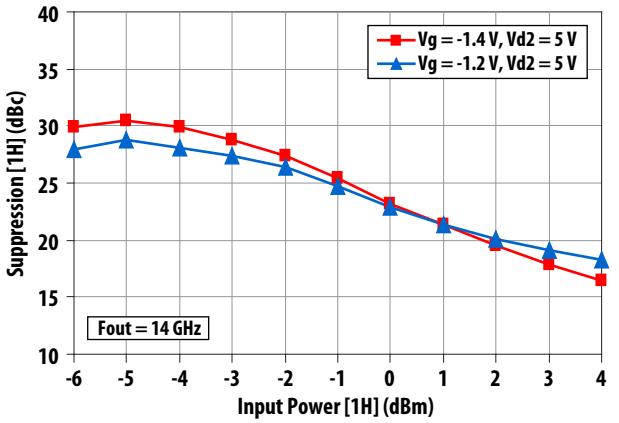


Figure 16. Fundamental Suppression [1H] vs Input Power @ Fout = 14 GHz

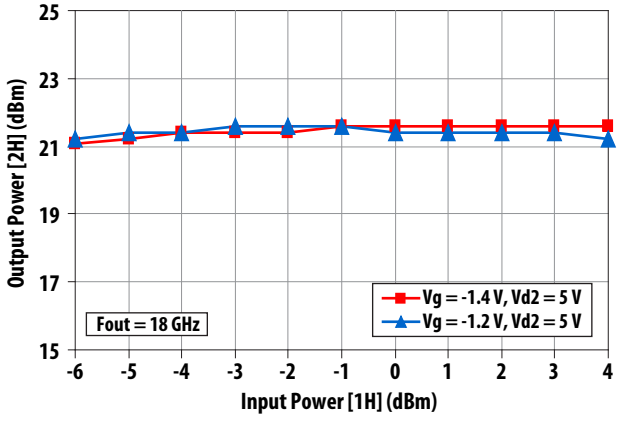


Figure 17. Output Power [2H] vs Input Power @ Fout = 18 GHz

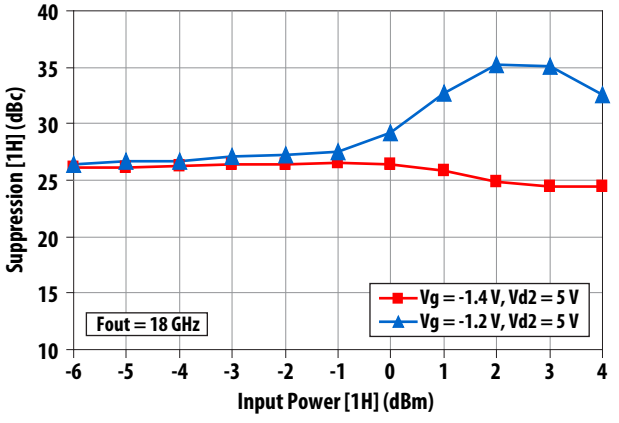


Figure 18. Fundamental Suppression [1H] vs Input Power @ Fout = 18 GHz

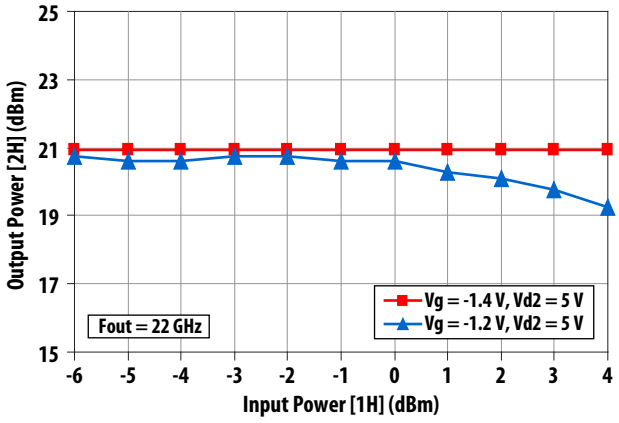


Figure 19. Output Power [2H] vs Input Power @ Fout = 22 GHz

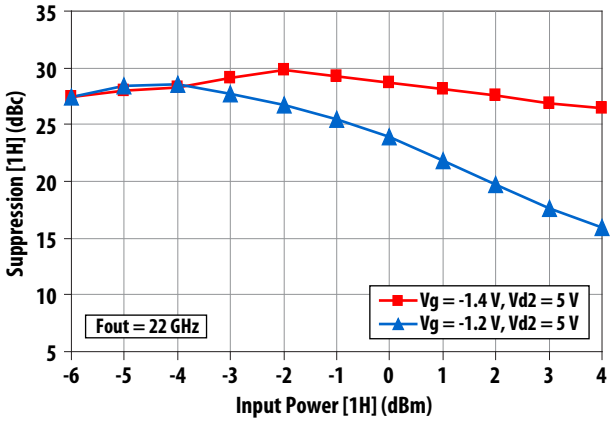


Figure 20. Fundamental Suppression [1H] vs Input Power @ Fout = 22 GHz

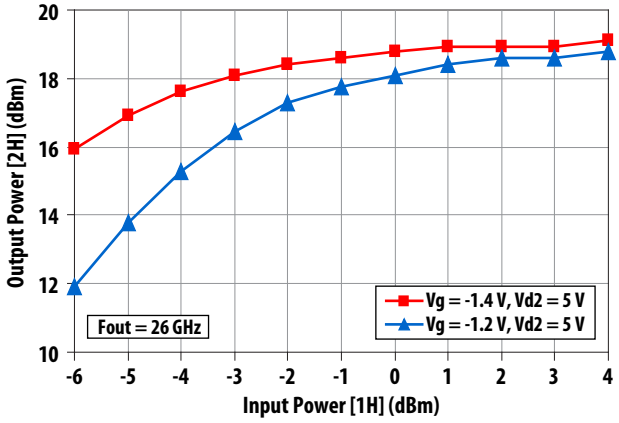


Figure 21. Output Power [2H] vs Input Power @ Fout = 26 GHz

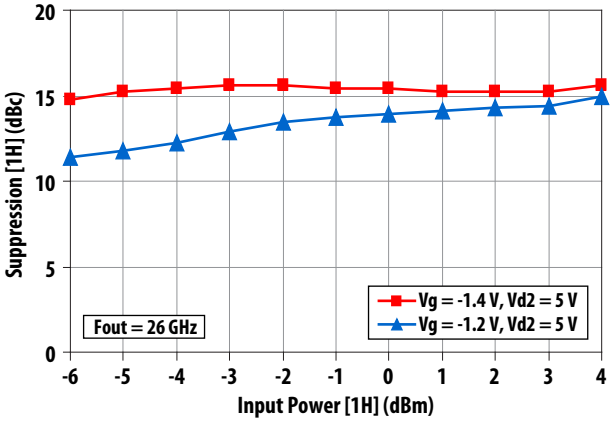
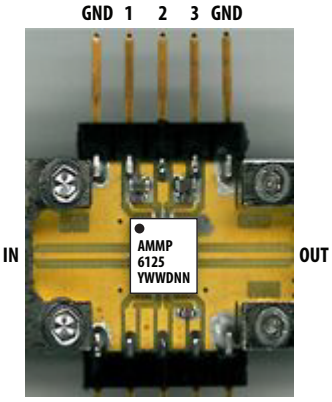


Figure 22. Fundamental Suppression [1H] vs Input Power @ Fout = 26 GHz

Evaluation Board Description and Application Circuit for AMMP-6125



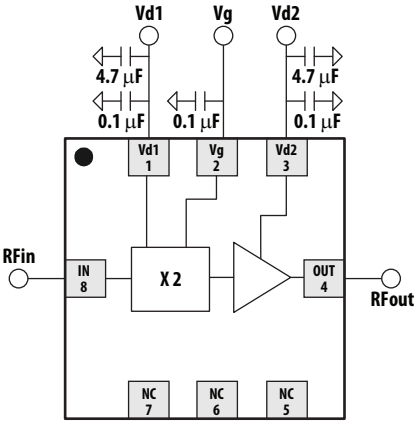


Table 4. Pin Description

Pin #	Function	Biasing	Comment
GND	GND		
1	Vd1	3.5 V	100 mA (measure current)
2	Vg	-1.2 V	5 µA (measure current)
3	Vd2	5.0 V	110 mA (measure current)
GND	GND		

Recommended quiescent DC bias condition for optimum power and linearity performance is Vd1 = 3.5 V, Vd2 = 5 V and Vg = -1.2 V. The gate voltage, Vg, biases the doubling circuit only; it does not adjust the amplifier bias current. Minor improvements in the AMMP-6125's output power and fundamental suppression can be obtained by adjusting Vg from -1.0 V to -1.5 V.

Package, Tape & Reel, and Ordering Information

Please refer to Avago Technologies Application Note 5521, AMxP-xxxx production Assembly Process (Land Pattern B).

Part Number Ordering Information

Part Number	Devices per Container	Container
AMMP-6125-BLKG	10	antistatic bag
AMMP-6125-TR1G	100	7″ Reel
AMMP-6125-TR2G	500	7″ Reel

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-3208EN - July 9, 2013