AK520S

ISDN Single Chip NT1/(U&S/T-Interface) Transceiver

Features

☐Fully integrated single chip NT1 (2B1Q·U-Interface + S Interface)

☐Automatic Activation and Deactivation control

☐eoc decoder function

☐CRC, febe processing function

☐Decision feedback equalizer (DFE) for reducing the influence of bridged taps etc.

☐Linear echo canceller provides in excess of 65dB echo cancelling

☐Excellent NEXT margin

☐Automatic support for ANSI T1.601 NT maintenance mode operations

☐8.192 MHz crystal oscillator generates both the U-Interface and S/T Interface timing

☐All timing are generated on chip

☐+5V single power supply

☐Low power consumption with CMOS technology: typical 310mW (ANSI T1.601 : Loop#1)

☐Power Down mode function:
in Driver high_impedance mode → 104mW(typ)
in Driver low_impedance mode → 130mw(typ)

☐80-pin LQFP surface-mount package

General Description

The AK520S combines an ISDN U-Interface transceiver with a S/T-Interface transceiver in a single IC. It performs all necessary activation control, encoding, scrambling, clock extraction, NT Maintenance Mode, and all other necessary functions for NT1. An NT1 for ISDN interface can be configured easily without microprocessor.

The AK520S U-Interface section fully meets ANSI T1.601(1992) and ETSI ETR-80(1995) specification for interfacing to the metallic loop on the network side of the Network Termination(NT). It uses echo cancelling and the 2B1Q line code to provide 2-wire transmission at 160 kbps. The AK520S receives and transmits eoc (embedded operations channel) message, activation bit, and supervisory bit in the M channel. In addition, it performs CRC and febe (far end block error) performance monitoring functions internally and automatically sends echoes bits to the LT in the appropriate frame position.
The AK520S S/T Interface section meets CCITT I.430 and ANSI T1.605 specifications of 4-wire, AMI coded, point-to-point or point-to-multipoint transmission at 192 kbps.

All the functions mentioned above are provided by using Hardware mode, one of two operation modes that AK520S offers. This mode is suitable for simple stand-alone NT1 application.
The AK520S also supports U-only interface using a Serial Interface, instead of the S/T Interface (Serial Interface mode). The Serial Interface provides read/write access to the U-Interface 2B+D data in the format defined by industry standard IOM-2 (ISDN-Oriented Modular revision-2) or GCI interface.

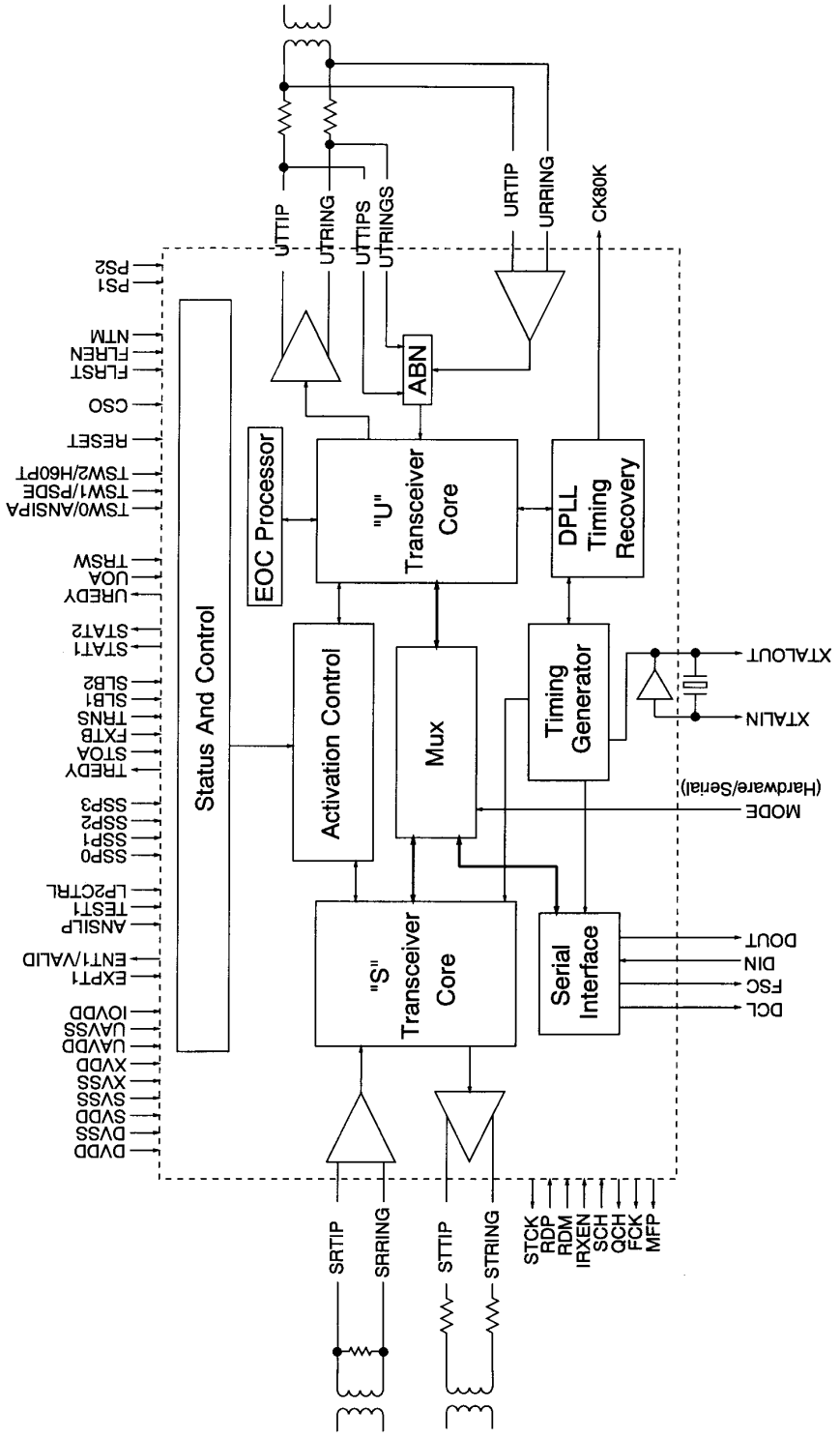
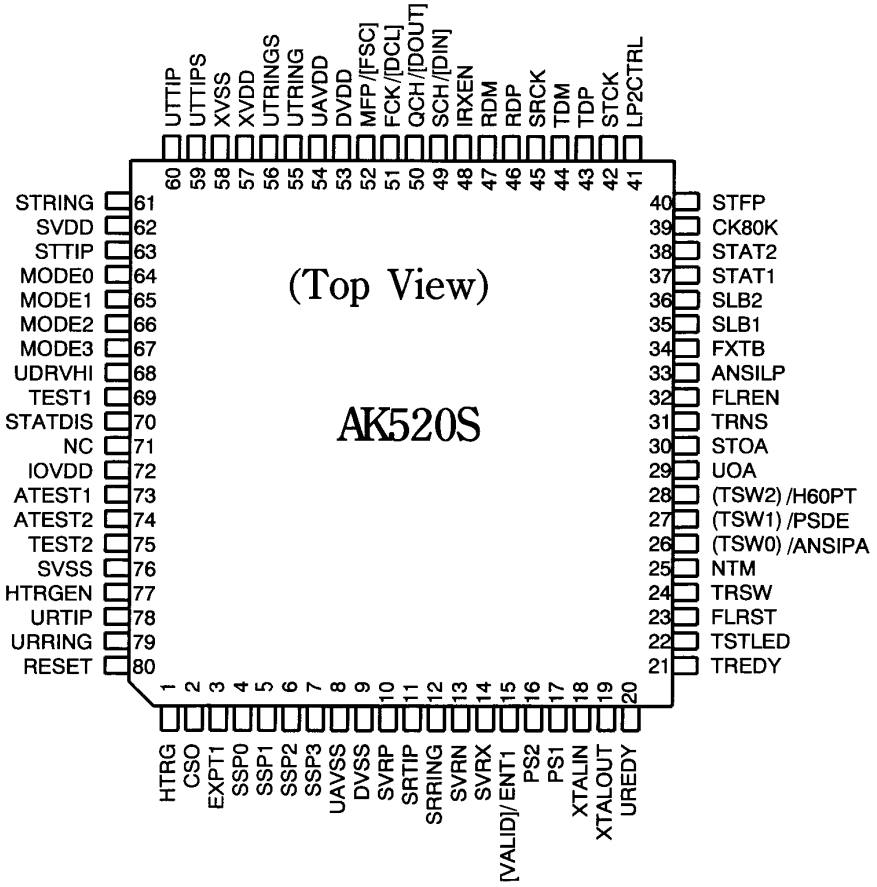


Fig 1 block diagram

■PIN CONFIGURATION



Notes:

1. Pin functions in the Serial Interface mode (when MODE0 is low) are shown in brackets:[ ].
2. Pin functions in the NT local test mode (when NTM is low) are shown in parentheses:( ).

Pin Description

Pin No.	Pin Name	I/O	Function
1	HTRG	I	HTRG. This input provides decoding for ANSI T1.601 NT maintenance mode signalling pulses which are automatically processed when HTRGEN(pin 77) is High.
2	CSO	I	Cold Start Only. Set High to force cold start activation. When CSO is Low, warm start activation is used when possible. This input is mapped to the M4 bit position as cso in the U-Interface frame.
3	EXPT1	I	T1 Timer Expiration. The external T1 timer sets this input High when the timer expires. When no external timer is used, pull this pin Low.
4 5 6 7	SSP0 SSP1 SSP2 SSP3	I	S Sampling point <0:3>. SSP0:SSP3 select the sampling point in time for the S/T-Interface when SVRX(pin 14) is High to select the external sampling mode. Fig 8 illustrates the SRCK and the sampling points which may be programmed.
8	UAVSS	-	U-Interface Analog Ground. Ground reference for the U-Interface analog circuitry except the line driver.
9	DVSS	-	Digital Ground. Ground reference for the digital circuitry.
10	SVRP	I	S Reference Positive Voltage. The potential difference between SVRP and SVRN defines the data decision level, or slicing level, for the S/T Interface when SVRX(pin 14) is High to select the external sampling mode.
11	SRTIP	I	S Receive TIP. S/T Interface analog differential input.
12	SRRING	I	S Receive RING. S/T Interface analog differential input.
13	SVRN	I	S Reference Negative Voltage. The potential difference between SVRP and SVRN defines the data decision level, or slicing level, for the S/T Interface when SVRX(pin 14) is High to select the external sampling mode.
14	SVRX	I	S External Sampling/Reference. When High, the sampling time for the S/T Interface is set by the 4 bits SSP0 to SSP3, and the decision level is set by SVRP and SVRN. When SVRX is Low, the data decision level and sampling phase are set internally.

Pin No.	Pin Name	I/O	Function
15	ENT1	O	Enable Timer 1. ENT1 goes High to enable the start of an external T1 timer.
	VALID (For Serial interface)	O	VALID goes High when U-Block acquires the ISW synchronization to indicate M channel in DIN is valid.
16	PS2	I	Power Status 2. This input is mapped into the M4 overhead bit to reflect NT power status as defined in T1.601. Refer to table 1-5.
17	PS1	I	Power Status 1. This input is mapped into the M4 overhead bit to reflect NT power status as defined in T1.601. Refer to table 1-5.
18	XTALIN	I	Crystal Input. Connects to an external 8.192 MHz crystal and a load capacitor of certain value to adjust its frequency to the center.
19	XTALOUT	O	Crystal Output. Connects to an external 8.192 MHz crystal and a load capacitor of certain value to adjust its frequency to the center.
20	UREDY	O	U-Interface Ready. Goes High when U-Interface synchronization is achieved. It is equivalent that UREDY goes high at H6(a), 6, 7, 8, 8(a)～(c), 9, and 11 of the H matrix except when loss of signal or loss of SYNC is occurred in these states.
21	TREDY	O	S/T Interface Ready. Goes High when the S/T interface receives INF03 and transmits INF04 (during the G3 state of the G matrix).
22	TSTLED	O	Test Mode Indication. Goes High during a test mode [remote loopback (eoc loop 2), local test (refer to "4. Test Function") and Maintenance Mode]. It is also High when both FLREN and FLRST are High.
23	FLRST	I	Full Reset. When FLREN(pin 32) is High, High level of FLRST forces a full reset(H1 state).
24	TRSW	O	DC Termination. Can be used to control the U-interface termination impedance. Refer to table 3-1.
25	NTM	I	NT Test Mode. Setting NTM Low activates the test mode specified by TSW0-TSW2. NTM is mapped to M4 bit as ntm in the U-Interface frame.

Pin No.	Pin Name	I/O	Function
26	TSW0/ANSIPA	I	Test Mode select 0 / Power On Activation. When NTM(pin 25) is Low, TSW0-TSW2 select one of the local test modes as in table 4-2. When NTM is High, this input selects the power-on activation control. When ANSIPA is High, the AK520S attempts U-Interface activation at power-on for ANSI applications. Setting ANSIPA Low disables power-on activation.
27	TSW1/PSDE	I	Test Mode Select 1 / Power Status Detection Enable. When NTM is Low, TSW0-TSW2 select one of the local test modes as in table 4-2. When NTM is High, High level of this input enables power status reporting using the PS1 and PS2 inputs.
28	TSW2/H60PT	I	Test Mode Select 2. When NTM is Low, TSW0-TSW2 select one of the local test modes as in table 4-2. When NTM is High, this input should be High for H matrix to conform to Table C.4 of ANSI T1.601-1992. When this input is Low, the state transient of H6→H6(a) occurs regardless of received act bit from LT. Received dea bit is ignored all the time.
29	UOA	I	Enable U-Interface Only Activation. When UOA is High, the AK520S allows activation of the U-Interface only according to uoa bit from LT.
30	STOA	I	S/T-interface Only Activation. Low level of STOA forces S/T-interface state machine to G3 state independent of U-interface status. It also allows U-Interface to attempt activation in case U-Interface is not activated.
31	TRNS	I	Transparent Loopback. Setting TRNS High enables loopback transparency. Refer to table 4-1.
32	FLREN	I	FLRST Enable. Setting FLREN High enables the FLRST input(pin 23) to force the H matrix to full reset state.
33	ANSILP	I	ANSI/$\overline{\text{ETSI}}$ for M bit (act bit) setting pin. Mapping of act bit to M4 is different between ANSI T1.601 and ETSI ETR-80 when Loop 2 is activated. When High, pin is set for ANSI. When Low, it is set for ETSI.
34	FXTB	I	S/T Reception Sampling Timing Switching. FXTB selects the Fixed timing mode for the S/T Interface when set Low. The Adaptive timing mode is selected when FXTB is High. Refer to "2-2. S/T Interface Receiver".

Pin No.	Pin Name	I/O	Function
35	SLB1	I	S/T B1 Loopback. A S/T side loopback of the B1 channel (loop C) is selected when this input is Low. G matrix is forced to G3. It also allows U-Interface to attempt activation in case it is not activated.
36	SLB2	I	S/T B2 Loopback. A S/T side loopback of the B2 channel (loop C) is selected when this input is Low. G matrix is forced to G3. It also allows U-Interface to attempt activation in case it is not activated.
37	STAT1	O	Status Output 1. This output provides an 8-bit serial status word synchronized with CK80K and framed by STFP.
38	STAT2	O	Status Output 2. This output provides an 8-bit serial status word synchronized with CK80K and framed by STFP.
39	CK80K	O	Clock - 80 kHz. U-interface 80 kHz recovered clock.
40	STFP	O	Status Frame Pulse. STFP defines the word boundaries for the STAT1 and STAT2 outputs as is shown in Fig 11 and Fig 12.
41	LP2CTRL	O	Loop2. This output goes High during γ Loop2. Refer to Fig 10.
42	STCK	O	S/T Clock. An 192 kHz clock synchronized with the S/T Interface transmit data.
43	TDP	O	S/T Transmit Positive Digital Output (active high). The S/T interface transmit data are put out on TDP and TDM when IRXEN is Low to enable the external driver mode. This pin is Low when IRXEN is High.
44	TDM	O	S/T Transmit Negative Digital Output (active low). The S/T Interface transmit data are put out on TDP and TDM when IRXEN is Low to enable the external driver mode. This pin is Low when IRXEN is High.
45	SRCK	O	S/T Clock. An 192 kHz S/T Interface recovered clock.
46	RDP	I	S/T Receiver Digital Input (active high). When IRXEN is Low, the output of the external S/T Interface receiver should drive the data on RDP and RDM and the SRTIP and SRRING inputs are ignored.
47	RDM	I	S/T Receiver Digital Input (active low) When IRXEN is Low, the output of the external S/T Interface receiver should drive the data on RDP and RDM and the SRTIP and SRRING inputs are ignored.
48	IRXEN	I	S/T Internal/External Mode Select. When this input is High, the internal S/T Interface receiver and driver are enabled. When IRXEN is Low, the external driver and receiver mode is selected.

Pin No.	Pin Name	I/O	Function
49	SCH	I	S Channel Input. Multiframe input for the S/T Interface.
	DIN (For Serial interface)	I	Serial Data Input. Serial data input for the Serial Interface.
50	QCH	O	Q Channel Output. Multiframe output for the S/T Interface.
	DOUT (For Serial interface)	O	Serial Data Output. Serial data output for the Serial Interface.
51	FCK	O	Frame Clock. A 4 kHz S/T Interface transmit frame pulse.
	DCL (For Serial interface)	O	Serial Data Clock. A 512 kHz serial clock for the Serial Interface.
52	MFP	O	Multi-Frame Pulse. Multiframe pulse for the Q/S channel.
	FSC (For Serial interface)	O	Serial Frame Sync. An 8 kHz frame pulse for the Serial Interface.
53	DVDD	-	Digital Power. Power supply input for the digital circuitry.
54	UAVDD	-	U-Interface Analog Power. +5V power supply input for the U-Interface analog circuitry except the line driver.
55	UTRING	O	U-Transmission RING. U-Interface differential driver output.
56	UTRINGS	I	U-Transmission RING sensing. U-Interface ABN input. Should be connected to UTRING.
57	XVDD	-	U-Interface Driver Power. +5V power supply for the line driver.
58	XVSS	-	U-Interface Driver Ground. Line Driver Ground reference.
59	UTTIPS	I	U-Transmit TIP Sense. U-Interface ABN input. Should be connected to UTTIP.
60	UTTIP	O	U-Transmit TIP. U-Interface differential driver output.
61	STRING	O	S Transmit RING. S/T-Interface differential driver output.
62	SVDD	-	S/T Interface Analog Power. +5V power supply input for the S-Interface analog circuitry.
63	STTIP	O	S-Transmit TIP. S-Interface differential driver output.
64	MODE0	I	Operation Mode Select. When this input is High, the AK520S operates in the Hardware mode. When this input is Low, the S/T Interface is disabled and the U-Interface 2B+D data becomes input and output on the Serial Interface.

Pin No.	Pin Name	I/O	Function
65	MODE1	I	Mode 1. This test mode input should be tied Low.
66	MODE2	I	Mode 2. This test mode input should be tied Low.
67	MODE3	I	Mode 3. This test mode input should be tied Low.
68	UDRVHI	I	U Driver Impedance. When this input is set Low, the U-Interface driver goes high impedance in the power down state(HI).
69	TEST1	I	Chip Test 1. This input should be tied High.
70	STATDIS	I	Status Disable. This input may be set High to disable the STAT1, STAT2 and CK80K outputs to conserve power when not required.
71	NC	-	No Connection.
72	IOVDD	-	I/O Buffer Power. +5V power supply pin for the I/O buffer circuitry.
73	ATEST1	O	Analog Test Output 1. This pin is analog test output. This pin should be left open.
74	ATEST2	O	Analog Test Output 2. This pin is analog test output. This pin should be left open.
75	TEST2	I	Chip Test 2. This input should be tied Low.
76	SVSS	-	S-Interface Analog Ground. Ground reference for the S/T-Interface analog circuitry.
77	HTRGEN	I	HTRG Enable. Setting this input High enables ANSI T1.601 maintenance mode decoding. An optoisolator is used to convert DC signalling on the U-Interface line into pulses at the HTRG input(pin 1).
78	URTIP	I	U-Interface Receive TIP. U-Interface differential receiver input.
79	URRING	I	U-Interface Receive RING. U-Interface differential receiver input.
80	RESET	I	Reset. Bring Low at power-up to initialize all internal circuits.

Absolute Maximum Ratings

Parameter	min	max	Unit
Power supply voltage (referenced to GND)	-0.3	6.0	V
Input voltage (excluding power supply pins)	VSS-0.3	VDD+0.3	V
Input current (excluding power supply pins)	-	±20	mA
Continuous output current (excluding power supply pins)	-	±25	mA
Continuous current (power supply pins, ground pins)	-	±80	mA
ESD (human body model)	-	2000	V
Power consumption	-	1	W
Storage temperature	-40	150	℃

Note: Operation at or beyond these limits may results in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operation Conditions

Parameter		記号	min	typ	max	Unit
Power supply voltage	pin : UAVDD, SVDD, XVDD, IOVDD	VDD	4.75	5.0	5.25	V
	pin : DVDD	DVDD	3.85(-20℃)	-	5.25	
			3.95(25℃)	-	5.25	
	(Note 1)		4.05(85℃)	-	5.25	
Operation temperature		T_A	-20	-	+85	℃

Note 1: The power supply for DVDD is provided from 5V(typ) power supply through external Silicon switching diode which decreases the voltage from 5V(typ) by 0.9V to 0.7V as is shown in Table above. (This voltage drop is in case of 20mA forward current of diode.)

Electrical Characteristics

■DC Characteristics

Parameter		Symbol	min	typ	max	Unit	Condition
Power Consumption	power down	W_{CC}	-	104	137	mW	Driver:high imp.
	power down		-	130	168		Driver:low imp.
	full operation		-	350	440		(Note 1)
High level input voltage		V_{IH}	0.7VDD	-	-	V	Digital input
Low level input voltage		V_{IL}	-	-	0.3VDD	V	Digital input
High level output voltage		V_{OH}	3.55	-	-	V	I_{OH} = 100μA
Low level output voltage		V_{OL}	-	-	0.45	V	I_{OL} = 500μA
Input leakage current		I_{IL}	-	-	±10	μA	$0 < V_{IN} < V_{CC}$

Note 1: Power consumption value at Null loop (reference: 334mW[typ] / Loop#1)
Use of the diode to DVDD pin

■ AC Characteristics (TA = -20 ～ 85℃, Vcc = 5.0 V ± 5%)

●Master Clock

Parameter	Symbol	min	typ	max	Unit	Remark
XTAL frequency	f_{xtal}	-	8.192	-	MHz	
XTAL permissible frequency deviation	f_{tol}	-	-	±100	ppm	(Note 1)

Note 1: Refer to Table 7 for further informations.

●Interface Signals and Status output Timing (refer to Fig 2)

Parameter	**Symbol**	**min**	**typ**	**max**	**Unit**	**Remark**
Serial·Interface						
DCL period	t_1	-	1.95	-	μs	
DCL pulse width (high level)	t_2	777	977	1177	ns	(Note 1)
DCL "↑" to DIN set up time	t_3	200	-	-	ns	
DCL "↑" to DIN hold time	t_4	200	-	-	ns	
DCL "↑" to DOUT valid	t_5	-	-	210	ns	(Note 1)
FSC period	t_6	-	125	-	μs	
FSC pulse width (high level)	t_7	3.71	3.91	4.11	μs	(Note 1)
1st DCL "↑" to FSC "↑"	t_8	-	-	210	ns	(Note 1)
SCH/QCH Interface						
FCK period	t_9	-	250	-	μs	
FCK pulse width (high level)	t_{10}	124.8	125.0	125.2	μs	(Note 1)
FCK "↓" to SCH set up time	t_{11}	200	-	-	ns	
FCK "↓" to SCH hold time	t_{12}	200	-	-	ns	
FCK "↓" to QCH valid	t_{13}	-	-	210	ns	(Note 1)
MFP period	t_{14}	-	5.0	-	ms	
MFP pulse width (low level)	t_{15}	249.8	250.0	250.2	μs	(Note 1)
last FCK "↓" to MFP "↓"	t_{16}	-	-	210	ns	(Note 1)
Status Output						
CK80K period	t_{17}	-	12.5	-	μs	
CK80K pulse width (high level)	t_{18}	6.05	6.25	6.45	μs	(Note 1)
CK80K "↓" to STAT1/2 valid	t_{19}	2.925	3.125	3.325	ns	(Note 1)
STFP period	t_{20}	-	100	-	μs	
STFP pulse width (high level)	t_{21}	12.3	12.5	12.7	μs	(Note 1)
last CK80K "↓" to STFP "↑"	t_{22}	2.925	3.125	3.325	μs	(Note 1)

Note 1: Load capacitance = 15 pF

●General Characteristics

Parameter	Symbol	min	typ	max	Unit	Remark
Input capacitance	C_{IN}	-	7	-	pF	
Transition time (digital output)	t_{TO}	-	-	50	ns	Note 1
Transition time (digital input)	t_{TI}	-	-	40	ns	
URTIP/URRING input dynamic range	-	-	-	6	V	Note 2
UTTIP/UTRING pulse amplitude accuracy	-	-5	-	+5	%	
UTTIP/UTRING output impedance	-	-	-	1	Ω	Note 3
URTIP/URRING input impedance	-	65	100	135	kΩ	

Note 1: Load capacitance = 15 pF

Note 2: Differential I/O

Note 3: Value at 40KHz. Not tested in production test. Parameters guaranteed by design and characterization.

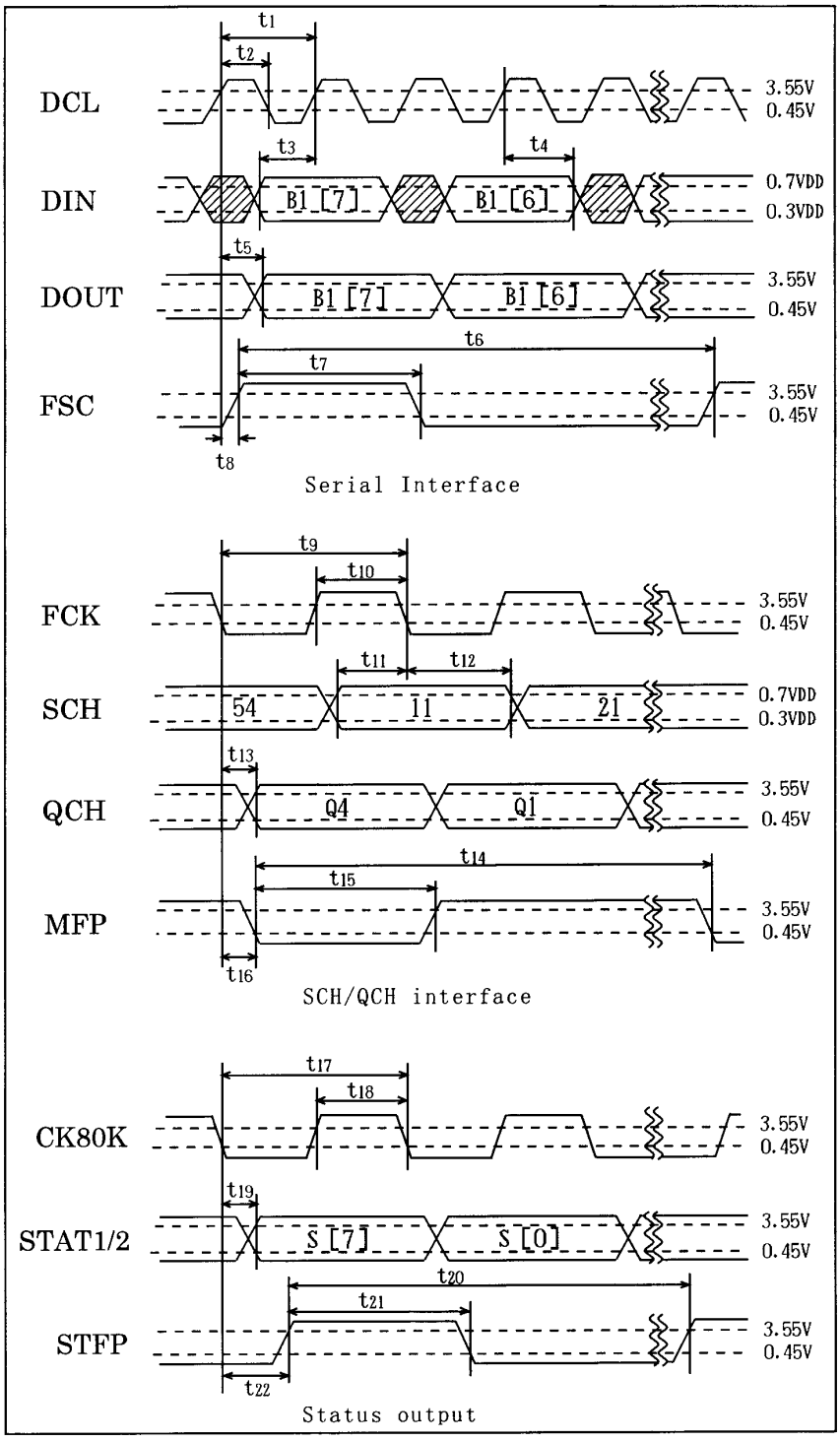


Fig. 2 Interface timings

●Reset pulse timing (refer to Fig. 3)

Parameter	Symbol	min	typ	max	Unit	Remark
Min. reset pulse width	t_{23}	100	-	-	ns	

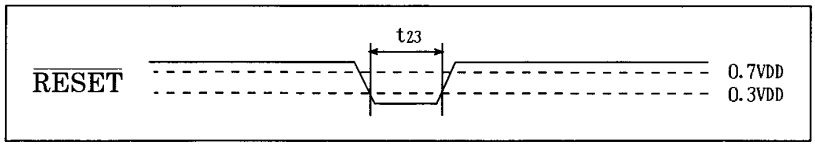


Fig. 3 Reset timing

Function Description

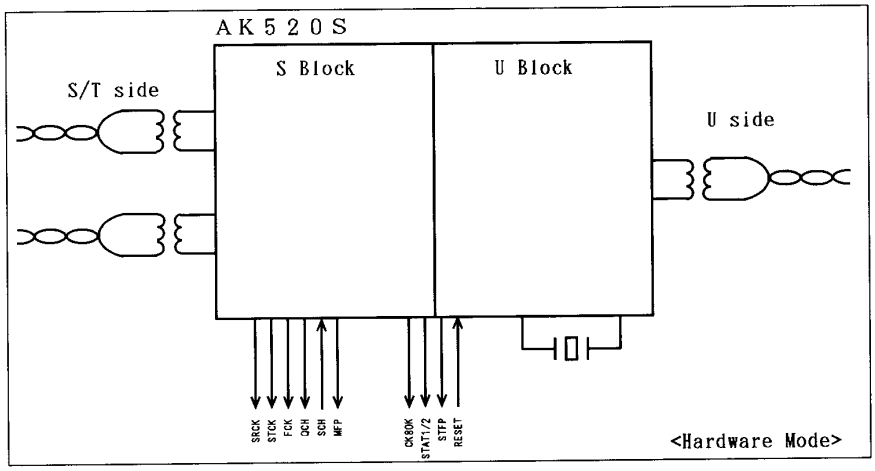
◇ Reset and Power-up Initialization

Bringing RESET (pin 80) Low forces the device to the Full Reset (H1) state and clears all internal registers so that a cold-start activation is required. Reset must be asserted each time the MODE0 input (pin 64) changes state to insure the device is initialized properly.
The FLRST input (pin 23) is used to force the device into the Full Reset (H1) state without clearing the internal registers. FLREN (pin 32) is the active-High enables signal used to gate FLRST. Bringing the FLRST input High when FLREN is High forces the device into the Full Reset state.
When NTM is High (to disable the local test mode specified by TSW0..2), the TSW0/ANSIPA input (pin 26) is used to enable or disable activation at power-up. ANSI T1.601 requires the NT1 to initiate DSL activation on power-up so that a warm-start activation may be used for a following TE initiated call. For ANSI applications, TSW0/ANSIPA should be pulled High at power-up. ETSI ETR-80 does not permit the NT1 to autonomously initiate activation on power-up, so TSW0/ANSIPA should be Low at power-up for these applications.
When the TSW0/ANSIPA input is High at power-up, the AK520S immediately enters the H2 state and begins transmitting the TN wake-up tone to initiate a cold start activation. If the UOA input (pin 29) is High the AK520S will be able to complete a cold-start DSL only activation with uoa=0 of M4 bit from LT preparing it for a later warm-start activation.

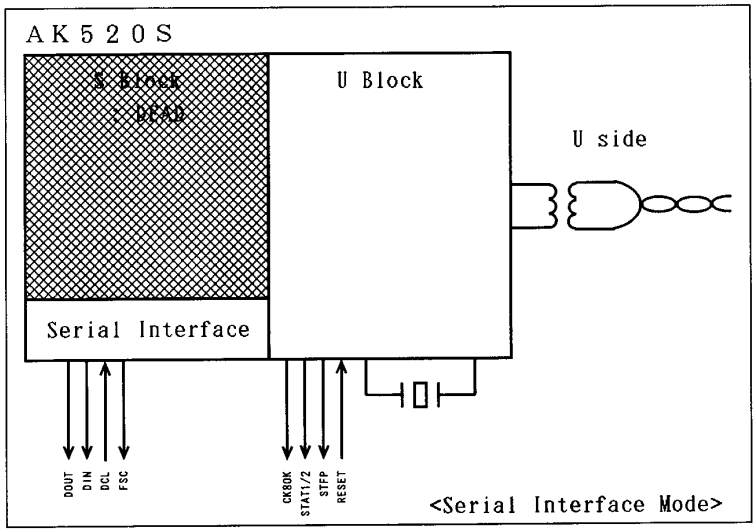
◇ Mode Selection

AK520S provides 2 modes, Hardware mode and Serial Interface mode, by using MODE0 input (pin 64) to enable the S/T-Interface or the Serial Interface. The RESET must be set Low to initialize the AK520S after MODE0 changes its state.

① Hardware mode (MODE0: High)
The Hardware mode provides all the functions required for NT1 component with ANSI T1.601 and ETSI ETR-80. It is suitable for simple stand-alone NT1 application as belows.



② Serial Interface mode (MODE0: Low)
The AK520S supports U-only interface using a Serial Interface (a digital, GCI format interface), instead of the S/T Interface. The Serial Interface provides read/write access to the U-Interface 2B+D data as shown below.



◇ Block Function

1. U-Interface

The AK520S U-Interface provides transmit pulse shaping, echo cancellation, receive signal detection, and timing extraction. The AK520S U-Interface fully meets the requirements of the 1992 revision of ANSI T1.601 and the 1995 revision of ETSI ETR-80. It also provides activation/deactivation, warm start activation, data framing, data scrambling, and buffering of received data to the 80 kHz transmit clock.

The AK520S line interface requires only a transformer, 2 termination resistors, a crystal and a basic protection diode as external components.

The AK520S U-Interface comprises of four main sections: transmitter, echo canceller, receiver and control logic section.

The Transmitter section is composed of framer/scrambler, 2B1Q encoder, filter, and line driver. Echo cancellation is performed by ABN (Adaptive Balancing Network) and digital echo canceller. The Receive section is composed of pre-filter, line equalizer, DFE (Decision Feedback Equalizer), and deframing/descrambling. The control logic section includes an ACTIVATE/DEACTIVATE state machine. It also controls the transmitter, adaptive balancing network, gain control circuit, the DPLL, and the digital filters.

The timing recovery is provided by the internal DPLL. The DPLL synchronizes U-Interface circuits with received data of U side, and also generates the timing for synchronization of U-Interface with S/T Interface.

1-1. Activation/Deactivation

Fig. 4 shows the state machine diagram of the activation/deactivation process. The transition from the Full Reset state to Full Activation involves 1) echo canceller (EC) training and convergence; 2) AGC, DPLL and DFE convergence; 3) SW/ISW synchronization. Full activation is achieved by a call request from LT or TE or by Power on Activation Request after reset. Once the U-Interface achieves full activation, the coefficient values for the various filters , and taps of DFE, echo canceller and others are stored on-chip. These stored values can be used for subsequent "warm-start" activation. The warm-start activation is quicker(< 300 ms) than initial "cold start" activation because the filter convergence process is bypassed using the stored values. The AK520S performs warm-start activation whenever possible, unless Cold Start Only is selected(CSO = 1).

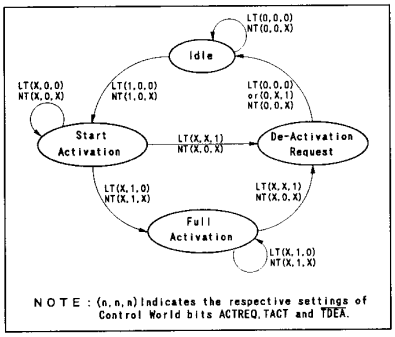


Fig. 4
U-Interface Activation State Machine

1-2. U-Interface Transmitter

The transmitter section includes a framer/scrambler, 2B1Q encorder, filters and the line driver. The data to be transmitted to the U-Interface is received from the S/T Interface or supplied from the Serial Interface. When fully activated, the input data is first framed and scrambled, and encoded to the 2B1Q line code. The 4-level 2B1Q coding scheme creates a quaternary symbol called "quat" from a pair of sequential bits called a di-bit. Each di-bit consists of a sign bit followed by a magnitude bit which are encoded as shown below.

Sign	Magnitude	Symbol	Voltage (V)
1	0	+3	+2.50
1	1	+1	+0.83
0	1	-1	-0.83
0	0	-3	-2.50

Fig. 5 shows the 2B1Q encoding. Quaternary symbols are generated by the fully differential switched-capacitor filter, followed by an active smoothing filter and then output by the line driver. An internal bandgap voltage reference circuit maintains the specified pulse height independent of power supply variations.

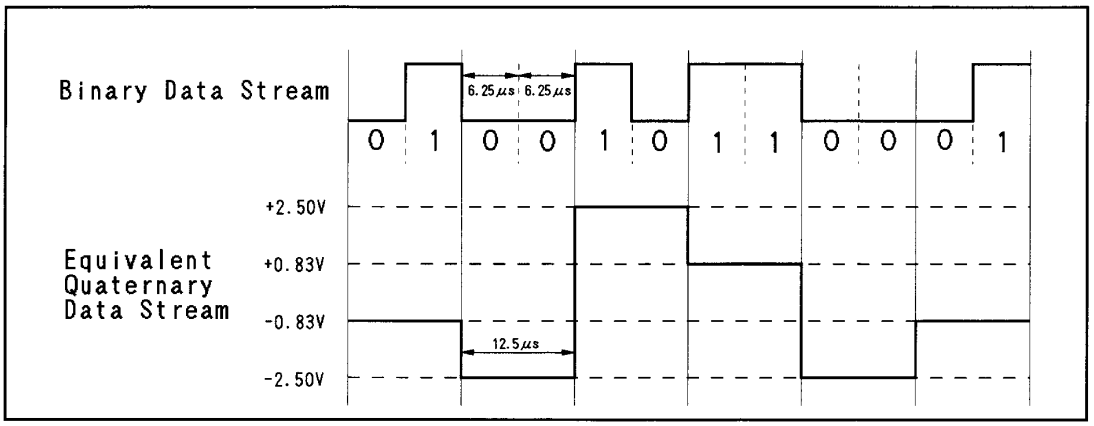


Fig. 5 2B1Q coding

1-3. U-Interface Framing Format

The AK520S U-Interface transmits a 120 quat (or 240 bit) frame as shown in Fig 6. Each frame starts with 18 internally generated sync word (SW), followed by 216 data bits and ends with 6 M channel bits. A superframe consists of eight 240-bit frames. Superframe alignment is indicated by an inverted sync word (ISW) in the first frame of every superframe. Fig. 6 shows the ISDN 2B+D format where the 216 data bits are structured as 12 blocks of 2B+D data. Each block of 2B+D data consists of two 8-bit B channels and a 2-bit D channel.

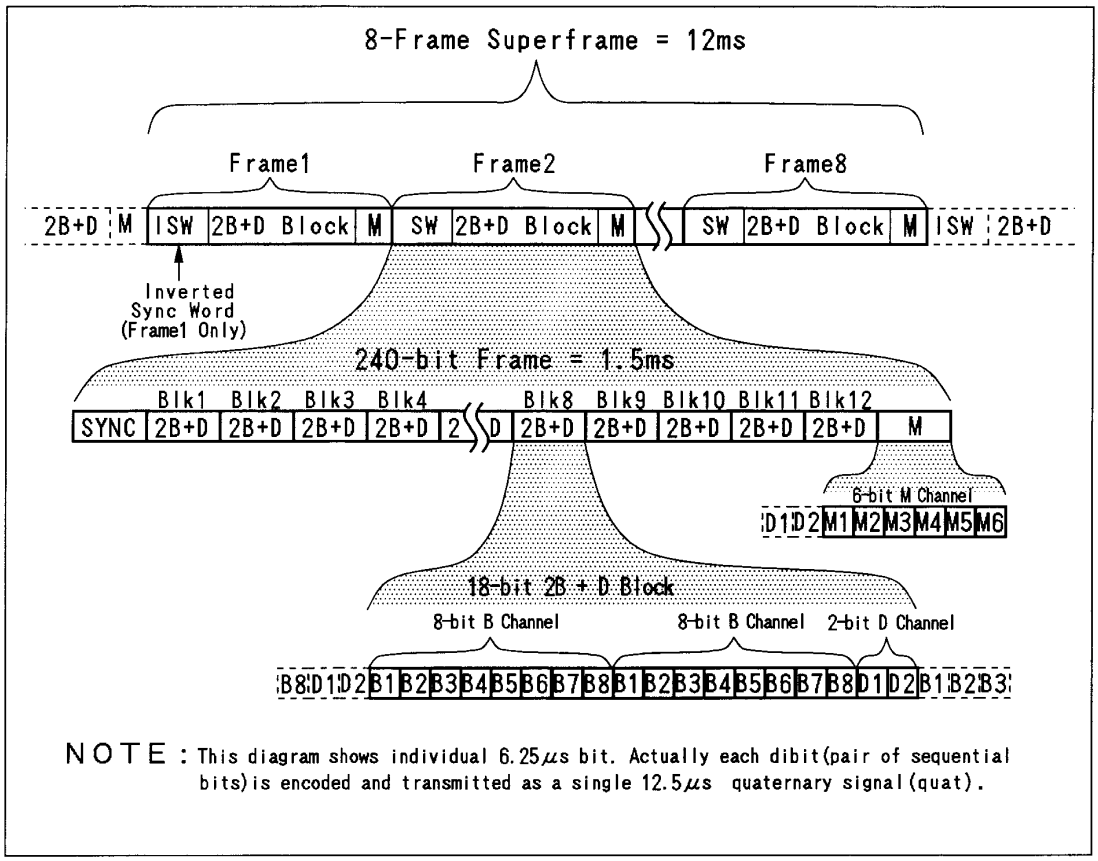


Fig. 6 U-Interface Framing Format

1-4. U-Interface Receiver

The receiver section includes pre-filter, line equalizer, a DFE, and deframing/descrambling. The signal at the URTIP and URRING inputs is processed by a low-pass filter, automatic gain control circuitry (AGC) and line equalization filter. The AGC circuit has a 24 dB gain range with discrete 6 dB steps. The AGC circuit is adapted only during cold start activation. The line equalization filter creates a robust timing function for baud rate phase extraction and also performs tail suppression on the receive signal and the echo response.

The analog signal is then sampled and fed to a summing node/comparator followed by a digital signal processor (DSP), where a DFE, slicer level tap, and offset tap values are updated. These components are continuously adapted to compensate for ISI due to time-varying line characteristics such as temperature, humidity and aging.

1-5. Echo Cancellation

The echo cancellation is performed by an analog adaptive balancing network (ABN) combined with digital linear echo canceller. The ABN achieves a minimum of 25dB of echo suppression with any of the cable characteristics specified in ANSI T1.601, including 15 loops with bridged taps and gauge changes. Digital echo cancellation is performed on the linear component of echo. The digital echo canceller is continually adapted, while the ABN is trained only during cold start activation.

1-6. U-Interface Timing Recovery

The timing recovery circuit uses a rate synchronizer with generate a high frequency internal clock from the master clock (MCLK) input. This extremely high-resolution DPLL achieves high performance echo cancelling without using complicated hardware such as a jitter compensator. The output clock from the DPLL is used directly to run the DSP, and is divided down to produce the various other clocks which run the digital and switched-capacitor analog circuits.

1-7. Data Synchronization

The DPLL synchronizes baud rate clock with received signal after equalization . The Serial Interface outputs and the ICLK are all synchronized with the internal clock generated by DPLL.

1-8. Overhead Channel Processing

The AK520S receives and transmits eoc (embedded operations channel) messages, activation bits and supervisory bits in the M-channel of the basic frame. It performs crc (cyclic redundancy check) and febe (far end block error) monitoring functions internally and automatically sends the result to the LT as febe bit in M channel at the appropriate frame position. The AK520S processes activation/deactivation message automatically, complying with ETR-80, CCITT I.430, ANSI T1.605 and T1.601. Table 1-1 and 1-2 shows the definition of the M1-M6 bits contained in a basic rate superframe.

		Framing	12x(2B+D)	Overhead bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Superframe #	Basic Frame #	Sync Word	12(2B+D)	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	aib	crc_{11}	crc_{12}
2, 3...	1	ISW							

Table 1-1 U-Interface Superframe Bit Groups-Network to NT

		Framing	12x(2B+D)	Overhead bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Superframe #	Basic Frame #	Sync Word	12(2B+D)	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	ps_1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1*	crc_{11}	crc_{12}
2, 3...	1	ISW							

Note : 1* --> Network indicator bit. Equal 1, reserved for network use.

Table 1-2 U-Interface Superframe Bit Groups-NT to Network

1) eoc (M1-M3 Bits)

The embedded operations channel (eoc) specified by ANSI T1.601 for bits M1-M3 provides for overhead communications between the LT and NT device. The AK520S, as an NT device, processes eoc messages from the LT automatically. The U-Interface uses two sets of 12 bits per superframe for eoc functions. Each set comprises three address bits, a data/ message indicator bit and eight information bits. When the local test is activated at NT side through NTM and TSW0-3, the eoc processor can not either process the received command nor send back eoc echo bit in same way. Table 1-3 shows the condition in which ntm=0 is sent, the way UTC is echoed back to LT as eoc echo in case ntm=0, and the eoc operation in the case.

ntm=0 transmit condition	NTM(pin 25)=0 or SLB1/SLB2=0
UTC transmit condition	Original condition for UTC defined in ANSI or When ntm=0 *In case "Return to Normal", eoc echo is "Return to Normal" instead.
eoc operation when ntm=0	In case of "ntm=0", message is not accepted by NT and all messages already received are cancelled.

Table 1-3 ntm, UTC transmit condition

2)M4 bits

The AK520S processes M4 bits automatically, complying with CCITT I.430, ANSI T1.605 and T1.601. The act, dea, aib and uoa M4 bits are debounced (3 in/3 out). The other M4 bits are not debounced. In case of the loopback, the processing of act bit depends on polarity of ANSILP as table 1-4. The PS1, PS2, NTM and CSO hardware inputs are mapped directly into the appropriate M4 bit positions and transmitted to the LT. The Received M4 bits and the febe bit can be read via the serial port in the Serial Interface mode. The definition of PS1/PS2 is given as table 1-5.

H matrix status	ANSILP	2B+D Loopback		B1 or B2 Loopback	
		uoa=1	uoa=0	uao=1	uoa=0
H6(a) H6 H7	1 (ANSI)	act=0	act=0	H7, H8 : act=1 H8(a~c), H6(a), H6 : act=0	H8(a~c) : act=0 others : not happen
H8 H8(a) H8(b) H8(c)	0 (ETSI)	act=1	act=1	H7, H8 : act=1 H8(a~c), H6(a), H6 : act=0	H8(a~c) : act=0 others : not happen
H9	1 (ANSI)	act=0	act=0	transmit same act bit as in previous state	transmit same act bit as in previous state
	0 (ETSI)	act=1	act=1	transmit same act bit as in previous state	transmit same act bit as in previous state

Table 1-4 act bit sent to LT during Loopbacks

NT status	ps1	ps2	Definition
All power normal	H	H	Primary and secondary power supplies are both normal.
Secondary power out	H	L	Primary power is normal, but the secondary power is marginal, unavailable, or not provided.
Primary power out	L	H	Primary power is marginal or unavailable, secondary power is normal.
Dying gasp	L	L	Both primary and secondary power are marginal or unavailable. The NT may shortly cease normal operation.

Table 1-5

3)crc (M5 and M6 bit)

The U-Interface uses 12 bits per superframe (bits M5 and M6 of basic frames 3 through 8) for a cyclic redundancy check (crc). The transmit section calculates the crc bits and injects them into the specified bit positions. The receive section compares the crc bits received from the LT with its own internally generated crc bits. Inconsistent result causes the AK520S to send febe (far end block error) as M channel bit to the LT and to set the nebe (near end block error) bit in the serial status word STAT1 as shown in Fig 11. The AK520S crc processing scheme fully complies with ANSI T1.601.

2. S/T Interface

The AK520S S/T Interface provides a four-wire, 192 kbps point-to-point or point-to-multi-point interface with up to eight ISDN TE terminals according to the requirements in CCITT I.430 and ANSI T1.605. Q and S channel bits are not processed internally.

2-1. S/T Interface Transmitter

The S/T Interface transmit circuit uses a differential line driver designed to drive the line through a 2:1 step down transformer. The line driver generates output pulses of 750 mV nominal amplitude, and it is independent of power supply changes (within the specified operational range).

2-2. S/T Interface Receiver

The AK520S receiver front end incorporates a continuous filter, a data decision comparator , and a high-resolution DPLL timing recovery circuit. The continuous filter eliminates out -of-band noise. The comparator recovers the data with optimized slicing threshold level to maintain consistent performance up to 1 km of 26 AWG (0.4 mm) cable. The DPLL allows the device to determine the optimum point for data sampling using a fixed or an adaptive algorithm.

Two timing recovery algorithms, fixed and adaptive timing, are provided for optimum performance across the wide variety of S Interface configurations and loop lengths supported. The Adaptive timing should be used for applications with both point-to-point configuration and short passive bus configuration in which the differential delays between TEs are up to 3.1 μs. If the differential delay between TEs is greater than 3.1 μs (as is possible in short passive bus configuration), then fixed timing should be selected by pulling FXTB (pin 34) Low.

2-3. T2 Timer

The internal T2 Timer value of AK520S is 75ms which is within the ANSI specification value (Spec; 25ms～100ms).

2-4. External Driver/Receiver Mode

By pulling down IRXEN (pin 48), S/T External Driver/Receiver Mode is selected. The AK520S can use external driver/receiver circuits in this mode. The pin assignment and functional specifications of the interface are as shown below.

Table 2-1 Driver/Receiver interface I/O terminals

I/O	Explanation
O	TDP: Transmission (active High)
O	TDM: Transmission (active Low)
I	RDP: Reception (active High)
I	RDM: Reception (active Low)
O	LP2CTRL: Loop 2 control output (only 2B + D complete loopback) 1 : Loop 2 setting 0 : Loop 2 cancelling
I	IRXEN: Receiver circuit switching 1 : Use of the internal receiver of the LSI (TDP/M, RDP/M are inactive) 0 : Use of a receiver connected externally to the LSI (TDP/M, RDP/M are active)

In the external driver/receiver mode, the loopback point is as shown below.

① When uoa = 1 (S/T is active), only the 2B + D complete loopback 2 would be executed outside the AK520S. The B1, B2 partial loopback 2 is executed inside the AK520S. At this time, the Loop2 control output becomes "H" (Loop 2 enable) to control the relay to form the loopback path outside of the chip.
② When uoa = 0 (no S/T start), all loop 2 (2B + D, B1, B2) is executed inside the AK520S, and INFO 0 is transmitted to the S/T point. At this time, the Loop 2 control output becomes "L" (Loop 2 disable).

The timing for S/T-Digital Interface is shown in Table 2-2 and Fig 7.
As is described in "2-5. External Sampling/Reference Mode", the Sampling CK provides the sampling time for the S/T data and clock recovery in the S/T External Sampling/Reference Mode. Set NTM=0 and TSW2~0=111 to observe Sampling CK through pin 51 (FCK).

Adaptive Timing (FXTB = H)	Default Sampling Timing (SVRX = L)			External Sampling Timing (SVRX = H)		
	min	typ	max	min	typ	max
Receive Side						
Trdata (Rdata period)	-	5.208μs	-	-	5.208μs	-
Twrdata (Rdata width)	5.168μs	5.208μs	5.248μs	5.168μs	5.208μs	5.248μs
Tdrck (SRCK delay)	160ns	-	300ns	160ns	-	300ns
Trck (SRCK period)	-	5.208μs	-	-	5.208μs	-
Tdsamp (Sampling CK delay) [Note 1]	3.90μs	3.99μs	4.08μs	-8.6 + 325.5*N ns	81.4 + 325.5*N ns	171.4 + 325.5*N ns
Thsamp (Sampling CK hold time)	200ns	-	-	200ns	-	-
Twsamp (Sampling CK width)	-	81.40ns	-	-	81.40ns	-
Tssamp (Sampling CK set up time)	200ns	-	-	200ns	-	-
Transmit Side						
Tofck (Offset between SRCK&STCK)		ND	[Note 2]		ND	
Ttck (STCK period)	-	5.208μs	-	-	5.208μs	-
Tdtdata (Tdata delay)	210ns	-	-	210ns	-	-
Ttdata(=Twtdata) (Tdata width&period)	-	5.208μs	-	-	5.208μs	-
Tdfck (FCK delay)	0	81.40ns	171.4ns	0	81.40ns	171.4ns

Fixed Timing (FXTB = L)	Default Sampling Timing (SVRX = L)			External Sampling Timing (SVRX = H)		
	min	typ	max	min	typ	max
Receive Side						
Trdata (Rdata period)	-	5.208μs	-	-	5.208μs	-
Twrdata (Rdata width)	5.168μs	5.208μs	5.248μs	5.168μs	5.208μs	5.248μs
Tdrck (SRCK delay)		ND			ND	
Trck (SRCK period)	-	5.208μs	-	-	5.208μs	-
Tdsamp (Sampling CK delay)	4.55μs	4.64μs	4.73μs	-8.6 325.5*N ns	81.4 + 325.5*N ns	171.4 + 325.5*N ns
Thsamp (Sampling CK hold time)	200ns	-	-	200ns	-	-
Twsamp (Sampling CK width)	-	81.40ns	-	-	81.40ns	-
Tssamp (Sampling CK set up time)	200ns	-	-	200ns	-	-
Transmit Side						
Tofck (Offset between SRCK&STCK)	112.8ns	162.8ns	212.8ns	112.8ns	162.8ns	212.8ns
Ttck (STCK period)	-	5.208μs	-	-	5.208μs	-
Tdtdata (Tdata delay)	210ns	-	-	210ns	-	-
Ttdata(=Twtdata) (Tdata width&period)	-	5.208μs	-	-	5.208μs	-
Tdfck (FCK delay)	0	81.4ns	171.4ns	0	81.4ns	171.4ns

[Note 1] N: Sampling Point as Fig 8.
[Note 2] ND: Not Defined

Table 2-2 Driver/Receiver interface signals

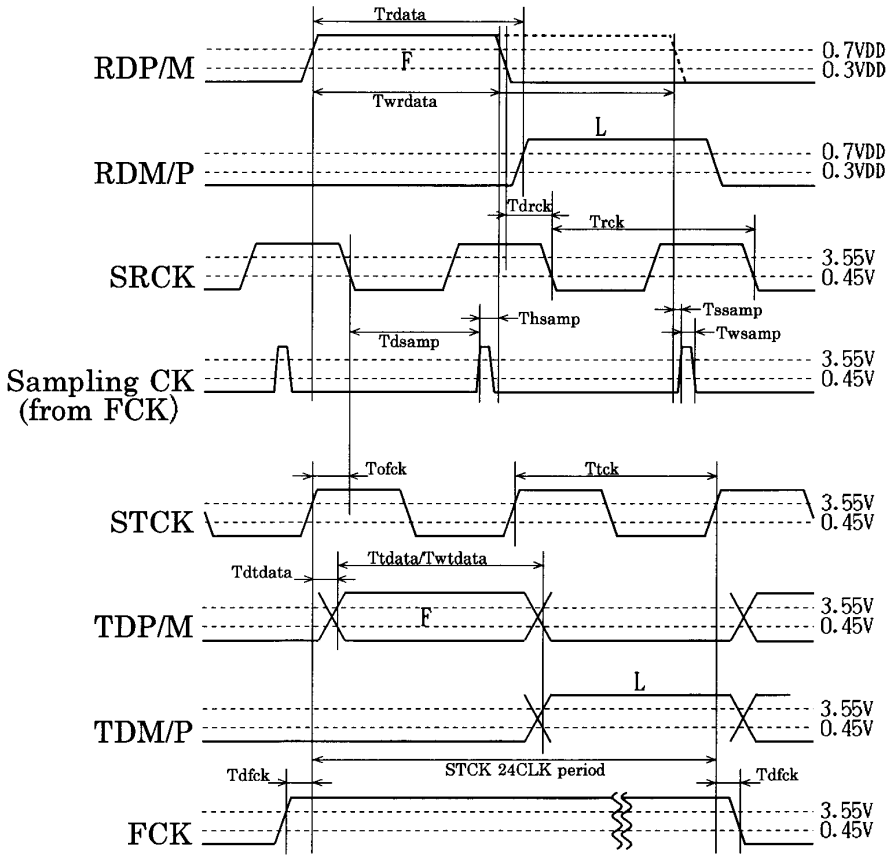


Fig 7 Driver/Receiver interface timings

2-5. External Sampling/Reference Mode

When SVRX is High, the AK520S allows the sampling phase for data and clock recovery to be externally controlled. The slicing level is defined as the voltage difference between the SVRP pin and the SVRN pin. The sampling phase can be set at any desired point by dividing SRCK (1/192 kHz) by SSP0/1/2/3 into sixteen of the period as shown in Fig 8.

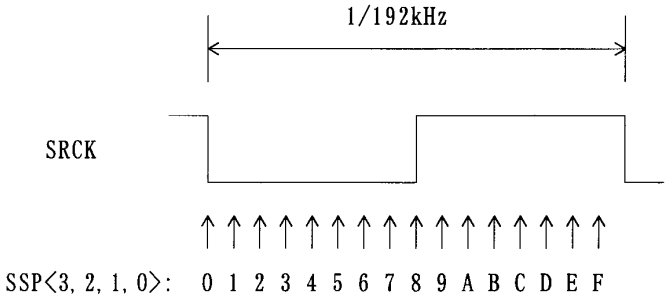


Fig 8

2-6. T1 Timer

The S/T activation procedure recommends the use of a timer to measure the legal response time of a TE as specified by ANSI T1.605 1991 (clause 7.2: Activation/Deactivation). The AK520S implements this function by providing control pins for an external timer (T1). Pin 15, ENT1, goes high to enable the external timer T1. Pin 3, EXPT1, is an input which should be set High to indicate expiration of the timer.
ENT1 goes high as soon as NT1 enters into G2 (Pending activation) state, and waits for INF03 from TE. Once INF03 is received, it acknowledges by sending INF04 and pulls ENT1 low. At this stage, an external timer will indicate the actual response time of the TE.
If INF03 is not received before the external timer expires, then EXPT1 will go high (received from external timer) and AK520S will send INF00 to TE, start timer T2 (to prevent unintentional reactivation), and enter into G4 (Pending Deactivation) state. When T1 timer functions are not used, pull EXPT1 pin low.

2-7. Q and S bits

The AK520S provides transparent access to Q and S bits. The received Q bits are output at pin 50 (QCH) for external processing, and S bits input at pin 49 (SCH) are inserted into appropriate slots for transmission. (If S/T Interface multiframing is not used, pin 49 must be tied to ground.) As shown in Fig 9, the S and Q channels are clocked by the 4 kHz FCK at pin 51. Framing for the S and Q channels is provided by the MFP output at pin 52.

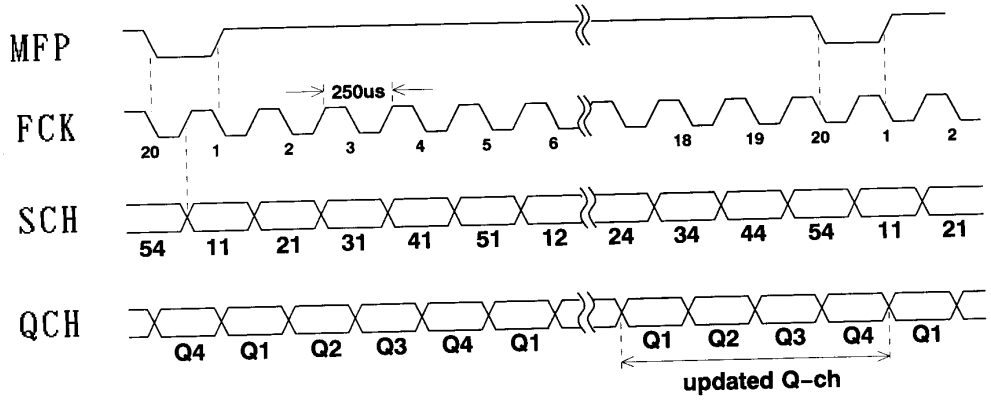


Fig 9

2-8. S Channel Loopback

In the Hardware mode, the AK520S provides independent controls for B1 and B2 loopback toward the TE. The SLB1 (pin 35) forces B1 loopback when set Low, while the SLB2 (pin 36) forces B2 loopback when set Low.

3. TRSW

TRSW is used to control the external DC termination circuitry to save the power consumption during H1 power down mode. Table 3-1 shows the TRSW output definition.

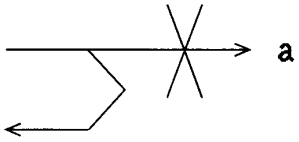
H matrix state	TRSW(Output)	Operation
H1	0 (OFF)	Power Down
Except H1	1 (ON)	Normal

Table 3-1

4. Test Functions

(1) External Control Pin I (8 bits)

Table 4-1 The external control pin I setting of AK520S (8 bits)

No	Pin Name	Description
1	UOA	Mode selection of uoa (M4-7 uoa bit effective/ineffective selection) H : u-only activation is supported (normal) uoa = 1 (M4-7) : S/T Inf. activation is enabled uoa = 0 (M4-7) : S/T Inf. activation is disabled L : u-only activation is not supported
2	STOA	S/T only activation H : Disabled (call by call) L : S/T Interface is activated. G state machine is forced to G3.
3	NTM	Local test mode (set by SW0～2) Enable H : Local test is disabled (normal) L : Local test mode ※When the local test starts (Low), ①TSTLED becomes High ② ntm=0 is mapped to M4-4 in case the U-Interface is synchronized
4	TSW0	Test mode selection (refer to table 4-2)
5	TSW1	
6	TSW2	
7	TRNS	Transparent/nontransparent loopback selection (Both U and S/T) H : Transparent loopback L : Nontransparent loopback ※ As the following figure shows, at the time of nontransparent loopback, the data "a" (loopbacked channel) becomes idle code binary "1". When 2B + D Loop2 is activated, INFO 0 instead of the framed binary "1" is sent to S/T. 
8	FLREN	Metallic test support Enable H: The FLRST input is enabled to support metallic test initiated by LT with losing sealing current. The external DC termination circuitry detects the loss of sealing current and it drives FLRST High. The FLRST High forces H state machine to Full Reset(H1) to metallic test by LT. L: Full reset input is ignored.

The AK520S provides the local NT1 test or diagnostic operations. These functions are activated when the NTM pin is asserted Low. When NTM is Low, the TSW0, TSW1 and TSW2 pins select the test mode as defined in Table 4-2, and ntm=0 is transmitted to the LT in the U-Interface M4-4 overhead bit position to indicate that the NT1 is performing a local test function.

Table 4-2 Test mode setting

No.	TSW0	TSW1	TSW2	Status
1	L	L	L	2B + D Complete Loopback (Loop 2) (Loopback to the U)
2	H	L	L	B1 + B2 Complete Loopback (Loop C) (Loopback to the S)
3	L	H	L	±3 single pulse transmission on U-Interface (0.1 ms cycle)
4	H	H	L	PN pattern transmission on U-Interface
5	L	L	H	±0 single pulse transmission on U-Interface (1 ms cycle)
6	H	L	H	INFO 2 transmission on S/T Interface Note: Independent of the status of U-Interface
7	L	H	H	INFO 4 transmission on S/T Interface Note: Independent of the status of U-Interface
8	H	H	H	(chip test)

(2)External Control Pin II (4 bits)

Table 4-3 AK520S external control pin II (4 bits) setting

No.	Pin Name	Status
1	SLB1	Partial (B1) loopback (Loop C) control H : B1 Loop C disable (normal) L : B1 Loop C enable
2	SLB2	Partial (B2) loopback (Loop C) control H : B2 Loop C disable (normal) L : B2 Loop C enable
3	FXTB	Timing switch for the S/T reception sampling H : Adaptive timing (normal) L : Fixed timing
4	PSDE	Power supply interruption detect/no detect The PSDE High enables PS1 and PS2 inputs mapped to M channel as ps1, ps2 to be sent to the LT. H : Interruption detect (normal). L : Interruption no detect (PS1= 1, PS2 = 0 Fix) When NTM="L", PSDE is fixed to "L" internally.

5. Loopback

(1) Loopback Types and Interface

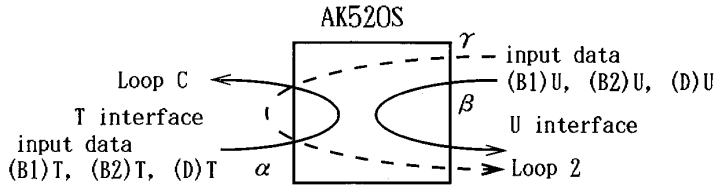


Fig 10

Loop C : Manual Loop C (B1+B2)
Manual Loop C (B1)
Manual Loop C (B2)
Loop 2 : Manual Loop 2 (2B+D)
eoc Loop 2 (2B+D)
eoc Loop 2 (B1)
eoc Loop 2 (B2)

Note 1: The loopback interface γ is for the case of using an external driver/receiver and 2B+D full loopback.
Note 2: Simultaneous Manual-LoopC and Manual-Loop2 is prohibited.
Note 3: Refer to table 5-2 for the output data corresponding to the U-Interface input data (B1)U, (B2)U, (D)U and the T interface input data (B1)T, (B2)T, (D)T.

(2) Loopback data and loopback interface in internal driver/receiver mode and in external driver/receiver mode
(Table 5-1)

Table 5-1

Driver/ receiver	Manual Loop C (B1+B2)	Manual Loop C (B1, B2)	Manual Loop 2(2B+D)	eoc Loop 2 (B1, B2)	eoc Loop 2(2B+D)
Internal	α	α	β	β	β
External	α	α	γ*	β	γ*

Note 1 :Refer to Fig. 10 for the loopback interface α, β and γ.
Note 2 :* indicates that loopback point becomes β instead of γ and S/T output becomes INFO0 when uoa=0 (M4-7) is received.

(3) Table 5-2, 5-3 shows the data flow at S/T & U point when Manual & eoc loopback are simultaneously activated and when one of loopbacks is activated, respectively.

Table 5-2 Data flow when Manual & eoc loopback simultaneously activated

	Loop Back		AK520S Spec.														Comment
ANSI/ ETSI	NT Manual LpC	from LT eoc Lp2	S/T Data B1	S/T Data B2	S/T Data D	S/T Data D.e	S/T op. B1	S/T op. B2	S/T op. D	U op. B1	U op. B2	U op. D	U Data B1	U Data B2	U Data D	NT → LT eoc echo message	
	(1) Non Transparent																
	B1+B2	2B+D	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	Unable To Comply	Manual LpC(B1+B2) has priority
	B1+B2	B1	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	Unable To Comply	Dch only transparent
	B1+B2	B2	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	Unable To Comply	
	B1+B2	B1+B2	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	Unable To Comply	
	ntm B1+B2	2B+D	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	Unable To Comply	ntm LpC(B1+B2) has priority
	ntm B1+B2	B1	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	Unable To Comply	Dch only transparent
	ntm B1+B2	B2	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	Unable To Comply	
	ntm B1+B2	B1+B2	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	Unable To Comply	
	B1	2B+D	S/T	U	U	S/T	⇄	→	→	–	←	←	1	S/T	S/T	Unable To Comply	Manual LpC(B1) has priority
	B1	B1	S/T	U	U	S/T	⇄	→	→	–	←	←	1	S/T	S/T	Unable To Comply	
	B1	B2	S/T	U	U	S/T	⇄	→	→	–	←	←	1	S/T	S/T	Unable To Comply	
	B1	B1+B2	S/T	U	U	S/T	⇄	→	→	–	←	←	1	S/T	S/T	Unable To Comply	
	B2	2B+D	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	1	S/T	Unable To Comply	Manual LpC(B2) has priority
	B2	B1	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	1	S/T	Unable To Comply	
	B2	B2	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	1	S/T	Unable To Comply	
	B2	B1+B2	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	1	S/T	Unable To Comply	
Both ANSI and ETSI	(2) Transparent																
	B1+B2	2B+D	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	Unable To Comply	Manual LpC(B1+B2) has priority
	B1+B2	B1	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	Unable To Comply	
	B1+B2	B2	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	Unable To Comply	
	B1+B2	B1+B2	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	Unable To Comply	
	ntm B1+B2	2B+D	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	Unable To Comply	ntm LpC(B1+B2) has priority
	ntm B1+B2	B1	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	Unable To Comply	
	ntm B1+B2	B2	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	Unable To Comply	
	ntm B1+B2	B1+B2	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	Unable To Comply	
	B1	2B+D	S/T	U	U	S/T	⇄	→	→	–	←	←	S/T	S/T	S/T	Unable To Comply	Manual LpC(B1) has priority
	B1	B1	S/T	U	U	S/T	⇄	→	→	–	←	←	S/T	S/T	S/T	Unable To Comply	
	B1	B2	S/T	U	U	S/T	⇄	→	→	–	←	←	S/T	S/T	S/T	Unable To Comply	
	B1	B1+B2	S/T	U	U	S/T	⇄	→	→	–	←	←	S/T	S/T	S/T	Unable To Comply	
	B2	2B+D	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	S/T	S/T	Unable To Comply	Manual LpC(B2) has priority
	B2	B1	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	S/T	S/T	Unable To Comply	
	B2	B2	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	S/T	S/T	Unable To Comply	
	B2	B1+B2	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	S/T	S/T	Unable To Comply	

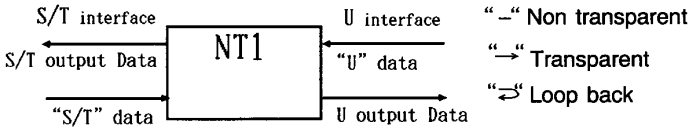


Table 5-3 Data flow at S/T & U point when one of loopbacks is set

	Loop Back		AK520S Spec.														Comment
ANSI/ ETSI	NT Manual LpC	from LT eoc Lp2	S/T Data B1	S/T Data B2	S/T Data D	S/T Data D.e	S/T op. B1	S/T op. B2	S/T op. D	U op. B1	U op. B2	U op. D	U Data B1	U Data B2	U Data D	NT → LT eoc echo message	
	(1) Non Transparent																
	B1+B2	–	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	–	
	ntm B1+B2	–	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	1	1	S/T	–	
	B1	–	S/T	U	U	S/T	⇄	→	→	–	←	←	1	S/T	S/T	–	
	B2	–	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	1	S/T	–	
	–	γ2B+D	INFO0 *1							⇄	⇄	⇄	U	U	U	2B+D Loopback	*1 Loop2 is realized outside chip by LP2CNT.
	–	β2B+D	INFO0							⇄	⇄	⇄	U	U	U	2B+D Loopback	
	–	B1	1	U	U	S/T	–	→	→	⇄	←	←	U	S/T	S/T	B1 Loopback	
	–	B2	U	1	U	S/T	→	–	→	←	⇄	←	S/T	U	S/T	B2 Loopback	
	–	B1+B2	1	1	U	S/T	–	–	→	⇄	⇄	←	U	U	S/T	B1or/B2 Loopback	
Both ANSI and ETSI	(2) Transparent																
	B1+B2	–	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	–	
	ntm B1+B2	–	S/T	S/T	U	S/T	⇄	⇄	→	–	–	←	S/T	S/T	S/T	–	
	B1	–	S/T	U	U	S/T	⇄	→	→	–	←	←	S/T	S/T	S/T	–	
	B2	–	U	S/T	U	S/T	→	⇄	→	←	–	←	S/T	S/T	S/T	–	
	–	γ2B+D *2	U	U	U	0	–	–	–	⇄	⇄	⇄	U	U	U	2B+D Loopback	*2 This is a case when act=1 from LT. When act=0 from LT, INFO2 is transmitted instead.
	–	β2B+D *2	U	U	U	0	–	–	–	⇄	⇄	⇄	U	U	U	2B+D Loopback	
	–	B1	U	U	U	S/T	–	→	→	⇄	←	←	U	S/T	S/T	B1 Loopback	
	–	B2	U	U	U	S/T	→	–	→	←	⇄	←	S/T	U	S/T	B2 Loopback	
	–	B1+B2	U	U	U	S/T	–	–	→	⇄	⇄	←	U	U	S/T	B1or/B2 Loopback	

6. Interface

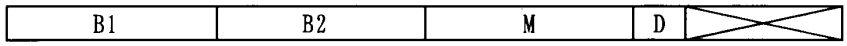
The different interfaces are effective in AK520S when in Hardware mode or in Serial Interface mode.

6-1. Serial Interface mode

The AK520S Serial Interface operates in the master timing mode (i.e., It generates the clock, DCL, and frame strobe, FSC) with the non-multiplexed frame format. The Serial Interface is the bi-directional and full-duplex digital interface. The transmitted and received data is interfaced through the separated input and output pins. The DOUT pin is a CMOS level output which is connected to the DIN pin of the external serial slave device(s). The DIN pin is an input whitch is connected to the open drain DOUT output pins of each slave device.

There are two cycles of the bit clock, DCL, for every serial bit period. The Data on the AK520S DIN is latched and must be valid on the second rising edge of DCL for each bit period. The AK520S updates the data on the DOUT output pin on the first rising edge of DCL for each bit period.

The AK520S serial frame structure is shown below. The frame consists of four bytes per 125 μs frame divided into four logical channels: B1, B2, M, and D. The final 6 bits are not used. The serial B1, B2 and D channels carry the U-Interface transmit and receive B1, B2, and D channel data. (Data are MSB first.)



B1 (7:0); B1 channel data (8 bits)
B2 (7:0); B2 channel data (8 bits)
M (7:0); M channel data (8 bits)
D (1:0); D channel data (2 bits)
N/A(5:0); Not Available (6 bits)

The serial M-channel bit positions on DOUT contain the information from the M4 bit position of the U-Interface basic frame and the nebe indicator as shown below. Note that M-1 represents the bit error at the NT and M-0 represents the bit error at the LT network.

	M-7	M-6	M-5	M-4	M-3	M-2	M-1	M-0
DOUT	act	dea	uoa	aib	UREDY	SE	nebe	febe
DIN	ACTR	tact	DR	-	1	1	1	1

The DIN data are available except during ISW sync acquisition. Activation is controlled through the serial M-channel. The serial controller can request activation by setting the ACTR (M-7) bit high. The AK520S will begin activation by sending the TN tone to the LT followed by SN1, SN2 and SN3 signals as activation proceeds. When the controller sets the tact (M-6) bit high, the AK520S will set U-Interface M4-act bit high, indicating to the LT that layer-1 activation is complete.

The local controller can notice to NT that no data to be transparent is in DIN data flow.

ACTR(Received INF01)=1	activation request
tact(Received INF03)=1	transmit "act=1"
DR(Received INF00)=1	TE dead

M-3～M-0 bits of DIN must be input "1" normally. (reserved for the test)

*Except for the act, all transmitted M channel data in the U-Interface superframe are generated by AK520S automatically.

6-2. Hardware mode

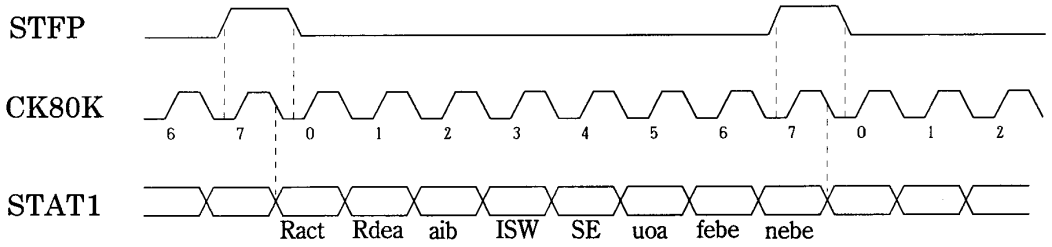
The Hardware mode is for simple applications requiring no microprocessor, like applications not requiring a multiframing function for the S/T Interface etc. However, the monitoring and the input of Q and S channel are possible via QCH, SCH, FCLK, and MFP pin.

The Hardware mode pins are assigned to bear the following functions.

FUNCTION	PIN	I/O
T1 Timer Enable	ENT1	OUT
T1 Timer Expiration	EXPT1	IN
Q-bit Output	QCH	OUT
S-bit Input	SCH	IN
Q/S Framing	MFP	OUT
Q/S Clock	FCK	OUT
Loopback (S/T channel B1)	SLB1	IN
Loopback (S/T channel B2)	SLB2	IN
Status Report #1	STAT1	OUT
Status Report #2	STAT2	OUT
Status Report Clock	CK80K	OUT
Status Report Framing	STFP	OUT

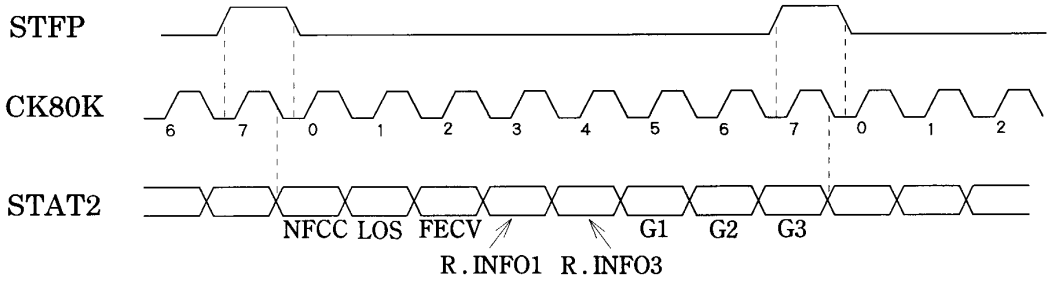
6-2-1. Status Outputs

The AK520S provides two serial output pins which indicate additional status information for the U and S/T transceivers with the Hardware mode. Only STAT1 is available in the Serial Interface mode. When STATDIS is Low each output provides a continuously updated 8-bit serial data word. Status outputs are valid only after ISW synchronization has been achieved. As shown in Fig 11 and 12, the status channels are clocked at 80 kHz by the CK80K output. The status word boundary is indicated by the STFP signal (pin 40). Fig 11 lists the bit assignments for STAT1 and Fig 12 lists bit assignments for STAT2. STATDIS may be set High to disable the STAT1, STAT2 and CK80K to conserve power when status information is not required.



bit0	Ract	: received act(:activation=1)
bit1	Rdea	: received dea(:deactivation=0)
bit2	aib	: received aib(:indicate interruption=1)
bit3	ISW	: synchronized superframe(:synchronize=1)
bit4	SE	: state transition error(:error=1)
bit5	uoa	: U-only-activation(:activate S/T=1)
bit6	febe	: received febe(:error=0)
bit7	nebe	: transmitted febe [near end block error](:error=0)

Fig 11 STAT1 Timing and Interface



bit0	NFCC	: notify of corrupted crc(:error=1)
bit1	LOS	: loss of signal(:loss=1)
bit2	FECV	: far end block code violation at the S(:error=1)
bit3	R. INFO1	: receiving INFO1(:INFO1=1)
bit4	R. INFO3	: receiving INFO3(:INFO3=1)
bit5	G1	: G1 state of S-finite state machine(:G1=1)
bit6	G2	: G2 state of S-finite state machine(:G2=1)
bit7	G3	: G3 state of S-finite state machine(:G3=1)

Fig 12 STAT2 Timing and Interface

7. NT Maintenance Mode

With the appropriate line interface components connected to the HTRG input (pin 1) the AK520S can decode and response to the AC and DC signalling sequences defined for NT maintenance operations in ANSI T1.601. Fig 13 shows the maintenance mode state diagram.
Bringing the HTRGEN input (pin 77) High enables maintenance mode processing. The AK520S provides both the insertion loss measurement mode (ILMT) and the quiet (QM) maintenance modes.
The maintenance mode decoder detects only valid trigger signals witch consist of;
- A 500 ms (or longer) start interval,
- Six, eight, or ten pulses at least 7.5 ms long
- A 500 ms (or longer) stop interval.

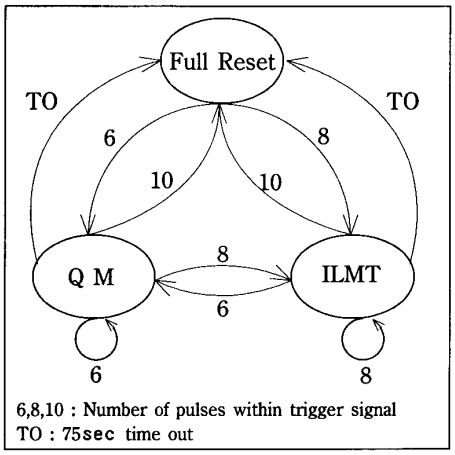


Fig 13 ANSI Maintenance Mode Processing

When a trigger signal containing six pulses is detected, the AK520S enters the quiet maintenance mode and will not respond to a TL wakeup tone from the LT. The device leaves the quiet mode when another trigger signal with ten pulses is received or a 75 second timeout period elapses sending it back to the Full Reset state. (If a valid trigger signal with eight pulses is detected in the quiet mode, the device immediately enters the ILMT maintenance mode.)
When a trigger signal containing eight pulses is detected, the AK520S enters the ILMT maintenance mode and begins transmission of an insertion loss measurement test signal. The ILMT maintenance mode continues until another trigger signal with ten pulses is received or a 75 second timeout period elapses sending it back to the Full Reset state. (If a valid trigger signal with six pulses is detected in the ILMT mode, the device immediately enters the quiet maintenance mode.)

Application Circuit

Fig 14 shows a circuit example for a general NT1 application of AK520S.

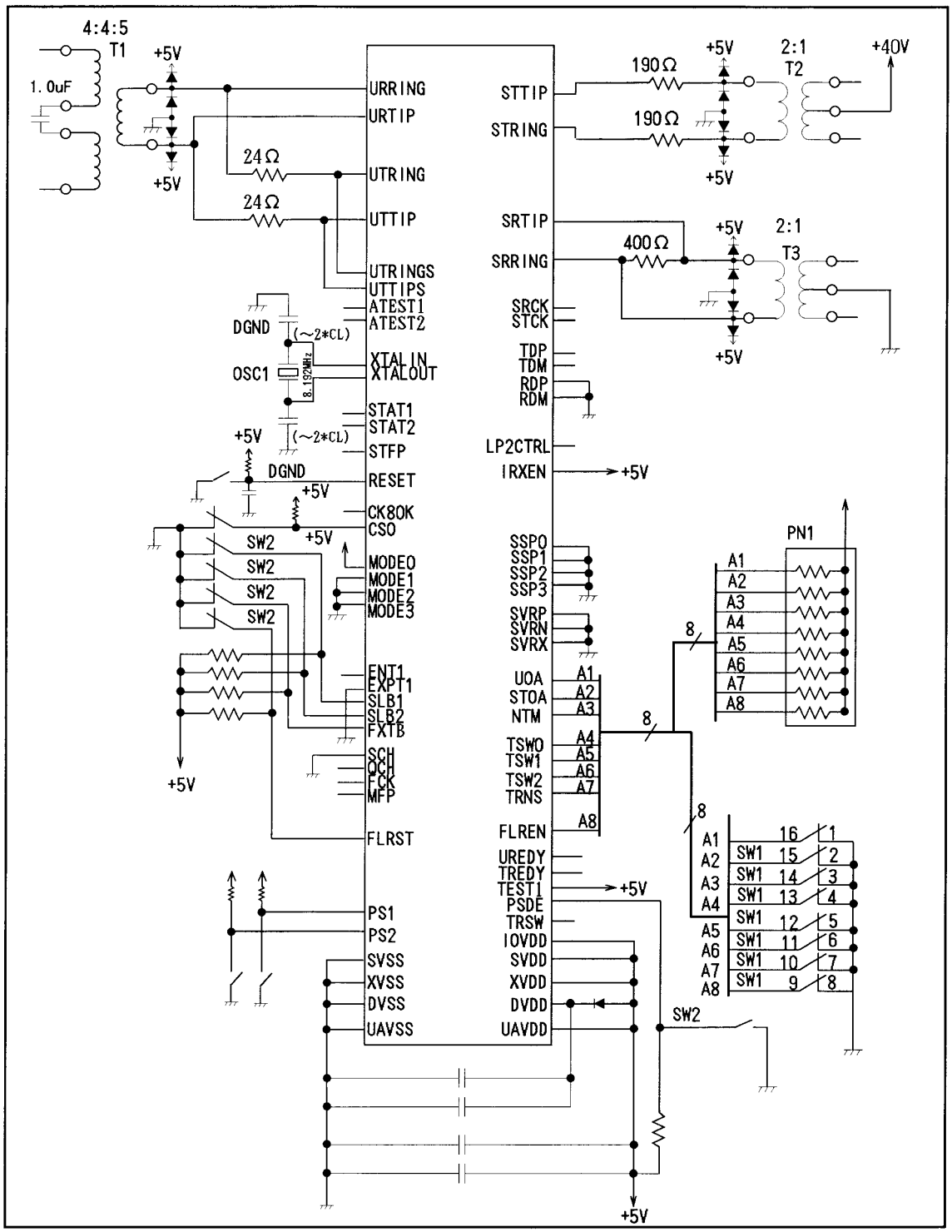


Fig 14 General NT1 application example

Table 7 shows the recommended values for external components.

Component	Parameter	Recommended Value
U I/F Line Transformer	Turns ratio	5:4:4, ± 1%
	Structure	Center tapped line side
	Chip side Inductance	10.5 mH ± 20%
	Leakage Inductance	47 μH ± 50%
	Interwinding Capacitance	170 pF Maximum
	DC Resistance(chip side, Rwp)	3.5 Ω Maximum
	DC Resistance(line side, Rws)	4.5 Ω Maximum
S/T I/F Line Transformers	Turns ratio	1:2, ± 1%
	Primary Inductance(line side)	30 mH ± 10%
	Leakage Inductance	100 μH Maximum
	Interwinding Capacitance	200 pF Maximum
	DC Resistance(Primary, Rwp)	10.0 Ω Maximum
	DC Resistance(Secondary, Rws)	5 Ω Maximum
Protection Diodes D1, D2, D3, D4	Type 1N4001 Silicon Diode	1 A, 50 V
Crystal (NT Side) (NOTE 1)	Normal frequency	8.192 MHz
	Operation Mode	Fundamental, parallel resonant
	Load Capacitance (CL)	10 pF Typical 16pF Maximum
	Shunt Capacitance (C0)	7pF Maximum
	Tolerance	±50 ppm (25 ℃)
	Range(includes characteristic of temperature and aging)	±100 ppm, -20 to +85 ℃
	Maximum ESR	35 Ω
	Drive Level	1.5 mArms Maximum
Crystal Loading Capacitors:NT Side	Capacitance, Tolerance, Rating	CL x 2 , ±5 %, 10 V (NOTE 2)
	Construction	NP0 ceramic or equivalent
U I/F In-line Resistors Rtu	Resistance, Tolerance, Rating	24.0 Ω, ±1 %, 1/4 W (NOTE 3)
S/T I/F In-line Resistors Rtst(TX side)	Resistance, Tolerance, Rating	191 Ω, ±1 %, 1/4 W (NOTE 3)
Rtsr(RX side)	Resistance, Tolerance, Rating	383 Ω, ±1 %, 1/4 W (NOTE 3)

(NOTE 1) In the case that crystal other than listed in this data sheet is intended to use, please consult with us.

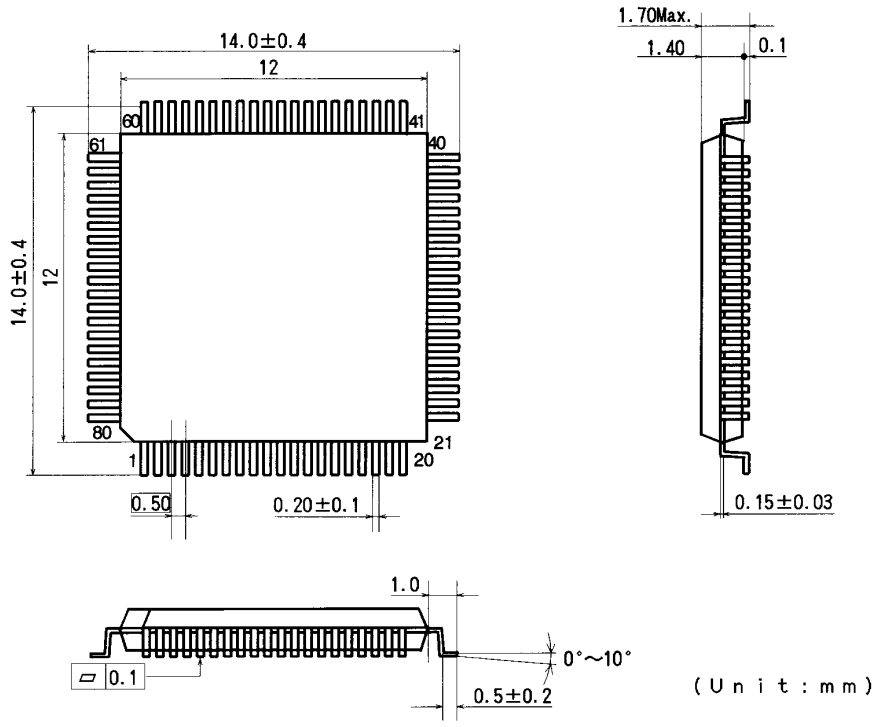
(NOTE 2) Please decide loading capacitor value of crystal with consideration to stray capacitance of board etc. to fit its oscillation to the center frequency.

(NOTE 3) Please decide In-line Resistors value with consideration to stray DC Resistance of transformer that is applied to conform impedance matching at the line interface.

Table 7 Recommended values for external components

Package

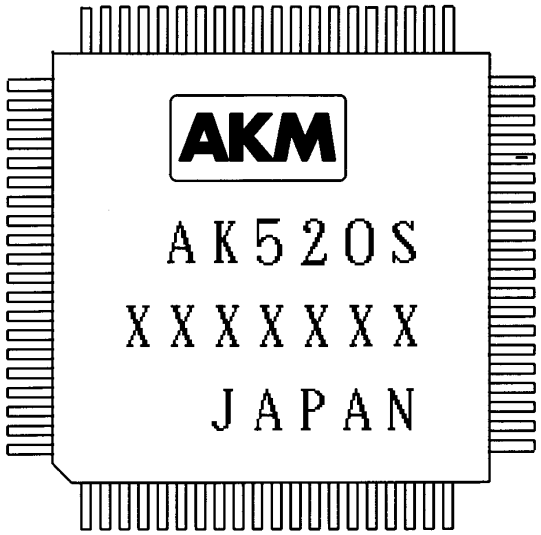
■Package Outline



(Unit: mm)

■Marking

(1)Asahi Kasei Logo
(2)Marking Code: AK520S
(3)Date Code: XXXXXX(7 digits)
(4)Country of Origin: JAPAN



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