AFE5808A 0.75 nV/√Hz, 65-MSPS, 158 mW/Channel, Fully-Integrated, 8-Channel, 14- and 12-Bit, Ultrasound Analog Front-End With Passive CW Mixer

1 Features

- 8-Channel Complete Analog Front-End
  - LNA, VCAT, PGA, LPF, ADC, and CW Mixer
- Programmable Gain Low-Noise Amplifier (LNA)
  - 24-, 18-, or 12-dB Gain
  - 0.25-, 0.5-, or 1-V_{PP} Linear Input Range
  - 0.63-, 0.7-, or 0.9-nV/√Hz Input-Referred Noise
  - Programmable Active Termination
- 40-dB, Low-Noise Voltage-Controlled Attenuator (VCAT)
- 24-, or 30-dB Programmable Gain Amplifier (PGA)
- 3rd-Order, Linear-Phase, Low-Pass Filter (LPF)
  - 10 MHz, 15 MHz, 20 MHz, or 30 MHz
- 14-bit Analog-to-Digital Converter (ADC)
  - 77-dBFS SNR at 65 MSPS
  - LVDS Outputs
- Noise and Power Optimizations (Full Chain)
  - 158 mW/CH at 0.75 nV/√Hz, 65 MSPS
  - 101 mW/CH at 1.1 nV/√Hz, 40 MSPS
  - 80 mW/CH in CW Mode
- Excellent Device-to-Device Gain Matching
  - ±0.5 dB (Typical) and ±0.9 dB (Maximum)
- Low Harmonic Distortion
- Fast and Consistent Overload Recovery
- Passive Mixer for Continuous Wave Doppler (CWD)
  - Low Close-in Phase Noise: –156 dBc/Hz at 1 KHz Off 2.5-MHz Carrier
  - Phase Resolution of 1/16λ
  - Support 16X, 8X, 4X and 1X CW Clocks
  - 12-dB Suppression on 3rd and 5th Harmonics
  - Flexible Input Clocks
- Small Package: 15-mm × 9-mm, 135-Pin NFBGA

2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipments

3 Description

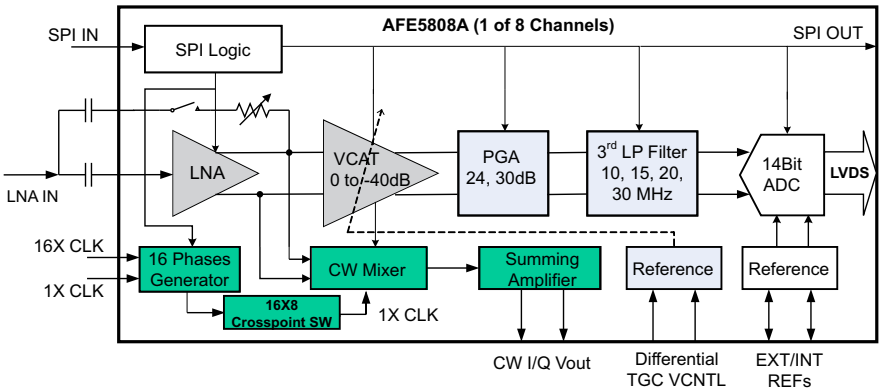
The AFE5808A is a highly-integrated, analog front-end (AFE) solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5808A integrates a complete time-gain-control (TGC) imaging path and a continuous wave Doppler (CWD) path. This device also enables users to select one of various power and noise combinations to optimize system performance. Therefore, the AFE5808A is an outstanding ultrasound analog front-end solution not only for high-end systems, but also for portable ones.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE5808A	NFBGA (135)	9.00 mm × 15.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2014) to Revision D — **Page**

- Added Device Information and ESD Ratings tables, and *Detailed Description*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections. ... 1
- Updated Pin Diagram. ... 6
- Deleted *Packaging/Ordering Information* table ... 9
- Updated ESD values to ±1000 (HBM) and ±250 (CDM). ... 9
- Updated $\omega_0 t+22.5^\circ$ to $\omega_0 t-22.5^\circ$ in Equation 2 ... 35
- Updated $t+1/16f_0$ to $t-1/16f_0$ in Equation 3 ... 37
- Added Application Companion Devices table. ... 57
- Added Figure 85. ... 64

Changes from Revision B (April 2012) to Revision C — **Page**

- Changed pin description of CLKM_16X from "In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKM for the CW mixer" to "... in-phase 1X CLKM for the CW mixer" ... 7
- Changed pin description of CLKP_16X from "In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKP for the CW mixer" to "... in-phase 1X CLKP for the CW mixer" ... 7
- Changed pin description of CLKM_1X from "In the 1X CW clock mode, this pin becomes the in-phase 1X CLKP for the CW mixer" to "... quadrature-phase 1X CLKP for the CW mixer" ... 7
- Changed pin description of CLKP_1X from "In the 1X CW clock mode, this pin becomes the in-phase 1X CLKP for the CW mixer" to "... quadrature-phase 1X CLKP for the CW mixer" ... 7
- Added min and max columns to Absolute Maximum Ratings table ... 9
- Changed CLK duty cycle from "35%~65%" to "33% to 66%" ... 12
- Deleted "In the 16X operation mode, the CW operation range is limited to 8 MHz due to the 16X CLK. The maximum clock frequency for the 16X CLK is 128 MHz. " in the footnote for CW Operation Range ... 12

- Added "After January, 2014, that is date code after 41XXXXX, the CW Clock frequency (16X mode) can be supported up to 145 MHz and approximately 33 to 50% duty cycle based on additional test screening." 12
- Changed 5V 1% duty cycle current from 16.5 mA to 26 mA. 13
- Changed Input Clock to Bit Clock and deleted "(for output data and frame clock)" 17
- Changed Input Clock to Bit Clock and deleted "(for output data and frame clock)" 17
- Added a note "The above timing data can be applied to 12-bit or 16-bit LVDS rates" 17
- Added "The maximum PGA output level can be above 2 V_{PP} even with the clamp circuit enabled" in the PGA description. 32
- Changed "10 Ω" to "approximately 10- to 15-Ω " in Figure 64 34
- Updated Figure 67 36
- Updated Figure 69 38
- Changed SPI pull down resistors from "100 kΩ" to "20 kΩ" 44
- Corrected a typo in Reg0x2[15:13], i.e. changed 0x2[15:3] to 0x2[15:13] 46
- Added Reg0x32[10] PGA_CLAMP_-6dB. 51
- Added a note " 0x32[10] needs to be set as 0" in the Reg0x33[7:5] description. 51
- Combined Reg 0x33[6:5] and 0x33[7] and added notes to PGA_CLAMP_LEVEL: "The maximum PGA output level can exceed 2 V_{PP} with the clamp circuit enabled. In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7] = 0". 51
- Added Note: 54[9] is only effective in CW mode. 52
- Added and reorganized Description of LNA Input Impedances Configuration 53
- Added Table 9 55
- Added text "TI recommends that $V_{CNTLM/P}$ noise is below 25 nV/$\sqrt{Hz}$ at 1 kHz and 5 nV/$\sqrt{Hz}$ at 50 kHz. In high channel count premium systems, the VCNTLM/P noise requirement is higher." 64
- Added a note "The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH " 67
- Added LMK048X into the CW clock application information section. 69
- Updated Figure 89 to include LMK devices 69
- Updated Figure 90 to include LMK devices 70
- Added LMK048X into the ADC clock application information section. 71
- Deleted "VREF_IN" from "The AFE5808A has a number of reference supplies needed to be bypassed." 74
- Added "To avoid noise coupling through supply pins, TI recommends to keep sensitive input pins, such as INM, INP, ACT pins aways from the AVDD 3.3 V and AVDD_5V planes. For example, either the traces or vias connected to these pins should NOT be routed across the AVDD 3.3 V and AVDD_5V planes, that is to avoid power planes under INM, INP, and ACT pins." in *Layout Guidelines* 74

Changes from Revision A (November 2011) to Revision B **Page**

- Added pin compatible device AFE5803 to the Description text 5
- Changed the PIN FUNCTIONS Descriptions 6
- Changed the t_{delay} Test Condiitons From: Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus half the input clock period (T). To: Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus 3/7 of the input clock period (T). 16
- Added Note: "In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7] = 0." 32
- Changed Figure 64 34
- Changed the CHANNEL_OFFSET_SUBSTRACTION_ENABLE: Address: 3[8] text 49
- Added Note: 59[8] is only effective in TGC test mode. 53
- Changed Figure 81 60

Changes from Original (October 2011) to Revision A **Page**

- Moved footnote "Low Noise Mode/Medium Power Mode/Low Power Mode" to the test condition for Input Referred Current Noise 10
- Changed CW signal carrier freq From 8 MHz Max To 8 MHz typical 12
- Changed CW Clock freq, 4X CLK From 32 MHz Max To 32 MHz typical 12
- Added footnote for CW Operation Range 12
- Added text to the Power Management Priority section 43
- Added text to the ADC Register Map section 46
- Added text to the CW Clock Selection section 69

5 Description (continued)

The AFE5808A device contains eight voltage controlled amplifiers (VCA), 14- and 12-bit analog-to-digital converters (ADC), and CW mixers. The VCA includes a low-noise amplifier (LNA), voltage-controlled attenuator (VCAT), programmable gain amplifier (PGA), and low-pass filter (LPF). The LNA gain is programmable to support 250 mV_{PP} to 1 V_{PP} input signals. Programmable active termination is also supported by the LNA. The ultralow noise VCAT provides an attenuation control range of 40 dB, and improves overall low gain SNR that benefits harmonic imaging and near field imaging. The PGA provides gain options of 24 dB and 30 dB. In front of the ADC, a LPF can be configured as 10 MHz, 15 MHz, 20 MHz, or 30 MHz to support ultrasound applications with different frequencies. The high-performance 14-bit, 65-MSPS ADC in the AFE5808A device achieves 77-dBFS SNR, and ensures excellent SNR at low-chain gain. The ADC LVDS outputs enable flexible system integration desired for miniaturized systems.

The AFE5808A device also incorporates a low-power passive mixer and a low-noise summing amplifier to accomplish on-chip CWD beamforming. Sixteen selectable phase-delays can be applied to each analog input signal. A unique 3rd- and 5th-order harmonic-suppression filter is implemented to enhance CW sensitivity.

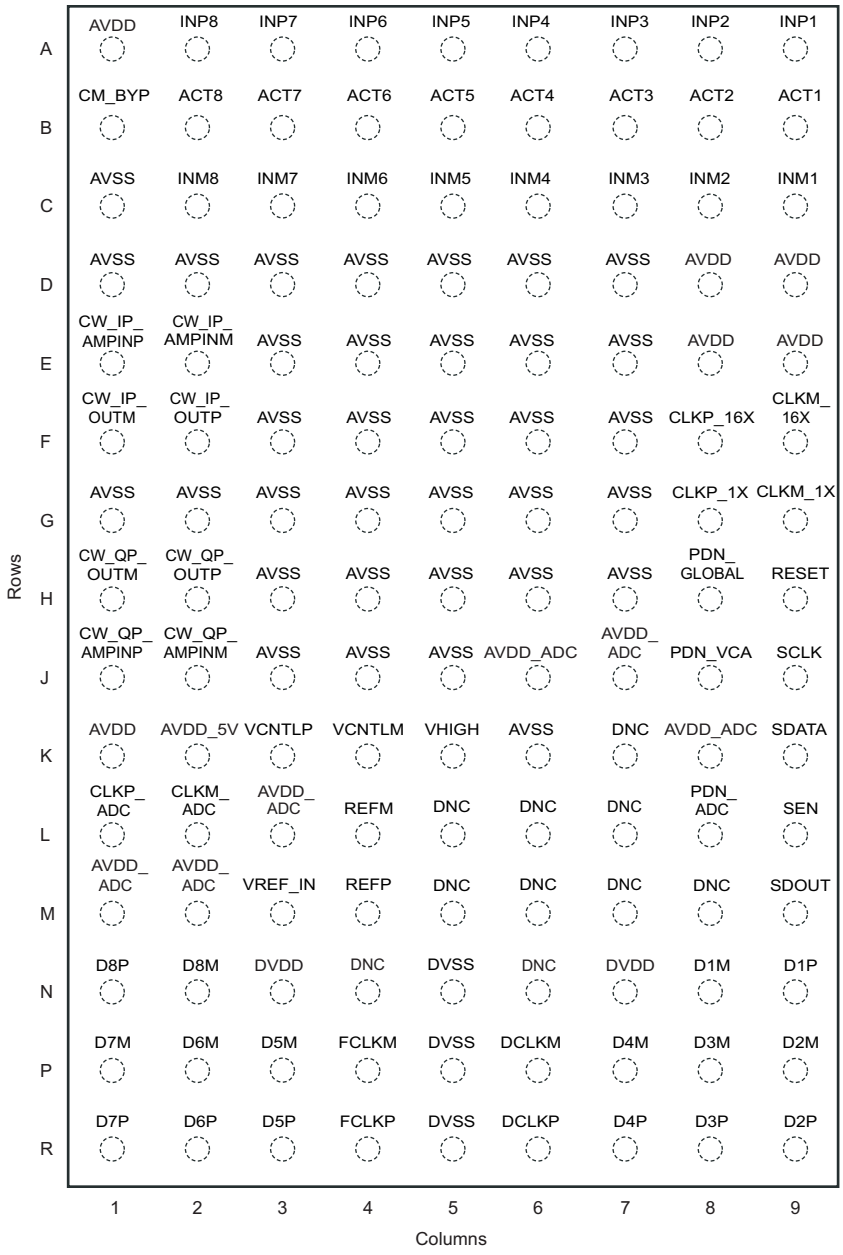
The AFE5808A is available in a 15-mm × 9-mm, 135-pin BGA package and it is specified for operation from 0°C to 85°C. This device is also pin-to-pin compatible with the AFE5803, AFE5807, and AFE5808.

NOTE

The AFE5808A is an enhanced version of AFE5808 and is recommended for new designs. Compared to the AFE5808, the AFE5808A expands the cutoff frequency range of the digital high-pass filter; increases the handling capability of extreme overload signals; and lowers the correlated noise significantly when high-impedance source appears.

6 Pin Configuration and Functions

ZCF Package
135-Pin NFBGA
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ACT1...ACT8	B9~ B2	I	Active termination input pins for CH1~8. 1-µF capacitors are recommended. See the *Application and Implementation* section.
AVDD	A1, D8, D9, E8, E9, K1	Supply	3.3-V Analog supply for LNA, VCAT, PGA, LPF and CWD blocks
AVDD_5V	K2	Supply	5-V Analog supply for LNA, VCAT, PGA, LPF and CWD blocks

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
AVDD_ADC	J6, J7, K8, L3, M1, M2	Supply	1.8-V Analog power supply for ADC
AVSS	C1, D1~D7, E3~E7, F3~F7, G1~G7, H3~H7,J3~J5, K6	—	Analog ground
CLKM_ADC	L2	I	Negative input of differential ADC clock. In the single-end clock mode, it can be tied to GND directly or through a 0.1-µF capacitor.
CLKP_ADC	L1	I	Positive input of differential ADC clock. In the single-end clock mode, it can be tied to clock signal directly or through a 0.1-µF capacitor.
CLKM_16X	F9	I	Negative input of differential CW 16X clock. Tie to GND when the CMOS clock mode is enabled. In the 4X and 8X CW clock modes, this pin becomes the 4X or 8X CLKM input. In the 1X CW clock mode, this pin becomes the in-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used.
CLKP_16X	F8	I	Positive input of differential CW 16X clock. In 4X and 8X clock modes, this pin becomes the 4X or 8X CLKP input. In the 1X CW clock mode, this pin becomes the in-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used.
CLKM_1X	G9	I	Negative input of differential CW 1X clock. Tie to GND when the CMOS clock mode is enabled (Refer to Figure 88 for details). In the 1X clock mode, this pin is the quadrature-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used.
CLKP_1X	G8	I	Positive input of differential CW 1X clock. In the 1X clock mode, this pin is the quadrature-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used.
CM_BYP	B1	Bias	Bias voltage and bypass to ground. ≥ 1 µF is recommended. To suppress the ultra low frequency noise, 10 µF can be used.
CW_IP_AMPINM	E2	O	Negative differential input of the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINM and CW_IP_OUTP. This pin becomes the CH7 PGA negative output when PGA test mode is enabled. Can be floated if not used.
CW_IP_AMPINP	E1	O	Positive differential input of the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINP and CW_IP_OUTM. This pin becomes the CH7 PGA positive output when PGA test mode is enabled. Can be floated if not used.
CW_IP_OUTM	F1	O	Negative differential output for the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINP andCW_IP_OUTPM. Can be floated if not used.
CW_IP_OUTP	F2	O	Positive differential output for the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINM and CW_IP_OUTP. Can be floated if not used.
CW_QP_AMPINM	J2	O	Negative differential input of the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINM and CW_QP_OUTP. This pin becomes CH8 PGA negative output when PGA test mode is enabled. Can be floated if not used.
CW_QP_AMPINP	J1	O	Positive differential input of the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINP and CW_QP_OUTM. This pin becomes CH8 PGA positive output when PGA test mode is enabled. Can be floated if not used.
CW_QP_OUTM	H1	O	Negative differential output for the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINP and CW_QP_OUTM. Can be floated if not used.
CW_QP_OUTP	H2	O	Positive differential output for the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINM and CW_QP_OUTP. Can be floated if not used.
D1M~D8M	N8, P9~P7, P3~P1, N2	O	ADC CH1~8 LVDS negative outputs
D1P~D8P	N9, R9~R7, R3~R1, N1	O	ADC CH1~8 LVDS positive outputs
DCLKM	P6	O	LVDS bit clock (7x) negative output
DCLKP	R6	O	LVDS bit clock (7x) positive output
DNC	K7, L5~L7,M5~M8, N4, N6	—	Do not connect. Must leave floated.
DVDD	N3, N7	Supply	ADC digital and I/O power supply, 1.8 V
DVSS	N5, P5, R5	—	ADC digital ground
FCLKM	P4	O	LVDS frame clock (1X) negative output
FCLKP	R4	O	LVDS frame clock (1X) positive output
INM1…INM8	C9~C2	I	CH1~8 complimentary analog inputs. Bypass to ground with ≥ 0.015-µF capacitors. The HPF response of the LNA depends on the capacitors.
INP1...INP8	A9~A2	I	CH1~8 analog inputs. AC couple to inputs with ≥ 0.1-µF capacitors.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PDN_ADC	L8	I	ADC partial (fast) power down control pin with an internal pull down resistor of 100 kΩ. Active High. Either 1.8-V or 3.3-V logic level can be used.
PDN_VCA	J8	I	VCA partial (fast) power down control pin with an internal pull down resistor of 20 kΩ. Active High. 3.3-V logic level is recommended.
PDN_GLOBAL	H8	I	Global (complete) power-down control pin for the entire chip with an internal pull down resistor of 20 kΩ. Active High. 3.3-V logic level is recommended.
REFM	L4	—	0.5-V reference output in the internal reference mode. Must leave floated in the internal reference mode. Adding test point on PCB is recommended for monitoring the reference output.
REFP	M4	—	1.5-V reference output in the internal reference mode. Must leave floated in the internal reference mode. Adding test point on PCB is recommended for monitoring the reference output.
RESET	H9	I	Hardware reset pin with an internal pull-down resistor of 20 kΩ. Active high, 3.3-V logic level is recommended.
SCLK	J9	I	Serial interface clock input with an internal pull-down resistor of 20 kΩ, 3.3-V logic level is recommended.
SDATA	K9	I	Serial interface data input with an internal pull-down resistor of 20 kΩ, 3.3-V logic level is recommended.
SDOUT	M9	O	Serial interface data readout. High impedance when readout is disabled, 1.8-V logic
SEN	L9	I	Serial interface enable with an internal pull up resistor of 20 kΩ. Active low, 3.3-V logic level is recommended.
VCNTLM	K4	I	Negative differential attenuation control pin. Common mode voltage is 0.75V.
VCNTLP	K3	I	Positive differential attenuation control pin. Common mode voltage is 0.75V.
VHIGH	K5	Bias	Bias voltage; bypass to ground with ≥ 1 µF.
VREF_IN	M3	Bias	ADC 1.4-V reference input in the external reference mode; bypass to ground with 0.1 µF.
DNC	K7, L5~L7, M5~M8, N4, N6	—	Do not connect. Must leave floated.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD	–0.3	3.9	V
	AVDD_ADC	–0.3	2.2	V
	AVDD_5V	–0.3	6	V
	DVDD	–0.3	2.2	V
Voltage between AVSS and LVSS		–0.3	0.3	V
Voltage at analog inputs and digital inputs		–0.3	min [3.6, AVDD + 0.3]	V
Peak solder temperature(2)			260	°C
Maximum junction temperature (T_J), any condition			105	°C
Operating temperature		0	85	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device complies with JSTD-020D.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
AVDD	3.15	3.6	V
AVDD_ADC	1.7	1.9	V
DVDD	1.7	1.9	V
AVDD_5V	4.75	5.5	V
Ambient temperature, T_A	0	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		AFE5808A ZCF (NFBGA) 135 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

At AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, no active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, internal 500-Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C (unless otherwise noted). Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
TGC FULL SIGNAL CHANNEL (LNA+VCAT+LPF+ADC)						
en (RTI)	Input voltage noise over LNA Gain (low noise mode)	Rs = 0 Ω, f = 2 MHz, LNA = 24 dB, 18 dB, and 12 dB, PGA = 24 dB		0.76/0.83/1.16		nV/√Hz
		Rs = 0 Ω, f = 2 MHz, LNA = 24 dB, 18 dB, and 12 dB, PGA = 30 dB		0.75/0.86/1.12		
	Input voltage noise over LNA Gain (low power mode)	Rs = 0 Ω, f = 2 MHz, LNA = 24 dB, 18 dB, and 12 dB, PGA = 24 dB		1.1/1.2/1.45		nV/√Hz
		Rs = 0 Ω, f = 2 MHz, LNA = 24 dB, 18 dB, and 12 dB, PGA = 30 dB		1.1/1.2/1.45		
	Input Voltage Noise over LNA Gain (Medium Power Mode)	Rs = 0 Ω, f = 2 MHz, LNA = 24 dB, 18 dB, and 12 dB, PGA = 24 dB		1/1.05/1.25		nV/√Hz
		Rs = 0 Ω, f = 2 MHz, LNA = 24 dB, 18 dB, and 12 dB, PGA = 30 dB		0.95/1.0/1.2		
	Input referred current noise	Low Noise Mode/Medium Power Mode/Low Power Mode		2.7/2.1/2		pA/√Hz
NF	Noise figure	Rs = 200 Ω, 200-Ω active termination, PGA = 24 dB, LNA = 12 dB, 18 dB, and 24 dB		3.85/2.4/1.8		dB
		Rs = 100 Ω, 100-Ω active termination, PGA = 24 dB, LNA = 12 dB, 18 dB, and 24 dB		5.3/3.1/2.3		dB
V_{MAX}	Maximum Linear Input Voltage	LNA gain = 24 dB, 18 dB, and 12 dB		250/500/1000		mV_{PP}
V_{CLAMP}	Clamp Voltage	Reg52[10:9] = 0, LNA = 24 dB, 18 dB, and 12 dB		350/600/1150		
	PGA Gain	Low noise mode		24/30		dB
		Medium and low power mode		24/28.5		
	Total gain	LNA = 24 dB, PGA = 30 dB, Low noise mode		54		dB
		LNA = 2 4dB, PGA = 30 dB, Med power mode		52.5		
		LNA = 24 dB, PGA = 30 dB, Low power mode		52.5		
	Ch-CH Noise Correlation Factor without Signal (1)	Summing of 8 channels		0		
	Ch-CH Noise Correlation Factor with Signal (1)	Full band (VCNTL = 0/0.8)		0.15/0.17		
		1MHz band over carrier (VCNTL= 0/0.8)		0.18/0.75		
	Signal to Noise Ratio (SNR)	VCNTL = 0.6 V (22-dB total channel gain)	68	70		dBFS
		VCNTL = 0, LNA = 18 dB, PGA = 24 dB	59.3	63		
		VCNTL = 0, LNA = 24 dB, PGA = 24 dB		58		
	Narrow Band SNR	SNR over 2-MHz band around carrier at VCNTL = 0.6 V (22 dB total gain)	75	77		dBFS
	Input Common-mode Voltage	At INP and INM pins		2.4		V
	Input resistance			8		kΩ
		Preset active termination enabled		50/100/200/400		Ω
	Input capacitance			20		pF
	Input Control Voltage	$V_{CNTLP} – V_{CNTLM}$	0		1.5	V
	Common-mode voltage	V_{CNTLP} and V_{CNTLM}		0.75		V
	Gain Range			-40		dB
	Gain Slope	V_{CNTL}= 0.1 to 1.1 V		35		dB/V
	Input Resistance	Between V_{CNTLP} and V_{CNTLM}		200		KΩ
	Input Capacitance	Between V_{CNTLP} and V_{CNTLM}		1		pF
	TGC Response Time	VCNT L= 0 to 1.5-V step function		1.5		µs
	3rd order-Low-pass Filter			10, 15, 20, 30		MHz
	Settling time for change in LNA gain			14		µs
	Settling time for change in active termination setting			1		µs

(1) Noise correlation factor is defined as Nc/(Nu+Nc), where Nc is the correlated noise power in single channel; and Nu is the uncorrelated noise power in single channel. Its measurement follows the below equation, in which the SNR of single channel signal and the SNR of summed eight channel signal are measured.

$$\frac{N_C}{N_U + N_C} = \frac{10^{-\frac{8CH\_SNR}{10}}}{10^{-\frac{1CH\_SNR}{10}}} \times \frac{1}{56} - \frac{1}{7}$$

Electrical Characteristics (continued)

At AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, no active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, internal 500-Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C (unless otherwise noted). Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
AC ACCURACY						
	LPF Bandwidth tolerance			±5%		
	CH-CH group delay variation	2 MHz to 15 MHz		2		ns
	CH-CH Phase variation	15-MHz signal		11		Degree
	Gain matching	0 V < VCNTL < 0.1 V (Dev-to-Dev)		±0.5		dB
		0.1 V < VCNTL < 1.1 V(Dev-to-Dev)	–0.9	±0.5	0.9	
		0.1 V < VCNTL < 1.1 V(Dev-to-Dev) Temp = 0°C and 85°C	–1.1	±0.5	1.1	
		1.1 V < VCNTL < 1.5 V(Dev-to-Dev)		±0.5		
	Gain matching	Channel-to-channel		±0.25		dB
	Output offset	V_{cntl}= 0, PGA = 30 dB, LNA = 24 dB	–75		75	LSB
AC PERFORMANCE						
HD2	Second-Harmonic Distortion	f_{IN} = 2 MHz; V_{OUT} = –1 dBFS		–60		dBc
		f_{IN} = 5 MHz; V_{OUT} = –1 dBFS		–60		
		f_{IN} = 5 MHz; V_{IN}= 500 mV_{PP}, V_{OUT} = –1 dBFS, LNA = 18 dB, V_{CNTL}= 0.88 V		–55		
		f_{IN} = 5 MHz; Vin = 250 mV_{PP}, V_{OUT} =–1 dBFS, LNA = 24 dB, V_{CNTL}= 0.88 V		–55		
HD3	Third-Harmonic Distortion	f_{IN} = 2 MHz; V_{OUT} = –1 dBFS		–55		dBc
		f_{IN} = 5 MHz; V_{OUT} = –1 dBFS		–55		
		f_{IN} = 5 MHz; VIN = 500 mV_{PP}, V_{OUT} = –1 dBFS, LNA = 18 dB, V_{CNTL}= 0.88 V		–55		
		f_{IN} = 5 MHz; VIN = 2 50 mV_{PP}, V_{OUT} = –1 dBFS, LNA = 24 dB, V_{CNTL}= 0.88 V		–55		
THD	Total Harmonic Distortion	f_{IN} = 2 MHz; V_{OUT}= –1 dBFS		–55		dBc
		f_{IN} = 5 MHz; V_{OUT}= –1 dBFS		–55		
IMD3	Intermodulation distortion	f1 = 5 MHz at –1 dBFS, f2 = 5.01 MHz at –27 dBFS		–60		dBc
XTALK	Cross-talk	f_{IN} = 5 MHz; V_{OUT}= –1 dBFS		–65		dB
	Phase Noise	1 kHz off 5 MHz (V_{CNTL}= 0 V)		–132		dBc/Hz
LNA						
	Input Referred Voltage Noise	Rs = 0 Ω, f = 2MHz, Rin = High Z, Gain = 24/18/12 dB		0.63/0.70/0.9		nV/√Hz
	High-Pass Filter	–3 dB Cut-off Frequency		50/100/150/200		KHz
	LNA linear output			4		V_{PP}
VCAT+ PGA						
	VCAT Input Noise	0-dB/–40-dB attenuation		2/10.5		nV/√Hz
	PGA Input Noise	24 dB/30 dB		1.75		nV/√Hz
	-3dB HPF cut-off Frequency			80		kHz

Electrical Characteristics (continued)

At AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, no active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, internal 500-Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C (unless otherwise noted). Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CW DOPPLER						
en (RTI)	Input voltage noise (CW)	1-channel mixer, LNA = 24 dB, 500-Ω feedback resistor		0.8		nV/√Hz
		8-channel mixer, LNA = 24 dB, 62.5-Ω feedback resistor		0.33		
en (RTO)	Output voltage noise (CW)	1-channel mixer, LNA = 24 dB, 500-Ω feedback resistor		12		nV/√Hz
		8-channel mixer, LNA = 24 dB, 62.5-Ω feedback resistor		5		
en (RTI)	Input voltage noise (CW)	1-channel mixer, LNA = 18 dB, 500-Ω feedback resistor		1.1		nV/√Hz
		8-channel mixer, LNA = 18 dB, 62.5-Ω feedback resistor		0.5		
en (RTO)	Output voltage noise (CW)	1-channel mixer, LNA = 18 dB, 500-Ω feedback resistor		8.1		nV/√Hz
		8-channel mixer, LNA = 18 dB, 62.5-Ω feedback resistor		4.0		
NF	Noise figure	Rs = 100 Ω, RIN = High Z, f_{IN} = 2 MHz (LNA, I/Q mixer and summing amplifier and filter)		1.8		dB
f_{CW}	CW Operation Range (2)	CW signal carrier frequency		8		MHz
	CW Clock frequency	1X CLK (16X mode)			8	MHz
		16X CLK(16X mode)			128(3)	
		4X CLK (4X mode)		32		
	AC coupled LVDS clock amplitude	CLKM_16X-CLKP_16X; CLKM_1X-CLKP_1X		0.7		V_{PP}
	AC coupled LVPECL clock amplitude			1.6		
	CLK duty cycle	1X and 16X CLKs	33%		66%	
	Common-mode voltage	Internal provided		2.5		V
V_{CMOS}	CMOS Input clock amplitude		4		5	V
	CW Mixer conversion loss			4		dB
	CW Mixer phase noise	1 kHz off 2-MHz carrier		156		dBc/Hz
DR	Input dynamic range	f_{IN} = 2 MHz, LNA = 24/18/12 dB		160/164/165		dBFS/Hz
IMD3	Intermodulation distortion	f1 = 5 MHz, f2 = 5.01 MHz, both tones at –8.5 dBm amplitude, 8 channels summed up in-phase, CW feedback resistor = 87 Ω		–50		dBc
		f1 = 5 MHz, F2 = 5.01 MHz, both tones at –8.5 dBm amplitude, Single channel case, CW feed back resistor = 500 Ω		–60		dBc
	I/Q Channel gain matching	16X mode		±0.04		dB
	I/Q Channel phase matching	16X mode		±0.1		Degree
	I/Q Channel gain matching	4X mode		±0.04		dB
	I/Q Channel phase matching	4X mode		±0.1		Degree
	Image rejection ratio	f_{IN} = 2.01 MHz, 300-mV input amplitude, CW clock frequency = 2 MHz		–50		dBc

(2) In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance, see application information: *CW clock selection*.
(3) After January, 2014, that is date code after 41XXXXX, the CW clock frequency (16X mode) can be supported up to 145 MHz and approximately 33 to 50% duty cycle based on additional test screening.

Electrical Characteristics (continued)

At AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, no active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, internal 500-Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C (unless otherwise noted). Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CW SUMMING AMPLIFIER						
V_{CMO}	Common-mode voltage	Summing amplifier inputs/outputs		1.5		V
	Summing amplifier output			4		V_{PP}
	Input referred voltage noise	100 Hz		2		nV/√Hz
		1 kHz		1.2		nV/√Hz
		2 kHz to 100 MHz		1		nV/√Hz
	Input referred current noise			2.5		pA/√Hz
	Unit gain bandwidth			200		MHz
	Max output current	Linear operation range		20		mApp
ADC SPECIFICATIONS						
	Sample rate		10		65	MSPS
SNR	Signal-to-noise ratio	Idle channel SNR of ADC 14b		77		dBFS
	Internal reference mode	REFP		1.5		V
		REFM		0.5		V
	External reference mode	VREF_IN voltage		1.4		V
		VREF_IN current		50		µA
	ADC input full-scale range			2		V_{PP}
	LVDS Rate	65 MSPS at 14 bit		910		Mbps
POWER DISSIPATION						
	AVDD Voltage		3.15	3.3	3.6	V
	AVDD_ADC Voltage		1.7	1.8	1.9	V
	AVDD_5V Voltage		4.75	5	5.5	V
	DVDD Voltage		1.7	1.8	1.9	V
	Total power dissipation per channel	TGC low-noise mode, 65 MSPS		158	190	mW/CH
		TGC low-noise mode, 40 MSPS		145		
		TGC medium-power mode, 40 MSPS		114		
		TGC low-power mode, 40 MSPS		101.5		
	AVDD (3.3V) Current	TGC low-noise mode, no signal		202	240	mA
		TGC medium-power mode, no signal		126		
		TGC low-power mode, no signal		99		
		CW-mode, no signal		147	170	
		TGC low-noise mode, 500-mV_{PP} input,1% duty cycle		210		
		TGC medium-power mode, 500-mV_{PP} input, 1% duty cycle		133		
		TGC low-power mode, 500-mV_{PP} input, 1% duty cycle		105		
		CW-mode, 500-mV_{PP} input		375		
	AVDD_5V Current	TGC mode, no signal		25.5	35	mA
		CW mode, no signal, 16X clock = 32 MHz		32		
		TGC mode, 500 mV_{PP} input,1% duty cycle		26		
		CW-mode, 500 mV_{PP} input		42.5		
	VCA Power dissipation	TGC low-noise mode, no signal		99	121	mW/CH
		TGC medium-power mode, no signal		68		
		TGC low-power mode, no signal		55.5		
		TGC low-noise mode, 500 mV_{PP} input,1% duty cycle		102.5		
		TGC medium-power mode, 500 mV_{PP} Input, 1% duty cycle		71		
		TGC low-power mode, 500 mV_{PP} input,1% duty cycle		59.5		
	CW Power dissipation	No signal, ADC shutdown, CW mode, no signal, 16X clock = 32 MHz		80		mW/CH
		500 mV_{PP} input, ADC shutdown , 16X clock = 32 MHz		173		
	AVDD_ADC(1.8V) Current	65 MSPS		187	205	mA
	DVDD(1.8V) Current	65 MSPS		77	110	mA

Electrical Characteristics (continued)

At AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, no active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, V_{OUT} = –1 dBFS, internal 500-Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C (unless otherwise noted). Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
ADC Power dissipation/CH	65 MSPS		59	69	mW/CH
	50 MSPS		51		
	40 MSPS		46		
	20 MSPS		35		
Power dissipation in power down mode	PDN_VCA = high, PDN_ADC = high		25		mW/CH
	Complete power-down, PDN_Global = high		0.6		
Power-down response time	Time taken to enter power down		1		µs
Power-up response time	VCA power down		2µs+1% of PDN time		µs
	ADC power down		1		
	Complete power down		2.5		ms
Power supply modulation ratio, AVDD and AVDD_5V	f_{IN} = 5 MHz, at 50-mV_{PP} noise at 1 kHz on supply(4)		–65		dBc
	f_{IN} = 5 MHz, at 50-mV_{PP} noise at 50 kHz on supply(4)		–65		dBc
Power supply rejection ratio	f = 10 kHz,VCNTL = 0 V (high gain), AVDD		–40		dBc
	f = 10 kHz,VCNTL = 0 V (high gain), AVDD_5V		–55		dBc
	f = 10 kHz,VCNTL = 1 V (low gain), AVDD		–50		dBc

(4) PSMR specification is with respect to input signal amplitude.

7.6 Digital Characteristics

Typical values are at +25°C, AVDD = 3.3 V, AVDD_5 = 5 V and AVDD_ADC = 1.8 V, DVDD = 1.8 V, 14 bit sample rate = 65 MSPS (unless otherwise noted). Minimum and maximum values are across the full temperature range: T_{MIN} = 0°C to T_{MAX} = 85°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
DIGITAL INPUTS AND OUTPUTS						
V_{IH}	Logic high input voltage		2		3.3	V
V_{IL}	Logic low input voltage		0		0.3	V
	Logic high input current			200		µA
	Logic low input current			200		µA
	Input capacitance			5		pF
V_{OH}	Logic high output voltage	SDOUT pin		DVDD		V
V_{OL}	Logic low output voltage	SDOUT pin		0		V
LVDS OUTPUTS						
	Output differential voltage	With 100-Ω external differential termination		400		mV
	Output offset voltage	Common-mode voltage		1100		mV
	FCLKP and FCLKM	1X clock rate	10		65	MHz
	DCLKP and DCLKM	7X clock rate	70		455	MHz
		6X clock rate	60		390	MHz
t_{su}	Data setup time(2)			350		ps
t_h	Data hold time(2)			350		ps
ADC INPUT CLOCK						
	CLOCK frequency		10		65	MSPS
	Clock duty cycle		45%	50%	55%	
	Clock input amplitude, differential(V_{CLKP_ADC}–V_{CLKM_ADC})	Sine-wave, ac-coupled	0.5			V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
	Common-mode voltage	biased internally		1		V
	Clock input amplitude V_{CLKP_ADC} (single-ended)	CMOS clock		1.8		V_{PP}

(1) The DC specifications refer to the condition where the LVDS outputs are not switching, but are permanently at a valid logic level 0 or 1 with 100-Ω external termination.
(2) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margins

7.7 Switching Characteristics

Typical values are at 25°C, AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, differential clock, C_{LOAD} = 5 pF, R_{LOAD} = 100 Ω, 14 bit, sample rate = 65MSPS (unless otherwise noted). Minimum and maximum values are across the full temperature range T_{MIN} = 0°C to T_{MAX} = 85°C with AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ta	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs	0.7	3		ns
	Aperture delay matching	Across channels within the same device		±150		ps
t_j	Aperture jitter			450		Fs rms
	ADC latency	Default, after reset, or 0 x 2 [12] = 1, LOW_LATENCY = 1		11/8		Input clock cycles
t_{delay}	Data and frame clock delay	Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus 3/7 of the input clock period (T).	3	5.4	7	ns
Δt_{delay}	Delay variation	At fixed supply and 20°C T difference. Device to device	–1		1	ns
t_{RISE}	Data rise time	Rise time measured from –100 to 100 mV, fall time measured from 100 mV to –100 mV, 10 MHz < f_{CLKIN} < 65 MHz		0.14		ns
t_{FALL}	Data fall time			0.15		
$t_{FCLKRISE}$	Frame clock rise time	Rise time measured from –100 mV to 100 mV, fall time measured from 100 mV to –100 mV, 10 MHz < f_{CLKIN} < 65 MHz		0.14		ns
$t_{FCLKFALL}$	Frame clock fall time			0.15		
	Frame clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge	48%	50%	52%	
$t_{DCLKRISE}$	Bit clock rise time	Rise time measured from –100 to 100 mV, fall time measured from 100 mV to –100 mV, 10 MHz < f_{CLKIN} < 65 MHz		0.13		ns
$t_{DCLKFALL}$	Bit clock fall time			0.12		
	Bit clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge 10 MHz < f_{CLKIN} < 65 MHz	46%		54%	

(1) Timing parameters are ensured by design and characterization; not production tested.

7.8 Timing Requirements

Minimum values across full temperature range T_{MIN} = 0°C to T_{MAX} = 85°C, AVDD_5V =5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	$\overline{SEN}$ fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to $\overline{SEN}$ rising edge	8			ns
t_8	SDOUT delay	12	20	28	ns

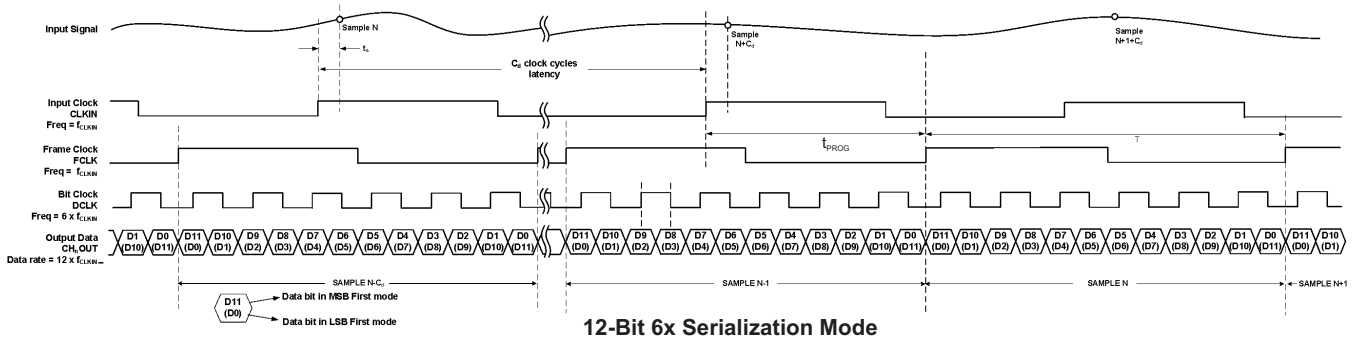
7.9 Output Interface Timing(1)(2)(3)

f_{CLKIN}, INPUT CLOCK FREQUENCY	SETUP TIME (t_{su}), ns			HOLD TIME (t_h), ns			t_{PROG} = (3/7)x T + t_{delay}, ns		
	DATA VALID TO BIT CLOCK ZERO-CROSSING			BIT CLOCK ZERO-CROSSING TO DATA INVALID			INPUT CLOCK ZERO-CROSS (rising edge) TO FRAME CLOCK ZERO-CROSS (rising edge)		
MHz	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65/14bit	0.24	0.37		0.24	0.38		11	12	12.5
50/14bit	0.41	0.54		0.46	0.57		13	13.9	14.4
40/14bit	0.55	0.70		0.61	0.73		15	16	16.7
30/14bit	0.87	1.10		0.94	1.1		18.5	19.5	20.1
20/14bit	1.30	1.56		1.46	1.6		25.7	26.7	27.3

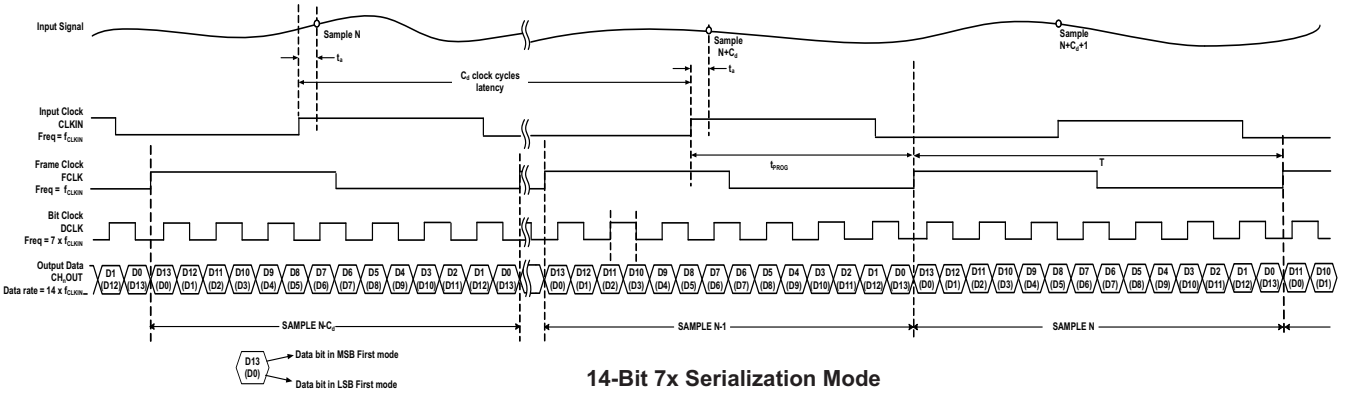
(1) FCLK timing is the same as for the output data lines. It has the same relation to DCLK as the data pins. Setup and hold are the same for the data and the frame clock.
(2) Data valid is logic HIGH = +100 mV and logic LOW = –100 mV
(3) Timing parameters are ensured by design and characterization; not production tested.

NOTE

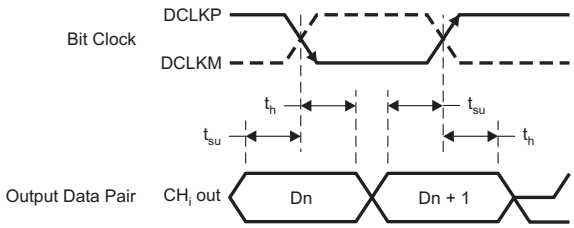
The previous timing data can be applied to 12-bit or 16-bit LVDS rates as well. For example, the maximum LVDS output rate at 65 MHz and 14-bit is equal to 910 MSPS, which is approximately equivalent to the rate at 56 MHz and 16-bit.



12-Bit 6x Serialization Mode



14-Bit 7x Serialization Mode



T0434-01

LVDS Setup and Hold Timing

Figure 1. LVDS Timing Diagrams

7.10 Typical Characteristics

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)

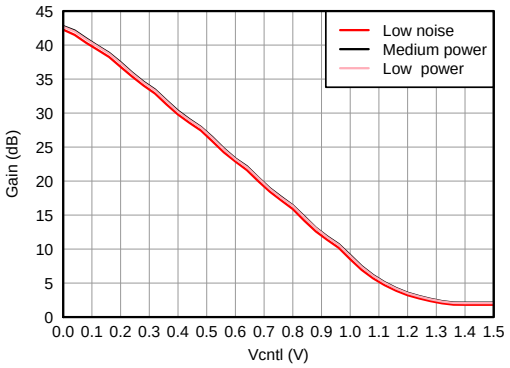


Figure 2. Gain vs VCNTL

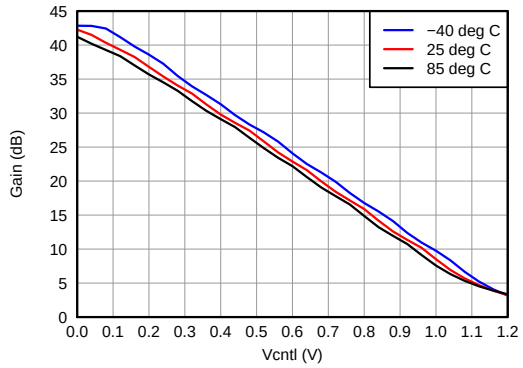
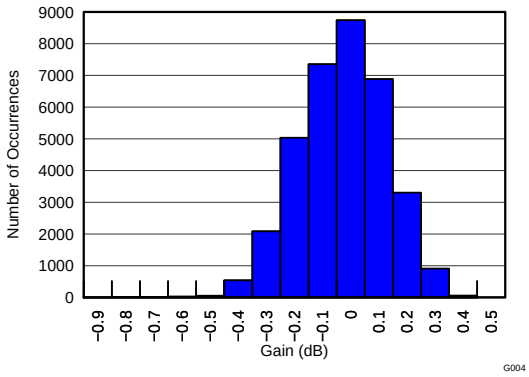
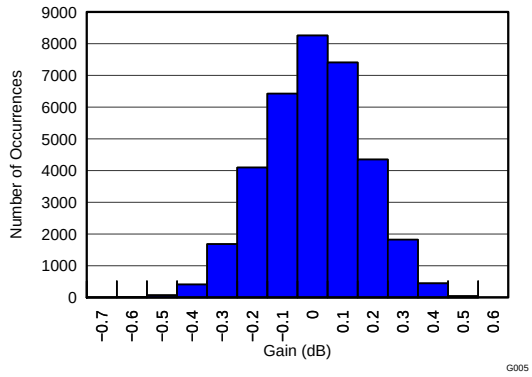


Figure 3. Gain Variation vs Temperature



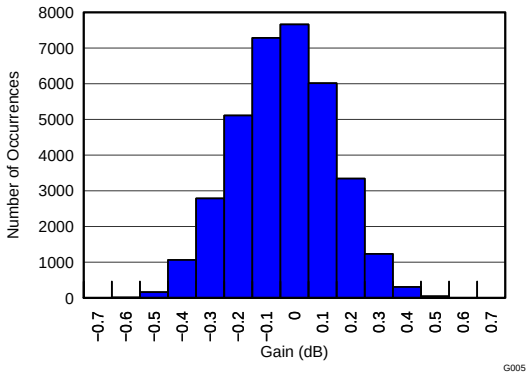
VCNTL = 0.3 V (34951 channels)

Figure 4. Gain Matching Histogram



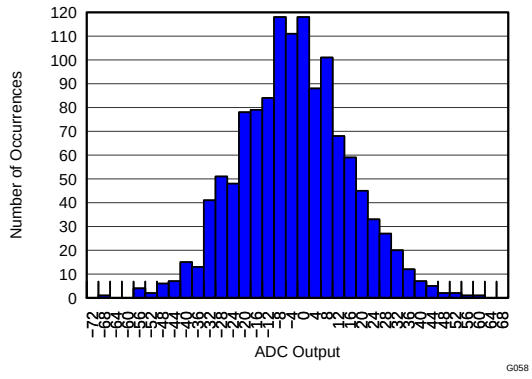
VCNTL = 0.6 V (34951 channels)

Figure 5. Gain Matching Histogram



VCNTL = 0.9 V (34951 channels)

Figure 6. Gain Matching Histogram



VCNTL = 0 V (1247 channels)

Figure 7. Output Offset Histogram

Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)

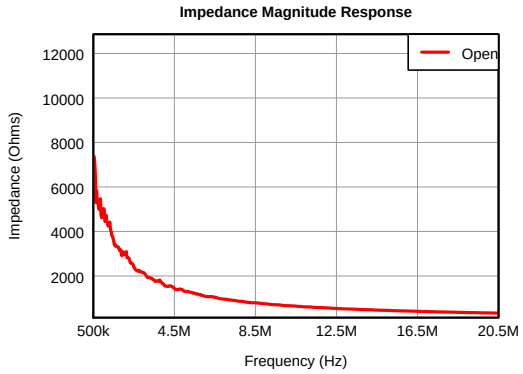


Figure 8. Input Impedance Without Active Termination (Magnitude)

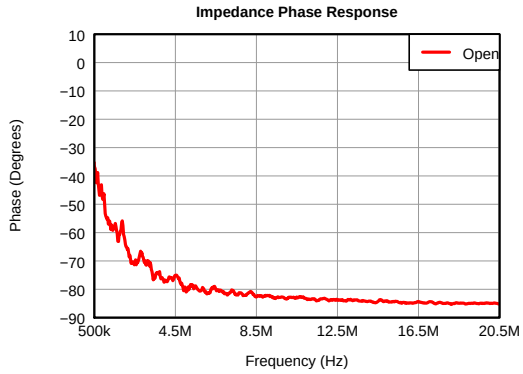


Figure 9. Input Impedance Without Active Termination (Phase)

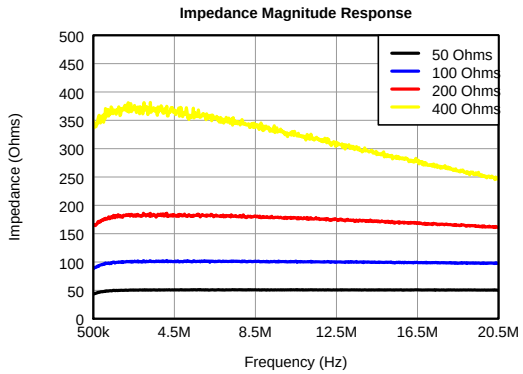


Figure 10. Input Impedance With Active Termination (Magnitude)

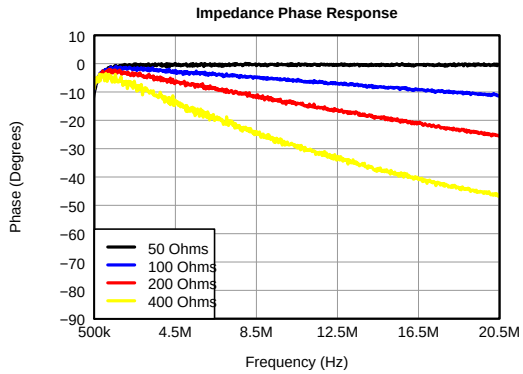


Figure 11. Input Impedance With Active Termination (Phase)

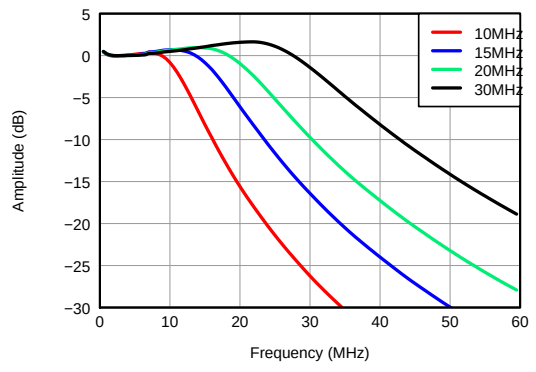


Figure 12. Low-Pass Filter Response

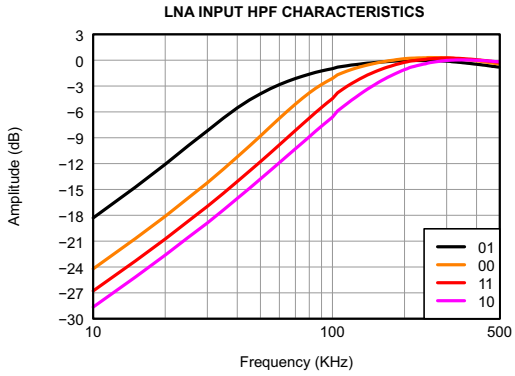


Figure 13. LNA High-Pass Filter Response vs Reg59 [3:2]

Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)

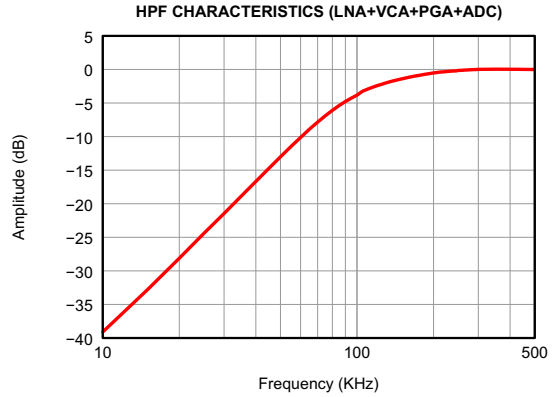
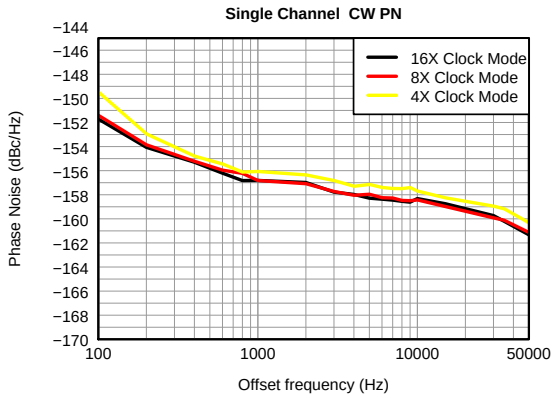
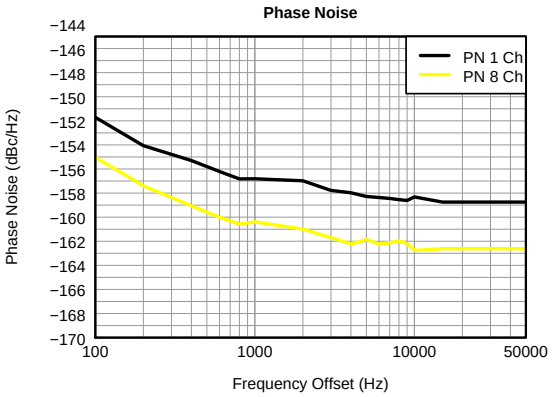


Figure 14. Full Channel High-Pass Filter Response at Default Register Setting



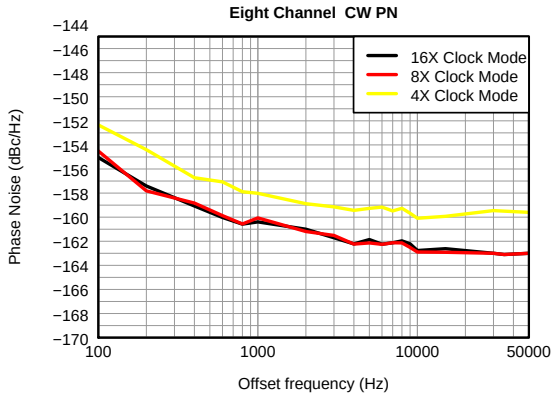
f_{IN} = 2 MHz

Figure 15. CW Phase Noise



f_{IN} = 2 MHz

Figure 16. CW Phase Noise, 1 Channel vs 8 Channel



f_{IN} = 2 MHz

Figure 17. CW Phase Noise vs Clock Modes

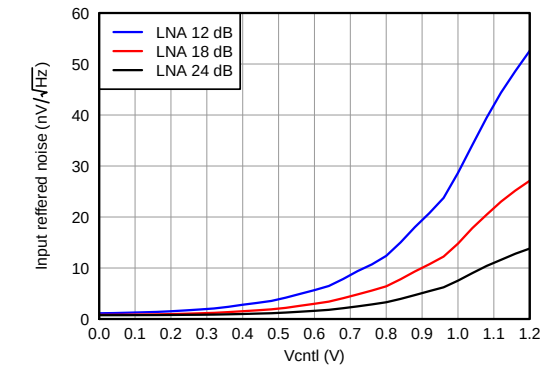


Figure 18. Input Referred Noise (IRN) and Low-Noise Mode

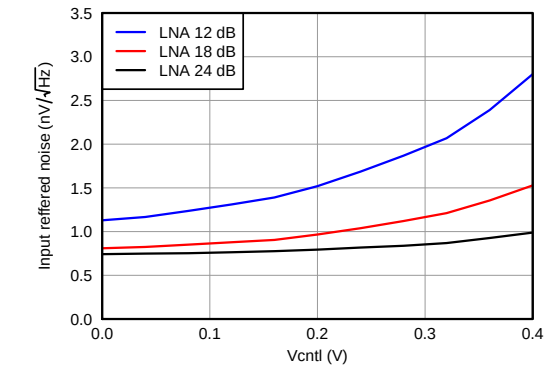


Figure 19. IRN and Low-Noise Mode Enlarged Version

Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)

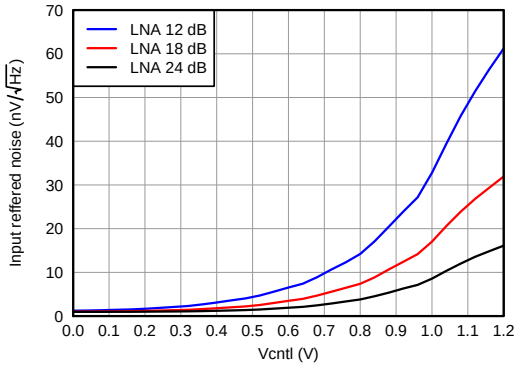


Figure 20. IRN and Medium-Power Mode

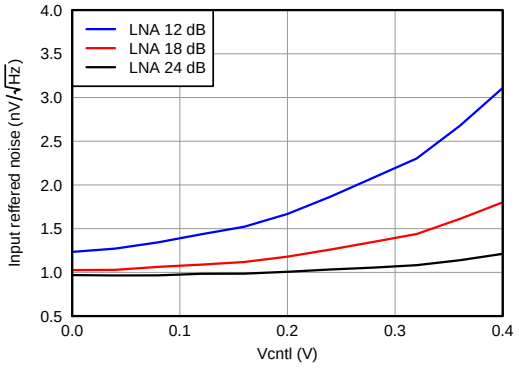


Figure 21. IRN and Medium-Power Mode Enlarged Version

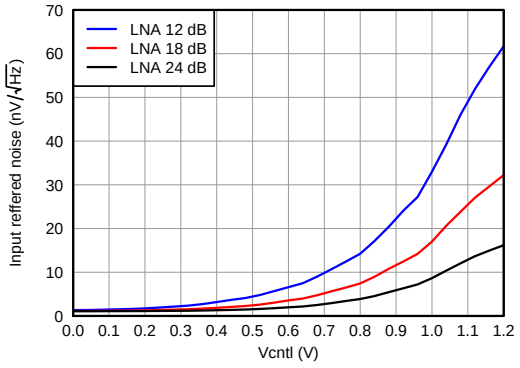


Figure 22. IRN and Low-Power Mode

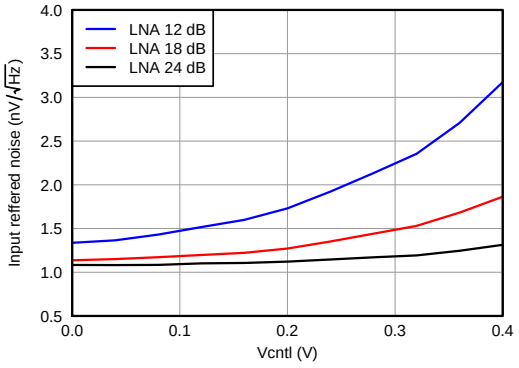


Figure 23. IRN and Low-Power Mode Enlarged Version

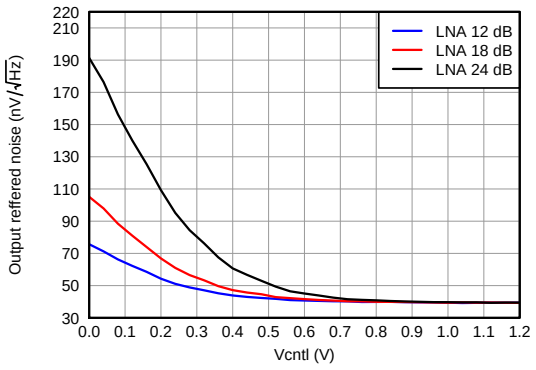


Figure 24. Output Referred Noise (ORN) and Low-Noise Mode

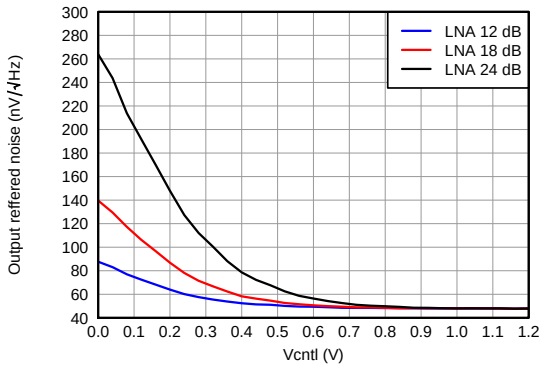


Figure 25. ORN and Medium-Power Mode

Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)

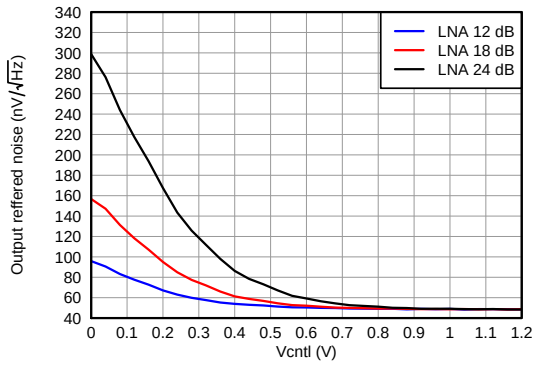


Figure 26. ORN and Low-Power Mode

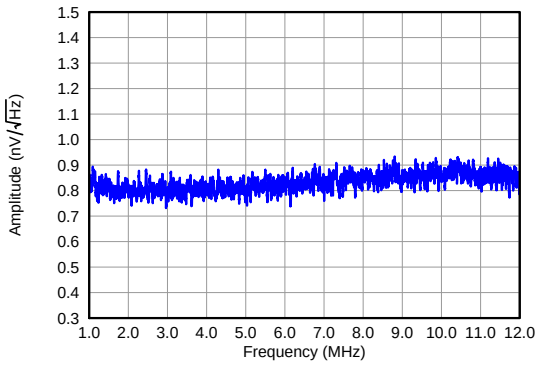


Figure 27. IRN and Low-Noise Mode

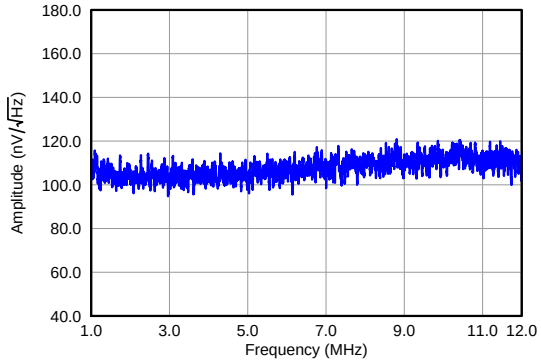


Figure 28. ORN, PGA = 24 dB and Low Noise Mode

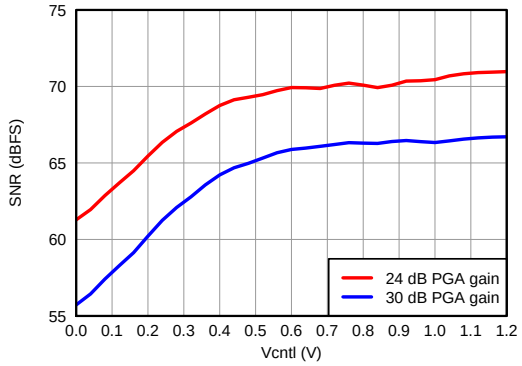


Figure 29. SNR, LNA = 18 dB and Low Noise Mode

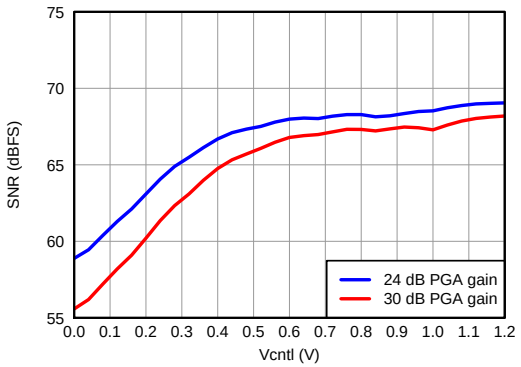


Figure 30. SNR, LNA = 18 dB and Low Power Mode

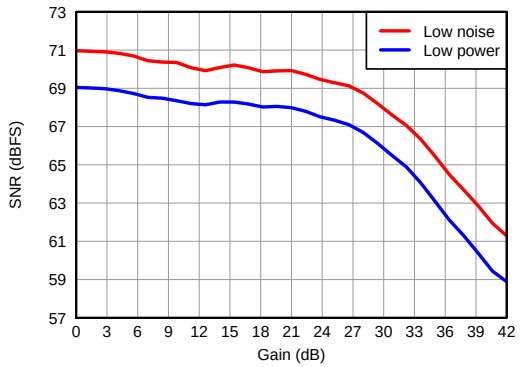


Figure 31. SNR vs Different Power Modes

Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)

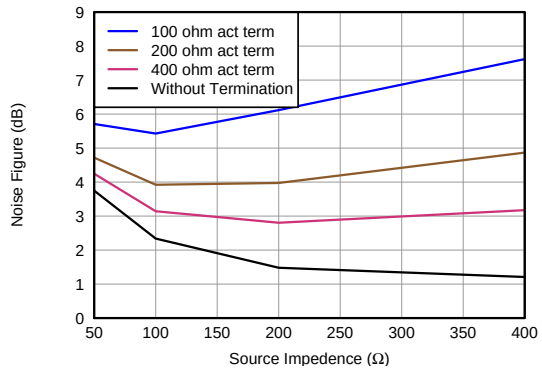


Figure 32. Noise Figure, LNA = 12 dB and Low Noise Mode

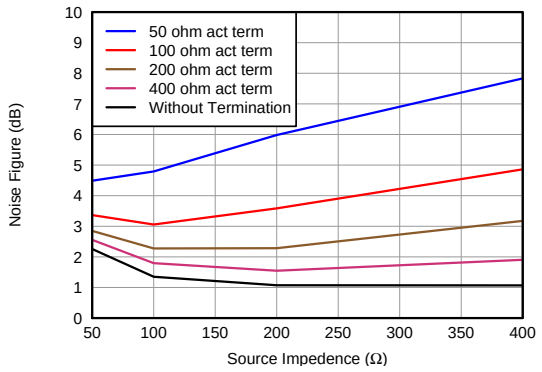


Figure 33. Noise Figure, LNA = 18 dB and Low Noise Mode

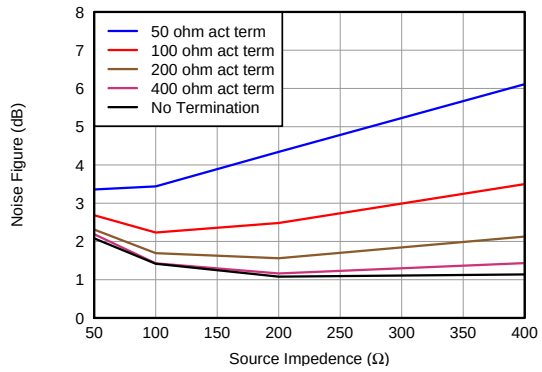


Figure 34. Noise Figure, LNA = 24 dB and Low Noise Mode

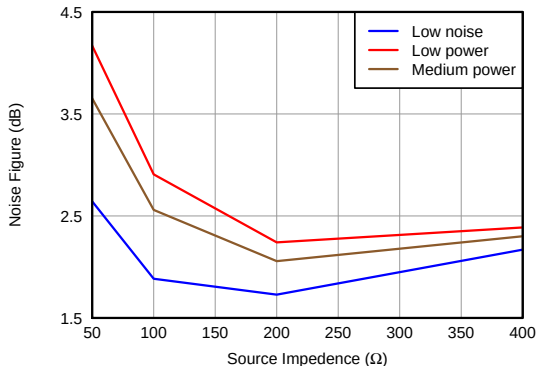


Figure 35. Noise Figure vs Power Modes With 400-Ω Termination

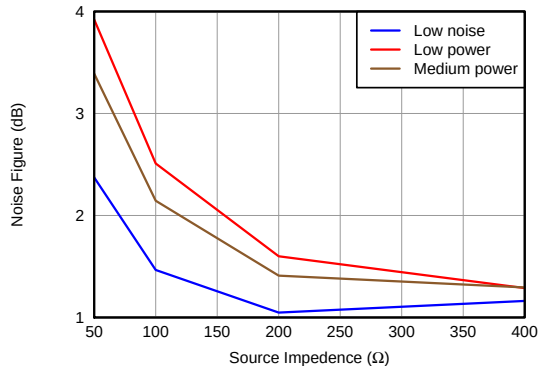
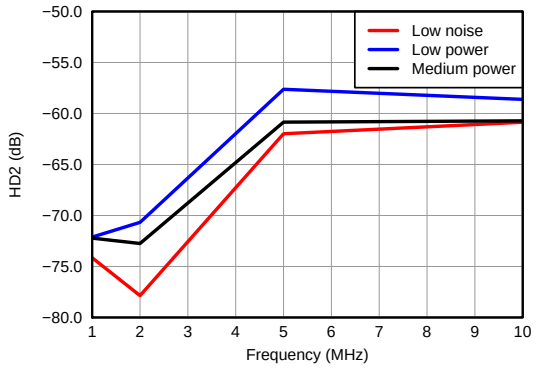


Figure 36. Noise Figure vs Power Modes Without Termination

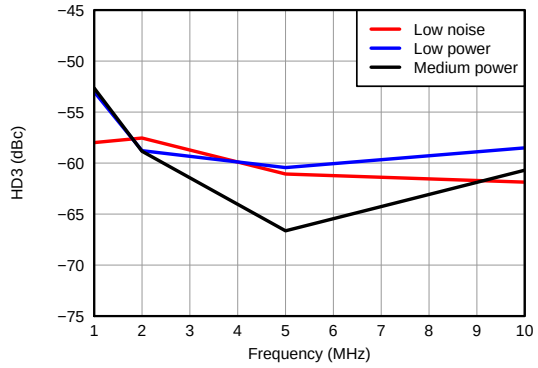


Vin = 500 mV_{PP} and V_{OUT} = –1 dBFS

Figure 37. HD2 vs Frequency

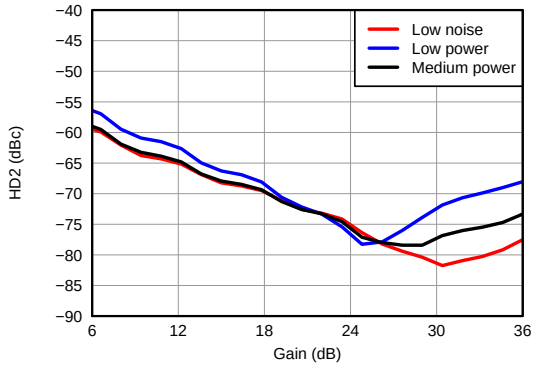
Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OUT}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)



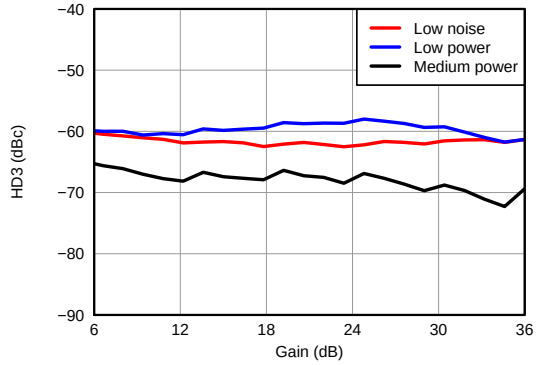
Vin = 500 mV_{PP} and V_{OUT} = –1 dBFS

Figure 38. HD3 vs Frequency



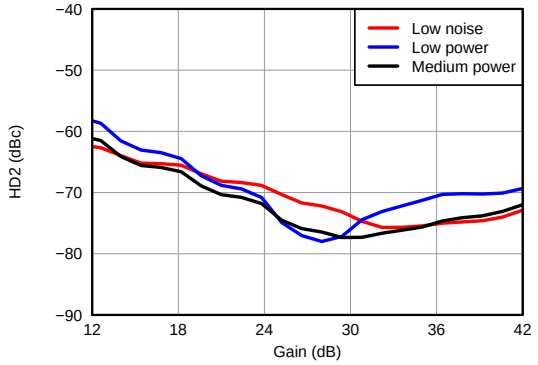
LNA = 12 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

Figure 39. HD2 vs Gain



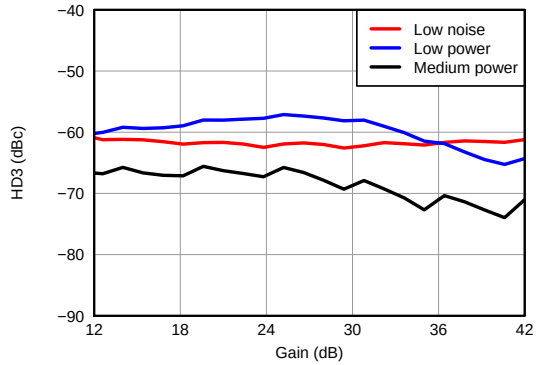
LNA = 12 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

Figure 40. HD3 vs Gain



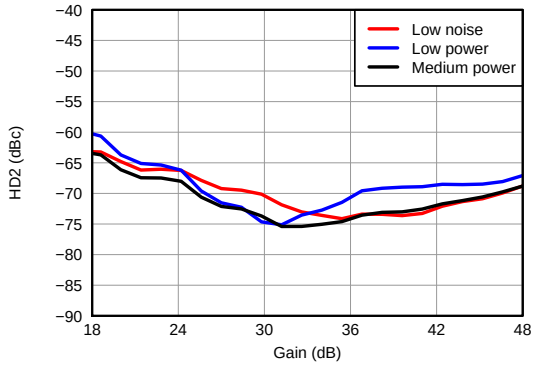
LNA = 18 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

Figure 41. HD2 vs Gain



LNA = 18 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

Figure 42. HD3 vs Gain

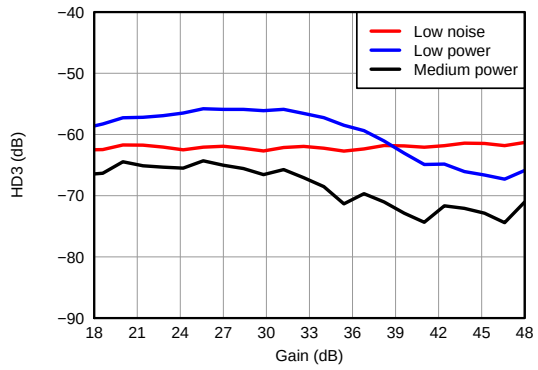


LNA = 24 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

Figure 43. HD2 vs Gain

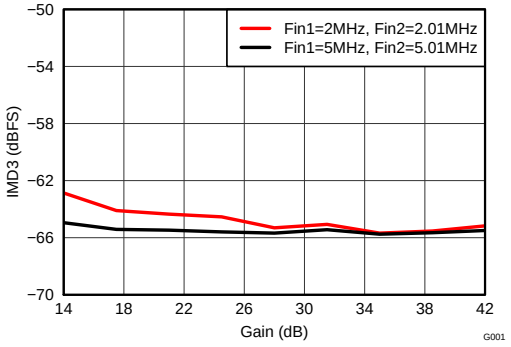
Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)



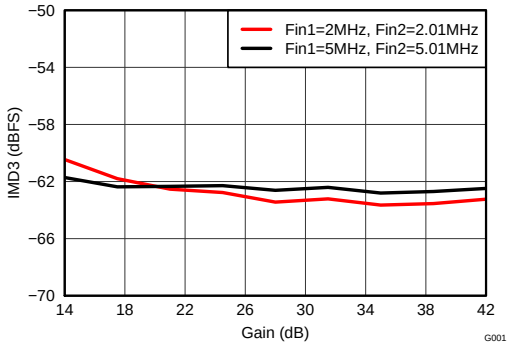
LNA = 24 dB and PGA = 24 dB and V_{OUT} = –1 dBFS

Figure 44. HD3 vs Gain



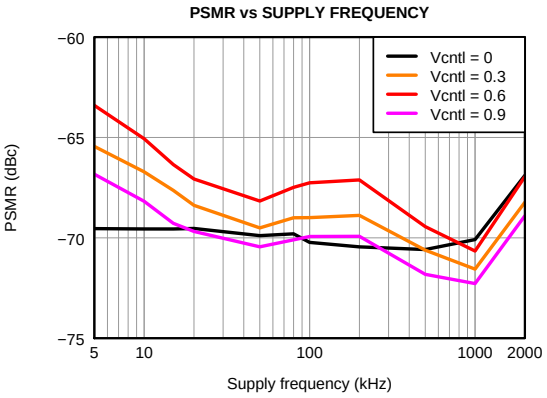
Fout1 = –1 dBFS and Fout2 = –21 dBFS

Figure 45. IMD3



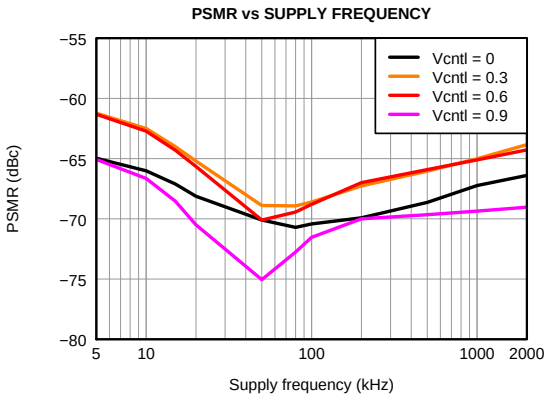
Fout1 = –7dBFS and Fout2 = –7dBFS

Figure 46. IMD3



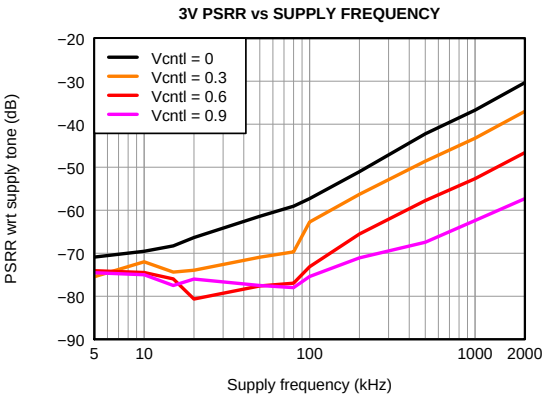
100 mV_{PP} Supply Noise With Different Frequencies

Figure 47. AVDD Power Supply Modulation Ratio



100 mV_{PP} Supply Noise With Different Frequencies

Figure 48. AVDD_5V Power Supply Modulation Ratio

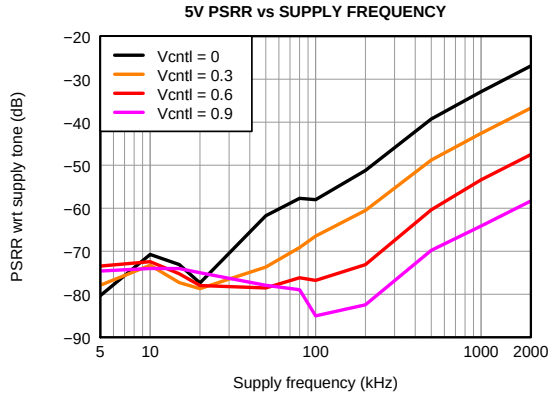


100 mV_{PP} Supply Noise With Different Frequencies

Figure 49. AVDD Power Supply Rejection Ratio

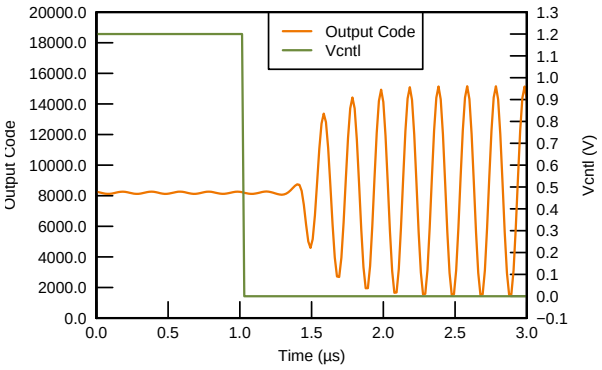
Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)



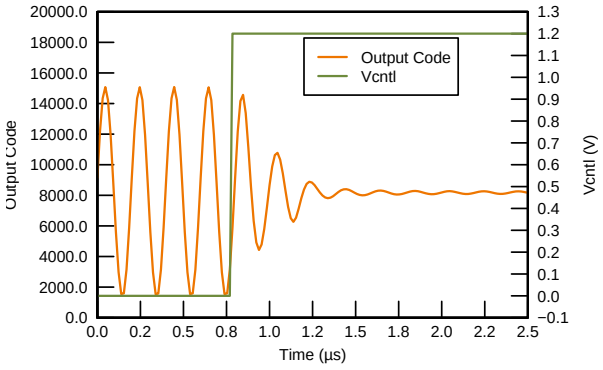
100 mV_{PP} Supply Noise With Different Frequencies

Figure 50. AVDD_5 V Power Supply Rejection Ratio



LNA = 18 dB and PGA = 24 dB

Figure 51. VCNTL Response Time



LNA = 18 dB and PGA = 24 dB

Figure 52. VCNTL Response Time

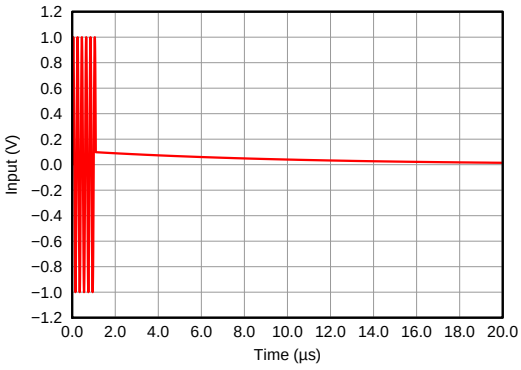


Figure 53. Pulse Inversion Asymmetrical Positive Input

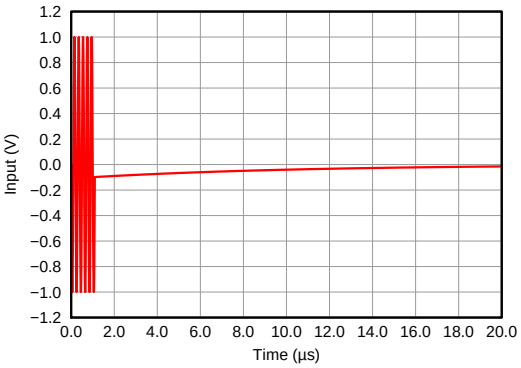
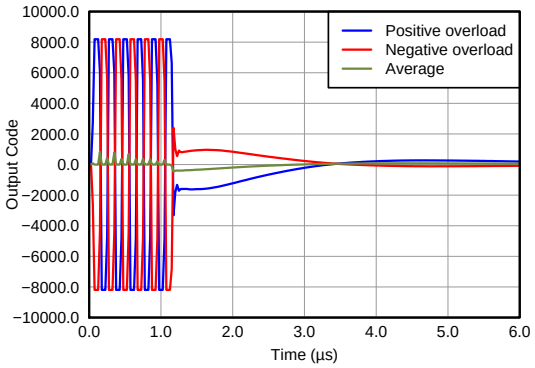


Figure 54. Pulse Inversion Asymmetrical Negative Input

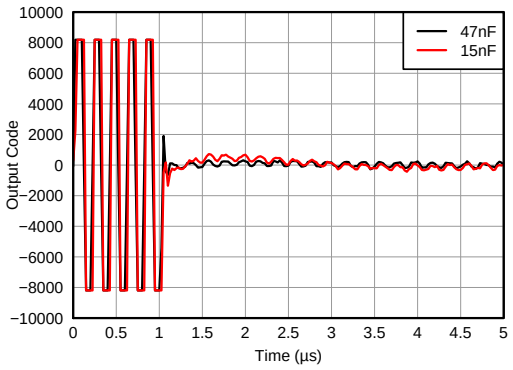


V_{IN} = 2 V_{PP}, PRF = 1 kHz, Gain = 21 dB

Figure 55. Pulse Inversion

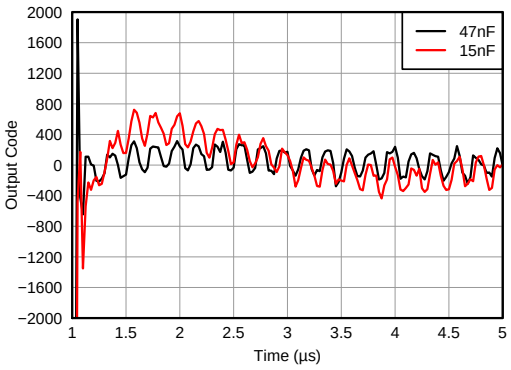
Typical Characteristics (continued)

at AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1-µF caps at INP and 15-nF caps at INM, No active termination, VCNTL = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 bit, sample rate = 65 MSPS, LPF filter = 15 MHz, low-noise mode, $V_{OU}T$ = –1 dBFS, 500-Ω CW feedback resistor, CMOS 16X clock, ADC configured in internal-reference mode, single-ended VCNTL mode, VCNTLM = GND, and ambient temperature T_A = 25°C (unless otherwise noted)



V_{IN} = 50 mV_{PP}/100 $µV_{PP}$, Max Gain

Figure 56. Overload Recovery Response vs INM Capacitor



V_{IN} = 50 mV_{PP}/100 $µV_{PP}$, Max Gain

Figure 57. Overload Recovery Response vs INM Capacitor (Zoomed)

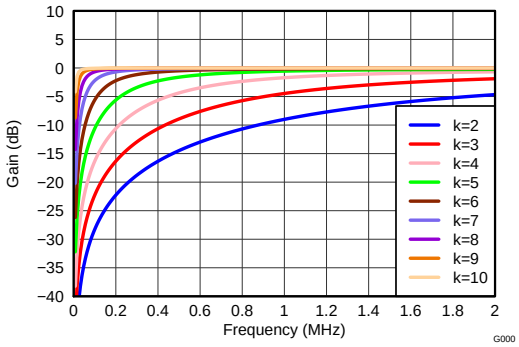


Figure 58. Digital High-Pass Filter Response

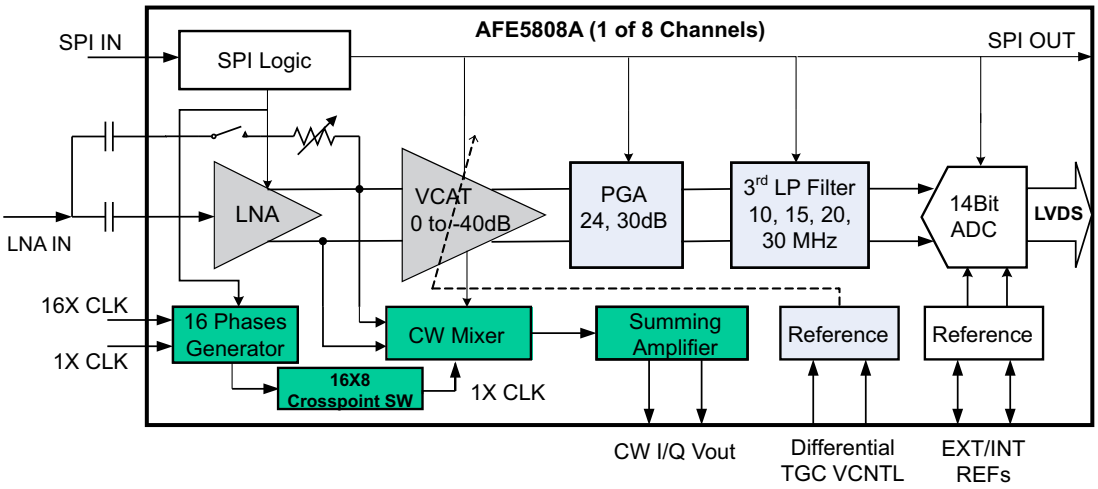
8 Detailed Description

8.1 Overview

The AFE5808A device is a highly integrated analog front-end (AFE) solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5808A device integrates a complete time-gain-control (TGC) imaging path and a continuous wave doppler (CWD) path. This device also enables users to select one of various power/noise combinations to optimize system performance. The AFE5808A device contains eight channels; each channel includes a low-noise amplifier (LNA), voltage controlled attenuator (VCAT), programmable gain amplifier (PGA), low-pass filter (LPF), 14-bit analog-to-digital converter (ADC), and CW mixer.

In addition, multiple features in the AFE5808A device are suitable for ultrasound applications, such as active termination, individual channel control, fast power-up and power-down response, programmable clamp voltage control, fast and consistent overload recovery, and so forth. Therefore the AFE5808A device brings premium image quality to ultra–portable, handheld systems all the way up to high-end ultrasound systems. See *Functional Block Diagram*.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low-Noise Amplifier (LNA)

In many high-gain systems, a low noise amplifier is critical for achieving overall performance. Using a new proprietary architecture, the LNA in the AFE5808A device delivers exceptional low-noise performance, while operating on a low quiescent current compared to CMOS-based architectures with similar noise performance. The LNA performs single-ended input to differential output voltage conversion. The LNA is configurable for a programmable gain of 24 dB, 18 dB, and 12 dB, and its input-referred noise is only 0.63 nV/$\sqrt{Hz}$ 0.70 nV/$\sqrt{Hz}$, and 0.9 nV/$\sqrt{Hz}$ respectively. Programmable gain settings result in a flexible linear input range up to 1 V_{PP}, realizing high signal handling capability demanded by new transducer technologies. Larger input signal can be accepted by the LNA; however the signal can be distorted since it exceeds the LNA's linear operation region. Combining the low noise and high input range, a wide input dynamic range is achieved consequently for supporting the high demands from various ultrasound imaging modes.

The LNA input is internally biased at approximately 2.4 V; the signal source should be AC-coupled to the LNA input by an adequately-sized capacitor, for example, ≥ 0.1 µF. To achieve low DC offset drift, the AFE5808A device incorporates a DC offset correction circuit for each amplifier stage. To improve the overload recovery, an integrator circuit is used to extract the DC component of the LNA output and then fed back to the LNA's complementary input for DC offset correction. This DC offset correction circuit has a high-pass response and can be treated as a high-pass filter. The effective corner frequency is determined by the capacitor C_{BYPASS} connected

Feature Description (continued)

at INM. With larger capacitors, the corner frequency is lower. For stable operation at the highest HP filer cut-off frequency, a ≥ 15-nF capacitor can be selected. This corner frequency scales almost linearly with the value of the C_{BYPASS}. For example, 15 nF gives a corner frequency of approximately 100 kHz, while 47 nF can give an effective corner frequency of 33 kHz. The DC offset correction circuit can also be disabled or enabled through register 52[12].

The AFE5808A device can be terminated passively or actively. Active termination is preferred in ultrasound application for reducing reflection from mismatches and achieving better axial resolution without degrading the noise figure too much. Active termination values can be preset to 50 Ω, 100 Ω, 200 Ω, and 400 Ω; other values also can be programmed by users through register 52[4:0]. A feedback capacitor is required between ACTx and the signal source as Figure 59 shows. On the active termination path, a clamping circuit is also used to create a low impedance path when overload signal is seen by the AFE5808A device. The clamp circuit limits large input signals at the LNA inputs, and it improves the overload recovery performance of the AFE5808A device. The clamp level can be set to 350 mV_{PP}, 600 mV_{PP}, and 1.15 V_{PP} automatically depending on the LNA gain settings when register 52[10:9] = 0. Other clamp voltages, such as 1.15 V_{PP}, 0.6 V_{PP}, and 1.5 V_{PP}, are also achievable by setting register 52[10:9]. This clamping circuit is also designed to obtain good pulse inversion performance and reduce the impact from asymmetric inputs.

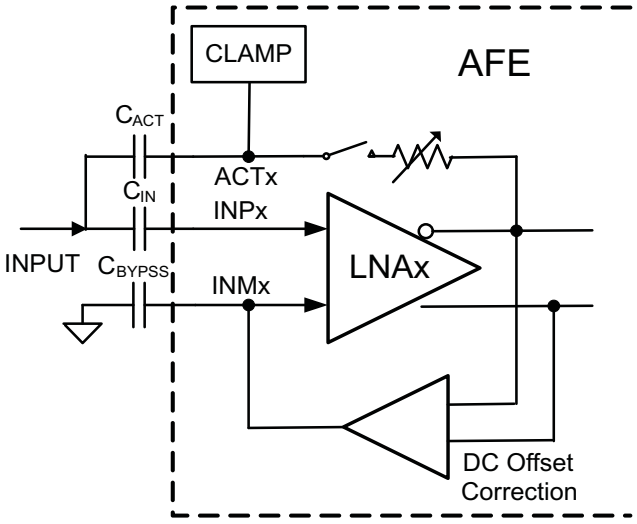


Figure 59. AFE5808A LNA With DC Offset Correction Circuit

8.3.2 Voltage-Controlled Attenuator

The voltage-controlled attenuator is designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB (see Figure 2) is constant for each equal increment of the control voltage (VCNTL) as shown in Figure 60. A differential control structure is used to reduce common mode noise. A simplified attenuator structure is shown in the following Figure 60 and Figure 61.

The attenuator is essentially a variable voltage divider that consists of the series input resistor (RS) and seven shunt FETs placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A7). VCNTL is the effective difference between VCNTLP and VCNTLM. Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V7 are equally spaced over the 0-V to 1.5-V control voltage range. As the control voltage increases through the input range of each clipping amplifier, the amplifier output rises from a voltage where the FET is nearly OFF to VHIGH where the FET is completely ON. As each FET approaches its ON state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned OFF, producing minimum signal attenuation. Similarly, high control voltages turn the FETs ON, leading to maximum signal attenuation. Therefore, each FET acts to decrease the shunt resistance of the voltage divider formed by Rs and the parallel FET network.

Feature Description (continued)

Additionally, a digitally controlled TGC mode is implemented to achieve better phase-noise performance in the AFE5808A device. The attenuator can be controlled digitally instead of the analog control voltage V_{CNTL}. This mode can be set by the register bit 59[7]. The variable voltage divider is implemented as a fixed series resistance and FET as the shunt resistance. Each FET can be turned ON by connecting the switches SW1-7. Turning on each of the switches can give approximately 6 dB of attenuation, which can be controlled by the register bits 59[6:4]. This digital control feature can eliminate the noise from the VCNTL circuit and ensures the better SNR and phase noise for TGC path.

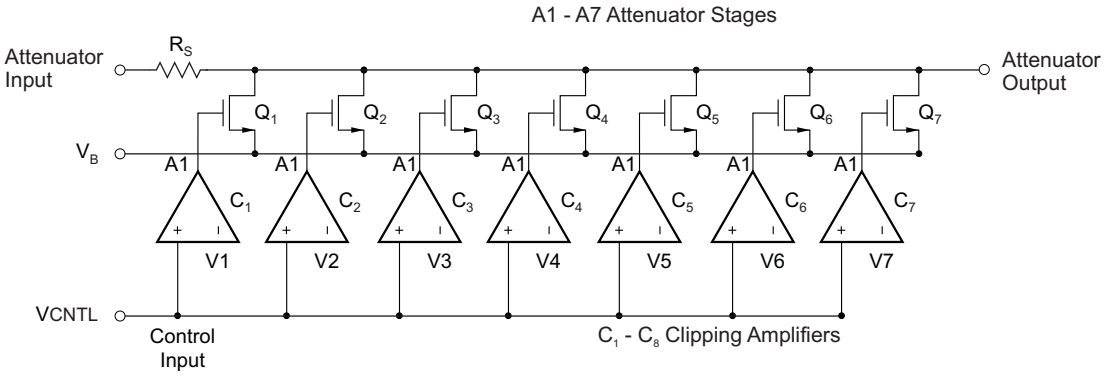


Figure 60. Simplified Voltage Controlled Attenuator (Analog Structure)

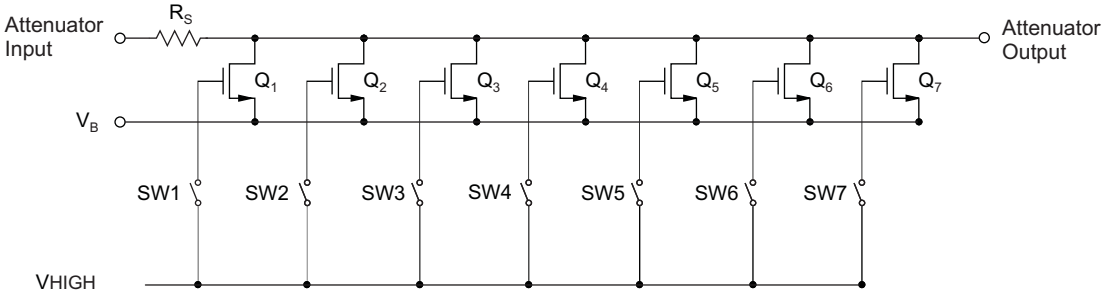


Figure 61. Simplified Voltage Controlled Attenuator (Digital Structure)

The voltage controlled attenuator noise follows a monotonic relationship to the attenuation coefficient. At higher attenuation, the input-referred noise is higher and conversely. The attenuator noise is then amplified by the PGA and becomes the noise floor at the ADC input. In the attenuator's high attenuation operating range, that is VCNTL is high, the attenuator input noise may exceed the LNA's output noise; the attenuator then becomes the dominant noise source for the following PGA stage and ADC. Therefore the attenuator's noise should be minimized compared to the LNA output noise. The AFE5808A's attenuator is designed for achieving low noise even at high attenuation (low channel gain) and realizing better SNR in the near field. Table 1 shows the input referred noise for different attenuations.

Table 1. Voltage-Controlled-Attenuator Noise vs Attenuation

ATTENUATION (dB)	ATTENUATOR INPUT REFERRED NOISE (nV/√Hz)
–40	10.5
–36	10
–30	9
–24	8.5
–18	6
–12	4
–6	3

Table 1. Voltage-Controlled-Attenuator Noise vs Attenuation (continued)

ATTENUATION (dB)	ATTENUATOR INPUT REFERRED NOISE (nV/√Hz)
0	2

8.3.3 Programmable Gain Amplifier

After the voltage controlled attenuator, a programmable gain amplifier (PGA) can be configured as 24 dB or 30 dB with a constant input referred noise of 1.75 nV/√Hz. The PGA structure consists of a differential voltage-to-current converter with programmable gain, current clamp (bias control) circuits, a transimpedance amplifier with a programmable low-pass filter, and a DC offset correction circuit. See Figure 62 for the simplified block diagram of the PGA.

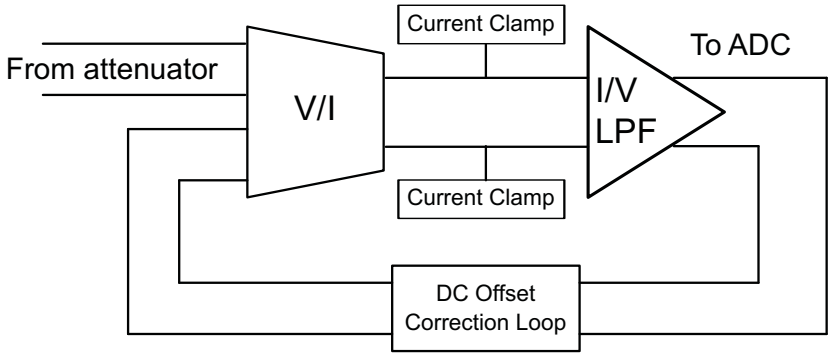


Figure 62. Simplified Block Diagram of PGA

Low input noise is always preferred in a PGA because its noise contribution should not degrade the ADC SNR too much after the attenuator. At the minimum attenuation (used for small input signals), the LNA noise dominates; at the maximum attenuation (large input signals), the PGA and ADC noise dominates. Thus 24-dB gain of PGA achieves better SNR as long as the amplified signals can exceed the noise floor of the ADC.

The PGA current clamp circuit can be enabled (register 51) to improve the overload recovery performance of the AFE. If we measure the standard deviation of the output just after overload, for 0.5 V V_{CNTL}, it is about 3.2 LSBs in normal case (that is, the output is stable in about 1 clock cycle after overload). With the current clamp circuit disabled, the value approaches 4 LSBs, meaning a longer time duration before the output stabilizes; however, with the current clamp circuit enabled, there will be degradation in HD3 for PGA output levels > –2dBFS. For example, for a –2-dBFS output level, the HD3 degrades by approximately 3 dB. To maximize the output dynamic range, the maximum PGA output level can be above 2 V_{PP} even with the clamp circuit enabled; the ADC in the AFE has excellent overload recovery performance to detect small signals right after the overload.

NOTE

In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7] = 0.

The AFE5808A device integrates an anti-aliasing filter in the form of a programmable low-pass filter (LPF) in the transimpedance amplifier. The LPF is designed as a differential, active, 3rd order filter with a typical 18 dB-per-octave roll-off. Programmable through the serial interface, the –1-dB frequency corner can be set to one of 10 MHz, 15 MHz, 20 MHz, and 30 MHz. The filter bandwidth is set for all channels simultaneously.

A selectable DC offset correction circuit is implemented in the PGA as well. This correction circuit is similar to the one used in the LNA. The circuit extracts the DC component of the PGA outputs and feeds back to the PGA's complimentary inputs for DC offset correction. This DC offset correction circuit also has a high-pass response with a cut-off frequency of 80 KHz.

8.3.4 Analog-to-Digital Converter

The analog-to-digital converter (ADC) of the AFE5808A device employs a pipelined converter architecture that consists of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 14-bit level. The 14 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the AFE5808A device operate from a common input clock (CLKP/M). The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 14x clock required for the serializer is generated internally from the CLKP/M pins. A 7x and a 1x clock are also given out in LVDS format, along with the data, to enable easy data capture. The AFE5808A device operates from internally-generated reference voltages that are trimmed to improve the gain matching across devices. The nominal values of REFP and REFM are 1.5 V and 0.5 V, respectively. Alternately, the device also supports an external reference mode that can be enabled using the serial interface.

Using serialized LVDS transmission has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the AFE5808A device.

8.3.5 Continuous-Wave (CW) Beamformer

Continuous-wave Doppler is a key function in mid-end to high-end ultrasound systems. Compared to the TGC mode, the CW path needs to handle high dynamic range along with strict phase noise performance. CW beamforming is often implemented in analog domain due to the mentioned strict requirements. Multiple beamforming methods are being implemented in ultrasound systems, including passive delay line, active mixer, and passive mixer. Among all of them, the passive mixer approach achieves optimized power and noise. The passive mixer satisfies the CW processing requirements, such as wide dynamic range, low phase noise, accurate gain and phase matching.

A simplified CW path block diagram and an in-phase or quadrature (I/Q) channel block diagram are illustrated in Figure 63 and Figure 64 respectively. Each CW channel includes a LNA, a voltage-to-current converter, a switch-based mixer, a shared summing amplifier with a low-pass filter, and clocking circuits. All blocks include well-matched in-phase and quadrature channels to achieve good image frequency rejection as well as beamforming accuracy. As a result, the image rejection ratio from an I/Q channel is better than -46 dBc, which is desired in ultrasound systems.

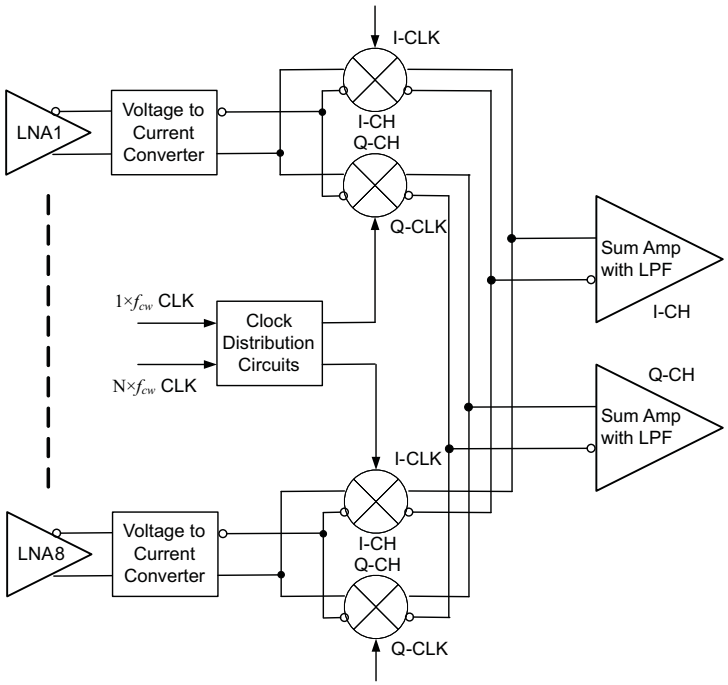
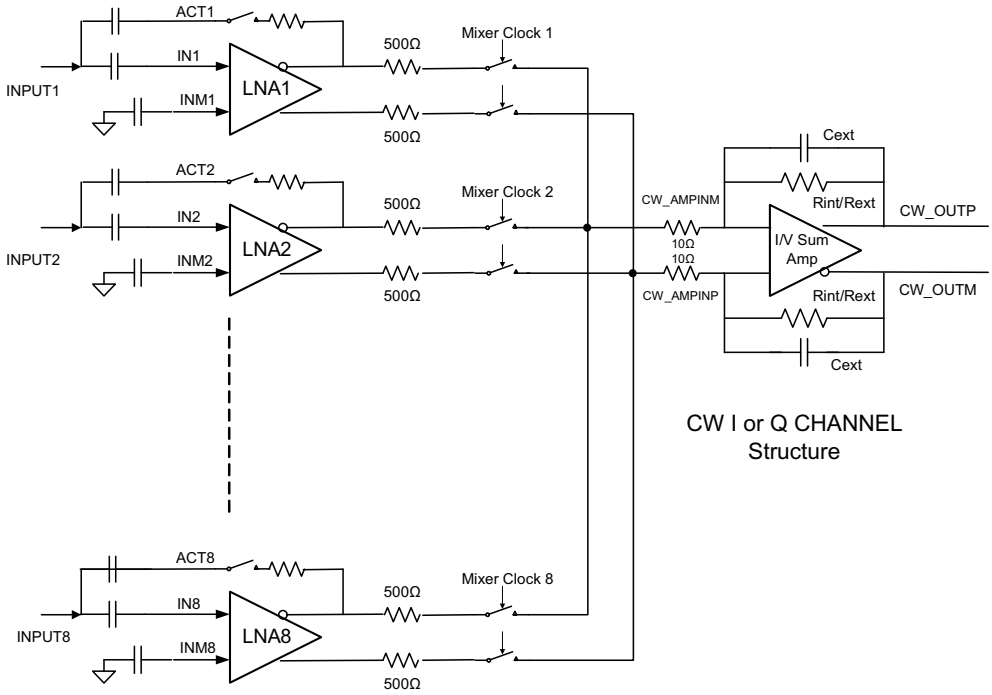


Figure 63. Simplified Block Diagram of CW Path



Note: the approximately 10-Ω to 15-Ω resistors at CW_AMPINM/P are due to internal IC routing and can create slight attenuation.

Figure 64. Complete In-Phase or Quadrature Phase Channel

The CW mixer in the AFE5808A device is passive and switch based; passive mixer adds less noise than active mixers. The CW mixer achieves good performance at low power. Figure 65 and Equation 1 describe the principles of mixer operation, where Vi(t), Vo(t), and LO(t) are input, output and local oscillator (LO) signals for a mixer respectively. The LO(t) is square-wave based and includes odd harmonic components as shown in Equation 1.

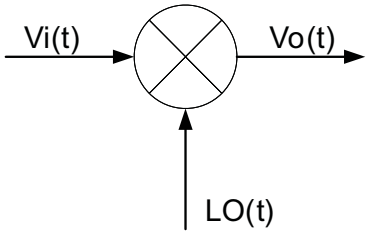


Figure 65. Block Diagram of Mixer Operation

$$Vi(t) = \sin\left(\omega_0 t + \omega_d t + \varphi\right) + f\left(\omega_0 t\right)$$

$$LO(t) = \frac{4}{\pi}\left[\sin\left(\omega_0 t\right) + \frac{1}{3}\sin\left(3\omega_0 t\right) + \frac{1}{5}\sin\left(5\omega_0 t\right)...\right]$$

$$Vo(t) = \frac{2}{\pi}\left[\cos\left(\omega_d t + \phi\right) - \cos\left(2\omega_0 t - \omega_d t + \phi\right)...\right] \quad (1)$$

From Equation 1, the 3rd and 5th order harmonics from the LO can interface with the 3rd and 5th order harmonic signals in the Vi(t); or the noise around the 3rd and 5th order harmonics in the Vi(t). Therefore, the mixer's performance is degraded. To eliminate this side effect due to the square-wave demodulation, a proprietary harmonic suppression circuit is implemented in the AFE5808A device. The 3rd and 5th harmonic components from the LO can be suppressed by over 12 dB. Thus the LNA output noise around the 3rd and 5th order harmonic bands will not be down-converted to base band. Hence, better noise figure is achieved. The conversion loss of the mixer is about –4 dB, which is derived from $20\log_{10}\frac{2}{\pi}$

The mixed current outputs of the 8 channels are summed together internally. An internal low-noise operational amplifier is used to convert the summed current to a voltage output. The internal summing amplifier is designed to accomplish low power consumption, low noise, and ease-of-use. CW outputs from multiple AFE5808A devices can be further combined on system board to implement a CW beamformer with more than 8 channels. More detailed information can be found in *Application and Implementation*.

Multiple clock options are supported in the AFE5808A CW path. Two CW clock inputs are required: N × f_{cw} clock and 1 × f_{cw} clock, where f_{cw} is the CW transmitting frequency and N could be 16, 8, 4, or 1. Users have the flexibility to select the most convenient system clock solution for the AFE5808A device. In the 16 × f_{cw} and 8 × f_{cw} modes, the 3rd and 5th harmonic suppression feature can be supported. Thus the 16 × f_{cw} and 8 × f_{cw} modes achieve better performance than the 4 × f_{cw} and 1 × f_{cw} modes.

8.3.5.1 16 × f_{cw} Mode

The 16 × f_{cw} mode achieves the best phase accuracy compared to other modes. The 16 × f_{cw} mode is the default mode for CW operation. In this mode, 16 × f_{cw} and 1 × f_{cw} clocks are required. 16×f_{cw} generates LO signals with 16 accurate phases. Multiple AFE5808A devices can be synchronized by the 1 × f_{cw}; that is, LO signals in multiple AFEs can have the same starting phase. The phase noise specification is critical only for the 16X clock. The 1X clock is for synchronization only, and it doesn't require low phase noise. See the *CW Clock Selection*.

The top level clock distribution diagram is shown in Figure 66. Each mixer's clock is distributed through a 16 × 8 cross-point switch. The inputs of the cross-point switch are 16 different phases of the 1x clock. TI recommends aligning the rising edges of the 1 × f_{cw} and 16 × f_{cw} clocks.

The cross-point switch distributes the clocks with appropriate phase delay to each mixer. For example, Vi(t) is a received signal with a delay of $\frac{1}{16}T$, a delayed LO(t) should be applied to the mixer to compensate for the $\frac{1}{16}T$ delay. Thus a 22.5º delayed clock, that is $\frac{2\pi}{16}$, is selected for this channel. The mathematic calculation is expressed in Equation 2.

$$\mathrm{Vi}(t)=\sin\left[\omega_0\left(t-\frac{1}{16f_0}\right)+\omega_d t\right]=\sin\left[\omega_0 t-22.5^\circ+\omega_d t\right]$$

$$\mathrm{LO}(t)=\frac{4}{\pi}\sin\left[\omega_0\left(t-\frac{1}{16f_0}\right)\right]=\frac{4}{\pi}\sin\left[\omega_0 t-22.5^\circ\right]$$

$$\mathrm{Vo}(t)=\frac{2}{\pi}\cos\left(\omega_d t\right)+f\left(\omega_n t\right) \quad (2)$$

Vo(t) represents the demodulated Doppler signal of each channel. When the doppler signals from N channels are summed, the signal-to-noise ratio improves.

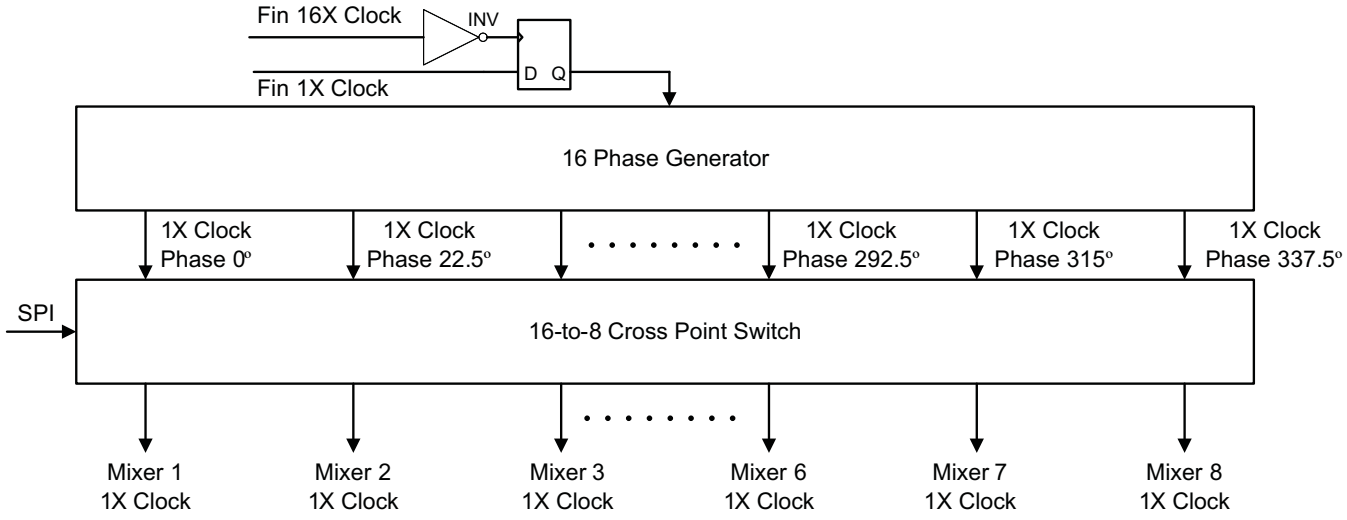


Figure 66. CW Mixer Clock Generation

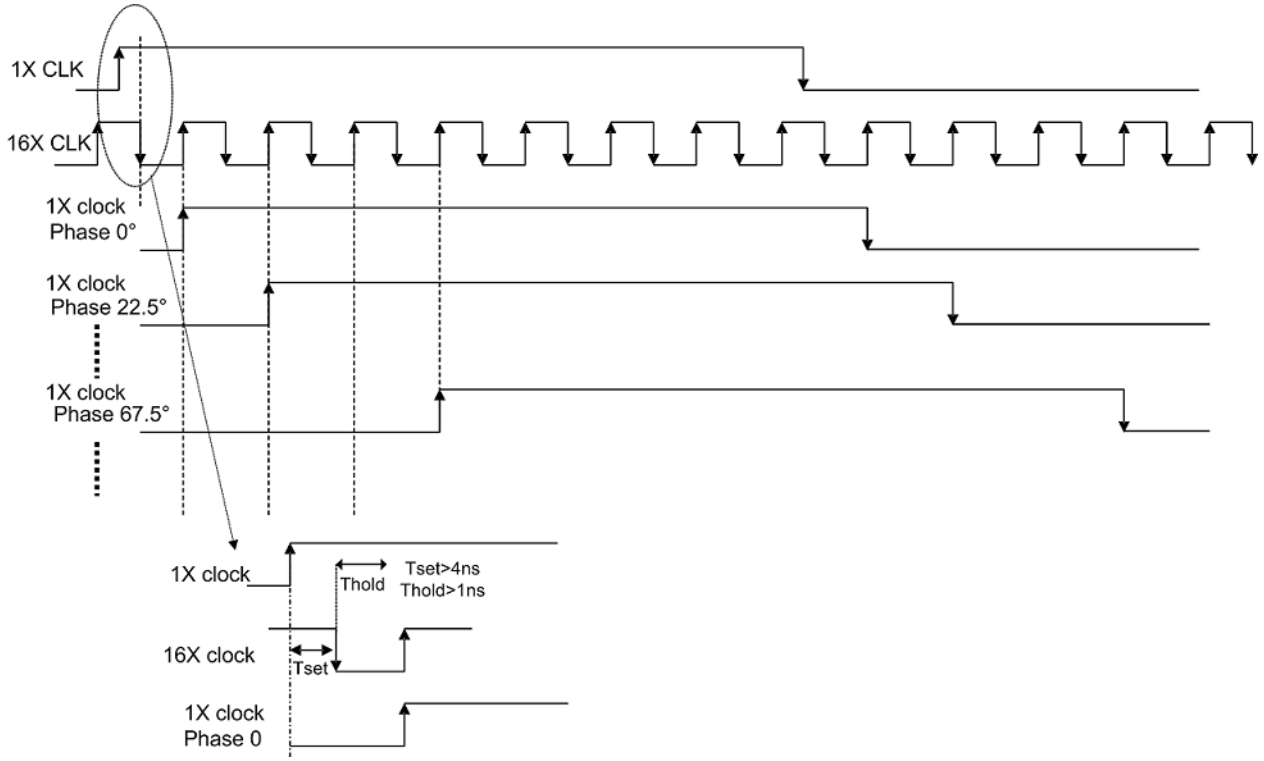


Figure 67. 1x and 16x CW Clock Timing

8.3.5.2 8 × f_{cw} and 4 × f_{cw} Modes

8 × f_{cw} and 4 × f_{cw} modes are alternative modes when higher frequency clock solution (that is 16 × f_{cw} clock) is not available in system. Figure 68 shows the block diagram of these two modes.

Good phase accuracy and matching are also maintained. Quadature clock generator is used to create in-phase and quadrature clocks with exactly 90° phase difference. The only difference between 8 × f_{cw} and 4 × f_{cw} modes is the accessibility of the 3rd and 5th harmonic suppression filter. In the 8 × f_{cw} mode, the suppression filter can be supported. In both modes, $\frac{1}{16}T$ phase delay resolution is achieved by weighting the in-phase and quadrature paths correspondingly. For example, if a delay of $\frac{1}{16}T$ or 22.5° is targeted, the weighting coefficients should follow Equation 3, assuming I_{in} and Q_{in} are sin($\omega_0 t$) and cos($\omega_0 t$) respectively:

$$I_{delayed}(t) = I_{in}\cos\left(-\frac{2\pi}{16}\right) + Q_{in}\sin\left(-\frac{2\pi}{16}\right) = I_{in}\left(t - \frac{1}{16f_0}\right)$$

$$Q_{delayed}(t) = Q_{in}\cos\left(-\frac{2\pi}{16}\right) - I_{in}\sin\left(-\frac{2\pi}{16}\right) = Q_{in}\left(t - \frac{1}{16f_0}\right) \quad (3)$$

Therefore, after I/Q mixers, phase delay in the received signals is compensated. The mixers' outputs from all channels are aligned and added linearly to improve the signal-to-noise ratio. TI recommends having the 4 × f_{cw} or 8 × f_{cw} and 1 × f_{cw} clocks aligned both at the rising edge.

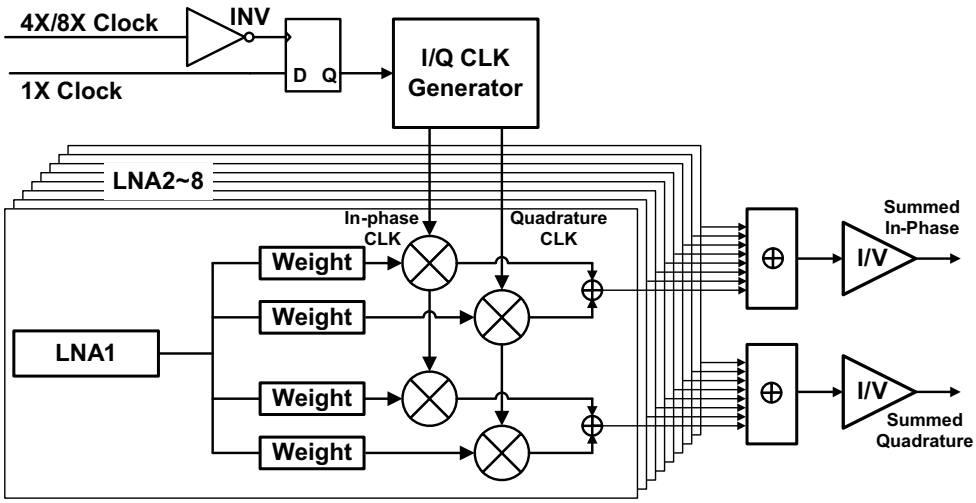


Figure 68. 8 X f_{cw} and 4 X f_{cw} Block Diagram

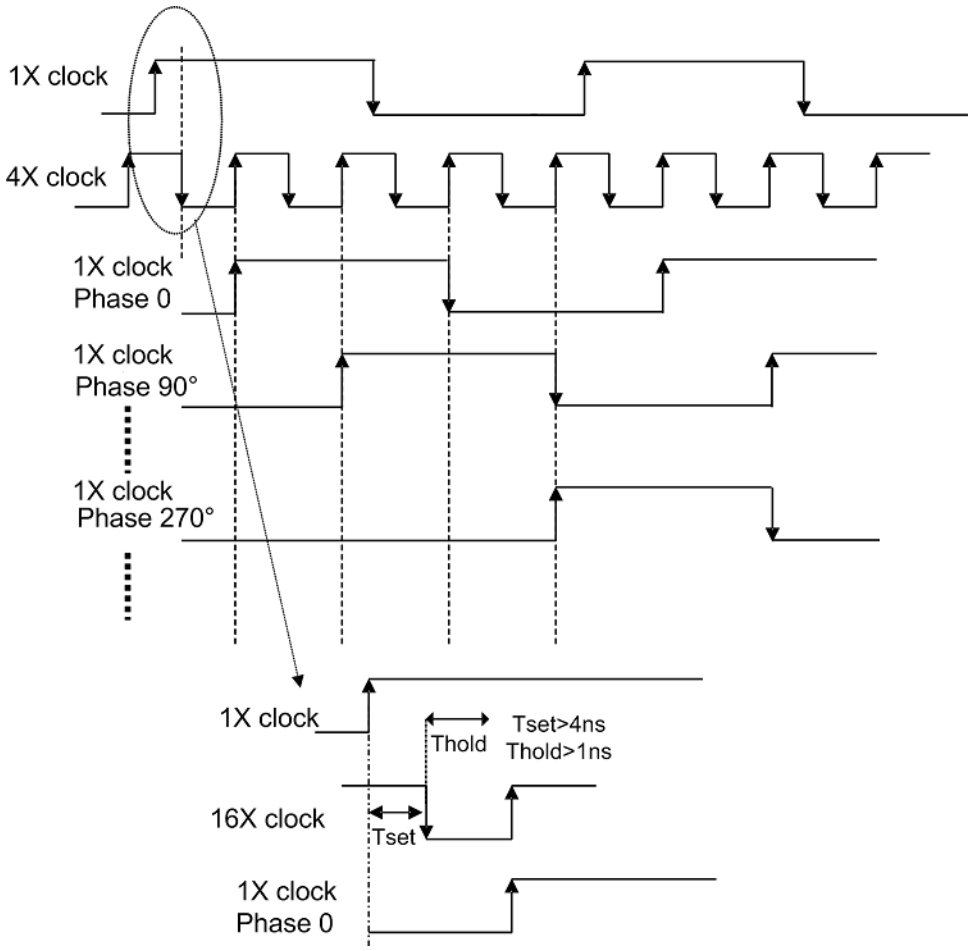


Figure 69. 8 x f_{cw} and 4 x f_{cw} Timing Diagram

8.3.5.3 1 × f_{cw} Mode

The 1x f_{cw} mode requires in-phase and quadrature clocks with low phase noise specifications. The $\frac{1}{16}T$ phase delay resolution is also achieved by weighting the in-phase and quadrature signals as described in the 8 × f_{cw} and 4 × f_{cw} modes.

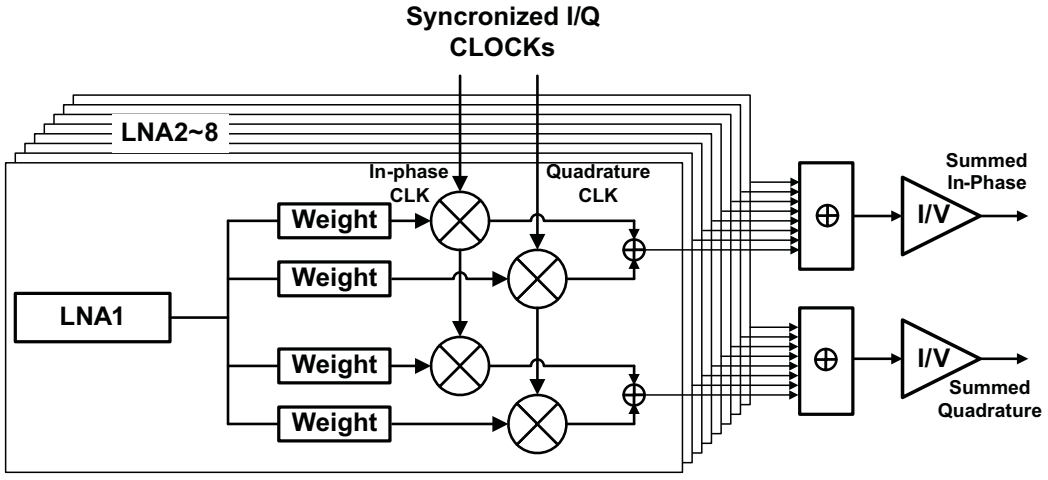


Figure 70. Block Diagram of 1 x f_{cw} mode

8.3.6 Equivalent Circuits

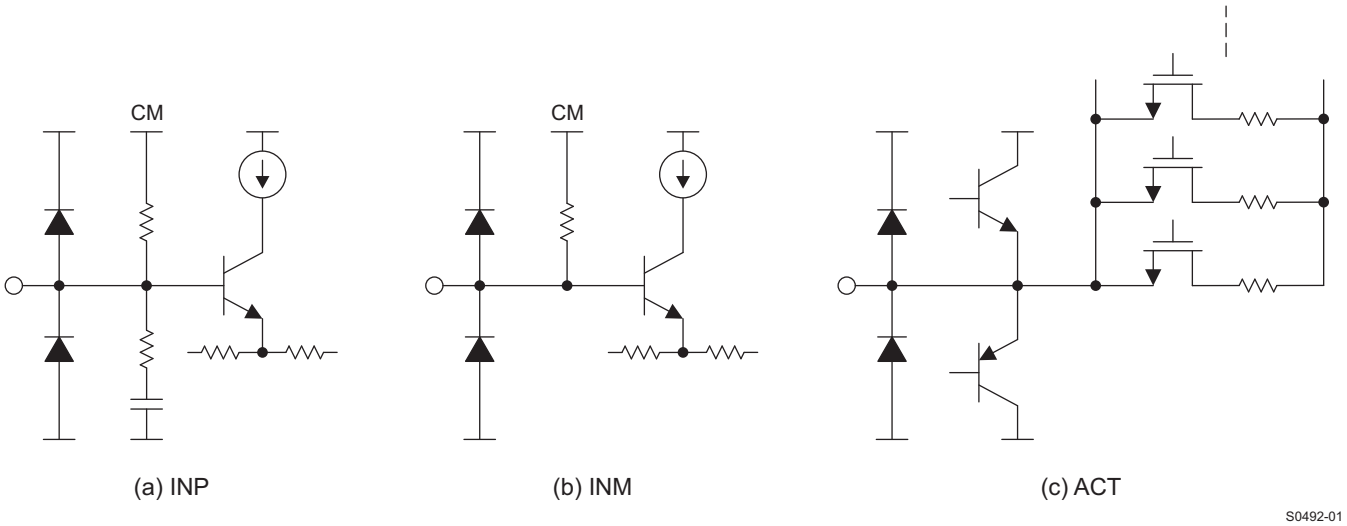


Figure 71. Equivalent Circuits of LNA inputs

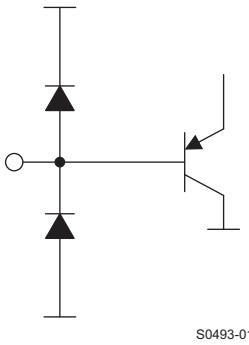


Figure 72. Equivalent Circuits of $V_{CNTLP/M}$

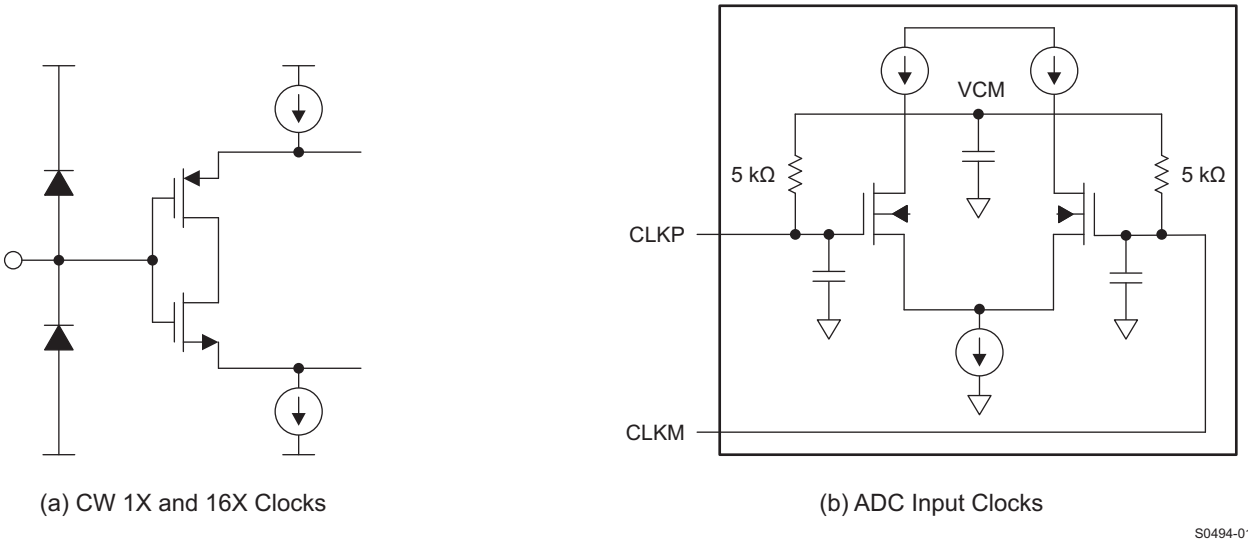


Figure 73. Equivalent Circuits of Clock Inputs

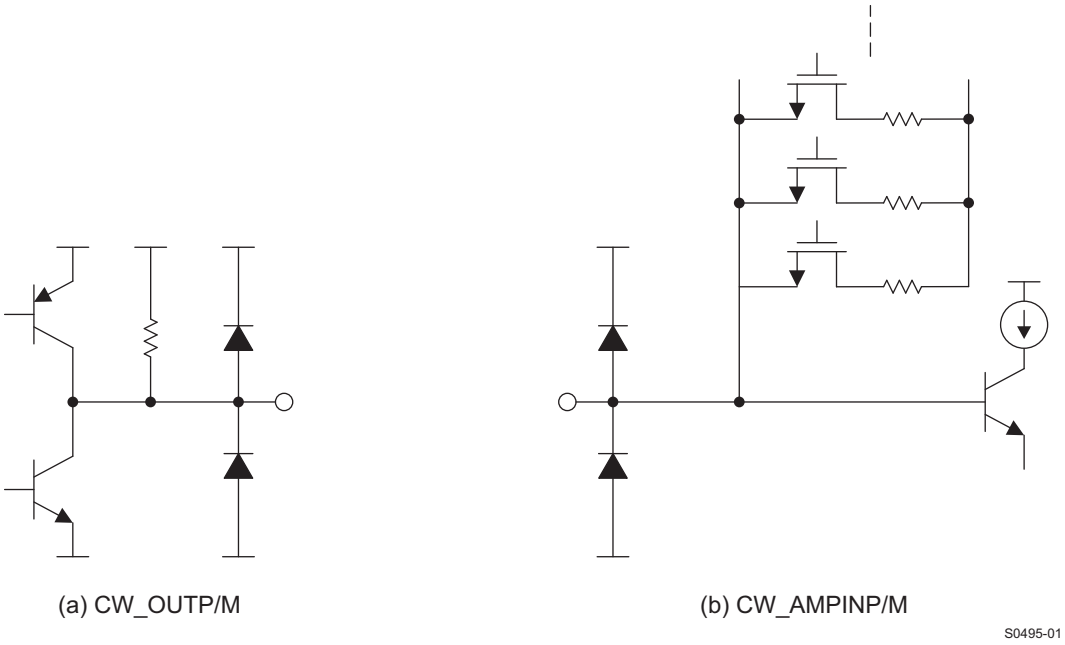


Figure 74. Equivalent Circuits of CW Summing Amplifier Inputs and Outputs

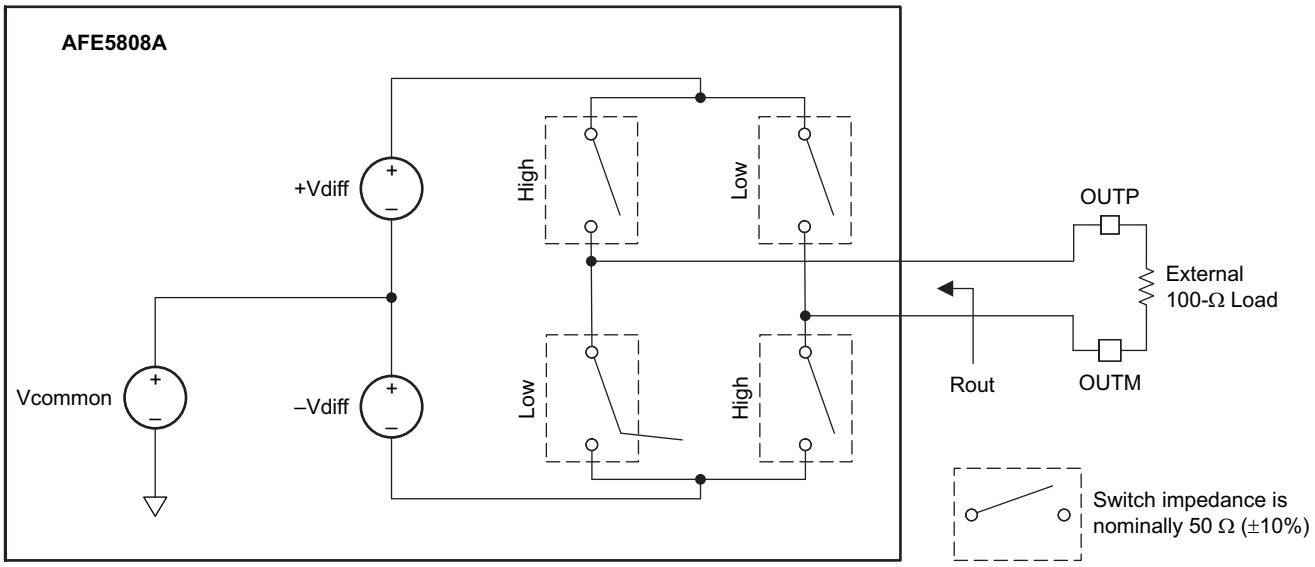


Figure 75. Equivalent Circuits of LVDS Outputs

8.3.7 LVDS Output Interface Description

The AFE5808A device has a LVDS output interface that supports multiple output formats. The ADC resolutions can be configured as 12 bit or 14 bit as shown in the LVDS timing diagrams Figure 1. The ADCs in the AFE5808A are running at 14 bit; 2 LSBs are removed when 12-bit output is selected; and two 0s are added at LSBs when 16-bit output is selected. Appropriate ADC resolutions can be selected for optimizing system performance-cost effectiveness. When the devices run at 16-bit mode, higher end FPGAs are required to process a higher rate of LVDS data. Corresponding register settings are shown in Table 5.

8.4 Device Functional Modes

The AFE5808A device is a highly-integrated AFE solution. The AFE5808A device has two functional modes: pulsed-wave imaging mode and continous-wave Doppler imaging mode. When the AFE5808A device operates in the pulsed-wave imaging mode, LNA, VCAT, PGA, LPF, and 14-bit ADC are active. In the CWD imaging mode, only LNA and CW mixer are enabled. Either mode can be enabled or programmed by the registers described in the following sections.

8.4.1 TGC Mode

By default, after reset the AFE is configured in TGC mode. Depending upon the system requirements, the device can be programmed in a suitable power mode using the register bits shown in Table 6. In the TGC mode, the digital demodulator after ADC can be enabled as well for further digital processing.

8.4.2 CW Mode

To configure the device in CW mode, set the CW_TGC_SEL (0x36[8]) register bit to 1. To save power, the voltage-controlled attenuator and programmable gain amplifier in the TGC path can be disabled by setting the 0x35[12] to 1. Also, the ADC can be powered down completely using the 0x1[0] . Usually only half the number of channels in a system are active in the CW mode. Thus, the individual channel control can power down unused channels and save power; see register 0x1[9:2] and 0x35[7:0].

8.4.3 TGC + CW Mode

In systems that require fast switching between the TGC and CW modes, either mode can be selected simply by setting the CW_TGC_SEL register bit.

8.4.4 Test Modes

The AFE5808A device includes multiple test modes to accelerate system development.

8.4.4.1 ADC Test Modes

The AFE5808A device can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. The device may also be made to output 6 preset patterns:

1. **Ramp:** Setting Register 2[15:13] = 111 causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full-scale code, the ADC output returns back to zero code and ramps again.
2. **Zeros:** The device can be programmed to output all 0s by setting Register 2[15:13] = 110.
3. **Ones:** The device can be programmed to output all 1s by setting Register 2[15:13] = 100.
4. **Deskew Pattern:** When 2[15:13] = 010; this mode replaces the 14-bit ADC output with the 01010101010101 word.
5. **Sync Pattern:** When 2[15:13] = 001, the normal ADC output is replaced by a fixed 11111110000000 word.
6. **Toggle:** When 2[15:13] = 101, the normal ADC output is alternating between 1s and 0s. The start state of ADC word can be either 1s or 0s.
7. **Custom Pattern:** This mode can be enabled when 2[15:13] = 011. Users can write the required VALUE into register bits <CUSTOM PATTERN>, which is Register 5[13:0]. Then, the device will output VALUE at its outputs, about 3 to 4 ADC clock cycles after the 24th rising edge of SCLK. So, the time taken to write one value is 24 SCLK clock cycles + 4 ADC clock cycles. To change the customer pattern value, users can repeat writing Register 5[13:0] with a new value. Due to the speed limit of SPI, the refresh rate of the custom pattern may not be high. For example, 128 points custom pattern takes approximately 128 × (24 SCLK clock cycles + 4 ADC clock cycles).

NOTE

Only one of the above ADC patterns can be active at any given instant.

Device Functional Modes (continued)

8.4.4.2 VCA Test Mode

The VCA has a test mode in which the CH7 and CH8 PGA outputs can be brought to the CW pins. By monitoring these PGA outputs, the functionality of VCA operation can be verified. The PGA outputs are connected to the virtual ground pins of the summing amplifier (CW_IP_AMPINM/P, CW_QP_AMPINM/P) through 5-kΩ resistors. The PGA outputs can be monitored at the summing amplifier outputs when the LPF capacitors C_{EXT} are removed. The signals at the summing amplifier outputs are attenuated due to the 5-kΩ resistors. The attenuation coefficient is $R_{INT/EXT}$ / 5 kΩ.

If users would like to check the PGA outputs without removing C_{EXT}, an alternative way is to measure the PGA outputs directly at the CW_IP_AMPINM/P and CW_QP_AMPINM/P when the CW summing amplifier is powered down.

Some registers are related to this test mode, PGA Test Mode Enable: Reg59[9]; Buffer Amplifier Power Down Reg59[8]; and Buffer Amplifier Gain Control Reg54[4:0]. Based on the buffer amplifier configuration, the registers can be set in different ways:

- **Configuration 1**
  - In this configuration, the test outputs can be monitored at CW_AMPINP/M.
  - Reg59[9] = 1; test mode enabled
  - Reg59[8] = 0; buffer amplifier powered-down
- **Configuration 2**
  - In this configuration, the test outputs can be monitored at CW_OUTP/M.
  - Reg59[9] = 1; test mode enabled
  - Reg59[8] = 1; buffer amplifier powered on
  - Reg54[4:0] = 10H; internal feedback 2-kΩ resistor enabled. Different values can be used as well.

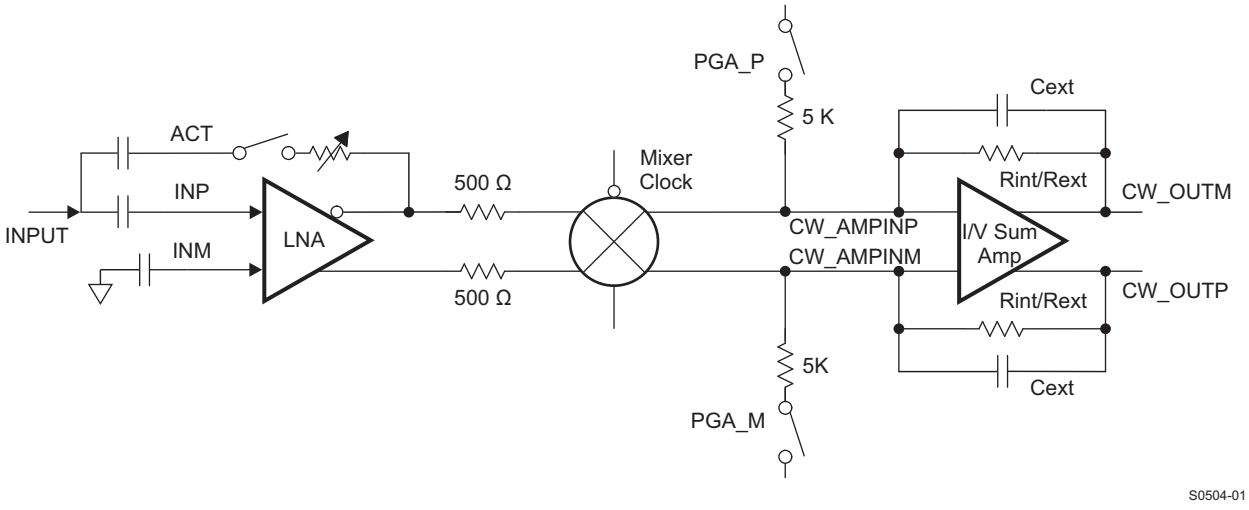


Figure 76. AFE5808A PGA Test Mode

8.4.5 Power Management

8.4.5.1 Power and Performance Optimization

The AFE5808A device has options to adjust power consumption and meet different noise performances. This feature would be useful for portable systems operated by batteries when low power is more desired. See *Electrical Characteristics* as well as the *Typical Characteristics* for more information.

Device Functional Modes (continued)

8.4.5.2 Power Management Priority

Power management plays a critical role to extend battery life and ensure long operation time. The AFE5808A device has fast and flexible power-down and power-up control, which can maximize battery life. The AFE5808A device can be powered down and powered up through external pins or internal registers. The following table indicates the affected circuit blocks and priorities when the power management is invoked. The higher priority controls can overwrite the lower priority ones. In the device, all the power down controls are logically ORed to generate final power down for different blocks. Thus, the higher priority controls can cover the lower priority ones. The AFE5808A register settings are maintained when the AFE5808A is in either partial power down mode or complete power down mode.

Table 2. Power Management Priority

PIN OR REGISTER	NAME	BLOCKS	PRIORITY
Pin	PDN_GLOBAL	All	High
Pin	PDN_VCA	LNA + VCAT+ PGA	Medium
Register	VCA_PARTIAL_PDN	LNA + VCAT+ PGA	Low
Register	VCA_COMPLETE_PDN	LNA + VCAT+ PGA	Medium
Pin	PDN_ADC	ADC	Medium
Register	ADC_PARTIAL_PDN	ADC	Low
Register	ADC_COMPLETE_PDN	ADC	Medium
Register	PDN_VCAT_PGA	VCAT + PGA	Lowest
Register	PDN_LNA	LNA	Lowest

8.4.5.3 Partial Power Up and Power Down Mode

The partial power-up and power-down mode is also called as fast power-up and power-down mode. In this mode, most amplifiers in the signal path are powered down, while the internal reference circuits remain active as well as the LVDS clock circuit (that is the LVDS circuit still generates its frame and bit clocks).

The partial power down function allows the AFE5808A device to wake up from a low-power state quickly. This configuration ensures that the external capacitors are discharged slowly; thus, a minimum wake-up time is needed as long as the charges on those capacitors are restored. The VCA wake-up response is typically about 2 µs or 1% of the power down duration whichever is larger. The longest wake-up time depends on the capacitors connected at INP and INM, as the wake-up time is the time required to recharge the caps to the desired operating voltages. For 0.1 µF at INP and 15 nF at INM can give a wake-up time of 2.5 ms. For larger capacitors this time will be longer. The ADC wake-up time is about 1 µs. Thus the AFE5808A wake-up time is more dependent on the VCA wake-up time. This also assumes that the ADC clock has been running for at least 50 µs before normal operating mode resumes. The power-down time is instantaneous, less than 1 µs.

This fast wake-up response is desired for portable ultrasound applications in which the power saving is critical. The pulse repetition frequency of a ultrasound system could vary from 50 KHz to 500 Hz, while the imaging depth (that is, the active period for a receive path) varies from 10 µs to hundreds of µs. The power saving can be pretty significant when a system's PRF is low. In some cases, only the VCA would be powered down while the ADC keeps running normally to ensure minimal impact to FPGAs.

In the partial power-down mode, the AFE5808A typically dissipates only 26 mW/ch, representing an 80% power reduction compared to the normal operating mode. This mode can be set using either pins (PDN_VCA and PDN_ADC) or register bits (VCA_PARTIAL_PDN and ADC_PARTIAL_PDN).

8.4.5.4 Complete Power-Down Mode

To achieve the lowest power dissipation of 0.7 mW/CH, the AFE5808A device can be placed into a complete power-down mode. This mode is controlled through the registers ADC_COMPLETE_PDN, VCA_COMPLETE_PDN or PDN_GLOBAL pin. In the complete power-down mode, all circuits including reference circuits within the AFE5808A device are powered down; and the capacitors connected to the AFE5808A device are discharged. The wake-up time depends on the time needed to recharge these capacitors. The wake-up time depends on the time that the AFE5808A device spends in shutdown mode. 0.1 µF at INP and 15 nF at INM can give a wake-up time close to 2.5 ms.

8.4.5.5 Power Saving in CW Mode

Usually only half the number of channels in a system are active in the CW mode. Thus the individual channel control through ADC_PDN_CH <7:0> and VCA_PDN_CH <7:0> can power down unused channels and save power consumption greatly. Under the default register setting in the CW mode, the voltage controlled attenuator, PGA, and ADC are still active. During the debug phase, both the PW and CW paths can be running simultaneously. In real operation, these blocks need to be powered down manually.

8.5 Programming

8.5.1 Serial Register Timing

8.5.1.1 Serial Register Write Description

Programming of different modes can be done through the serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. All these pins have a pulldown resistor to GND of 20 kΩ. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every rising edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiple of 24-bit words within a single active SEN pulse (there is an internal counter that counts groups of 24 clocks after the falling edge of SEN). The interface can work with the SCLK frequency from 20 MHz down to low speeds (a few Hz) and even with non-50% duty cycle SCLK. The data is divided into two main portions: a register address (8 bits) and the data itself (16 bits) to load on the addressed register. When writing to a register with unused bits, these must be set to 0. Figure 77 shows this process.

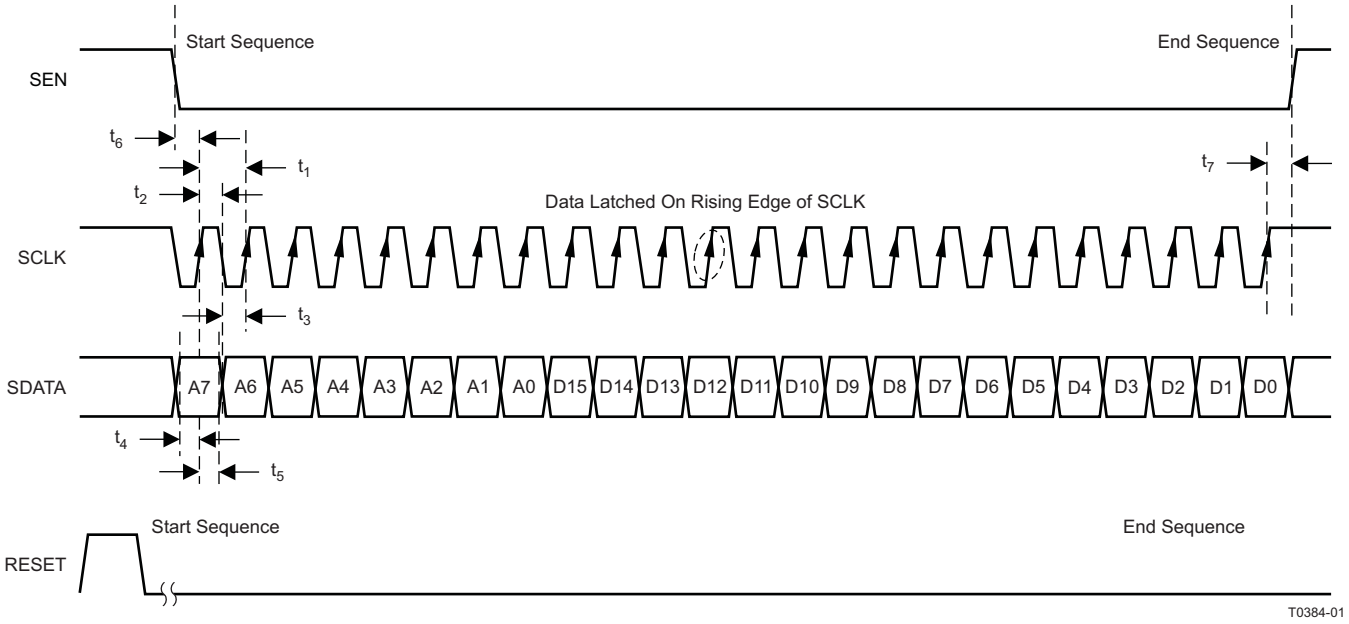


Figure 77. SPI Timing

Programming (continued)

8.5.1.2 Register Readout Description

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic test to verify the serial interface communication between the external controller and the AFE. First, the <REGISTER READOUT ENABLE> bit (Reg0[1]) needs to be set to '1', then the user should initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read. The data bits are **don't care**. The device will output the contents (D15-D0) of the selected register on the SDOUT pin. SDOUT has a typical delay t8 of 20 ns from the falling edge of the SCLK. For lower speed SCLK, SDOUT can be latched on the rising edge of SCLK. For higher speed SCLK, for example, the SCLK period lesser than 60 ns, TI recommends latching the SDOUT at the next falling edge of SCLK. Figure 78 shows this operation (the time specifications follow the same information provided. In the readout mode, users still can access the <REGISTER READOUT ENABLE> through SDATA/SCLK/SEN. To enable serial register writes, set the <REGISTER READOUT ENABLE> bit back to '0'.

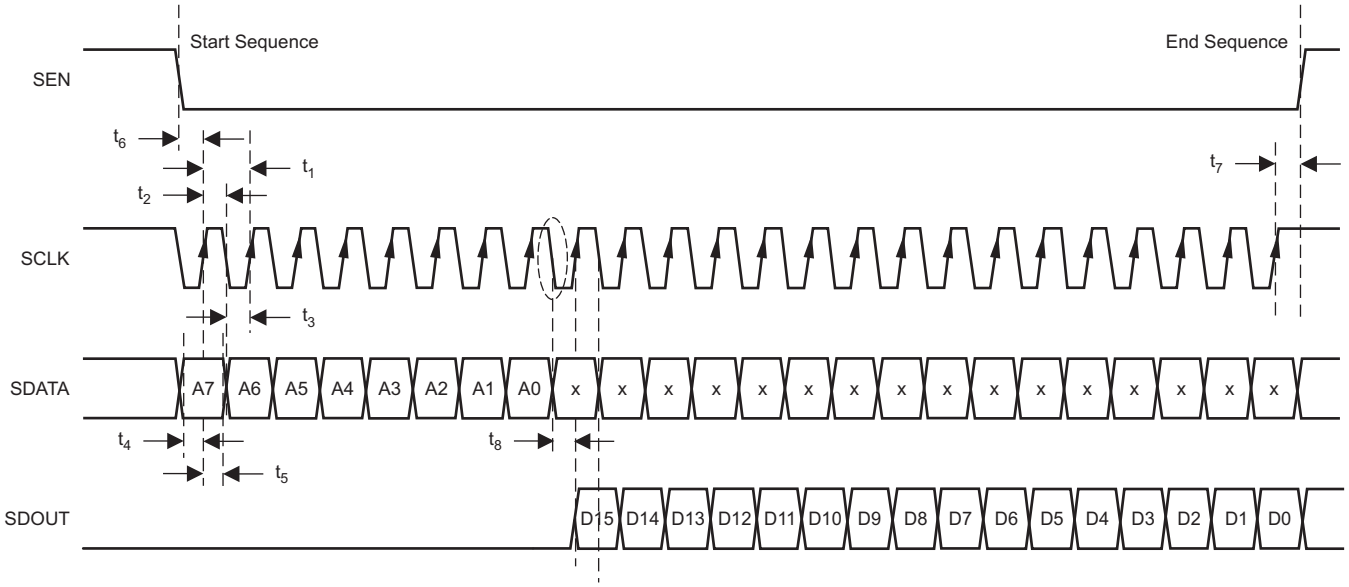


Figure 78. Serial Interface Register Read

The AFE5808A SDOUT buffer is tri-stated and will get enabled only when 0[1] (REGISTER READOUT ENABLE) is enabled. SDOUT pins from multiple AFE5808As can be tied together without any pullup resistors. Level shifter SN74AUP1T04 can be used to convert 1.8-V logic to 2.5-V/3.3-V logics if needed.

8.6 Register Maps

A reset process is required at the AFE5808A initialization stage. Initialization can be done in one of two ways:

1. Through a hardware reset by applying a positive pulse in the RESET pin
2. Through a software reset using the serial interface by setting the SOFTWARE RESET bit to high. Setting this bit initializes the internal registers to the respective default values (all zeros) and then self-resets the SOFTWARE RESET bit to low. In this case, the RESET pin can stay low (inactive).

After reset, all ADC and VCA registers are set to '0', that is default settings. During register programming, all reserved/unlisted register bits need to be set as '0'. Register settings are maintained when the AFE5808A device is in either partial power down mode or complete power down mode.

8.6.1 ADC Register Map

Table 3. ADC Register Map

ADDRESS (DEC)	ADDRESS (HEX)	DEFAULT VALUE	FUNCTION	DESCRIPTION
0[0]	0x0[0]	0	SOFTWARE_RESET	0: Normal operation; 1: Resets the device and self-clears the bit to '0'
0[1]	0x0[1]	0	REGISTER_READOUT_ENABLE	0:Disables readout; 1: enables readout of register at SDOUT Pin
1[0]	0x1[0]	0	ADC_COMPLETE_PDN	0: Normal 1: Complete Power down
1[1]	0x1[1]	0	LVDS_OUTPUT_DISABLE	0: Output Enabled; 1: Output disabled
1[9:2]	0x1[9:2]	0	ADC_PDN_CH<7:0>	0: Normal operation; 1: Power down. Power down Individual ADC channels. 1[9]→CH8…1[2]→CH1
1[10]	0x1[10]	0	PARTIAL_PDN	0: Normal Operation; 1: Partial Power Down ADC
1[11]	0x1[11]	0	LOW_FREQUENCY_ NOISE_SUPPRESSION	0: No suppression; 1: Suppression Enabled
1[13]	0x1[13]	0	EXT_REF	0: Internal Reference; 1: External Reference. VREF_IN is used. Both 3[15] and 1[13] should be set as 1 in the external reference mode
1[14]	0x1[14]	0	LVDS_OUTPUT_RATE_2X	0: 1x rate; 1: 2x rate. Combines data from 2 channels on 1 LVDS pair. When ADC clock rate is low, this feature can be used
1[15]	0x1[15]	0	SINGLE-ENDED_CLK_MODE	0: Differential clock input; 1: Single-ended clock input
2[2:0]	0x2[2:0]	0	RESERVED	Set to 0
2[10:3]	0x2[10:3]	0	POWER-DOWN_LVDS	0: Normal operation; 1: PDN Individual LVDS outputs. 2[10]→CH8…2[3]→CH1
2[11]	0x2[11]	0	AVERAGING_ENABLE	0: No averaging; 1: Average 2 channels to increase SNR
2[12]	0x2[12]	0	LOW_LATENCY	0: Default Latency with digital features supported, 11 cycle latency 1: Low Latency with digital features bypassed, 8 cycle latency
2[15:13]	0x2[15:13]	0	TEST_PATTERN_MODES	000: Normal operation; 001: Sync; 010: De-skew; 011: Custom; 100:All 1's; 101: Toggle; 110: All 0's; 111: Ramp
3[7:0]	0x3[7:0]	0	INVERT_CHANNELS	0: No inverting; 1:Invert channel digital output. 3[7]→CH8;3[0]→CH1
3[8]	0x3[8]	0	CHANNEL_OFFSET_ SUBSTRACTION_ENABLE	0: No offset subtraction; 1: Offset value Subtract Enabled
3[9:11]	0x3[9:11]	0	RESERVED	Set to 0

Register Maps (continued)

Table 3. ADC Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	DEFAULT VALUE	FUNCTION	DESCRIPTION
3[12]	0x3[12]	0	DIGITAL_GAIN_ENABLE	0: No digital gain; 1: Digital gain Enabled
3[14:13]	0x3[14:13]	0	SERIALIZED_DATA_RATE	Serialization factor 00: 14x 01: 16x 10: reserved 11: 12x when 4[1] = 1. In the 16x serialization rate, two 0s are filled at two LSBs (see Table 5)
3[15]	0x3[15]	0	ENABLE_EXTERNAL_ REFERENCE_MODE	0: Internal reference mode; 1: Set to external reference mode Note: both 3[15] and 1[13] should be set as 1 when configuring the device in the external reference mode
4[1]	0x4[1]	0	ADC_RESOLUTION_SELECT	0: 14bit; 1: 12bit
4[3]	0x4[3]	0	ADC_OUTPUT_FORMAT	0: 2's complement; 1: Offset binary
4[4]	0x4[4]	0	LSB_MSB_FIRST	0: LSB first; 1: MSB first
5[13:0]	0x5[13:0]	0	CUSTOM_PATTERN	Custom pattern data for LVDS output (2[15:13] = 011)
10[8]	0xA[8]	0	SYNC_PATTERN	0: Test pattern outputs of 8 channels are NOT synchronized. 1: Test pattern outputs of 8 channels are synchronized.
13[9:0]	0xD[9:0]	0	OFFSET_CH1	Value to be subtracted from channel 1 code
13[15:11]	0xD[15:11]	0	DIGITAL_GAIN_CH1	0 to 6 dB in 0.2-dB steps
15[9:0]	0xF[9:0]	0	OFFSET_CH2	value to be subtracted from channel 2 code
15[15:11]	0xF[15:11]	0	DIGITAL_GAIN_CH2	0 to 6dB in 0.2-dB steps
17[9:0]	0x11[9:0]	0	OFFSET_CH3	value to be subtracted from channel 3 code
17[15:11]	0x11[15:11]	0	DIGITAL_GAIN_CH3	0 to 6 dB in 0.2-dB steps
19[9:0]	0x13[9:0]	0	OFFSET_CH4	value to be subtracted from channel 4 code
19[15:11]	0x13[15:11]	0	DIGITAL_GAIN_CH4	0 to 6 dB in 0.2-dB steps
21[0]	0x15[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH1-4	0: Disable the digital HPF filter; 1: Enable for 1-4 channels
21[4:1]	0x15[4:1]	0	DIGITAL_HPF_FILTER_K_CH1-4	Set K for the high-pass filter (k from 2 to 10, that is 0010B to 1010B). This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k / (2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (see Table 4 and Figure 58)
25[9:0]	0x19[9:0]	0	OFFSET_CH8	value to be subtracted from channel 8 code
25[15:11]	0x19[15:11]	0	DIGITAL_GAIN_CH8	0 to 6 dB in 0.2-dB steps
27[9:0]	0x1B[9:0]	0	OFFSET_CH7	value to be subtracted from channel 7 code
27[15:11]	0x1B[15:11]	0	DIGITAL_GAIN_CH7	0 to 6dB in 0.2-dB steps
29[9:0]	0x1D[9:0]	0	OFFSET_CH6	value to be subtracted from channel 6 code
29[15:11]	0x1D[15:11]	0	DIGITAL_GAIN_CH6	0 to 6 dB in 0.2-dB steps
31[9:0]	0x1F[9:0]	0	OFFSET_CH5	value to be subtracted from channel 5 code
31[15:11]	0x1F[15:11]	0	DIGITAL_GAIN_CH5	0 to 6 dB in 0.2-dB steps
33[0]	0x21[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH5-8	0: Disable the digital HPF filter; 1: Enable for 5-8 channels
33[4:1]	0x21[4:1]	0	DIGITAL_HPF_FILTER_K_CH5-8	Set K for the high-pass filter (k from 2 to 10, 010B to 1010B) This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k / (2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (see Table 4 and Figure 58)
66[15]	0x42[15]	0	DITHER	0: Disable dither function. 1: Enable dither function. Improve the ADC linearity with slight noise degradation.

8.6.2 ADC Register/Digital Processing Description

The ADC in the AFE5808A device has extensive digital processing functionalities that can be used to enhance ultrasound system performance. The digital processing blocks are arranged as in Figure 79.

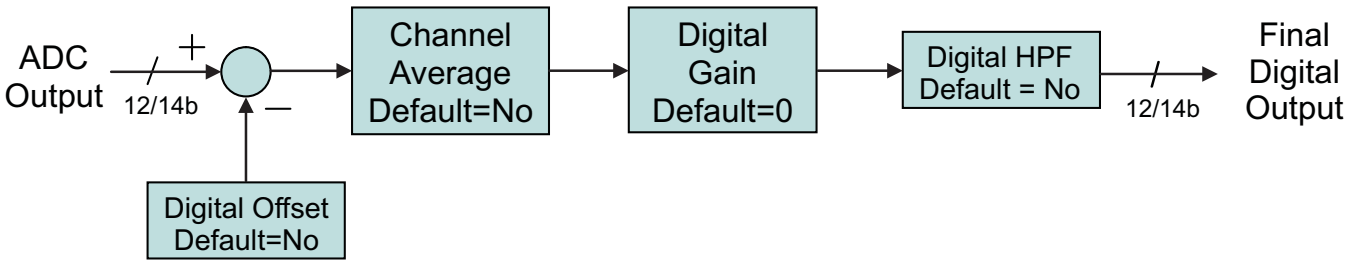


Figure 79. ADC Digital Block Diagram

8.6.2.1 AVERAGING_ENABLE: Address: 2[11]

When set to 1, two samples, corresponding to two consecutive channels, are averaged (channel 1 with 2, 3 with 4, 5 with 6, and 7 with 8). If both channels receive the same input, the net effect is an improvement in SNR. The averaging is performed as:

- Channel 1 + channel 2 comes out on channel 3
- Channel 3 + channel 4 comes out on channel 4
- Channel 5 + channel 6 comes out on channel 5
- Channel 7 + channel 8 comes out on channel 6

8.6.2.2 ADC_OUTPUT_FORMAT: Address: 4[3]

The ADC output, by default, is in 2's-complement mode. Programming the ADC_OUTPUT_FORMAT bit to 1 inverts the MSB, and the output becomes straight-offset binary mode.

8.6.2.3 DIGITAL_GAIN_ENABLE: Address: 3[12]

Setting this bit to 1 applies to each channel i the corresponding gain given by DIGTAL_GAIN_CHi <15:11>. The gain is given as 0dB + 0.2dB × DIGTAL_GAIN_CHi<15:11>. For instance, if DIGTAL_GAIN_CH5<15:11> = 3, channel 5 is increased by 0.6dB gain. DIGTAL_GAIN_CHi <15:11> = 31 produces the same effect as DIGTAL_GAIN_CHi <15:11> = 30, setting the gain of channel i to 6dB.

8.6.2.4 DIGITAL_HPF_ENABLE

- CH1-4: Address 21[0]
- CH5-8: Address 33[0]

8.6.2.5 DIGITAL_HPF_FILTER_K_CHX

- CH1-4: Address 21[4:1]
- CH5-8: Address 3[4:1]

This group of registers controls the characteristics of a digital high-pass transfer function applied to the output data, following Equation 4.

$$y(n) = \frac{2^k}{2^k + 1}\left[x(n) - x(n-1) + y(n-1)\right] \quad (4)$$

These digital HPF registers (one for the first four channels and one for the second group of four channels) describe the setting of K. The digital high pass filter can be used to suppress low frequency noise which commonly exists in ultrasound echo signals. The digital filter can significantly benefit near field recovery time due to T/R switch low frequency response. Table 4 shows the cut-off frequency vs K, also see Figure 58.

Table 4. Digital HPF –1-dB Corner Frequency vs K and Fs

k	40 MSPS	50 MSPS	65 MSPS
2	2780 kHz	3480 kHz	4520 kHz
3	1490 kHz	1860 kHz	2420 kHz
4	770 kHz	960 kHz	1250 kHz

8.6.2.6 LOW_FREQUENCY_NOISE_SUPPRESSION: Address: 1[11]

The low-frequency noise suppression mode is especially useful in applications where good noise performance is desired in the frequency band of 0 MHz to 1 MHz (around DC). Setting this mode shifts the low-frequency noise of the AFE5808A device to approximately Fs / 2, thereby moving the noise floor around DC to a much lower value. Register bit 1[11] is used for enabling or disabling this feature. When this feature is enabled, power consumption of the device increases by approximately 1 mW/CH.

8.6.2.7 LVDS_OUTPUT_RATE_2X: Address: 1[14]

The output data always uses a DDR format, with valid/different bits on the positive as well as the negative edges of the LVDS bit clock, DCLK. The output rate is set by default to 1X (LVDS_OUTPUT_RATE_2X = 0), where each ADC has one LVDS stream associated with it. If the sampling rate is low enough, two ADCs can share one LVDS stream, thereby lowering the power consumption devoted to the interface. The unused outputs will output zero. To avoid consumption from those outputs, no termination must not be connected to them. The distribution on the used output pairs is done in the following way:

- Channel 1 and channel 2 come out on channel 3. Channel 1 comes out first.
- Channel 3 and channel 4 come out on channel 4. Channel 3 comes out first.
- Channel 5 and channel 6 come out on channel 5. Channel 5 comes out first.
- Channel 7 and channel 8 come out on channel 6. Channel 7 comes out first.

8.6.2.8 CHANNEL_OFFSET_SUBSTRACTION_ENABLE: Address: 3[8]

Setting this bit to 1 enables the subtraction of the value on the corresponding OFFSET_CHx<9:0> (offset for channel i) from the ADC output. The number is specified in 2s-complement format. For example, OFFSET_CHx<9:0> = 11 1000 0000 means subtract 128. For OFFSET_CHx<9:0> = 00 0111 1111 the effect is to subtract 127. In effect, both addition and subtraction can be performed. Note that the offset is applied before the digital gain (see ***ADC_OUTPUT_FORMAT**: Address: 4[3]*). The whole data path is 2s-complement throughout internally, with digital gain being the last step. Only when ADC_OUTPUT_FORMAT = 1 (straight binary output format) is the 2s-complement word translated into offset binary at the end.

8.6.2.9 SERIALIZED_DATA_RATE: Address: 3[14:13]

Table 5. Corresponding Register Settings

LVDS Rate	12 bit (6X DCLK)	14 bit (7X DCLK)	16 bit (8X DCLK)
Reg 3 [14:13]	11	00	01
Reg 4 [2:0]	010	000	000
Description	2 LSBs removed	N/A	2 0s added at LSBs

8.6.2.10 TEST_PATTERN_MODES: Address: 2[15:13]

The AFE5808A device can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. The device may also be made to output 6 preset patterns:

1. **Ramp:** Setting Register 2[15:13] = 111 causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.
2. **Zeros:** The device can be programmed to output all zeros by setting Register 2[15:13] = 110;
3. **Ones:** The device can be programmed to output all 1s by setting Register 2[15:13] = 100;
4. **Deskew Patten:** When 2[15:13] = 010; this mode replaces the 14-bit ADC output with the 01010101010101 word.
5. **Sync Pattern:** When 2[15:13] = 001, the normal ADC output is replaced by a fixed 11111110000000 word.

6. **Toggle:** When 2[15:13] = 101, the normal ADC output is alternating between 1's and 0's. The start state of ADC word can be either 1's or 0's.
7. **Custom Pattern:** It can be enabled when 2[15:13] = 011;. Users can write the required VALUE into register bits <CUSTOM PATTERN> which is Register 5[13:0]. Then the device will output VALUE at its outputs, about 3 to 4 ADC clock cycles after the 24th rising edge of SCLK. So, the time taken to write one value is 24 SCLK clock cycles + 4 ADC clock cycles. To change the customer pattern value, users can repeat writing Register 5[13:0] with a new value. Due to the speed limit of SPI, the refresh rate of the custom pattern may not be high. For example, 128 points custom pattern will take approximately 128 × (24 SCLK clock cycles + 4 ADC clock cycles).

NOTE

Only one of the above patterns can be active at any given instant.

8.6.2.11 SYNC_PATTERN: Address: 10[8]

By enabling this bit, all channels' test pattern outputs are synchronized. When 10[8] is set as 1, the ramp patterns of all 8 channels start simultaneously.

8.6.3 VCA Register Map

Table 6. VCA Register Map

ADDRESS (DEC)	ADDRESS (HEX)	DEFAULT VALUE	FUNCTION	DESCRIPTION
50[10]	0x32[10]	0	PGA_CLAMP_-6dB	0: No clamp enabled. 1: The PGA output linearity will be degraded when PGA output signal is higher than –6 dBFS, 1 V_{PP}. The PGA output is limited to about 1.6 V_{PP}. ADC is not overloaded while its dynamic range is reduced by 2 dB. This setting will reduce the channel gain by about 1.5 dB. Note: 0x33[7:5] needs to be set as 000 in the low noise mode or 100 in the low/medium power mode.
51[0]	0x33[0]	0	RESERVED	0
51[3:1]	0x33[3:1]	0	LPF_PROGRAMMABILITY	000: 15 MHz, 010: 20 MHz, 011: 30 MHz, 100: 10 MHz
51[4]	0x33[4]	0	PGA_INTEGRATOR_DISABLE (PGA_HPF_DISABLE)	0: Enable 1: Disables offset integrator for PGA. See explanation for the PGA integrator function in *Application and Implementation* section
51[7:5]	0x33[7:5]	0	PGA_CLAMP_LEVEL	Low Noise mode: 53[11:10] = 00 000: –2 dBFS 010: 0 dBFS 1XX: Clamp is disabled Low power/Medium Power mode; 53[11:10] = 01/10 100: –2 dBFS 110: 0 dBFS 0XX: clamp is disabled Note: 0x32[10] needs to be set as 0. Note: the clamp circuit makes sure that PGA output is in linear range. For example, at 000 setting, PGA output HD3 will be worsen by 3 dB at –2 dBFS ADC input. In normal operation, clamp function can be set as 000 in the low noise mode. The maximum PGA output level can exceed 2 V_{PP} with the clamp circuit enabled. In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7] = 0.
51[13]	0x33[13]	0	PGA_GAIN_CONTROL	0:24 dB; 1:30 dB.
52[4:0]	0x34[4:0]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_CNTL	See Table 8 Reg 52[5] should be set as '1' to access these bits
52[5]	0x34[5]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_ENABLE	0: Disables; 1: Enables internal active termination individual resistor control
52[7:6]	0x34[7:6]	0	PRESET_ACTIVE_ TERMINATIONS	00: 50 Ω, 01: 100 Ω, 10: 200 Ω, 11: 400 Ω. (Note: the device will adjust resistor mapping (52[4:0]) automatically. 50-Ω active termination is NOT supported in 12 dB LNA setting. Instead, '00' represents high impedance mode when LNA gain is 12 dB)
52[8]	0x34[8]	0	ACTIVE TERMINATION ENABLE	0: Disables; 1: Enables active termination
52[10:9]	0x34[10:9]	0	LNA_INPUT_CLAMP_SETTING	00: Auto setting, 01: 1.5 V_{PP}, 10: 1.15 V_{PP} and 11: 0.6 V_{PP}
52[11]	0x34[11]	0	RESERVED	Set to 0
52[12]	0x34[12]	0	LNA_INTEGRATOR_DISABLE (LNA_HPF_DISABLE)	0: Enables; 1: Disables offset integrator for LNA. See the explanation for this function in the following section
52[14:13]	0x34[14:13]	0	LNA_GAIN	00: 18 dB; 01: 24 dB; 10: 12 dB; 11: Reserved
52[15]	0x34[15]	0	LNA_INDIVIDUAL_CH_CNTL	0: Disable; 1: Enable LNA individual channel control. See Register 57 for details

Table 6. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	DEFAULT VALUE	FUNCTION	DESCRIPTION
53[7:0]	0x35[7:0]	0	PDN_CH<7:0>	0: Normal operation; 1: Powers down corresponding channels. Bit7→CH8, Bit6→CH7…Bit0→CH1. PDN_CH will shut down whichever blocks are active depending on TGC mode or CW mode
53[8]	0x35[8]	0	RESERVED	Set to 0
53[9]	0x35[9]	0	RESERVED	Set to 0
53[10]	0x35[10]	0	LOW_POWER	0: Low noise mode; 1: Sets to low power mode (53[11] = 0). At 30 dB PGA, total chain gain may slightly change. See typical characteristics
53[11]	0x35[11]	0	MED_POWER	0: Low noise mode; 1: Sets to medium power mode(53[10] = 0). At 30 dB PGA, total chain gain may slightly change. See typical characteristics
53[12]	0x35[12]	0	PDN_VCAT_PGA	0: Normal operation; 1: Powers down VCAT (voltage-controlled-attenuator) and PGA
53[13]	0x35[13]	0	PDN_LNA	0: Normal operation; 1: Powers down LNA only
53[14]	0x35[14]	0	VCA_PARTIAL_PDN	0: Normal operation; 1: Powers down LNA, VCAT, and PGA partially(fast wake response)
53[15]	0x35[15]	0	VCA_COMPLETE_PDN	0: Normal operation; 1: Powers down LNA, VCAT, and PGA completely (slow wake response). This bit can overwrite 53[14].
54[4:0]	0x36[4:0]	0	CW_SUM_AMP_GAIN_CNTL	Selects Feedback resistor for the CW Amplifier as per Table 8 below
54[5]	0x36[5]	0	CW_16X_CLK_SEL	0: Accepts differential clock; 1: Accepts CMOS clock
54[6]	0x36[6]	0	CW_1X_CLK_SEL	0: Accepts CMOS clock; 1: Accepts differential clock
54[7]	0x36[7]	0	RESERVED	Set to 0
54[8]	0x36[8]	0	CW_TGC_SEL	0: TGC Mode; 1 : CW Mode Note : VCAT and PGA are still working in CW mode. They should be powered down separately through 53[12]
54[9]	0x36[9]	0	CW_SUM_AMP_ENABLE	0: enables CW summing amplifier; 1: disables CW summing amplifier Note: 54[9] is only effective in CW mode.
54[11:10]	0x36[11:10]	0	CW_CLK_MODE_SEL	00: 16X mode; 01: 8X mode; 10: 4X mode; 11: 1X mode
55[3:0]	0x37[3:0]	0	CH1_CW_MIXER_PHASE	0000→1111, 16 different phase delays, see Table 12
55[7:4]	0x37[7:4]	0	CH2_CW_MIXER_PHASE	
55[11:8]	0x37[11:8]	0	CH3_CW_MIXER_PHASE	
55[15:12]	0x37[15:12]	0	CH4_CW_MIXER_PHASE	
56[3:0]	0x38[3:0]	0	CH5_CW_MIXER_PHASE	
56[7:4]	0x38[7:4]	0	CH6_CW_MIXER_PHASE	
56[11:8]	0x38[11:8]	0	CH7_CW_MIXER_PHASE	
56[15:12]	0x38[15:12]	0	CH8_CW_MIXER_PHASE	
57[1:0]	0x39[1:0]	0	CH1_LNA_GAIN_CNTL	00: 18 dB; 01: 24 dB; 10: 12 dB; 11: Reserved REG52[15] should be set as '1'
57[3:2]	0x39[3:2]	0	CH2_LNA_GAIN_CNTL	

Table 6. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	DEFAULT VALUE	FUNCTION	DESCRIPTION
57[5:4]	0x39[5:4]	0	CH3_LNA_GAIN_CNTL	00: 18 dB; 01: 24 dB; 10: 12 dB; 11: Reserved REG52[15] should be set as '1'
57[7:6]	0x39[7:6]	0	CH4_LNA_GAIN_CNTL	
57[9:8]	0x39[9:8]	0	CH5_LNA_GAIN_CNTL	
57[11:10]	0x39[11:10]	0	CH6_LNA_GAIN_CNTL	
57[13:12]	0x39[13:12]	0	CH7_LNA_GAIN_CNTL	
57[15:14]	0x39[15:14]	0	CH8_LNA_GAIN_CNTL	
59[3:2]	0x3B[3:2]	0	HPF_LNA	00: 100 kHz; 01: 50 kHz; 10: 200 kHz; 11: 150 kHz with 0.015 µF on INMx
59[6:4]	0x3B[6:4]	0	DIG_TGC_ATT_GAIN	000: 0-dB attenuation; 001: 6-dB attenuation; N: ~N×6-dB attenuation when 59[7] = 1
59[7]	0x3B[7]	0	DIG_TGC_ATT	0: disable digital TGC attenuator; 1: enable digital TGC attenuator
59[8]	0x3B[8]	0	CW_SUM_AMP_PDN	0: Power down; 1: Normal operation Note: 59[8] is only effective in TGC test mode.
59[9]	0x3B[9]	0	PGA_TEST_MODE	0: Normal CW operation; 1: PGA outputs appear at CW outputs

8.6.4 AFE5808A VCA Register Description

8.6.4.1 LNA Input Impedances Configuration (Active Termination Programmability)

Different LNA input impedances can be configured through the register 52[4:0]. By enabling and disabling the feedback resistors between LNA outputs and ACTx pins, LNA input impedance is adjustable accordingly. Table 7 describes the relationship between LNA gain and 52[4:0] settings. The input impedance settings are the same for both TGC and CW paths.

The AFE5808A device also has 4 preset active termination impedances as described in 52[7:6]. An internal decoder is used to select appropriate resistors corresponding to different LNA gain.

The input impedance of AFE can be programmed through Register 52[8:0]. Each bit of Register 52[4:0] controls one active termination resistor. The below tables indicate the nominal impedance values when individual active termination resistors are selected. More details can be found in *Active Termination*. Table 8 shows the corresponding impedances under different Register 52[4:0] values, while Table 9 shows the Register 52[4:0] settings under different impedances.

NOTE

Table 8 and Table 9 show norminal input impedance values. Due to silicon process varation, the actual values can vary some.

Table 7. Register 52[4:0] Description

52[4:0]/0x34[4:0]	FUNCTION
00000	No feedback resistor enabled
00001	Enables 450-Ω feedback resistor
00010	Enables 900-Ω feedback resistor
00100	Enables 1800-Ω feedback resistor
01000	Enables 3600-Ω feedback resistor
10000	Enables 4500-Ω feedback resistor

Table 8. Register 52[4:0] vs LNA Input Impedances

52[4:0]/0x34[4:0]	00000	00001	00010	00011	00100	00101	00110	00111
LNA:12dB	High Z	150 Ω	300 Ω	100 Ω	600 Ω	120 Ω	200 Ω	86 Ω
LNA:18dB	High Z	90 Ω	180 Ω	60 Ω	360 Ω	72 Ω	120 Ω	51 Ω
LNA:24dB	High Z	50 Ω	100 Ω	33 Ω	200 Ω	40 Ω	66.67 Ω	29 Ω
52[4:0]/0x34[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
LNA:12dB	1200 Ω	133 Ω	240 Ω	92 Ω	400 Ω	109 Ω	171 Ω	80 Ω
LNA:18dB	720 Ω	80 Ω	144 Ω	55 Ω	240 Ω	65 Ω	103 Ω	48 Ω
LNA:24dB	400 Ω	44 Ω	80 Ω	31 Ω	133 Ω	36 Ω	57 Ω	27 Ω
52[4:0]/0x34[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
LNA:12dB	1500 Ω	136 Ω	250 Ω	94 Ω	429 Ω	111 Ω	176 Ω	81 Ω
LNA:18dB	900 Ω	82 Ω	150 Ω	56 Ω	257 Ω	67 Ω	106 Ω	49 Ω
LNA:24dB	500 Ω	45 Ω	83 Ω	31 Ω	143 Ω	37 Ω	59 Ω	27 Ω
52[4:0]/0x34[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
LNA:12dB	667 Ω	122 Ω	207 Ω	87 Ω	316 Ω	102 Ω	154 Ω	76 Ω
LNA:18dB	400 Ω	73 Ω	124 Ω	52 Ω	189 Ω	61 Ω	92 Ω	46 Ω
LNA:24dB	222 Ω	41 Ω	69 Ω	29 Ω	105 Ω	34 Ω	51 Ω	25 Ω

Table 9. LNA Input Impedances vs. Register 52[4:0]

Z (Ω)	LNA:12dB	LNA:18dB	LNA:24dB	Z (Ω)	LNA:12dB	LNA:18dB	LNA:24dB	Z (Ω)	LNA:12dB	LNA:18dB	LNA:24dB
25			11111	67		10101		143			10100
27			10111/01111	69			11010	144		01010	
29			00111/11011	72		00101		150	00001	10010	
31			01011/10011	73		11001		154	11110		
33			00011	76	11111			171	01110		
34			11101	80	01111	01001	01010	176	10110		
36			01101	81	10111			180		00010	
37			10101	82		10001		189		11100	
40			00101	83			10010	200	00110		00100
41			11001	86	00111			207	11010		
44			01001	87	11011			222			11000
45			10001	90		00001		240	01010	01100	
46		11111		92	01011	11110		250	10010		
48		01111		94	10011			257		10100	
49		10111		100	00011		00010	300	00010		
50			00001	102	11101			316	11100		
51			00111/11110	103		01110		360		00100	
52		11011		105			11100	400	01100	11000	01000
55		01011		106		10110		429	10100		
56		10011		109	01101			500			10000
57			01110	111	10101			600	00100		
59			10110	120	00101	00110		667	11000		
60		00011		122	11001			720		01000	
61		11101		124		11010		900		10000	
65		01101		133	01001		01100	1200	01000		
66.7			00110	136	10001			1500	10000		

8.6.4.2 Programmable Gain for CW Summing Amplifier

Different gain can be configured for the CW summing amplifier through the register 54[4:0]. By enabling and disabling the feedback resistors between the summing amplifier inputs and outputs, the gain is adjustable accordingly to maximize the dynamic range of CW path. Table 10 describes the relationship between the summing amplifier gain and 54[4:0] settings.

Table 10. Register 54[4:0] Description

54[4:0]/0x36[4:0]	FUNCTION
00000	No feedback resistor
00001	Enables 250-Ω feedback resistor
00010	Enables 250-Ω feedback resistor
00100	Enables 500-Ω feedback resistor
01000	Enables 1000-Ω feedback resistor
10000	Enables 2000-Ω feedback resistor

Table 11. Register 54[4:0] vs Summing Amplifier Gain

54[4:0]/0x36[4:0]	**00000**	**00001**	**00010**	**00011**	**00100**	**00101**	**00110**	**00111**
CW I/V Gain	N/A	0.5	0.5	0.25	1	0.33	0.33	0.2
54[4:0]/0x36[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
CW I/V Gain	2	0.4	0.4	0.22	0.67	0.29	0.29	0.18
54[4:0]/0x36[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
CW I/V Gain	4	0.44	0.44	0.24	0.8	0.31	0.31	0.19
54[4:0]/0x36[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
CW I/V Gain	1.33	0.36	0.36	0.21	0.57	0.27	0.27	0.17

8.6.4.3 Programmable Phase Delay for CW Mixer

Accurate CW beamforming is achieved through adjusting the phase delay of each channel. In the AFE5808A device, 16 different phase delays can be applied to each LNA output, and it meets the standard requirement of typical ultrasound beamformer, that is $\frac{1}{16}\lambda$ beamformer resolution. Table 10 describes the relationship between the phase delays and the register 55 and 56 settings.

Table 12. CW Mixer Phase Delay vs Register Settings
CH1: 55[3:0], CH2: 55[7:4], CH3: 55[11:8], CH4: 55[15:12],
CH5: 56[3:0], CH6: 56[7:4], CH7: 56[11:8], CH8: 56[15:12],

CHX_CW_MIXER_PHASE	0000	0001	0010	0011	0100	0101	0110	0111
PHASE SHIFT	0	22.5°	45°	67.5°	90°	112.5°	135°	157.5°
CHX_CW_MIXER_PHASE	1000	1001	1010	1011	1100	1101	1110	1111
PHASE SHIFT	180°	202.5°	225°	247.5°	270°	292.5°	315°	337.5°

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The AFE5808A device is a highly integrated analog front-end solution. To maximize its performance, users must carefully optimize its surrounding circuits, such as T/R switch, VCNTL circuits, audio ADCs for CW path, clock distribution network, synchronized power supplies and digital processors. Some common practices are described below.

Table 13 lists companion TI devices that are used to complete the analog signal chain in a system.

Table 13. Application Companion Devices

PART NUMBER	PART DESCRIPTION	FUNCTIONS
THS4130, SLOS318	Fully Differential Input/Output Low Noise Amplifier With Shutdown	TGC VCNTL Opamp, CW summing amplifier and active filter
OPA1632, SBOS286	Fully Differential I/O Audio Amplifier	TGC VCNTL amplifier, CW summing amplifier and active filter
OPA2211, SBOS377	1.1nV/$\sqrt{Hz}$ Noise, Low Power, Precision Operational Amplifier	CW summing amplifier and active filter
LME49990, SNOSB16	Ultra-low Distortion, Ultra-low Noise Operational Amplifier	CW summing amplifier and active filter
LMH6629, SNOSB18	Ultra-Low Noise, High-Speed Operational Amplifier with Shutdown	CW summing amplifier and active filter
ADS8413, SLAS490	16-bit, Unipolar Diff Input, 2MSPS Sampling rate, 4.75V to 5.25V ADC with LVDS Serial Interface	CW Audio ADC
ADS8881, SBAS547	18-Bit, 1-MSPS, Serial Interface, microPower, Truly-Differential Input, SAR ADC	CW Audio ADC
DAC7811, SBAS337	12-Bit, Serial Input, Multiplying Digital to Analog Converter	TGC VCNTL Digital to Analog Converter
LMK04800, SNAS489	Low Noise Clock Jitter Cleaner With Dual Cascaded PLLs and Integrated 1.9 GHz VCO	Jitter cleaner and clock synthesizer
CDCM7005, SCAS793	High Performance, Low Phase Noise, Low Skew Clock Synchronizer	Jitter cleaner and clock synthesizer
CDCE72010, SCAS858	10 Outputs Low Jitter Clock Synchronizer and Jitter Cleaner	Jitter cleaner and clock synthesizer
CDCLVP1208, SCAS890	Low Jitter, 2-Input Selectable 1:8 Universal-to-LVPECL Buffer	Clock buffer
LMK00308, SNAS576	3.1-GHz Differential Clock Buffer/Level Translator	Clock buffer
LMK01000, SNAS437	1.6 GHz High Performance Clock Buffer, Divider, and Distributor	Clock buffer
SN74AUP1T04, SCES800	Low Power, 1.8/2.5/3.3-V Input, 3.3-V CMOS Output, Single Inverter Gate	1.8V/2.5V/3.3V Level shifter for SPI
UCC28250, SLUSA29	Advanced PWM Controller with Pre-Bias Operation	Synchronized DC-DC power supply controller

9.2 Typical Application

Figure 80 lists a typical application circuit diagram. The configuration for each block is discussed in the following sections.

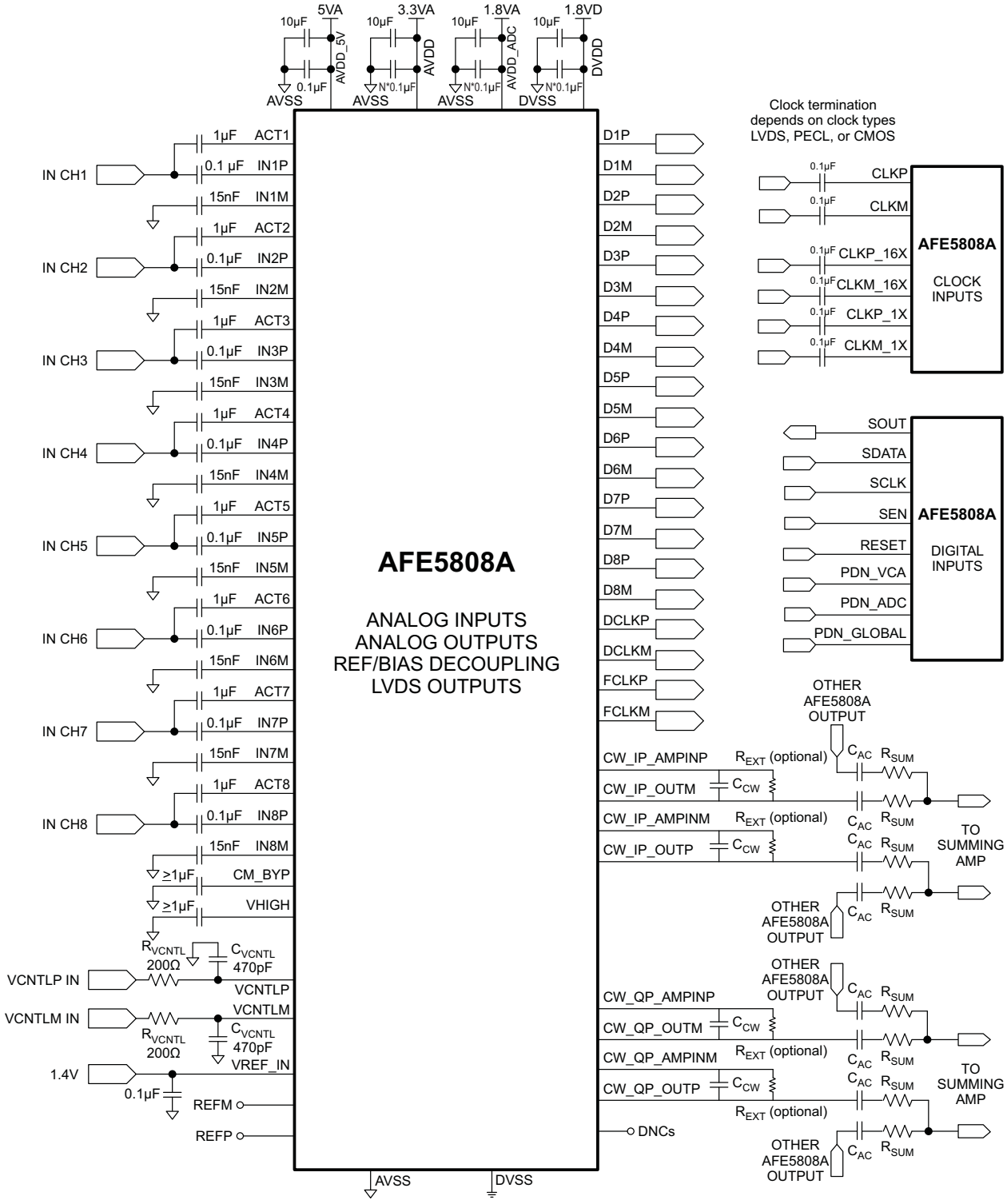


Figure 80. Typical Application Circuit

Typical Application (continued)

9.2.1 Design Requirements

Table 14 shows the typical requirements for a traditional medical ultrasound imaging system.

Table 14. Design Parameters

PARAMETER	EXAMPLE VALUES
Signal center frequency (f_0)	1 MHz to approximately 20 MHz
Signal bandwidth (BW)	10% to approximately 100% of f_0
Overloaded signals due to T/R switch leakage	approximately 2 V_{PP}
Maximum input signal amplitude	100 mV_{PP} to 1 V_{PP}
Transducer noise level	1 nV/$\sqrt{Hz}$
Dynamic range	151 dBc/Hz
Time gain compensation range	40 dB
Total harmonic distortion	40 dBc at 5MHz

9.2.2 Detailed Design Procedure

Medical ultrasound imaging is a widely-used diagnostic technique that enables visualization of internal organs including their size, structure, and blood flow estimation. An ultrasound system uses a focal imaging technique that involves time shifting, scaling, and intelligently summing the echo energy using an array of transducers to achieve high imaging performance. The concept of focal imaging provides the ability to focus on a single point in the scan region. By subsequently focusing at different points, an image is assembled.

When initiating an imaging, a pulse is generated and transmitted from each of the 64 transducer elements. The pulse, now in the form of mechanical energy, propagates through the body as sound waves, typically in the frequency range of 1 MHz to 15 MHz. The sound waves are attenuated as they travel through the objects being imaged, and the attenuation coefficients α are about 0.54 dB/(MHz×cm) in soft tissue and 6 to approximately 10 dB/(MHz×cm) in bone. Most medical ultrasound systems use the reflection imaging mode and the total signal attenuation is calculated by 2 × depth × α × f_0. As the signal travels, portions of the wave front energy are reflected. Signals that are reflected immediately after transmission are very strong because they are from reflections close to the surface; reflections that occur long after the transmit pulse are very weak because they are reflecting from deep in the body. As a result of the limitations on the amount of energy that can be put into the imaging object, the industry developed extremely sensitive receive electronics with wide dynamic range.

Receive echoes from focal points close to the surface require little, if any, amplification. This region is referred to as the near field. However, receive echoes from focal points deep in the body are extremely weak and must be amplified by a factor of 100 or more. This region is referred to as the far field. In the high-gain (far field) mode, the limit of performance is the sum of all noise sources in the receive chain. In high-gain (far field) mode, system performance is defined by its overall noise level, which is limited by the noise level of the transducer assembly and the receive low-noise amplifier (LNA). However in the low-gain (near field) mode, system performance is defined by the maximum amplitude of the input signal that the system can handle. The ratio between noise levels in high-gain mode and the signal amplitude level in low-gain mode is defined as the dynamic range of the system. The high integration and high dynamic range of the device make it ideally suited for ultrasound imaging applications.

The device includes an integrated LNA and VCAT (which use the gain that can be changed with enough time to handle both near- and far-field systems), a low-pass antialiasing filter to limit the noise bandwidth, an ADC with high SNR performance, and a CW mixer. Figure 80 illustrates an application circuit of the device.

Use the following steps to design medical ultrasound imaging systems:

1. Use the signal center frequency and signal bandwidth to select an appropriate ADC sampling frequency.

2. Use the time gain compensation range to select the range of the VCNTL signal.

3. Use the transducer noise level and maximum input signal amplitude to select the appropriate LNA gain. The device input-referred noise level reduces with higher LNA gain. However, higher LNA gain leads to lower input signal swing support.

4. Select different passive components for different device pins as shown in Figure 80.

5. Select the appropriate input termination configuration as discussed in *Active Termination*.

6. Select the clock configuration for the ADC and CW clocks as discussed in *CW Clock Selection* and *ADC Clock Configurations*.

9.2.2.1 LNA Configuration

9.2.2.1.1 LNA Input Coupling and Decoupling

The LNA closed-loop architecture is internally compensated for maximum stability without the need of external compensation components. The LNA inputs are biased at 2.4 V and AC coupling is required. A typical input configuration is shown in Figure 81. C_{IN} is the input AC coupling capacitor. C_{ACT} is a part of the active termination feedback path. Even if the active termination is not used, the C_{ACT} is required for the clamp functionality. Recommended values for C_{ACT} = 1 µF and C_{IN} are ≥ 0.1 µF. A pair of clamping diodes is commonly placed between the T/R switch and the LNA input. Schottky diodes with suitable forward drop voltage (for example, the BAT754/54 series, the BAS40 series, the MMBD7000 series, or similar) can be considered depending on the transducer echo amplitude.

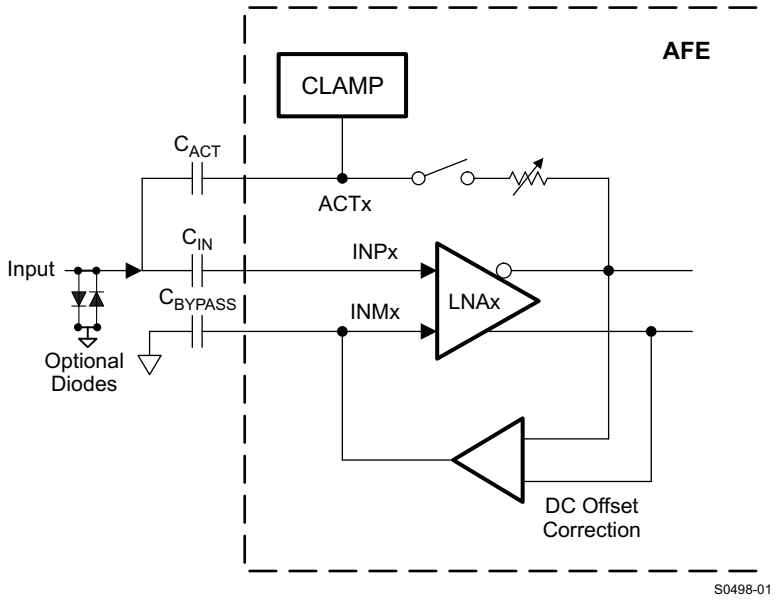


Figure 81. LNA Input Configurations

This architecture minimizes any loading of the signal source that may otherwise lead to a frequency-dependent voltage divider. The closed-loop design yields low offsets and offset drift. C_{BYPASS} (≥0.015 µF) is used to set the high-pass filter cut-off frequency and decouple the complimentary input. Its cut-off frequency is inversely proportional to the C_{BYPASS} value, The HPF cut-off frequency can be adjusted through the register 59[3:2] a Table 15 lists. Low frequency signals at T/R switch output, such as signals with slow ringing, can be filtered out. In addition, the HPF can minimize system noise from DC-DC converters, pulse repetition frequency (PRF) trigger, and frame clock. Most ultrasound systems' signal processing unit includes digital high-pass filters or band-pass filters (BPFs) in FPGAs or ASICs. Further noise suppression can be achieved in these blocks. In addition, a digital HPF is available in the AFE5808A ADC. If low frequency signal detection is desired in some applications, the LNA HPF can be disabled.

Table 15. LNA HPF Settings (C_{BYPASS} = 15 nF)

Reg59[3:2] (0x3B[3:2])	FREQUENCY
00	100 kHz
01	50 kHz
10	200 kHz
11	150 kHz

CM_BYP and VHIGH pins, which generate internal reference voltages, need to be decoupled with ≥ 1-µF capacitors. Bigger bypassing capacitors (> 2.2 µF) may be beneficial if low frequency noise exists in system.

9.2.2.1.2 LNA Noise Contribution

The noise spec is critical for LNA and it determines the dynamic range of entire system. The LNA of the AFE5808A achieves low power and an exceptionally low-noise voltage of 0.63 nV/√Hz, and a low current noise of 2.7 pA/√Hz.

Typical ultrasonic transducer's impedance Rs varies from tens of ohms to several hundreds of ohms. Voltage noise is the dominant noise in most cases; however, the LNA current noise flowing through the source impedance (Rs) generates additional voltage noise.

$$LNA\_Noise_{total} = \sqrt{V_{LNAnoise}^2 + R_s^2 \times I_{LNAnoise}^2} \quad (5)$$

The AFE5808A device achieves low noise figure (NF) over a wide range of source resistances as shown in Figure 32, Figure 33, and Figure 34.

9.2.2.1.3 Active Termination

In ultrasound applications, signal reflection exists due to long cables between transducer and system. The reflection results in extra ringing added to echo signals in PW mode. Since the axial resolution depends on echo signal length, such ringing effect can degrade the axial resolution. Hence, either passive termination or active termination, is preferred if good axial resolution is desired. Figure 82 shows three termination configurations:

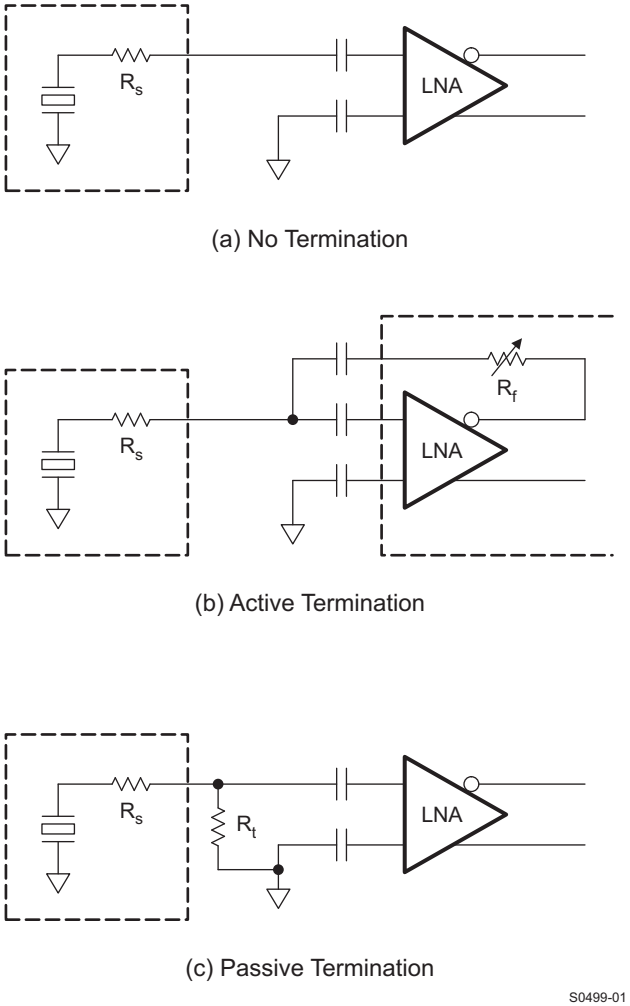


Figure 82. Termination Configurations

Under the no termination configuration, the input impedance of the AFE5808A device is about 6 kΩ (8 K//20 pF) at 1 MHz. Passive termination requires external termination resistor R_t, which contributes to additional thermal noise.

The LNA supports active termination with programmable values, as shown in Figure 83.

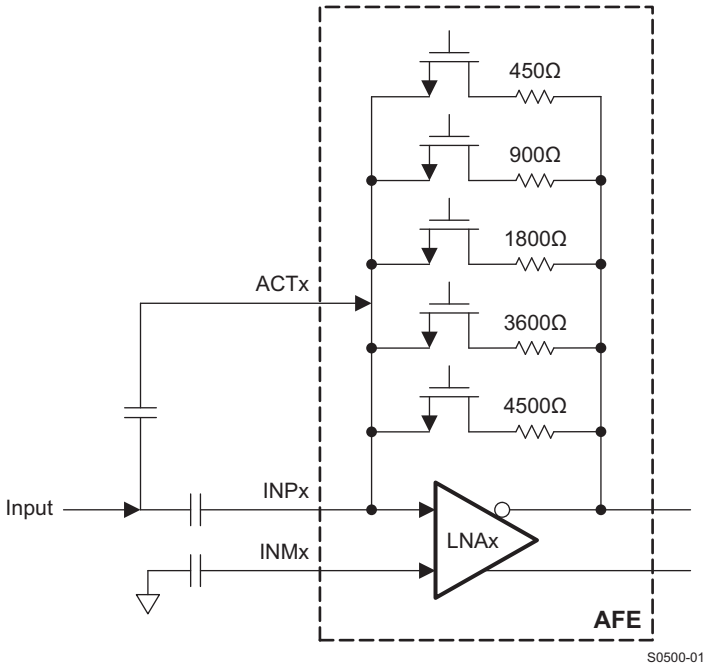


Figure 83. Active Termination Implementation

The AFE5808A device has four pre-settings 50 Ω,100 Ω, 200 Ω, and 400 Ω, which are configurable through the registers. Other termination values can be realized by setting the termination switches shown in Figure 83. Register [52] is used to enable these switches. The input impedance of the LNA under the active termination configuration approximately follows:

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} \quad (6)$$

Table 7 lists the LNA R_{IN}s under different LNA gains. System designers can achieve fine tuning for different probes.

The equivalent input impedance is given by Equation 7, where R_{IN} (8 K) and C_{IN} (20 pF) are the input resistance and capacitance of the LNA.

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} \,//\, C_{IN} \,//\, R_{IN} \quad (7)$$

Therefore the ZIN is frequency dependent and it decreases as frequency increases shown in Figure 10. Since approximately 2 MHz to 10 MHz is the most commonly used frequency range in medical ultrasound, this rolling-off effect does not impact system performance greatly. Active termination can be applied to both CW and TGC modes. Because each ultrasound system includes multiple transducers with different impedances, the flexibility of impedance configuration is a great plus.

Figure 32, Figure 33, and Figure 34 shows the NF under different termination configurations. It indicates that no termination achieves the best noise figure; active termination adds less noise than passive termination. Thus termination topology should be carefully selected based on each use scenario in ultrasound.

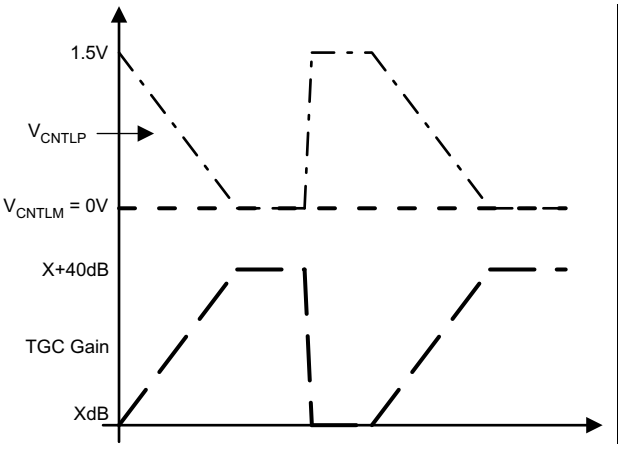
9.2.2.1.4 LNA Gain Switch Response

The LNA gain is programmable through SPI. The gain switching time depends on the SPI speed as well as the LNA gain response time. During the switching, glitches might occur and they can appear as artifacts in images. LNA gain switching in a single imaging line may not be preferred, although digital signal processing might be used here for glitch suppression.

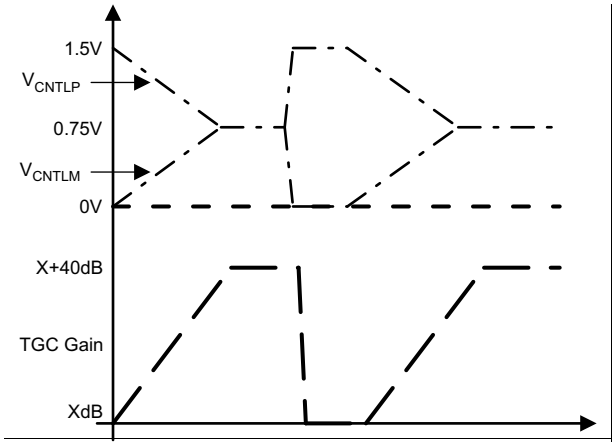
9.2.2.2 Voltage-Controlled-Attenuator

The attenuator in the AFE5808A device is controlled by a pair of differential control inputs, the $V_{CNTLM/P}$ pins. The differential control voltage spans from 0 V to 1.5 V. This control voltage varies the attenuation of the attenuator based on its linear-in-dB characteristic. AFE5808A's maximum attenuation (minimum channel gain) appears at $V_{CNTLP} - V_{CNTLM}$= 1.5 V, and minimum attenuation (maximum channel gain) occurs at $V_{CNTLP} - V_{CNTLM}$ = 0. The typical gain range is 40 dB and remains constant, independent of the PGA setting.

When only single-ended V_{CNTL} signal is available, this 1.5-V_{PP} signal can be applied on the V_{CNTLP} pin with the V_{CNTLM} pin connected to ground. As shown in Figure 84, TGC gain curve is inversely proportional to the $V_{CNTLP} - V_{CNTLM}$.



(a) Single-Ended Input at V_{CNTLP}



(b) Differential Inputs at V_{CNTLP} and V_{CNTLM}

W0004-01

Figure 84. V_{CNTLP} and V_{CNTLM} Configurations

As discussed in the theory of operation, the attenuator architecture uses seven attenuator segments that are equally spaced in order to approximate the linear-in-dB gain-control slope. This approximation results in a monotonic slope; the gain ripple is typically less than ±0.5 dB.

The control voltage input ($V_{CNTLM/P}$ pins) represents a high-impedance input. The $V_{CNTLM/P}$ pins of multiple AFE5808A devices can be connected in parallel with no significant loading effects. When the voltage level (V_{CNTLP}-V_{CNTLM}) is above 1.5 V or below 0 V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level respectively. TI recommends limiting the voltage from –0.3 V to 2 V.

When the AFE5808A device operates in CW mode, the attenuator stage remains connected to the LNA outputs. Therefore, TI recommends powering down the VCA using the PDN_VCA register bit. In this case, V_{CNTLP} – V_{CNTLM} voltage does not matter.

The AFE5808A gain-control input has a –3-dB bandwidth of approximately 800 kHz. This wide bandwidth, although useful in many applications (for example fast V_{CNTL} response), can also allow high-frequency noise to modulate the gain control input and finally affect the Doppler performance. In practice, this modulation can easily be avoided by additional external filtering (RV_{CNTL} and CV_{CNTL}) at $V_{CNTLM/P}$ pins as Figure 75 shows. However, the external filter's cut-off frequency cannot be kept too low as this results in low gain response time. Without external filtering, the gain control response time is typically less than 1 µs to settle within 10% of the final signal level of 1 V_{PP} (–6 dBFS) output as indicated in Figure 51 and Figure 52.

Typical $V_{CNTLM/P}$ signals are generated by an 8 to 12 bit 10 MSPS digital to analog converter (DAC) and a differential operation amplifier. TI's DACs, such as TLV5626 and DAC7821/11 (10 MSPS/ 12 bit), could be used to generate TGC control waveforms. Differential amplifiers with output common mode voltage control (for example THS4130 and OPA1632) can connect the DAC to the $V_{CNTLM/P}$ pins. The buffer amplifier can also be configured as an active filter to suppress low frequency noise. The $V_{CNTLM/P}$ circuit shall achieve low noise in order to prevent the $V_{CNTLM/P}$ noise being modulated to RF signals. TI recommends that $V_{CNTLM/P}$ noise is below 25 nV/√Hz at 1 kHz and 5 nV/√Hz at 50 kHz.In high channel count premium systems, the $V_{CNTLM/P}$ noise requirement is higher as shown in Figure 85.

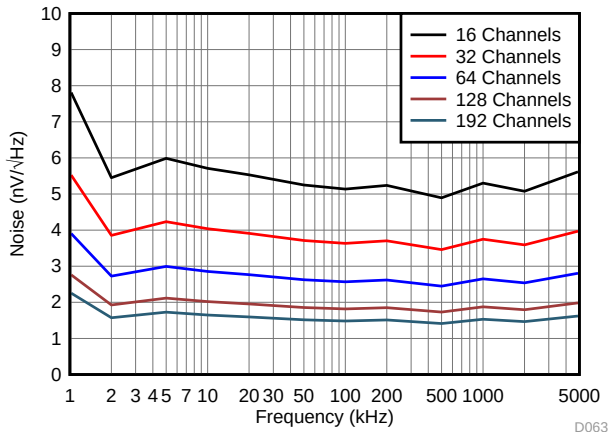


Figure 85. Allowed Noise on the VCNTL Signal Across Frequency and Different Channels

More information can be found in the data sheet, *THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers* (SLOS318), and the application note, *Design for a Wideband Differential Transimpedance DAC Output* (SBAA150). The V_{CNTL} vs Gain curves can be found in Figure 2. Table 16 shows the absolute gain vs V_{CNTL}, which may help program DAC correspondingly.

In PW Doppler and color Doppler modes, V_{CNTL} noise should be minimized to achieve the best close-in phase noise and SNR. Digital V_{CNTL} feature is implemented to address this need in the AFE5808A device. In the digital V_{CNTL} mode, no external V_{CNTL} is needed.

Table 16. V_{CNTLP}–V_{CNTLM} vs Gain Under Different LNA and PGA Gain Settings (Low Noise Mode)

$V_{CNTLP} - V_{CNTLM}$ (V)	Gain (dB) LNA = 12 dB PGA = 24 dB	Gain (dB) LNA = 18 dB PGA = 24 dB	Gain (dB) LNA = 24 dB PGA = 24 dB	Gain (dB) LNA = 12 dB PGA = 30 dB	Gain (dB) LNA = 18 dB PGA = 30 dB	Gain (dB) LNA = 24 dB PGA = 30 dB
0	36.45	42.45	48.45	42.25	48.25	54.25
0.1	33.91	39.91	45.91	39.71	45.71	51.71
0.2	30.78	36.78	42.78	36.58	42.58	48.58
0.3	27.39	33.39	39.39	33.19	39.19	45.19
0.4	23.74	29.74	35.74	29.54	35.54	41.54
0.5	20.69	26.69	32.69	26.49	32.49	38.49
0.6	17.11	23.11	29.11	22.91	28.91	34.91
0.7	13.54	19.54	25.54	19.34	25.34	31.34
0.8	10.27	16.27	22.27	16.07	22.07	28.07
0.9	6.48	12.48	18.48	12.28	18.28	24.28
1	3.16	9.16	15.16	8.96	14.96	20.96
1.1	–0.35	5.65	11.65	5.45	11.45	17.45
1.2	–2.48	3.52	9.52	3.32	9.32	15.32
1.3	–3.58	2.42	8.42	2.22	8.22	14.22
1.4	–4.01	1.99	7.99	1.79	7.79	13.79
1.5	–4	2	8	1.8	7.8	13.8

9.2.2.3 CW Operation

9.2.2.3.1 CW Summing Amplifier

To simplify CW system design, a summing amplifier is implemented in the AFE5808A device to sum and convert 8-channel mixer current outputs to a differential voltage output. Low noise and low power are achieved in the summing amplifier while maintaining the full dynamic range required in CW operation.

This summing amplifier has 5 internal gain adjustment resistors that can provide 32 different gain settings (register 54[4:0], Figure 83 and Table 10). System designers can easily adjust the CW path gain depending on signal strength and transducer sensitivity. For any other gain values, an external resistor option is supported. The gain of the summation amplifier is determined by the ratio between the 500-Ω resistors after LNA and the internal or external resistor network $R_{EXT/INT}$. Thus the matching between these resistors plays a more important role than absolute resistor values. Better than 1% matching is achieved on chip. Due to process variation, the absolute resistor tolerance could be higher. If external resistors are used, the gain error between I/Q channels or among multiple AFEs may increase. TI recommends using internal resistors to set the gain to achieve better gain matching (across channels and multiple AFEs). With the external capacitor C_{EXT}, this summing amplifier has 1st order LPF response to remove high frequency components from the mixers, such as 2f0±fd. Its cut-off frequency is using Equation 8.

$$f_{HP} = \frac{1}{2\pi R_{INT/EXT} C_{EXT}} \quad (8)$$

When different gain is configured through register 54[4:0], the LPF response varies as well.

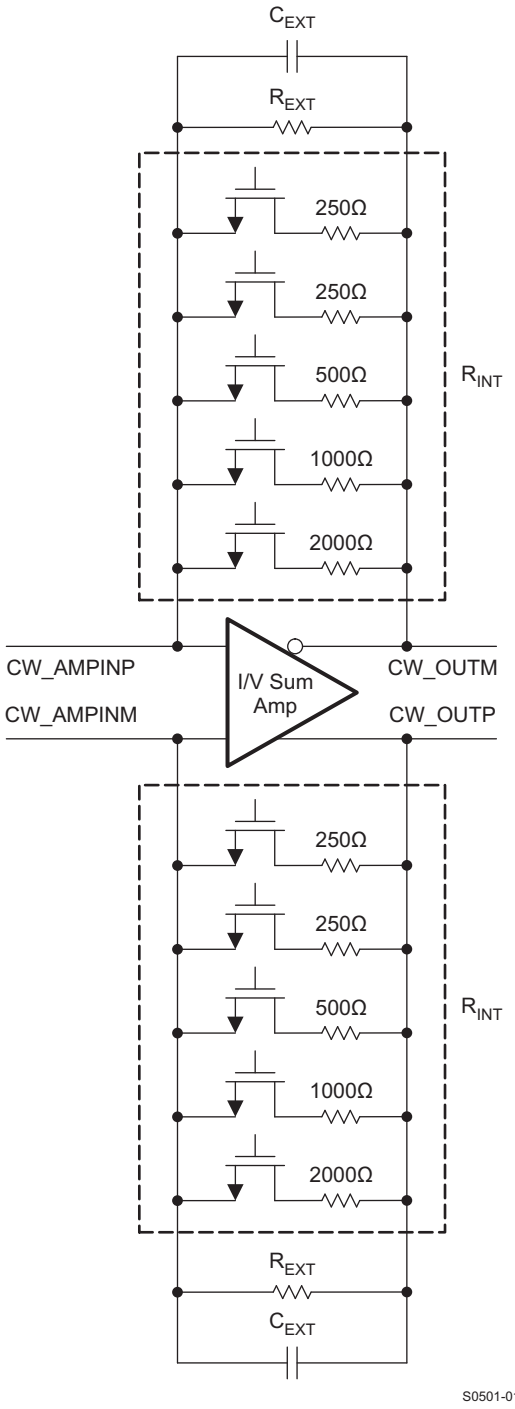


Figure 86. CW Summing Amplifier Block Diagram

Multiple AFE5808A devices are usually utilized in parallel to expand CW beamformer channel count. These AFE5808A devices' CW outputs can be summed and filtered externally further to achieve desired gain and filter response. AC coupling capacitors C_{AC} are required to block the DC component of the CW carrier signal. C_{AC} can vary from 1 µF to 10 µF depending on the desired low frequency Doppler signal from slow blood flow. Multiple AFE5808A devices' I/Q outputs can be summed together with a low noise external differential amplifiers before 16/18-bit differential audio ADCs. TI's ultralow noise differential precision amplifier OPA1632 and THS4130 are suitable devices.

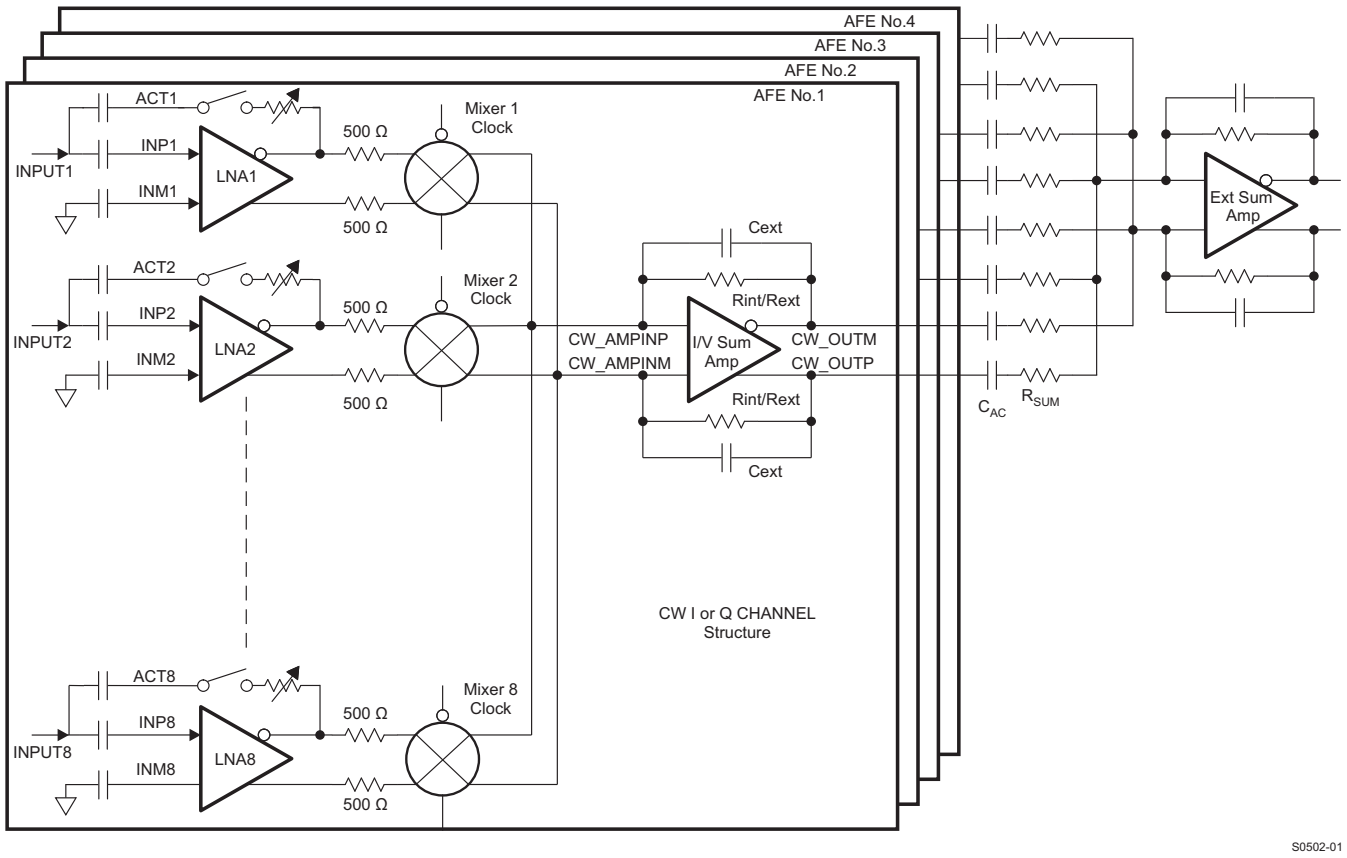


Figure 87. CW Circuit With Multiple AFE5808As

The CW I/Q channels are well matched internally to suppress image frequency components in Doppler spectrum. Low tolerance components and precise operational amplifiers should be used for achieving good matching in the external circuits as well.

NOTE

The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH respectively. Depending on users' CW Doppler complex FFT processing, swapping I/Q channels in FPGA or DSP may be needed in order to get correct blood flow directions.

9.2.2.3.2 CW Clock Selection

The AFE5808A device can accept differential LVDS, LVPECL, and other differential clock inputs as well as single-ended CMOS clock. An internally generated VCM of 2.5 V is applied to CW clock inputs (that is CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X). Since this 2.5-V VCM is different from the one used in standard LVDS or LVPECL clocks, AC coupling is required between clock drivers and the AFE5808A CW clock inputs. When CMOS clock is used, CLKM_1X and CLKM_16X should be tied to ground. Common clock configurations are shown in Figure 88. To achieve good signal integrity, TI recommends appropriate termination.

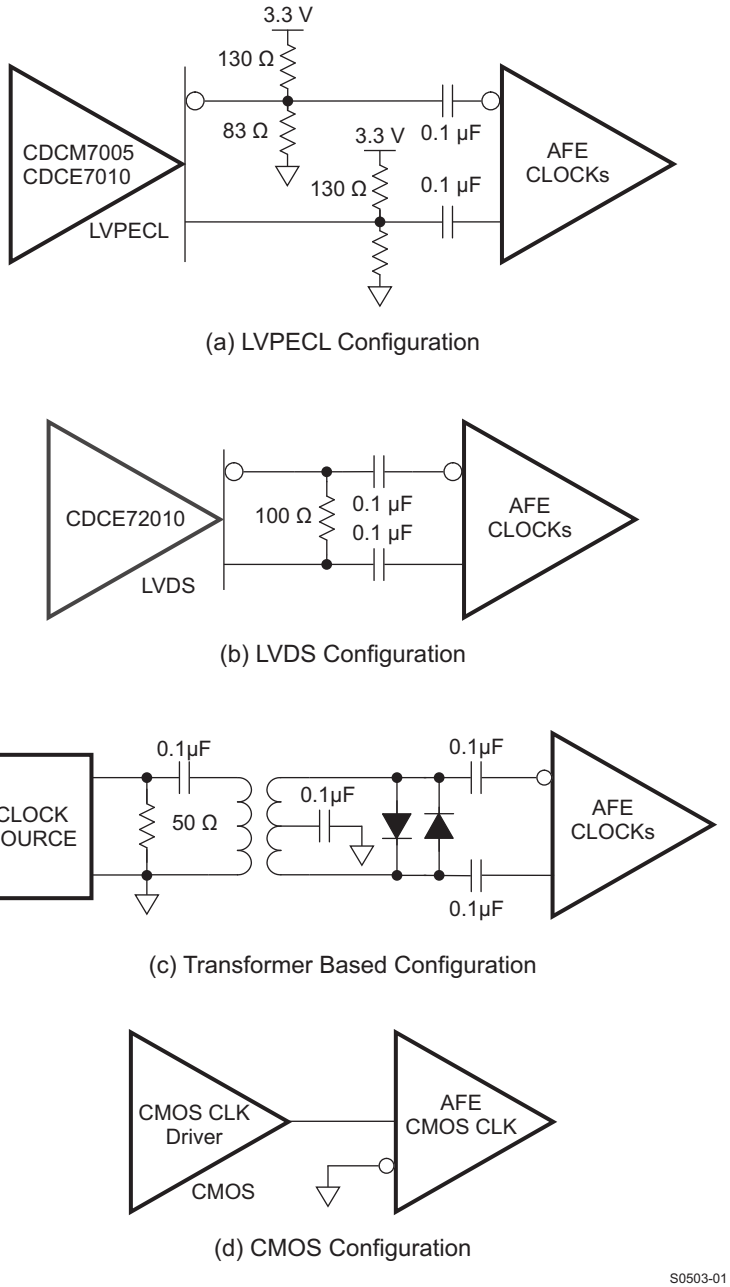


Figure 88. Clock Configurations

The combination of the clock noise and the CW path noise can degrade the CW performance. The internal clocking circuit is designed for achieving excellent phase noise required by CW operation. The phase noise of the AFE5808A CW path is better than 155 dBc/Hz at 1-kHz offset. Consequently the phase noise of the mixer clock inputs needs to be better than 155 dBc/Hz.

In the 16/8/4 × f_{cw} operations modes, low phase noise clock is required for 16/8/4 × f_{cw} clocks (that is CLKP_16X/ CLKM_16X pins) to maintain good CW phase noise performance. The 1 × f_{cw} clock (that is CLKP_1X/ CLKM_1X pins) is only used to synchronize the multiple AFE5808A chips and is not used for demodulation. Thus 1 × f_{cw} clock's phase noise is not a concern. However, in the 1 × f_{cw} operation mode, low phase noise clocks are required for both CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X pins since both of them are used for mixer demodulation. In general, higher slew rate clock has lower phase noise; thus clocks with high amplitude and fast slew rate are preferred in CW operation. In the CMOS clock mode, 5-V CMOS clock can achieve the highest slew rate.

Clock phase noise can be improved by a divider as long as the divider's phase noise is lower than the target phase noise. The phase noise of a divided clock can be improved approximately by a factor of 20logN dB where N is the dividing factor of 16, 8, or 4. If the target phase noise of mixer LO clock 1×f_{cw} is 160 dBc/Hz at 1 kHz off carrier, the 16 × f_{cw} clock phase noise should be better than 160 – 20log16 = 136 dBc/Hz. TI's jitter cleaners LMK048X/CDCM7005/CDCE72010 exceed this requirement and can be selected for the AFE5808A device. In the 4X/1X modes, higher quality input clocks are expected to achieve the same performance since N is smaller. Thus the 16X mode is a preferred mode since it reduces the phase noise requirement for system clock design. In addition, the phase delay accuracy is specified by the internal clock divider and distribution circuit. In the 16X operation mode, the CW operation range is limited to 8 MHz due to the 16X CLK. The maximum clock frequency for the 16X CLK is 128 MHz. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance (for example, the phase noise is degraded by 9 dB at 15 MHz, compared to 2 MHz).

As the channel number in a system increases, clock distribution becomes more complex. It is not preferred to use one clock driver output to drive multiple AFEs since the clock buffer's load capacitance increases by a factor of N. As a result, the falling and rising time of a clock signal is degraded. A typical clock arrangement for multiple AFE5808A devices is shown in Figure 89. Each clock buffer output drives one AFE5808A device to achieve the best signal integrity and fastest slew rate, that is better phase noise performance. When clock phase noise is not a concern, for example, the 1 × f_{cw} clock in the 16/8/4 × f_{cw} operation modes, one clock driver output may excite more than one AFE5808A device. Nevertheless, special considerations must be applied in such a clock distribution network design. In typical ultrasound systems, TI recommends generating all clocks from a same clock source, such as 16 × f_{cw}, 1 × f_{cw} clocks, audio ADC clocks, RF ADC clock, pulse repetition frequency signal, frame clock, and so forth. By doing this, interference due to clock asynchronization can be minimized.

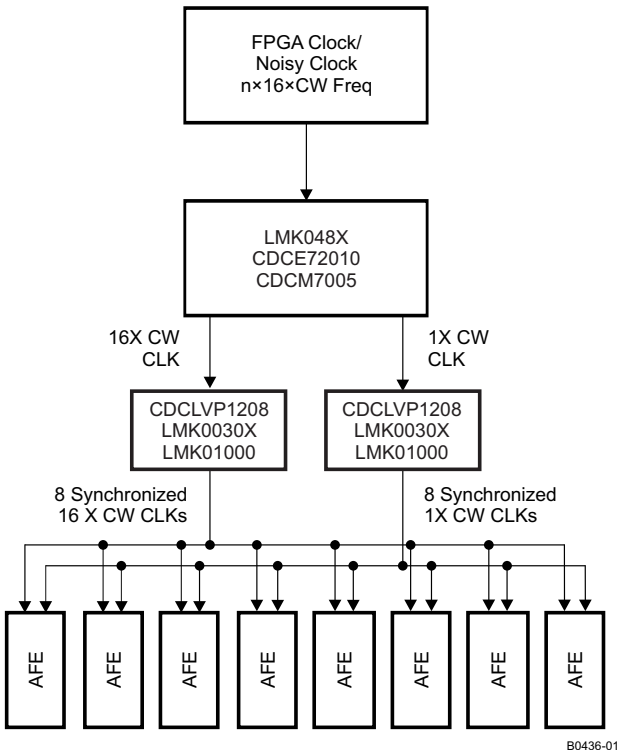


Figure 89. CW Clock Distribution

9.2.2.3.3 CW Supporting Circuits

As a general practice in CW circuit design, in-phase and quadrature channels should be strictly symmetrical by using well matched layout and high accuracy components.

In systems, additional high-pass wall filters (20 Hz to 500 Hz) and low-pass audio filters (10 kHz to 100 kHz) with multiple poles are usually needed. Since CW Doppler signal ranges from 20 Hz to 20 kHz, noise under this range is critical. Consequently low noise audio operational amplifiers are suitable to build these active filters for CW post-processing, for example OPA1632 or OPA2211. More filter design techniques can be found from www.ti.com. TI's active filter design tool http://www.ti.com/lsds/ti/analog/webench/webench-filters.page.

The filtered audio CW I/Q signals are sampled by audio ADCs and processed by DSP or PC. Although CW signal frequency is from 20 Hz to 20 kHz, higher sampling rate ADCs are still preferred for further decimation and SNR enhancement. Due to the large dynamic range of CW signals, high resolution ADCs (≥ 16 bit) are required, such as ADS8413 (2 MSPS/16 bit/92 dBFS SNR) and ADS8472 (1 MSPS/16 bit/95 dBFS SNR). ADCs for in-phase and quadature-phase channels must be strictly matched, not only amplitude matching but also phase matching, to achieve the best I/Q matching. In addition, the in-phase and quadrature ADC channels must be sampled simultaneously.

9.2.2.4 ADC Operation

9.2.2.4.1 ADC Clock Configurations

To ensure that the aperture delay and jitter are the same for all channels, the AFE5808A device uses a clock tree network to generate individual sampling clocks for each channel. The clock, for all the channels, are matched from the source point to the sampling circuit of each of the eight internal ADCs. The variation on this delay is described in the aperture delay parameter of the output interface timing. Its variation is given by the aperture jitter number of the same table.

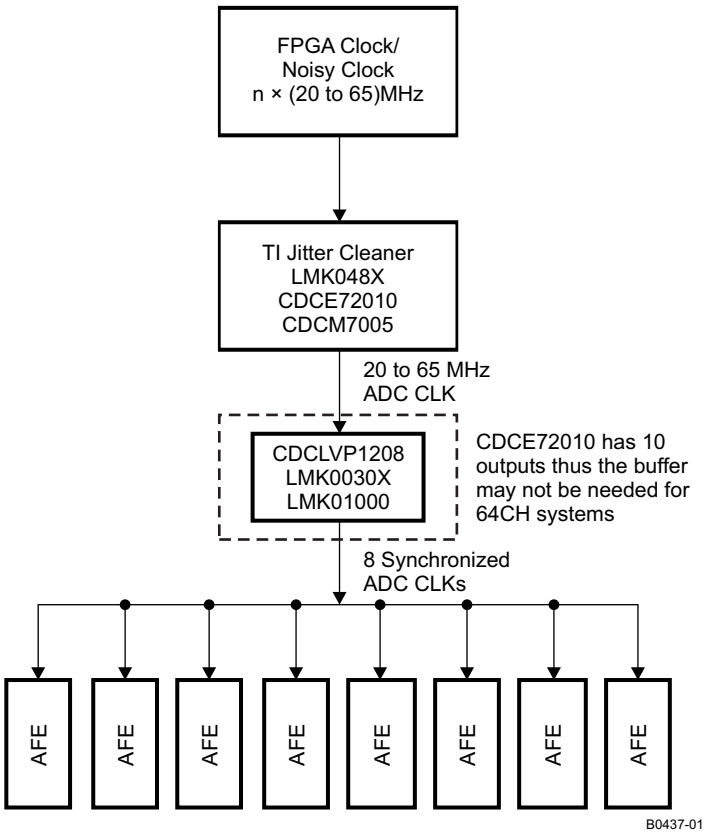


Figure 90. ADC Clock Distribution Network

The AFE5808A ADC clock input can be driven by differential clocks (sine wave, LVPECL or LVDS) or singled clocks (LVCMOS) similar to CW clocks as shown in Figure 88. In the single-end case, TI recommends using low jitter square signals (LVCMOS levels, 1.8-V amplitude). See the TI technical brief, *Clocking High-Speed Data Converters* SLYT075 for further details on the theory.

The jitter cleaner LMK048X/CDCM7005/CDCE72010 is suitable to generate the AFE5808A's ADC clock and ensure the performance for the 14-bit ADC with 77-dBFS SNR. A clock distribution network is shown in Figure 90.

9.2.2.4.2 ADC Reference Circuit

The ADC's voltage reference can be generated internally or provided externally. When the internal reference mode is selected, the REFP/M becomes output pins and should be floated. When 3[15] = 1 and 1[13] = 1, the device is configured to operate in the external reference mode in which the VREF_IN pin should be driven with a 1.4-V reference voltage and REFP/M must be left open. Since the input impedance of the VREF_IN is high, no special drive capability is required for the 1.4-V voltage reference

The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system would have about 12 octal AFEs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the AFEs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips. When the external reference mode is used, a solid reference plane on a printed circuit board can ensure minimal voltage variation across devices. More information on voltage reference design can be found in the TI technical brief, *How the Voltage Reference Affects ADC Performance, Part 2* (SLYT339). The dominant gain variation in the AFE5808A comes from the VCA gain variation. The gain variation contributed by the ADC reference circuit is much smaller than the VCA gain variation. Hence, in most systems, using the ADC internal reference mode is sufficient to maintain good gain matching among multiple AFE5808As. In addition, the internal reference circuit without any external components achieves satisfactory thermal noise and phase noise performance.

9.2.3 Application Curves

Figure 91 shows the output SNR of one AFE channel from VCNTL = 0 V and VCNTL = 1.2 V, respectively, with an input signal at 5 MHz captured at a sample rate of 50 MHz. VCNTL = 0 V represents far field while VCNTL = 1.2 V represents near field. Figure 92 shows the CW phase noise or dyanmic range of a singe AFE channel.

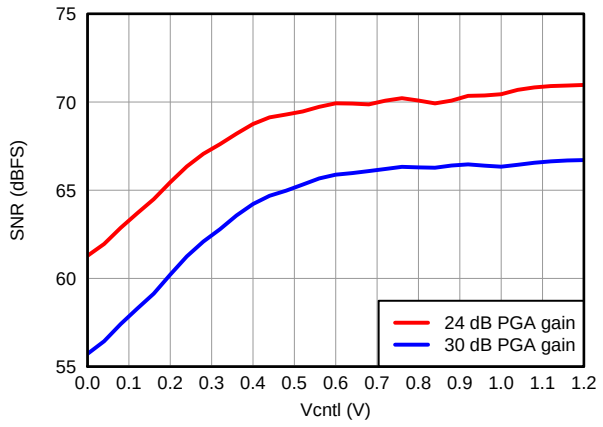


Figure 91. SNR vs VCNTL at 18-dB LNA

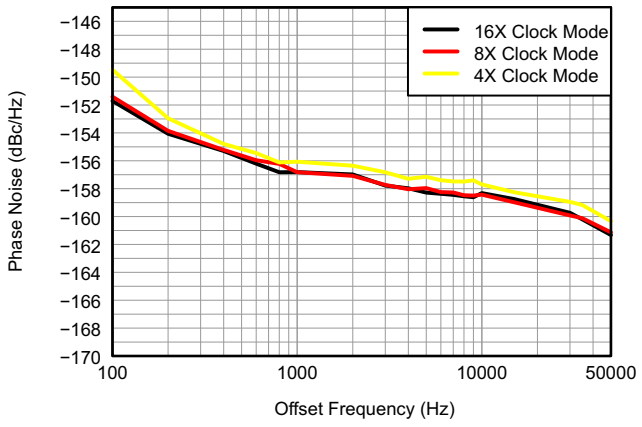


Figure 92. CW Phase Noise at FIN = 2 MHz

9.3 Do's and Don'ts

9.3.1 Driving the Inputs (Analog or Digital) Beyond the Power-Supply Rails

For device reliability, an input must not go more than 300 mV below the ground pins or 300 mV above the supply pins as suggested in the *Absolute Maximum Ratings* table. Exceeding these limits, even on a transient basis, can cause faulty or erratic operation and can impair device reliability.

9.3.2 Driving the Device Signal Input With an Excessively High Level Signal

The device offers consistent and fast overload recovery with a 6-dB overloaded signal. For very large overload signals (> 6 dB of the linear input signal range), TI recommends back-to-back Schottky clamping diodes at the input to limit the amplitude of the input signal. See the *LNA Input Coupling and Decoupling* section for more details.

9.3.3 Driving the VCNTL Signal With an Excessive Noise Source

Noise on the VCNTL signal gets directly modulated with the input signal and causes higher output noise and reduction in SNR performance. Maintain a noise level for the VCNTL signal as discussed in the *Voltage-Controlled-Attenuator* section.

9.3.4 Using a Clock Source With Excessive Jitter, an Excessively Long Input Clock Signal Trace, or Having Other Signals Coupled to the ADC or CW Clock Signal Trace

These situations cause the sampling interval to vary, causing an excessive output noise and a reduction in SNR performance. For a system with multiple devices, the clock tree scheme must be used to apply an ADC or CW clock. See the *Switching Characteristics* section for clock mismatch between devices, which can lead to latency mismatch and reduction in SNR performance. Clocks generated by FPGA may include excessive jitter and must be evaluated carefully before driving ADC or CW circuits.

9.3.5 LVDS Routing Length Mismatch

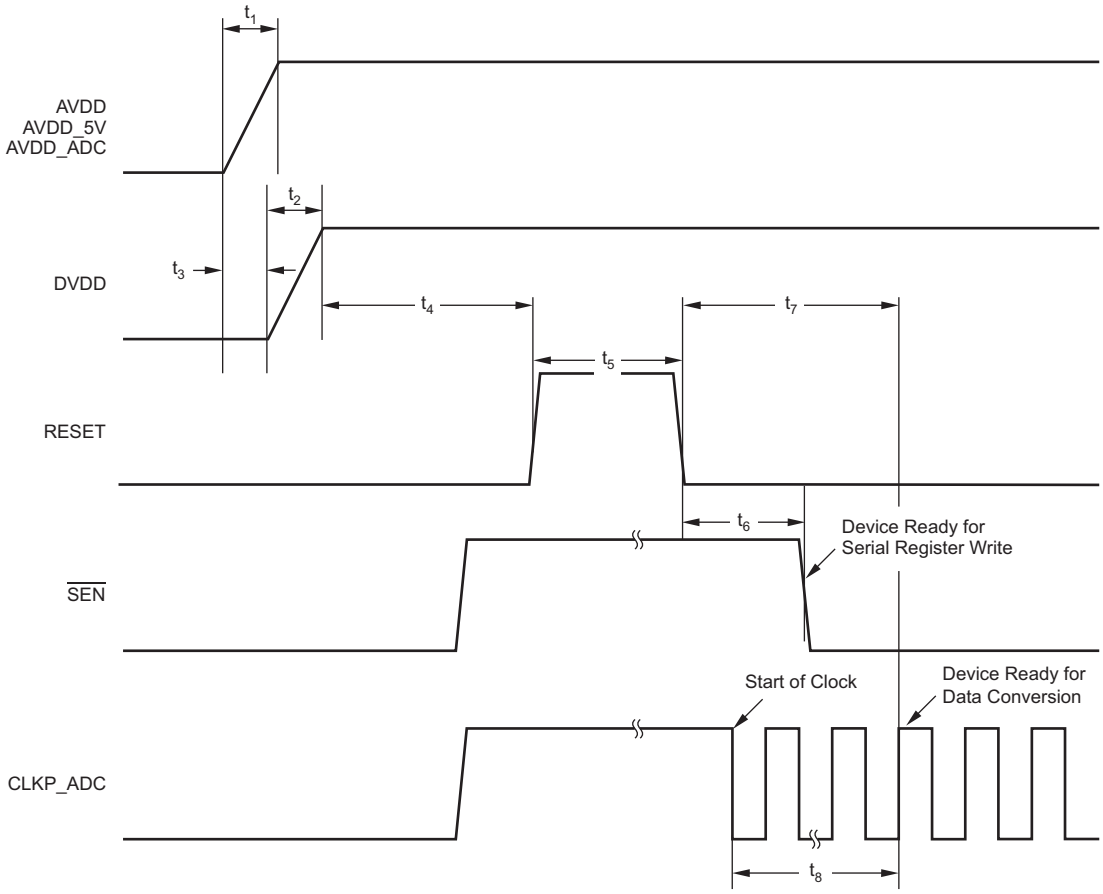
The routing length of all LVDS lines routing to the FPGA must be matched to avoid any timing related issue. For systems with multiple devices, the LVDS serialized data clock (DCLKP, DCLKM) and the frame clock (FCLKP, FCLKM) of each individual device must be used to deserialize the corresponding LVDS serialized data (DnP, DnM).

9.3.6 Failure to Provide Adequate Heat Removal

Use the appropriate thermal parameter listed in the *Thermal Information* table and an ambient, board, or case temperature in order to calculate device junction temperature. A suitable heat removal technique must be used to keep the device junction temperature below the maximum limit of 105°C.

10 Power Supply Recommendations

In a mixed-signal system design, power supply and grounding design plays a significant role. The AFE5808A device distinguishes between two different grounds: AVSS (analog ground) and DVSS (digital ground). In most cases, it should be adequate to lay out the printed-circuit-board (PCB) to use a single ground plane for the AFE5808A device. Take care to partition this ground plane properly between various sections within the system to minimize interactions between analog and digital circuitry. Alternatively, the digital (DVDD) supply set consisting of the DVDD and DVSS pins can be placed on separate power and ground planes. For this configuration, the AVSS and DVSS grounds should be tied together at the power connector in a star layout. In addition, optical isolator or digital isolators, such as ISO7240, can separate the analog portion from the digital portion completely. Consequently they prevent digital noise to contaminate the analog portion. Table 2 lists the related circuit blocks for each power supply. Recommended power up sequence is shown in Figure 93.



10 µs < t1 < 50 ms, 10 µs < t2 < 50 ms, –10 ms < t3 < 10 ms, t4 > 10 ms, t5 > 100 ns, t6 > 100 ns, t7 > 10 ms, and t8 > 100 µs.

The AVDDx and DVDD power-on sequence does not matter as long as –10 ms < t3 < 10 ms. Similar considerations apply while shutting down the device.

Figure 93. Recommended Power-up Sequencing and Reset Timing

Table 17. Supply vs Circuit Blocks

POWER SUPPLY	GROUND	CIRCUIT BLOCKS
AVDD (3.3VA)	AVSS	LNA, attenuator, PGA with current clamp and BPF, reference circuits, CW summing amplifier, CW mixer, VCA SPI
AVDD_5V (5VA)	AVSS	LNA, CW clock circuits, reference circuits
AVDD_ADC (1.8VA)	AVSS	ADC analog and reference circuits
DVDD (1.8VD)	DVSS	LVDS and ADC SPI

All bypassing and power supplies for the AFE5808A should be referenced to their corresponding ground planes. All supply pins should be bypassed with 0.1-µF ceramic chip capacitors (size 0603 or smaller). To minimize the lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors 2.2 µF to 10 µF, effective at lower frequencies) may also be used on the main supply pins. These components can be placed on the PCB in proximity (< 0.5 inch or 12.7 mm) to the AFE5808A device itself.

The AFE5808A device has a number of reference supplies needed to be bypassed, such as CM_BYP, and VHIGH. These pins should be bypassed with at least 1 µF; higher value capacitors can be used for better low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors (size 0402, > 1 µF) and place them as close as possible to the device pins.

High-speed mixed signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer/drivers. For the AFE5808A device, the interaction between the analog and digital supplies within the device is ensured to keep to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductance of the supply and ground pins leads to improved noise suppression. For this reason, multiple pins are used to connect each supply and ground sets. Take care to maintain low inductance properties throughout the design of the PCB layout by using proper planes and layer thickness.

11 Layout

11.1 Layout Guidelines

Proper grounding and bypassing, short lead length, and the use of ground and power-supply planes are particularly important for high-frequency designs. Achieving optimum performance with a high-performance device such as the AFE5808A requires careful attention to the PCB layout to minimize the effects of board parasitics and optimize component placement. A multilayer PCB usually ensures best results and allows convenient component placement. To maintain proper LVDS timing, all LVDS traces should follow a controlled impedance design. In addition, all LVDS trace lengths should be equal and symmetrical; TI recommends to keep trace length variations less than 150 mil (0.150 inch or 3.81 mm).

NOTE

To avoid noise coupling through supply pins, TI recommends to keep sensitive input pins, such as INM, INP, ACT pins aways from the AVDD 3.3 V and AVDD_5V planes. For example, either the traces or vias connected to these pins should NOT be routed across the AVDD 3.3 V and AVDD_5V planes, that is to avoid power planes under INM, INP, and ACT pins.

In addition, appropriate delay matching should be considered for the CW clock path, especially in systems with high channel count. For example, if clock delay is half of the 16x clock period, a phase error of 22.5°C could exist. Thus the timing delay difference among channels contributes to the beamformer accuracy.

Additional details on BGA PCB layout techniques can be found in the Texas Instruments Application Report, *MicroStar BGA Packaging Reference Guide* (SSYZ015), which can be downloaded from www.ti.com.

11.2 Layout Example

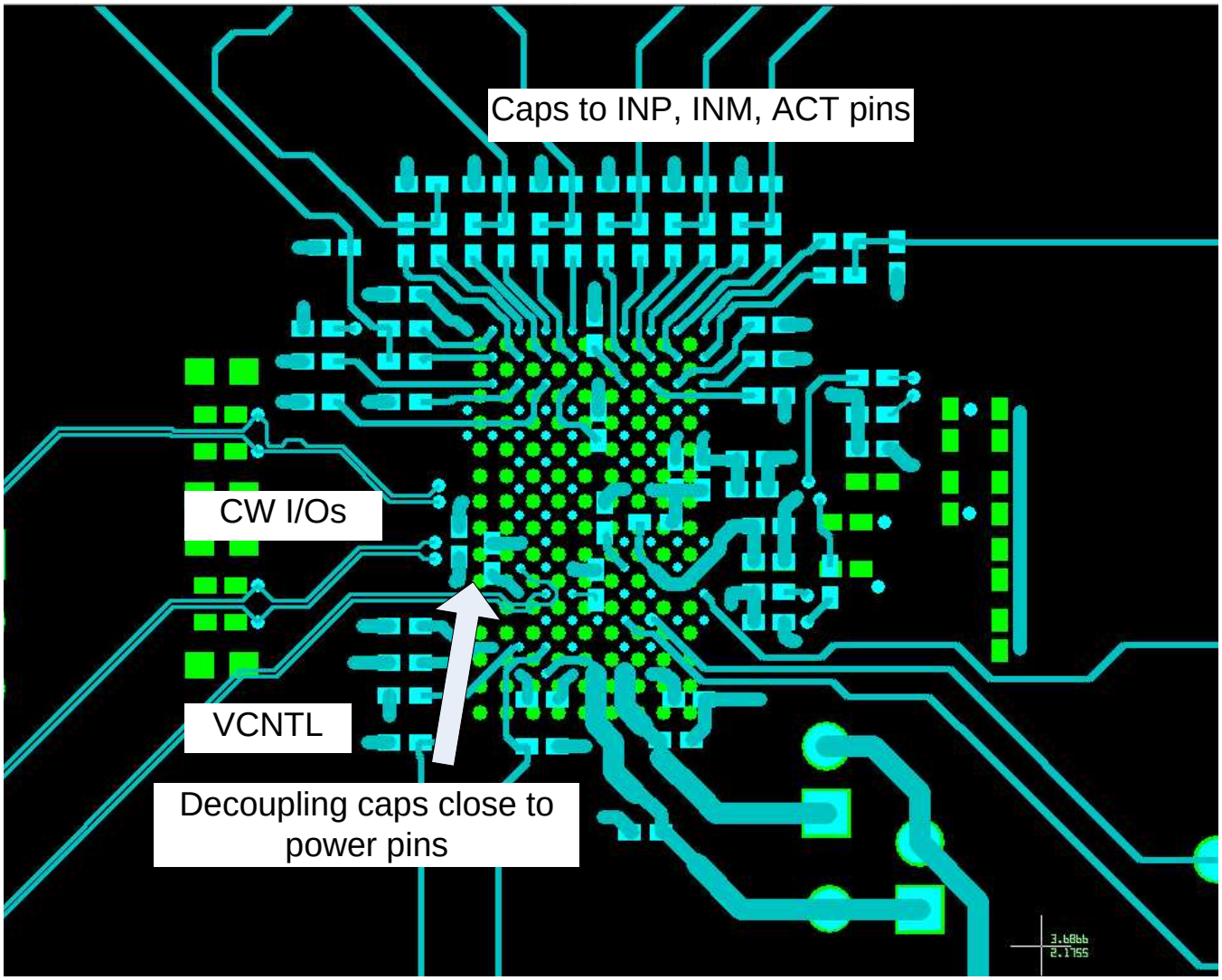


Figure 94. Layout Example: I/O Routing

Layout Example (continued)

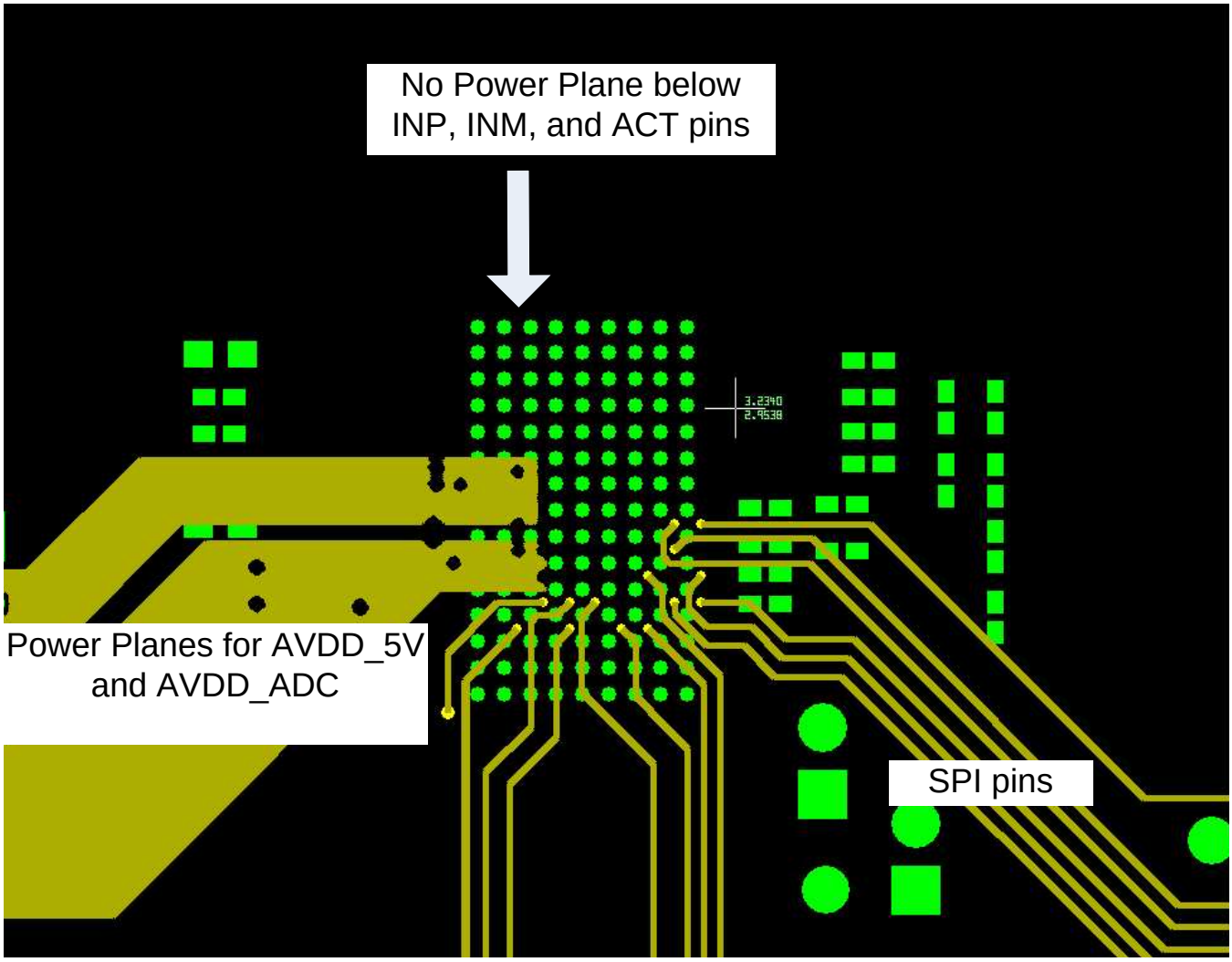


Figure 95. Layout Example: Power Plane

Layout Example (continued)

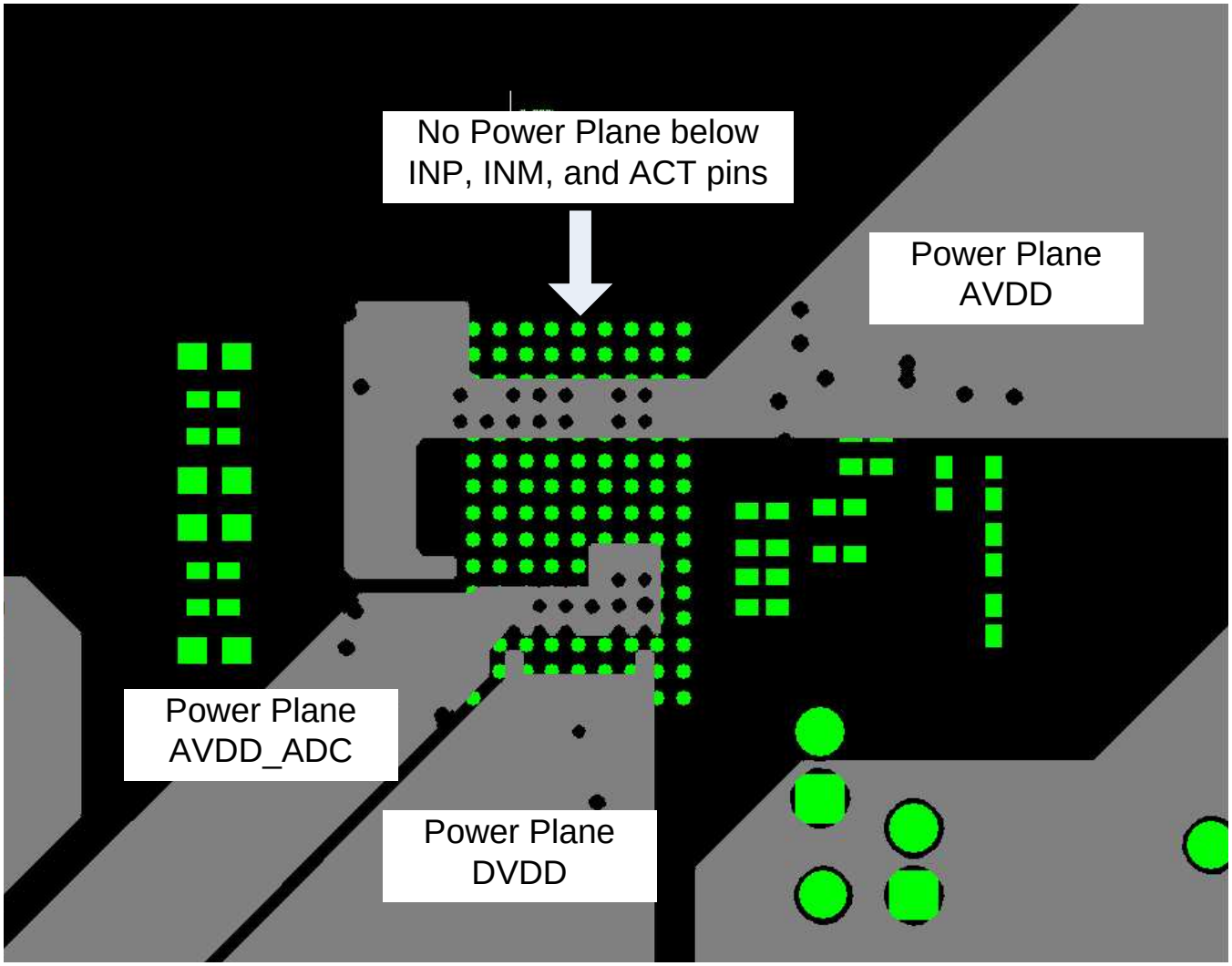


Figure 96. Layout Example: Power Plane

Layout Example (continued)

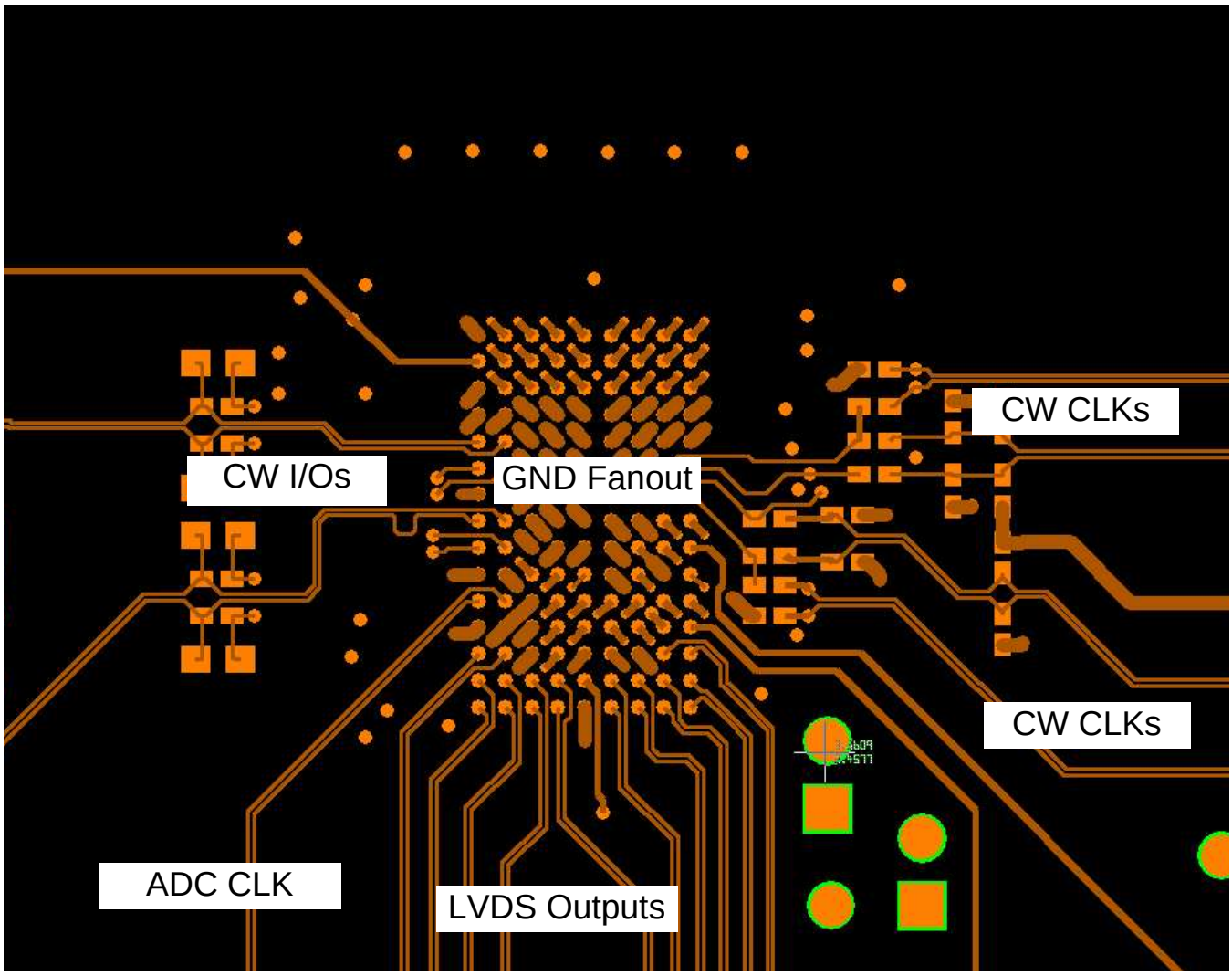


Figure 97. Layout Example: LVDS and CLK I/Os

12 Device and Documentation Support

12.1 Related Documentation

For related documentation see the following:

- *THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers*, SLOS318.
- *Design for a Wideband Differential Transimpedance DAC Output*, SBAA150.
- *Clocking High-Speed Data Converters*, SLYT075.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE5808AZCF	ACTIVE	NFBGA	ZCF	135	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 85	AFE5808A	Samples
HPA01093ZCF	ACTIVE	NFBGA	ZCF	135	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 85	AFE5808A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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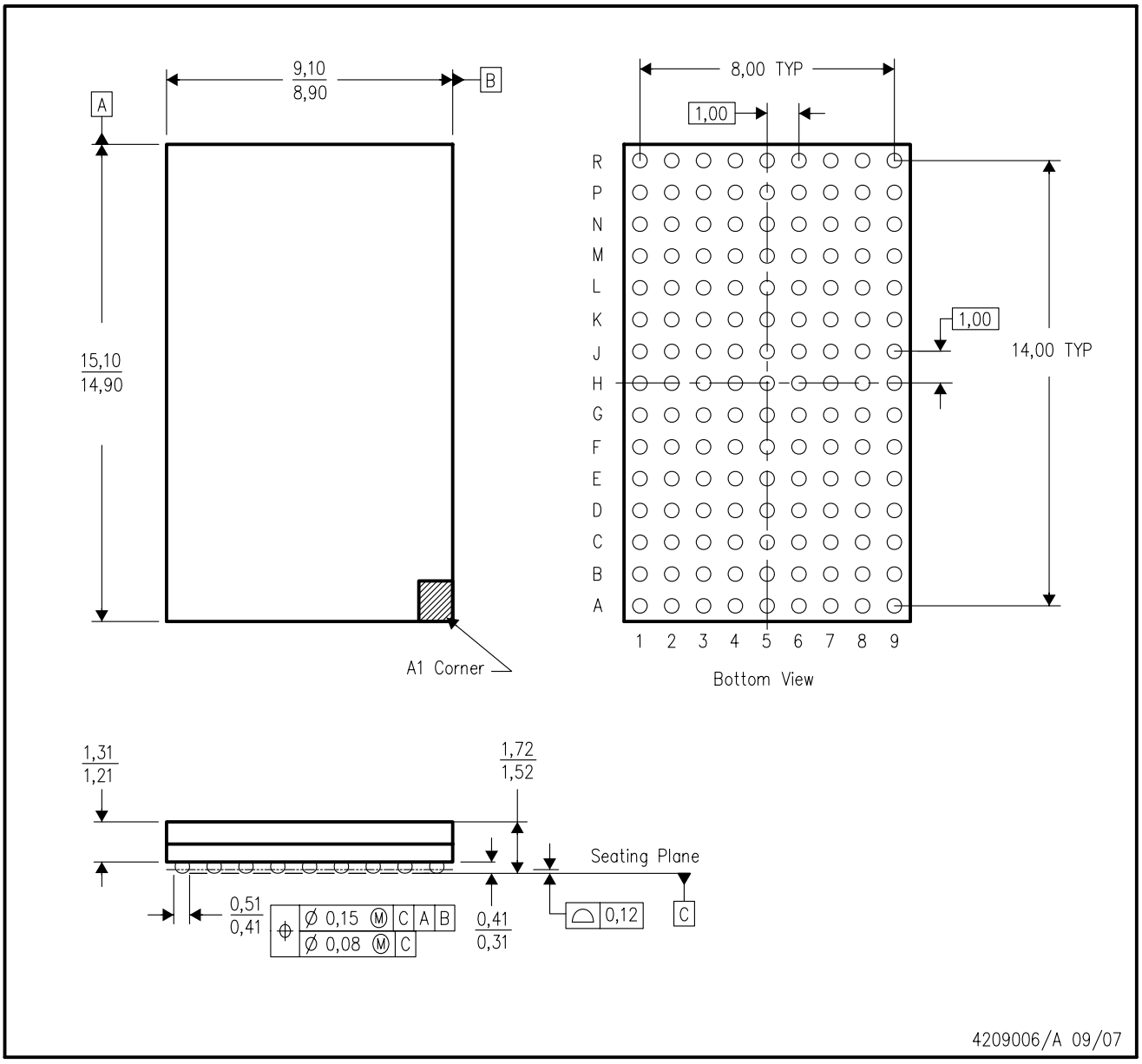
ZCF (R–PBGA–N135) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994 .
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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