CMOS, 170 MHz, Triple, 10-Bit High Speed Video DAC

ADV7123-EP

FEATURES

- 170 MSPS throughput rate
- Triple, 10-bit digital-to-analog converters (DACs)
- SFDR
  - −70 dB at f_{CLK} = 50 MHz; f_{OUT} = 1 MHz
  - −53 dB at f_{CLK} = 140 MHz; f_{OUT} = 40 MHz
- RS-343A-/RS-170-compatible output
- Complementary outputs
- DAC output current range: 2.0 mA to 26.5 mA
- TTL-compatible inputs
- Internal reference: 1.235 V
- Single-supply 3.3 V operation
- 48-lead LFCSP package
- Low power dissipation: 30 mW minimum at 3 V
- Low power standby mode: 6 mW typical at 3 V
- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Digital video systems
- High resolution color graphics
- Digital radio modulation
- Image processing
- Instrumentation
- Video signal reconstruction

FUNCTIONAL BLOCK DIAGRAM

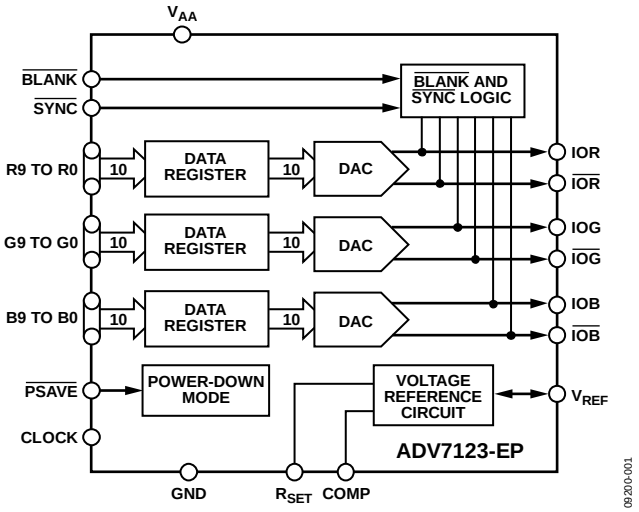

Figure 1.

GENERAL DESCRIPTION

The ADV7123-EP is a triple, high speed digital-to-analog converter (DAC) on a single monolithic chip. It consists of three high speed, 10-bit video DACs with complementary outputs, a standard TTL input interface, and a high impedance, analog output current source.

The ADV7123-EP has three separate 10-bit-wide input ports. A single 3.3 V power supply and clock are the only components required to make the part functional. The ADV7123-EP has additional video control signals: composite $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$. The ADV7123-EP also has a power save mode.

The ADV7123-EP is fabricated in a 5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The ADV7123-EP is available in a 48-lead LFCSP package.

Full details about this enhanced product are available in the ADV7123 data sheet, which should be consulted in conjunction with this data sheet.

PRODUCT HIGHLIGHTS

1. Guaranteed monotonic to 10 bits.
2. Compatible with a wide variety of high resolution color graphics systems, including RS-343A and RS-170.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

7/10—Revision 0: Initial Version

SPECIFICATIONS

V_{AA} = 3.0 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[1] unless otherwise noted; $T_{J\,MAX}$ = 110°C.

Table 1.

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments[1]
STATIC PERFORMANCE					
Resolution (Each DAC)			10	Bits	R_{SET} = 680 Ω
Integral Nonlinearity (BSL)	−1	+0.5	+1	LSB	R_{SET} = 680 Ω
Differential Nonlinearity	−1	+0.25	+1	LSB	R_{SET} = 680 Ω
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}		0.8		V	
Input Current, I_{IN}	−1		+1	μA	V_{IN} = 0.0 V or V_{DD}
$\overline{PSAVE}$ Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		26.5	mA	Green DAC, $\overline{SYNC}$ = high
	2.0		18.5	mA	RGB DAC, $\overline{SYNC}$ = low
DAC-to-DAC Matching		1.0		%	
Output Compliance Range, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		70		kΩ	
Output Capacitance, C_{OUT}		10		pF	
Offset Error		0	0	% FSR	Tested with DAC output = 0 V
Gain Error[3]		0		% FSR	FSR = 17.62 mA
VOLTAGE REFERENCE, EXTERNAL					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
VOLTAGE REFERENCE, INTERNAL					
Voltage Reference, V_{REF}		1.235		V	
POWER DISSIPATION					
Digital Supply Current[4]		2.2	5.0	mA	f_{CLK} = 50 MHz
		6.5	12.0	mA	f_{CLK} = 140 MHz
		7.5	13.5	mA	f_{CLK} = 170 MHz
Analog Supply Current		67	72	mA	R_{SET} = 560 Ω
		8		mA	R_{SET} = 4933 Ω
Standby Supply Current		2.1	5.0	mA	$\overline{PSAVE}$ = low, digital and control inputs at V_{DD}
Power Supply Rejection Ratio		0.1	0.5	%/%	

[1] Temperature range T_{MIN} to T_{MAX}: −55°C to +105°C.
[2] These maximum/minimum specifications are guaranteed by characterization over the 3.0 V to 3.6 V range.
[3] Gain error = {(Measured (FSC)/Ideal (FSC) − 1) × 100}, where Ideal (FSC) = $V_{REF}/R_{SET} \times K \times$ (0x3FFH) and K = 7.9896.
[4] Digital supply is measured with a continuous clock that has data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

DYNAMIC SPECIFICATIONS

V_{AA} = 3.0 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 680 Ω, C_L = 10 pF. All specifications are at T_A = 25°C, unless otherwise noted; $T_{J\,MAX}$ = 110°C.

Table 2.

Parameter[1]	Min	Typ	Max	Unit
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist[2]				
Single-Ended Output				
f_{CLK} = 50 MHz; f_{OUT} = 1.00 MHz		67		dBc
f_{CLK} = 50 MHz; f_{OUT} = 2.51 MHz		67		dBc
f_{CLK} = 50 MHz; f_{OUT} = 5.04 MHz		63		dBc
f_{CLK} = 50 MHz; f_{OUT} = 20.2 MHz		55		dBc
f_{CLK} = 100 MHz; f_{OUT} = 2.51 MHz		62		dBc
f_{CLK} = 100 MHz; f_{OUT} = 5.04 MHz		60		dBc
f_{CLK} = 100 MHz; f_{OUT} = 20.2 MHz		54		dBc
f_{CLK} = 100 MHz; f_{OUT} = 40.4 MHz		48		dBc
f_{CLK} = 140 MHz; f_{OUT} = 2.51 MHz		57		dBc
f_{CLK} = 140 MHz; f_{OUT} = 5.04 MHz		58		dBc
f_{CLK} = 140 MHz; f_{OUT} = 20.2 MHz		52		dBc
f_{CLK} = 140 MHz; f_{OUT} = 40.4 MHz		41		dBc
Double-Ended Output				
f_{CLK} = 50 MHz; f_{OUT} = 1.00 MHz		70		dBc
f_{CLK} = 50 MHz; f_{OUT} = 2.51 MHz		70		dBc
f_{CLK} = 50 MHz; f_{OUT} = 5.04 MHz		65		dBc
f_{CLK} = 50 MHz; f_{OUT} = 20.2 MHz		54		dBc
f_{CLK} = 100 MHz; f_{OUT} = 2.51 MHz		67		dBc
f_{CLK} = 100 MHz; f_{OUT} = 5.04 MHz		63		dBc
f_{CLK} = 100 MHz; f_{OUT} = 20.2 MHz		58		dBc
f_{CLK} = 100 MHz; f_{OUT} = 40.4 MHz		52		dBc
f_{CLK} = 140 MHz; f_{OUT} = 2.51 MHz		62		dBc
f_{CLK} = 140 MHz; f_{OUT} = 5.04 MHz		61		dBc
f_{CLK} = 140 MHz; f_{OUT} = 20.2 MHz		55		dBc
f_{CLK} = 140 MHz; f_{OUT} = 40.4 MHz		53		dBc
Spurious-Free Dynamic Range Within a Window				
Single-Ended Output				
f_{CLK} = 50 MHz; f_{OUT} = 1.00 MHz; 1 MHz Span		77		dBc
f_{CLK} = 50 MHz; f_{OUT} = 5.04 MHz; 2 MHz Span		73		dBc
f_{CLK} = 140 MHz; f_{OUT} = 5.04 MHz; 4 MHz Span		64		dBc
Double-Ended Output				
f_{CLK} = 50 MHz; f_{OUT} = 1.00 MHz; 1 MHz Span		74		dBc
f_{CLK} = 50 MHz; f_{OUT} = 5.00 MHz; 2 MHz Span		73		dBc
f_{CLK} = 140 MHz; f_{OUT} = 5.00 MHz; 4 MHz Span		60		dBc
Total Harmonic Distortion				
f_{CLK} = 50 MHz; f_{OUT} = 1.00 MHz				
T_A = 25°C		66		dBc
T_{MIN} to T_{MAX}		65		dBc
f_{CLK} = 50 MHz; f_{OUT} = 2.00 MHz		64		dBc
f_{CLK} = 100 MHz; f_{OUT} = 2.00 MHz		64		dBc
f_{CLK} = 140 MHz; f_{OUT} = 2.00 MHz		55		dBc

Parameter[1]	Min	Typ	Max	Unit
DAC PERFORMANCE				
Glitch Impulse		10		pV-sec
DAC-to-DAC Crosstalk[3]		23		dB
Data Feedthrough[4, 5]		22		dB
Clock Feedthrough[4, 5]		33		dB

[1] These maximum/minimum specifications are guaranteed by characterization over the 3.0 V to 3.6 V range.
[2] The ADV7123-EP exhibits high performance when operating with an internal voltage reference, V_{REF}.
[3] DAC-to-DAC crosstalk is measured by holding one DAC high while the other two DACs are making low-to-high and high-to-low transitions.
[4] Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.
[5] TTL input values are 0 V to 3 V, with input rise/fall times of 3 ns, measured at the 10% and 90% points. Timing reference points are 50% for inputs and outputs.

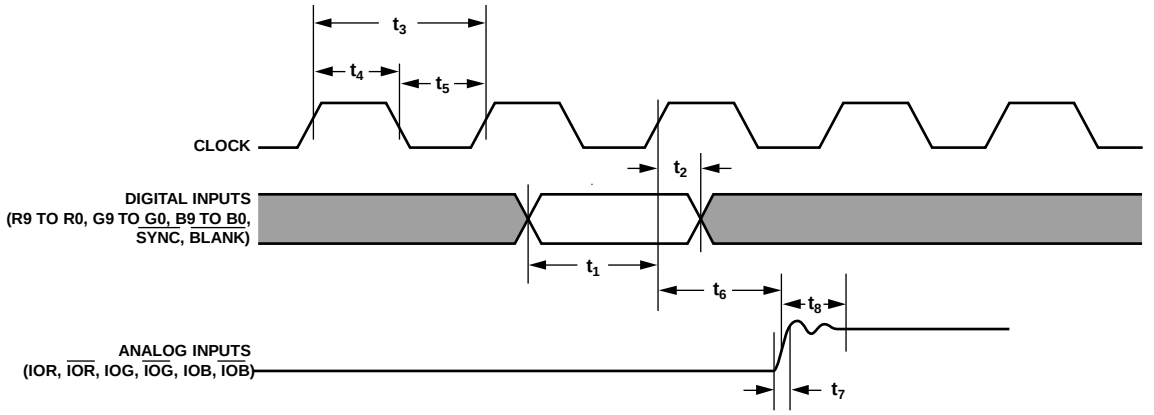
TIMING SPECIFICATIONS

V_{AA} = 3.0 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[1] unless otherwise noted; $T_{J\,MAX}$ = 110°C.

Table 3.

Parameter[2, 3]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG OUTPUTS						
Analog Output Delay	t_6		7.5		ns	
Analog Output Rise/Fall Time[4]	t_7		1.0		ns	
Analog Output Transition Time[5]	t_8		15		ns	
Analog Output Skew[6]	t_9		1	2	ns	
CLOCK CONTROL						
CLOCK Frequency[7]	f_{CLK}			170	MHz	
Data and Control Setup	t_1	0.68			ns	
Data and Control Hold	t_2	2.9			ns	
CLOCK Period	t_3	5.88			ns	
CLOCK Pulse Width High[6]	t_4	2.6			ns	f_{CLK_MAX} = 170 MHz
CLOCK Pulse Width Low[6]	t_5	2.6			ns	f_{CLK_MAX} = 170 MHz
Pipeline Delay[6]	t_{PD}	1.0	1.0	1.0	Clock cycles	
$\overline{\text{PSAVE}}$ Up Time[6]	t_{10}		4	10	ns	

[1] Temperature range T_{MIN} to T_{MAX}: −55°C to +105°C.
[2] These maximum/minimum specifications are guaranteed by characterization over the 3.0 V to 3.6 V range.
[3] Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}).
[4] Rise time was measured from the 10% to 90% point of zero to full-scale transition, fall time from the 90% to 10% point of a full-scale transition.
[5] Measured from the 50% point of full-scale transition to within 2% of the final output value.
[6] Guaranteed by characterization.
[7] f_{CLK} maximum specification production tested at 125 MHz.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION.
3. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{AA} to GND	7 V
Voltage on Any Digital Pin	GND − 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A)	−55°C to +105°C
Storage Temperature (T_S)	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase Soldering (1 Minute)	220°C
I_{OUT} to GND[1]	0 V to V_{AA}

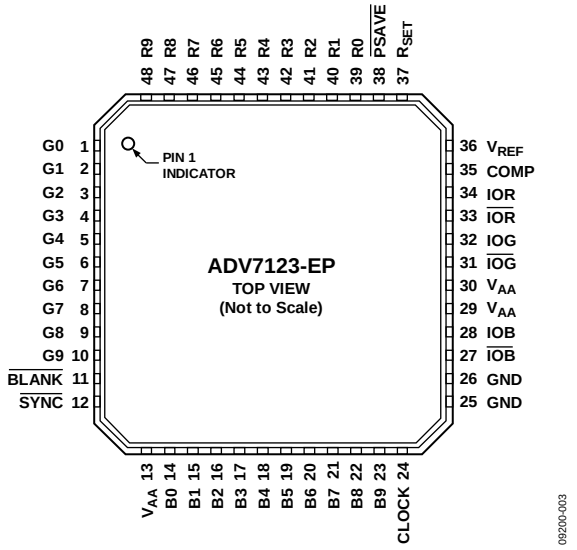
[1] Analog output short circuit to any power supply or common GND can be of an indefinite duration.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE ON THE UNDERSIDE OF THE PACKAGE MUST BE SOLDERED TO THE GROUND PLANE TO INCREASE THE RELIABILITY OF THE SOLDER JOINTS AND TO MAXIMIZE THE THERMAL CAPABILITY OF THE PACKAGE.

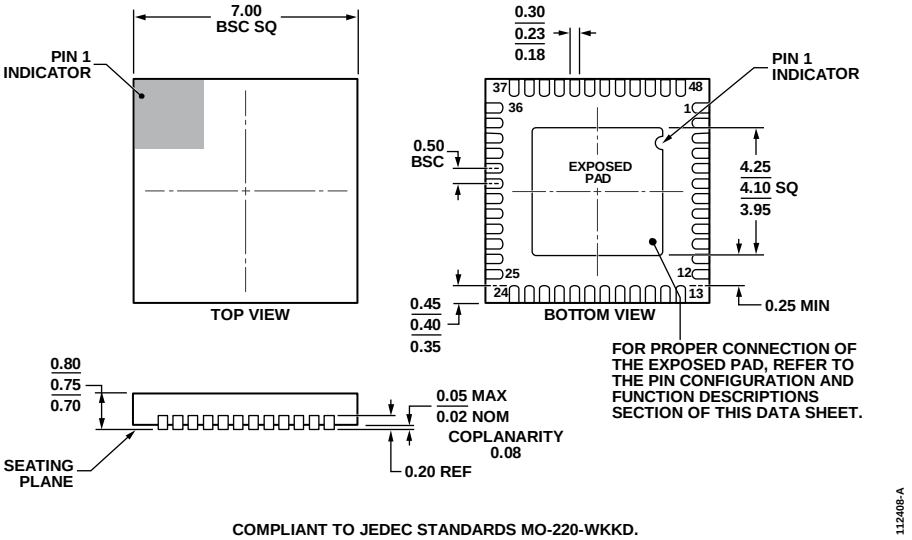
Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 10, 14 to 23, 39 to 48	G0 to G9, B0 to B9, R0 to R9	Red, Green, and Blue Pixel Data Inputs (TTL Compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0, and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular printed circuit board (PCB) power or ground plane.
11	$\overline{\text{BLANK}}$	Composite Blank Control Input (TTL Compatible). A Logic 0 on this control input drives the analog outputs—IOR, IOB, and IOG—to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a Logic 0, the R0 to R9, G0 to G9, and B0 to B9 pixel inputs are ignored.
12	$\overline{\text{SYNC}}$	Composite Sync Control Input (TTL Compatible). A Logic 0 on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source. The sync current is internally connected to the IOG analog output. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK. If sync information is not required on the green channel, the $\overline{\text{SYNC}}$ input should be tied to Logic 0.
13, 29, 30	V_{AA}	Analog Power Supply (3.3 V ± 10%). All V_{AA} pins on the ADV7123-EP must be connected.
24	CLOCK	Clock Input (TTL Compatible). The rising edge of CLOCK latches the R0 to R9, G0 to G9, B0 to B9, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ pixel and control inputs. Typically, the CLOCK input is the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
25, 26	GND	Ground. The GND pins must be connected.
27, 31, 33	$\overline{\text{IOB}}$, $\overline{\text{IOG}}$, $\overline{\text{IOR}}$	Differential Red, Green, and Blue Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75 Ω coaxial cable. If the complementary outputs are not required, these outputs should be tied to ground.
28, 32, 34	IOB, IOG, IOR	Red, Green, and Blue Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
35	COMP	Compensation Pin for the Internal Reference Amplifier. A 0.1 µF ceramic capacitor must be connected between COMP and V_{AA}.
36	V_{REF}	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V). The V_{REF} pin is normally terminated to V_{AA} through a 0.1 µF capacitor. However, the ADV7123-EP can be overdriven by an external 1.23 V reference (AD1580), if required.

Pin No.	Mnemonic	Description
37	R_{SET}	A resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. For nominal video levels into a doubly terminated 75 Ω load, R_{SET} = 530 Ω. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by R_{SET} (Ω) = 11,445 × V_{REF} (V)/*IOG* (mA) The relationship between R_{SET} and the full-scale output current on IOR, IOG, and IOB is given by *IOG* (mA) = 11,445 × V_{REF} (V)/R_{SET} (Ω) ($\overline{\text{SYNC}}$ being asserted) *IOR, IOB* (mA) = 7989.6 × V_{REF} (V)/R_{SET} (Ω) The equation for IOG is the same as that for IOR and IOB when $\overline{\text{SYNC}}$ is not being used, that is, $\overline{\text{SYNC}}$ is tied permanently low.
38	$\overline{\text{PSAVE}}$	Power Save Control Pin. Reduced power consumption is available on the ADV7123-EP when this pin is active.
EP	Exposed Pad	The exposed paddle on the underside of the package must be soldered to the ground plane to increase the reliability of the solder joints and to maximize the thermal capability of the package.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD.

Figure 4. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
7 mm × 7 mm Body, Very Very Thin Quad
(CP-48-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Speed Option	Package Description	Package Option
ADV7123SCP170EP-RL	−55°C to +105°C	170 MHz	48-Lead LFCSP_WQ	CP-48-5

[1] Available in 3.3 V version only.

NOTES

NOTES

D09200-0-7/10(0)