# Triple-Channel Digital Isolator with Programmable Default Output

# ADuM1310

## FEATURES

- Pb-free, 16-lead, wide body SOIC package
- Low power operation
  - 5 V operation
    - 1.0 mA per channel max @ 0 Mbps to 2 Mbps
    - 3.5 mA per channel max @ 10 Mbps
  - 3 V operation
    - 0.7 mA per channel max @ 0 Mbps to 2 Mbps
    - 2.1 mA per channel max @ 10 Mbps
- 3 V/5 V level translation
- High temperature operation: 105°C
- Up to 10 Mbps data rate (NRZ)
- Programmable default output state
- Safety and regulatory approvals
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE certificate of conformity
    - DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01
    - DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000
    - $V_{IORM}$ = 560 V peak

## APPLICATIONS

- General-purpose, unidirectional, multichannel isolation

## GENERAL DESCRIPTION

The ADuM1310[1] is a unidirectional, triple-channel digital isolator based on Analog Devices, Inc. *i*Coupler® technology. Combining high speed CMOS and monolithic coreless transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical concerns that arise with optocouplers, such as uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects, are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discretes is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices run at one-tenth to one-sixth the power consumption of optocouplers at comparable signal data rates.

The ADuM1310 isolator provides three independent isolation channels at data rates up to 10 Mbps. It operates with the supply voltage of either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. This product also has a default output control pin. This allows the user to define the logic state the outputs are to adopt in the absence of the input $V_{DD1}$ power. Unlike other optocoupler alternatives, the ADuM1310 has a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

## FUNCTIONAL BLOCK DIAGRAM

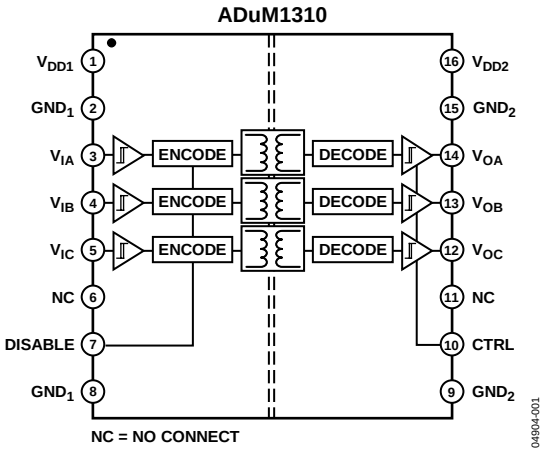


*Figure 1.*

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and other pending patents.

**Rev. E**




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**10/04—Data Sheet Changed from Rev. Sp0 to Rev. SpA**

Changes to Table 5 ..... 9

**6/04—Revision Sp0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V OPERATION

4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 5 V; all voltages are relative to their respective ground.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Total Supply Current, Three Channels[1] | | | | | | |
| $V_{DD1}$ Supply Current, Quiescent | $I_{DD1 (Q)}$ | | 2.4 | 3.2 | mA | $V_{IA} = V_{IB} = V_{IC} = V_{ID} = 0$ |
| $V_{DD2}$ Supply Current, Quiescent | $I_{DD2 (Q)}$ | | 1.2 | 1.6 | mA | $V_{IA} = V_{IB} = V_{IC} = V_{ID} = 0$ |
| $V_{DD1}$ Supply Current, 10 Mbps Data Rate | $I_{DD1 (10)}$ | | 6.6 | 9.0 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current, 10 Mbps Data Rate | $I_{DD2 (10)}$ | | 2.1 | 3.0 | mA | 5 MHz logic signal frequency |
| Input Currents | $I_{IA}$, $I_{IB}$, $I_{IC}$, $I_{ID}$, $I_{CTRL}$, $I_{DISABLE}$ | −10 | +0.01 | +10 | μA | 0 ≤ $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$, $V_{DISABLE}$ ≤ $V_{DD1}$, 0 ≤ $V_{CTRL}$ ≤ $V_{DD2}$ |
| Logic High Input Threshold | $V_{IH}$ | | | 2.0 | V | |
| Logic Low Input Threshold | $V_{IL}$ | 0.8 | | | V | |
| Logic High Output Voltages | $V_{OAH}$, $V_{OBH}$, $V_{OCH}$, $V_{ODH}$ | $V_{DD1}$, $V_{DD2}$ − 0.4 | 4.8 | | V | $I_{Ox}$ = −4 mA, $V_{Ix} = V_{IxH}$ |
| Logic Low Output Voltages | $V_{OAL}$, $V_{OBL}$, $V_{OCL}$, $V_{ODL}$ | | 0.2 | 0.4 | V | $I_{Ox}$ = +4 mA, $V_{Ix} = V_{IxL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| Minimum Pulse Width[2] | PW | | | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[3] | | 10 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | 20 | 30 | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4] | PWD | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew[5] | $t_{PSK}$ | | | 30 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching[6] | $t_{PSKCD}$ | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Output Rise/Fall Time (10% to 90%) | $t_R/t_F$ | | 2.5 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output[7] | $\|CM_H\|$ | 25 | 35 | | kV/μs | $V_{Ix} = V_{DD1}/V_{DD2}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output[7] | $\|CM_L\|$ | 25 | 35 | | kV/μs | $V_{Ix}$ = 0 V, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | 1.2 | | Mbps | |
| Input Enable Time[8] | $t_{ENABLE}$ | | | 2.0 | μs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 or $V_{DD1}$ |
| Input Disable Time[8] | $t_{DISABLE}$ | | | 5.0 | μs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 or $V_{DD1}$ |
| Input Dynamic Supply Current per Channel[9] | $I_{DDI (D)}$ | | 0.19 | | mA/Mbps | |
| Output Dynamic Supply Current per Channel[9] | $I_{DDO (D)}$ | | 0.05 | | mA/Mbps | |

[1] Supply current values are for all four channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 4 through Figure 6 for information on the per-channel supply current as a function of the data rate for unloaded and loaded conditions. See Figure 7 and Figure 8 for total $I_{DD1}$ and $I_{DD2}$ supply currents as a function of the data rate for the ADuM1310 channel configurations.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] $t_{PHL}$ propagation delay is measured from the 50% level of the falling edge of the $V_{Ix}$ signal to the 50% level of the falling edge of the $V_{Ox}$ signal. $t_{PLH}$ propagation delay is measured from the 50% level of the rising edge of the $V_{Ix}$ signal to the 50% level of the rising edge of the $V_{Ox}$ signal.

[5] $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ and/or $t_{PLH}$ that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels within the same component.

[7] $CM_H$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ > 0.8 $V_{DD2}$. $CM_L$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL logic state (see Table 9).

[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 4 through Figure 6 for information on the per-channel supply current as a function of the data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

## ELECTRICAL CHARACTERISTICS—3 V OPERATION

2.7 V ≤ $V_{DD1}$ ≤ 3.6 V, 2.7 V ≤ $V_{DD2}$ ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 3.0 V; all voltages are relative to their respective ground.

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| ADuM1310, Total Supply Current, Three Channels[1] | | | | | | |
| $V_{DD1}$ Supply Current, Quiescent | $I_{DD1 (Q)}$ | | 1.2 | 1.6 | mA | $V_{IA}$ = $V_{IB}$ = $V_{IC}$ = $V_{ID}$ = 0 |
| $V_{DD2}$ Supply Current, Quiescent | $I_{DD2 (Q)}$ | | 0.8 | 1.0 | mA | $V_{IA}$ = $V_{IB}$ = $V_{IC}$ = $V_{ID}$ = 0 |
| $V_{DD1}$ Supply Current, 10 Mbps Data Rate | $I_{DD1 (10)}$ | | 3.4 | 4.9 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current, 10 Mbps Data Rate | $I_{DD2 (10)}$ | | 1.1 | 1.3 | mA | 5 MHz logic signal frequency |
| Input Currents | $I_{IA}$, $I_{IB}$, $I_{IC}$, $I_{ID}$, $I_{CTRL}$, $I_{DISABLE}$ | −10 | +0.01 | +10 | µA | 0 ≤ $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$, $V_{DISABLE}$ ≤ $V_{DD1}$, 0 ≤ $V_{CTRL}$ ≤ $V_{DD2}$ |
| Logic High Input Threshold | $V_{IH}$ | | | 1.6 | V | |
| Logic Low Input Threshold | $V_{IL}$ | 0.4 | | | V | |
| Logic High Output Voltages | $V_{OAH}$, $V_{OBH}$, $V_{OCH}$, $V_{ODH}$ | $V_{DD1}$, $V_{DD2}$ − 0.4 | 2.8 | | V | $I_{Ox}$ = −4 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltages | $V_{OAL}$, $V_{OBL}$, $V_{OCL}$, $V_{ODL}$ | | 0.2 | 0.4 | V | $I_{Ox}$ = +4 mA, $V_{Ix}$ = $V_{IxL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| Minimum Pulse Width[2] | PW | | | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[3] | | 10 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | 20 | 30 | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4] | PWD | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew (Equal Temperature)[5] | $t_{PSK}$ | | | 30 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching[6] | $t_{PSKCD}$ | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Output Rise/Fall Time (10% to 90%) | $t_R$/$t_F$ | | 2.5 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output[7] | $\|CM_H\|$ | 25 | 35 | | kV/µs | $V_{Ix}$ = $V_{DD1}$/$V_{DD2}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output[7] | $\|CM_L\|$ | 25 | 35 | | kV/µs | $V_{Ix}$ = 0 V, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Refresh Rate | $f_r$ | | 1.1 | | Mbps | |
| Input Enable Time[8] | $t_{ENABLE}$ | | | 2.0 | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 or $V_{DD1}$ |
| Input Disable Time[8] | $t_{DISABLE}$ | | | 5.0 | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 or $V_{DD1}$ |
| Input Dynamic Supply Current per Channel[9] | $I_{DDI (D)}$ | | 0.10 | | mA/Mbps | |
| Output Dynamic Supply Current per Channel[9] | $I_{DDO (D)}$ | | 0.03 | | mA/Mbps | |

[1] Supply current values are for all channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 4 through Figure 6 for information on the per-channel supply current as a function of the data rate for unloaded and loaded conditions. See Figure 7 through Figure 8 for total $I_{DD1}$ and $I_{DD2}$ supply currents as a function of the data rate.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[4] $t_{PHL}$ propagation delay is measured from the 50% level of the falling edge of the $V_{Ix}$ signal to the 50% level of the falling edge of the $V_{Ox}$ signal. $t_{PLH}$ propagation delay is measured from the 50% level of the rising edge of the $V_{Ix}$ signal to the 50% level of the rising edge of the $V_{Ox}$ signal.

[5] $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ and/or $t_{PLH}$ that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[6] Channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels within the same component.

[7] $CM_H$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ > 0.8 $V_{DD2}$. $CM_L$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[8] Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL logic state (see Table 9).

[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 4 through Figure 6 for information on the per-channel supply current as a function of the data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

## ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

5 V/3 V operation[1]: 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 2.7 V ≤ $V_{DD2}$ ≤ 3.6 V; 3 V/5 V operation: 2.7 V ≤ $V_{DD1}$ ≤ 3.6 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A$ = 25°C; $V_{DD1}$ = 3.0 V, $V_{DD2}$ = 5 V; or $V_{DD1}$ = 5 V, $V_{DD2}$ = 3.0 V.

**Table 3.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| ADuM1310, Total Supply Current, Three Channels[2] | | | | | | |
| $V_{DD1}$ Supply Current, Quiescent | $I_{DDI (Q)}$ | | | | | |
| 5 V/3 V Operation | | | 2.4 | 3.2 | mA | $V_{IA} = V_{IB} = V_{IC} = V_{ID} = 0$ |
| 3 V/5 V Operation | | | 1.2 | 1.6 | mA | $V_{IA} = V_{IB} = V_{IC} = V_{ID} = 0$ |
| $V_{DD2}$ Supply Current, Quiescent | $I_{DDO (Q)}$ | | | | | |
| 5 V/3 V Operation | | | 0.8 | 1.0 | mA | $V_{IA} = V_{IB} = V_{IC} = V_{ID} = 0$ |
| 3 V/5 V Operation | | | 1.2 | 1.6 | mA | $V_{IA} = V_{IB} = V_{IC} = V_{ID} = 0$ |
| $V_{DD1}$ Supply Current, 10 Mbps Data Rate | $I_{DD1 (10)}$ | | | | | |
| 5 V/3 V Operation | | | 6.5 | 8.2 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 3.4 | 4.9 | mA | 5 MHz logic signal frequency |
| $V_{DD2}$ Supply Current, 10 Mbps Data Rate | $I_{DD2 (10)}$ | | | | | |
| 5 V/3 V Operation | | | 1.1 | 1.3 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 1.9 | 2.2 | mA | 5 MHz logic signal frequency |
| Input Currents | $I_{IA}$, $I_{IB}$, $I_{IC}$, $I_{ID}$, $I_{CTRL}$, $I_{DISABLE}$ | −10 | +0.01 | +10 | μA | $0 \le V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{DISABLE} \le V_{DD1}$, $0 \le V_{CTRL} \le V_{DD2}$ |
| Logic High Input Threshold | $V_{IH}$ | | | | | |
| 5 V/3 V Operation | | | | 2.0 | V | |
| 3 V/5 V Operation | | | | 1.6 | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | | | |
| 5 V/3 V Operation | | 0.8 | | | V | |
| 3 V/5 V Operation | | 0.4 | | | V | |
| Logic High Output Voltages | $V_{OAH}$, $V_{OBH}$, $V_{OCH}$, $V_{ODH}$ | $V_{DD1}/V_{DD2}$ − 0.4 | $V_{DD1}/V_{DD2}$ − 0.2 | | V | $I_{Ox}$ = −4 μA, $V_{Ix} = V_{IxH}$ |
| Logic Low Output Voltages | $V_{OAL}$, $V_{OBL}$, $V_{OCL}$, $V_{ODL}$ | | 0.2 | 0.4 | V | $I_{Ox}$ = +4 μA, $V_{Ix} = V_{IxL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| Minimum Pulse Width[3] | PW | | | 100 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Maximum Data Rate[4] | | 10 | | | Mbps | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay[5] | $t_{PHL}$, $t_{PLH}$ | 20 | 30 | 50 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[5] | PWD | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L$ = 15 pF, CMOS signal levels |
| Propagation Delay Skew[6] | $t_{PSK}$ | | | 30 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Channel-to-Channel Matching[7] | $t_{PSKCD}$ | | | 5 | ns | $C_L$ = 15 pF, CMOS signal levels |
| Output Rise/Fall Time (10% to 90%) | $t_R/t_f$ | | | | | |
| 5 V/3 V Operation | | | 3.0 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| 3 V/5 V Operation | | | 2.5 | | ns | $C_L$ = 15 pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output[8] | $\lvert CM_H \rvert$ | 25 | 35 | | kV/μs | $V_{Ix} = V_{DD1}/V_{DD2}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output[8] | $\lvert CM_L \rvert$ | 25 | 35 | | kV/μs | $V_{Ix}$ = 0 V, $V_{CM}$ = 1000 V, transient magnitude = 800 V |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Refresh Rate | $f_r$ | | | | | |
| 5 V/3 V Operation | | | 1.2 | | Mbps | |
| 3 V/5 V Operation | | | 1.1 | | Mbps | |
| Input Enable Time[9] | $t_{ENABLE}$ | | | 2.0 | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 or $V_{DD1}$ |
| Input Disable Time[9] | $t_{DISABLE}$ | | | 5.0 | µs | $V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$ = 0 or $V_{DD1}$ |
| Input Dynamic Supply Current per Channel[10] | $I_{DDI (D)}$ | | | | | |
| 5 V/3 V Operation | | | 0.19 | | mA/Mbps | |
| 3 V/5 V Operation | | | 0.10 | | mA/Mbps | |
| Output Dynamic Supply Current per Channel[10] | $I_{DDO (D)}$ | | | | | |
| 5 V/3 V Operation | | | 0.03 | | mA/Mbps | |
| 3 V/5 V Operation | | | 0.05 | | mA/Mbps | |

[1] All voltages are relative to their respective ground.

[2] Supply current values are for all channels combined running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 4 through Figure 6 for information on the per-channel supply current as a function of the data rate for unloaded and loaded conditions. See Figure 7 through Figure 8 for total $I_{DD1}$ and $I_{DD2}$ supply currents as a function of the data rate.

[3] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[4] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[5] $t_{PHL}$ propagation delay is measured from the 50% level of the falling edge of the $V_{Ix}$ signal to the 50% level of the falling edge of the $V_{Ox}$ signal. $t_{PLH}$ propagation delay is measured from the 50% level of the rising edge of the $V_{Ix}$ signal to the 50% level of the rising edge of the $V_{Ox}$ signal.

[6] $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ and/or $t_{PLH}$ that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[7] Channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels within the same component.

[8] $CM_H$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. $CM_L$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[9] Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL logic state (see Truth Table – Table 9).

[10] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 4 through Figure 6 for information on the per-channel supply current as a function of the data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

## PACKAGE CHARACTERISTICS

**Table 4.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resistance (Input-to-Output)[1] | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input-to-Output)[2] | $C_{I-O}$ | | 2.2 | | pF | f = 1 MHz |
| Input Capacitance[2] | $C_I$ | | 4.0 | | pF | |
| IC Junction-to-Case Thermal Resistance, Side 1 | $\theta_{JCI}$ | | 33 | | °C/W | Thermocouple located at center of package underside |
| IC Junction-to-Case Thermal Resistance, Side 2 | $\theta_{JCO}$ | | 28 | | °C/W | Thermocouple located at center of package underside |

[1] Device considered a 2-terminal device. Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 shorted together and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

**Table 5.**

| Parameter | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | | 2500 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 7.7 min | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 8.1 min | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 min | mm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1) |

## DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS

The ADuM1310 isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits. The * marking on packages denotes DIN EN 60747-5-2 approval for 560 V peak working voltage. Category I through Category IV listed in the characteristic column are per DIN EN 60747-5-2 definition.

**Table 6.**

| Description | Symbol | Characteristic | Unit |
|---|---|---|---|
| Installation Classification per DIN VDE 0110 | | | |
| For Rated Mains Voltage ≤150 V rms | | I to IV | |
| For Rated Mains Voltage ≤300 V rms | | I to III | |
| For Rated Mains Voltage ≤400 V rms | | I to II | |
| Climatic Classification | | 40/105/21 | |
| Pollution Degree (DIN VDE 0110, Table 1) | | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 560 | V peak |
| Input-to-Output Test Voltage, Method b1 | $V_{PR}$ | 1050 | V peak |
| $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, $t_m$ = 1 sec, Partial Discharge <5 pC | | | |
| Input-to-Output Test Voltage, Method A | $V_{PR}$ | | |
| After Environmental Tests Subgroup 1 | | | |
| $V_{IORM} \times 1.6 = V_{PR}$, $t_m$ = 60 sec, Partial Discharge <5 pC | | 896 | V peak |
| After Input and/or Safety Test Subgroup 2/3 | | | |
| $V_{IORM} \times 1.2 = V_{PR}$, $t_m$ = 60 sec, Partial Discharge <5 pC | | 672 | V peak |
| Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR}$ = 10 sec) | $V_{TR}$ | 4000 | V peak |
| Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure; see Figure 2) | | | |
| Case Temperature | $T_S$ | 150 | °C |
| Side 1 Current | $I_{S1}$ | 265 | mA |
| Side 2 Current | $I_{S2}$ | 335 | mA |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | $>10^9$ | Ω |

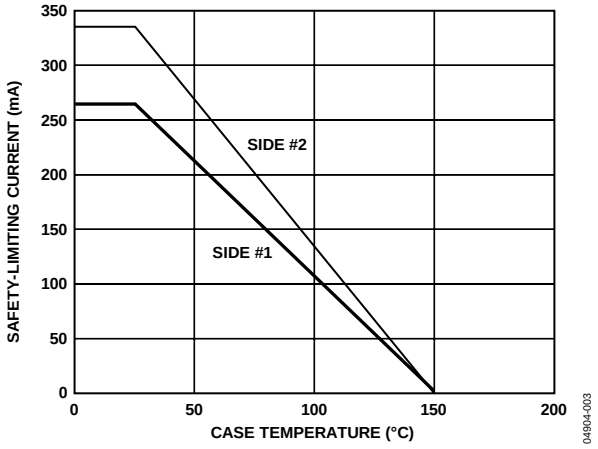



*Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN EN 60747-5-2*

## RECOMMENDED OPERATING CONDITIONS

**Table 7.**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | –40 | +105 | °C |
| Supply Voltages[1] | $V_{DD1}$, $V_{DD2}$ | 2.7 | 5.5 | V |
| Input Signal Rise and Fall Times | | | 1.0 | ms |

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 8.**

| Parameter | Rating |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Operating Temperature | −40°C to +105°C |
| Supply Voltages[1] | −0.5 V to +6.5 V |
| Input Voltage[1, 2] | −0.5 V to $V_{DDI}$ + 0.5 V |
| Output Voltage[1, 2] | −0.5 $V_{DDO}$ + 0.5 V to $V_{DDO}$ + 0.5 V |
| Average Output Current per Pin[3] | |
| Side 1 | −18 mA to +18 mA |
| Side 2 | −22 mA to +22 mA |
| Common-Mode Transients[4] | −100 kV/µs to +100 kV/µs |

[1] All voltages are relative to their respective ground.
[2] $V_{DDI}$ and $V_{DDO}$ refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 2 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

## REGULATORY INFORMATION

In accordance with UL1577, each ADuM1310 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 µA).

In accordance with DIN EN 60747-5-2, each ADuM1310 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC).

The ADuM1310 is approved by the following organizations:

**UL:** Recognized under 1577 Component Recognition Program.

**CSA:** Approved under CSA Component Acceptance Notice #5A.

**VDE:** Certified according to
DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, and
DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Table 9. Truth Table (Positive Logic)**

| $V_{IX}$ Input[1] | CTRL Input | $V_{DISABLE}$ State | $V_{DD1}$ State[1] | $V_{DD2}$ State[1] | $V_{OX}$ Output[1] | Notes |
|---|---|---|---|---|---|---|
| H | X | L or NC | Powered | Powered | H | Normal operation, data is high. |
| L | X | L or NC | Powered | Powered | L | Normal operation, data is low. |
| X | H or NC | H | X | Powered | H | Inputs disabled. Outputs are in the default state as determined by CTRL. |
| X | L | H | X | Powered | L | Inputs disabled. Outputs are in the default state as determined by CTRL. |
| X | H or NC | X | Unpowered | Powered | H | Input unpowered. Outputs are in the default state as determined by CTRL. Outputs return to input state within 1 µs of $V_{DD1}$ power restoration. See the Power-Up/Power-Down Considerations section for more details. |
| X | L | X | Unpowered | Powered | L | Input unpowered. Outputs are in the default state as determined by CTRL. Outputs return to input state within 1 µs of $V_{DD1}$ power restoration. See the Power-Up/Power-Down Considerations section for more details. |
| X | X | X | Powered | Unpowered | Z | Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1 µs of $V_{DD2}$ power restoration. See the Power-Up/Power-Down Considerations section for more details. |

[1] $V_{IX}$ and $V_{OX}$ refer to the input and output signals of a given channel (A, B, C, or D).

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

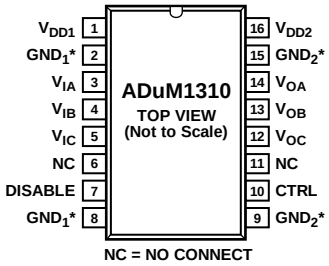



*Figure 3. Pin Configuration*

**Table 10. ADuM1310 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V. |
| 2 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected; connecting both pins to $GND_1$ is recommended. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{IC}$ | Logic Input C. |
| 6 | NC | No Connect. |
| 7 | DISABLE | Input Disable. Disables the isolator inputs and refreshes. Outputs take on logic state determined by CTRL. |
| 8 | $GND_1$ | Ground 1. Ground reference for Isolator Side 1. Pin 8 and Pin 2 are internally connected; connecting both pins to $GND_1$ is recommended. |
| 9 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected; connecting both pins to $GND_2$ is recommended. |
| 10 | CTRL | Default Output Control. Controls the logic state the outputs take on when the input power is off. $V_{OA}$, $V_{OB}$, and $V_{OC}$ outputs are high when CTRL is high or disconnected and $V_{DD1}$ is off. $V_{OA}$, $V_{OB}$, and $V_{OC}$ outputs are low when CTRL is low and $V_{DD1}$ is off. When $V_{DD1}$ power is on, this pin has no effect. |
| 11 | NC | No Connect. |
| 12 | $V_{OC}$ | Logic Output C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected; connecting both pins to $GND_2$ is recommended. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V. |

# TYPICAL PERFORMANCE CHARACTERISTICS

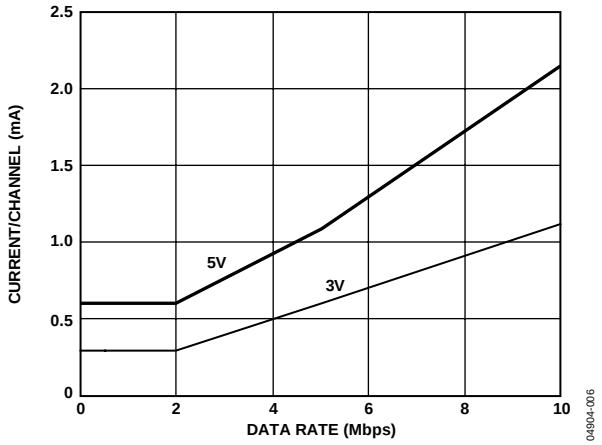



*Figure 4. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3 V Operation*

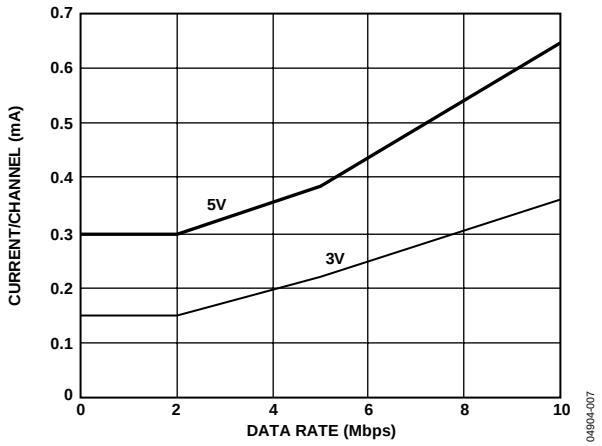



*Figure 5. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)*

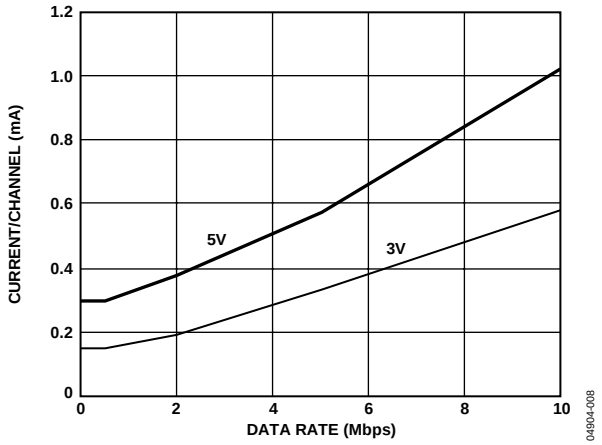



*Figure 6. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)*

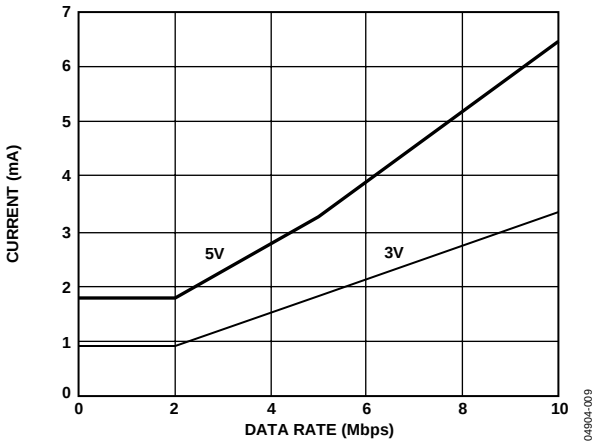



*Figure 7. Typical ADuM1310 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3 V Operation*

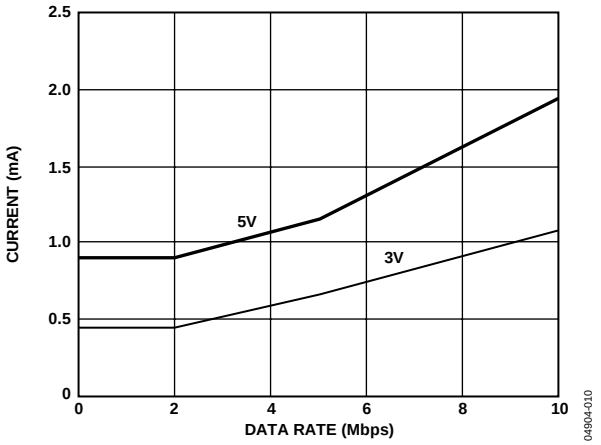



*Figure 8. Typical ADuM1310 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3 V Operation*

# APPLICATION INFORMATION

## PC BOARD LAYOUT

The ADuM1310 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 9). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for $V_{DD1}$ and between Pin 15 and Pin 16 for $V_{DD2}$. The capacitor value should be between 0.01 μF and 0.1 μF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

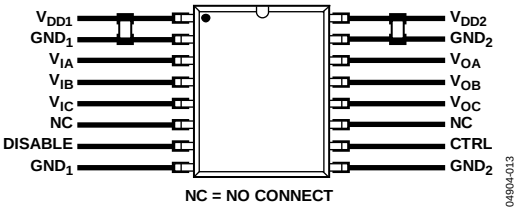



*Figure 9. Recommended Printed Circuit Board Layout*

## PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the length of time it takes for a logic signal to propagate through a component. The input to output propagation delay time for a high to low transition may differ from the propagation delay time of a low to high transition.

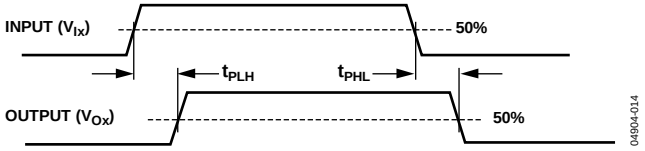



*Figure 10. Propagation Delay Parameters*

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM1310 component.

Propagation delay skew refers to the maximum amount the propagation delay differs among multiple ADuM1310 components operated under the same conditions.

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable, and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than 2 μs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no pulses for more than about 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default state (see Table 9) by the watchdog timer circuit.

The magnetic field immunity of the ADuM1310 is determined by the changing magnetic field which induces a voltage in the transformer's receiving coil large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The ADuM1310's 3 V operating condition is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold of about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2; n = 1, 2, \ldots, N$$

where:

$\beta$ is the magnetic flux density (gauss).
$N$ is the number of turns in the receiving coil.
$r_n$ is the radius of the $n^{th}$ turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM1310 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 11.

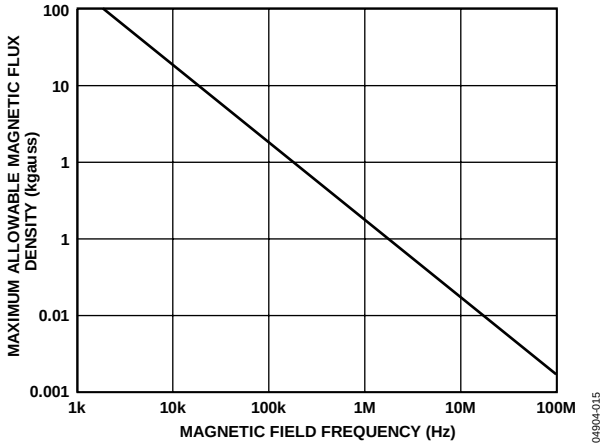



*Figure 11. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1310 transformers. Figure 12 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM1310 is extremely immune and can be affected only by extremely large currents operated at high frequency, very close to the component. For the 1 MHz example noted, a 0.5 kA current needed to be placed 5 mm away from the ADuM1310 to affect the operation of the component.

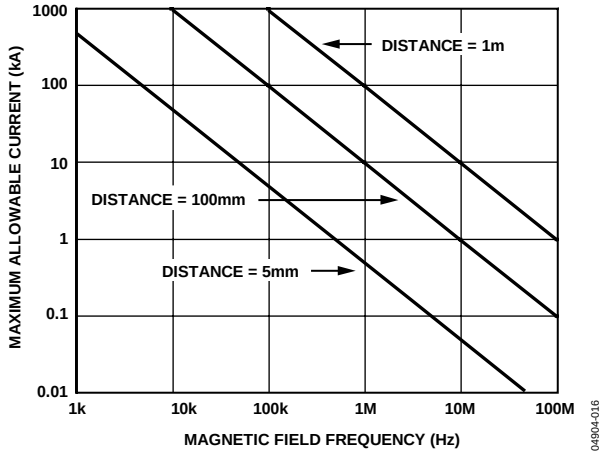



*Figure 12. Maximum Allowable Current for Various Current-to-ADuM1310 Spacings*

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The supply current at a given channel of the ADuM1310 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f \le 0.5f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

$C_L$ is the output load capacitance (pF).

$V_{DDO}$ is the output supply voltage (V).

$f$ is the input logic signal frequency (Hz, half of the input data rate, NRZ signaling).

$f_r$ is the input stage refresh rate (bps).

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total $I_{DD1}$ and $I_{DD2}$ supply current, the supply currents for each input and output channel corresponding to $I_{DD1}$ and $I_{DD2}$ are calculated and totaled. Figure 4 and Figure 5 provide per-channel supply currents as a function of the data rate for an unloaded output condition. Figure 6 provides per-channel supply current as a function of the data rate for a 15 pF output condition. Figure 7 through Figure 8 provide total $I_{DD1}$ and $I_{DD2}$ supply current as a function of the data rate for the ADuM1310.

## POWER-UP/POWER-DOWN CONSIDERATIONS

Given that the ADuM1310 has separate supplies on either side of the isolation barrier, the power-up and power-down characteristics relative to each supply voltage need to be considered individually.

As shown in Table 9, when $V_{DD1}$ input power is off, the ADuM1310 outputs take on a default condition as determined by the state of the CTRL pin. As the $V_{DD1}$ supply is increased/decreased, the output of each channel transitions from/to the default condition to/from the state matching its respective signals (see Figure 13 and Figure 14).

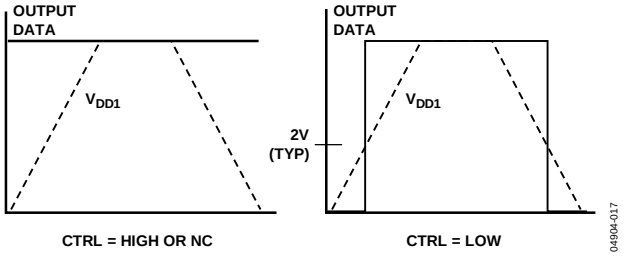



*Figure 13. $V_{DD1}$ Power-Up/Power-Down Characteristics, Input Data = High*

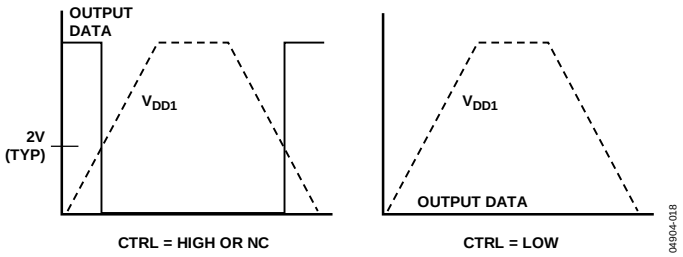



*Figure 14. $V_{DD1}$ Power-Up/Power-Down Characteristics, Input Data = Low*

When $V_{DD1}$ crosses the threshold for activating the refresh circuit (approximately 2 V), there can be a delay of up to 2 µs before the output is updated to the correct state, depending on the timing of the next refresh pulse. When $V_{DD1}$ is reduced from an on state below the 2 V threshold, there can be a delay of up to 5 µs before the output takes on its default state determined by the CTRL signal. This corresponds to the duration that the watchdog timer circuit at the input is designed to wait before triggering an output default state.

When the $V_{DD2}$ output supply is below the level at which the ADuM1310 output transistors are biased (about 1 V), the outputs take on a high impedance state. When $V_{DD2}$ is above a value of about 2 V, each channel output takes on a state matching that of its respective input. Between the values of 1 V and 2 V, the outputs are set low. This behavior is shown in Figure 15 and Figure 16.

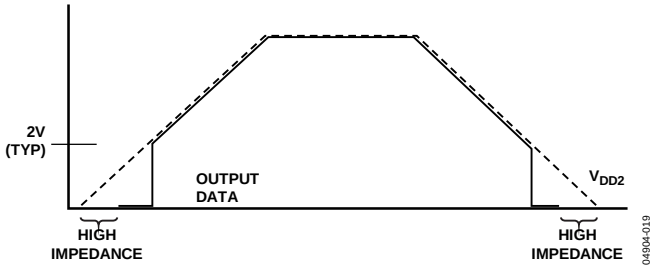



*Figure 15. $V_{DD2}$ Power-Up/Power-Down Characteristics, Input Data = High*

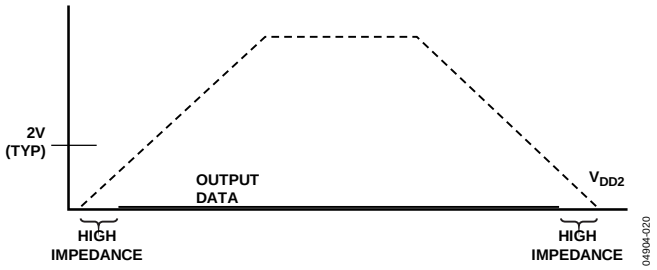
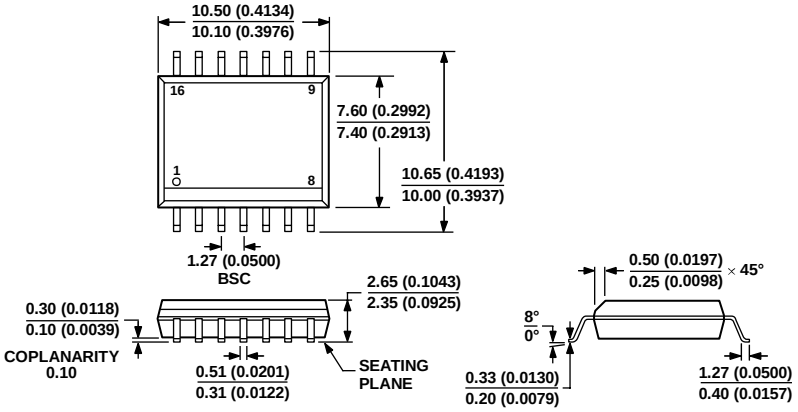



*Figure 16. $V_{DD2}$ Power-Up/Power-Down Characteristics, Input Data = Low*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

*Figure 17. 16-Lead Standard Small Outline Package [SOIC_W]*
*Wide Body (RW-16)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model | Number of Channels | Maximum Data Rate (Mbps) | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|---|
| ADuM1310BRWZ[1] | 3 | 10 | −40°C to +105°C | 16-Lead Wide Body SOIC_W | RW-16 |
| ADuM1310BRWZ-RL[1, 2] | 3 | 10 | −40°C to +105°C | 16-Lead Wide Body SOIC_W | RW-16 |

[1] Z = Pb-free part.
[2] The addition of an -RL suffix designates a 13-inch (1,000 units) tape and reel option.

## NOTES


D04904-0-10/06(E)