16-BIT, 40/80 MSPS ADCs WITH DDR LVDS/CMOS OUTPUTS

Check for Samples: ADS5560, ADS5562

FEATURES

- **16-Bit Resolution**
- **Maximum Sample Rate**
  - **ADS5562 - 80 MSPS**
  - **ADS5560 - 40 MSPS**
- **Total Power**
  - **865 mW at 80MSPS**
  - **674 mW at 40MSPS**
- **No Missing Codes**
- **High SNR 84 dBFS (3 MHz IF)**
- **85 dBc SFDR (3 MHz IF)**
- **Low Frequency Noise Suppression Mode**
- **Programmable Fine Gain, 1dB steps Until 6dB Maximum Gain**
- **Double Data Rate (DDR) LVDS and Parallel CMOS Output Options**
- **Internal/External Reference Support**
- **3.3-V Analog and Digital Supply**
- **Pin-for-Pin with ADS5547 Family**
- **48-QFN Package (7 mm × 7 mm)**

APPLICATIONS

- **Medical Imaging - MRI**
- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Test and Measurement Instrumentation**
- **High Definition Video**

DESCRIPTION

ADS556X is a high performance 16-bit A/D converter family with sampling rates up to 80 MSPS. It supports very high SNR for input frequencies in the first Nyquist zone. The device includes a low frequency noise suppression mode that improves the noise from DC to about 1MHz.

In addition to high performance, the device offers several flexible features such as output interface (either Double Data Rate LVDS or parallel CMOS) and fine gain in 1dB steps until 6dB maximum gain.

Innovative techniques, such as DDR LVDS and an internal reference that does not require external decoupling capacitors, have been used to achieve significant savings in pin-count. This results in a compact 7 mm x 7 mm 48 pin QFN package.

The device can be put in an external reference mode, where the VCM pin behaves as the external reference input. For applications where power is important, ADS556X offers power down modes and automatic power scaling at lower sample rates.

It is specified over the industrial temperature range (-40°C to +85°C).

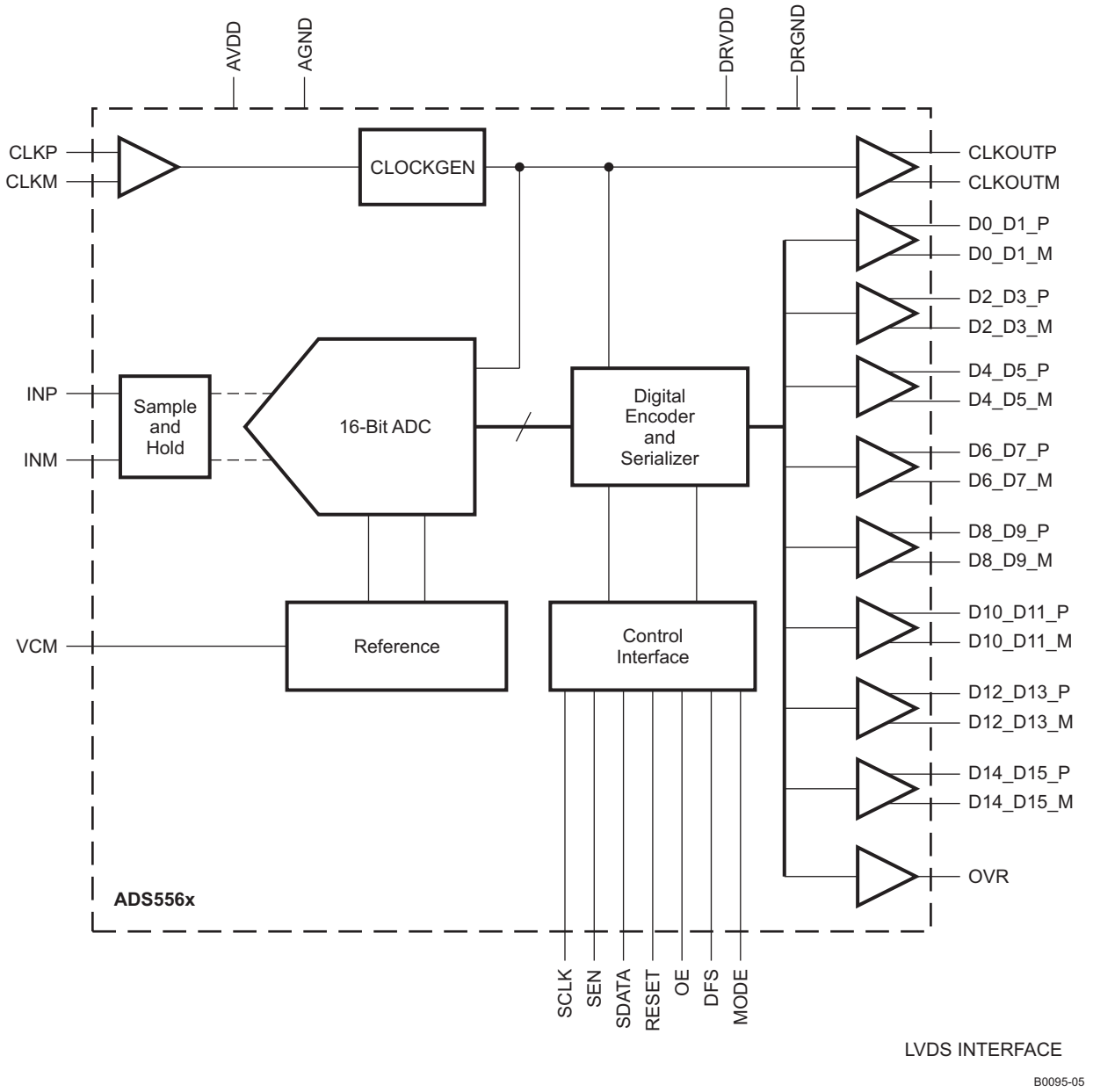


Table 1. PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
ADS5562	QFN-48	RGZ	–40°C to 85°C	AZ5562	ADS5562IRGZT	Tape and Reel, small
					ADS5562IRGZR	Tape and Reel, large
ADS5560	QFN-48	RGZ	–40°C to 85°C	AZ5560	ADS5560IRGZT	Tape and Reel, small
					ADS5560IRGZR	Tape and Reel, large

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
AVDD	Supply voltage range		–0.3 V to 3.9	V
DRVDD	Supply voltage range		–0.3 V to 3.9	V
	Voltage between AGND and DRGND		-0.3 to 0.3	V
	Voltage between AVDD and DRVDD		-0.3 to 3.3	V
	Voltage applied to VCM pin (in external reference mode)		-0.3 to 1.8	V
	Voltage applied to analog input pins	INP, INM	–0.3 V to minimum (3.6, AVDD + 0.3 V)	V
		CLKP, CLKM(2), MODE		
		RESET, SCLK, SDATA, SEN, OE, DFS	-0.3V to minimum (3.6, DRVDD+0.3V)	V
T_A	Operating free-air temperature range		–40 to 85	°C
T_{jmax}	Operating junction temperature range		125	°C
T_{STG}	Storage temperature range		–65 to 150	°C
	Lead temperature 1,6 mm (1/16") from the case for 10 seconds		220	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is <|0.3V|). This prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS5560, ADS5562	UNITS
		QFN-48 RGZ	
θ_{JA}	Junction-to-ambient thermal resistance(2)	27.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	12.4	
θ_{JB}	Junction-to-board thermal resistance(4)	4.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	4.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
SUPPLIES AND REFERENCES					
AVDD	Analog supply voltage	3	3.3	3.6	V
DRVDD	Digital supply voltage	3	3.3	3.6	V
ANALOG INPUTS					
	Differential input voltage range (with default fine gain=1 dB)		3.56		V_{PP}
	Input common-mode voltage		1.5 ±0.1		V
	Voltage applied on VCM in external reference mode		1.5 ±0.05		V

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

				MIN	TYP	MAX	UNIT
CLOCK INPUT							
	Sample rate	ADS5562	DEFAULT SPEED mode	> 25		80	MSPS
			LOW SPEED mode (1)	1		25	MSPS
		ADS5560	DEFAULT SPEED mode	> 25		40	MSPS
			LOW SPEED mode	1		25	MSPS
	Supported clock waveform formats		Sine wave, LVPECL, LVDS, LVCMOS				
	Clock amplitude, ac-coupled, differential (V_{CLKP} - V_{CLKM})			0.4			V_{PP}
	Clock duty cycle			45%	50%	55%	
DIGITAL OUTPUTS							
C_L	Maximum external load capacitance from each output pin to DRGND (LVDS and CMOS modes)				5		pF
R_L	Differential external load resistance between the LVDS output pairs (LVDS mode)				100		Ω
	Operating free-air temperature			-40		85	°C

(1) See Low sampling frequency operation in application section for details.

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*.
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Max Rated, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5562			ADS5560			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			16		bits
ANALOG INPUT									
	Differential input voltage range (1)			3.56			3.56		V_{PP}
	Differential input capacitance			5			5		pF
	Analog input bandwidth			300			300		MHz
	Analog input common mode current (per input pin)			6.6			6.6		µA/MSPS
VCM	Common mode output voltage	Internal reference mode		1.5			1.5		V
	VCM output current capability	Internal reference mode		±4			±4		mA
DC ACCURACY									
	No Missing Codes	0 dB gain		Assured			Assured		
DNL	Differential non-linearity		-0.95	0.5	3	-0.95	0.5	3	LSB
INL	Integral non-linearity		-8.5	±3	8.5	-8.5	±3	8.5	LSB
	Offset error		-25	±10	25	-25	±10	25	mV
	Offset error temperature coefficient			0.005			0.005		mV/°C
	Variation of offset error across AVDD supply			1.5			1.5		mV/V
	There are two sources of gain error: i) internal reference inaccuracy and ii) channel gain error								
E_{GREF}	Gain error due to internal reference inaccuracy alone		-2.5	±1	2.5	-2.5	±1	2.5	%FS
E_{CHAN}	Channel gain error alone		-2.5	± 1	2.5	-2.5	± 1	2.5	%FS
	Channel gain error temperature coefficient			0.01			0.01		Δ%/°C
POWER SUPPLY									
IAVDD	Analog supply current			210	250		160	190	mA

(1) The full-scale voltage range is a function of the fine gain settings. See Table 24.

ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*.
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Max Rated, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5562			ADS5560			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
IDRVDD	Digital supply current, C_L = 5 pF	LVDS mode I_O = 3.5 mA, R_L = 100 Ω		52			44		mA
		CMOS mode F_{IN} = 3 MHz		60			37		mA
	Total power	LVDS mode		865	1100		674	810	mW
	Standby power	STANDBY mode with clock running		155			135		mW
	Clock stop power			125	150		125	150	mW

ELECTRICAL CHARACTERISTICS (Continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *0 dB fine gain* (1).

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Max Rated, *default fine gain (1dB),* unless otherwise noted.

PARAMETER	TEST CONDITIONS		ADS5562 Fs = 80 MSPS			ADS5560 Fs = 40 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
AC CHARACTERISTICS									
SNR Signal to noise ratio	F_{IN} = 3 MHz	LVDS interface		84			84.3		dBFS
	F_{IN} = 10 MHz		79	83.8		80	84		
	F_{IN} = 25 MHz			83.2			82.5		
	F_{IN} = 30 MHz			82.8			81.8		
	F_{IN} = 3 MHz	CMOS interface		81.7			83.5		dBFS
	F_{IN} = 10 MHz		77	81.4		78	83.1		
	F_{IN} = 25 MHz			80.7			81.8		
	F_{IN} = 30 MHz			80.4			81.6		
RMS output noise	Inputs tied to common-mode			1.42			1.42		LSB
SINAD Signal to noise and distortion ratio	F_{IN} = 3 MHz	LVDS interface		80.5			83.2		dBFS
	F_{IN} = 10 MHz		75	80.5		76	83		
	F_{IN} = 25 MHz			79.5			79		
	F_{IN} = 30 MHz			79			77		
	F_{IN} = 3 MHz	CMOS interface		80.5			82		dBFS
	F_{IN} = 10 MHz		73.5	80.2		75	81.4		
	F_{IN} = 25 MHz			79.3			79.3		
	F_{IN} = 30 MHz			77.9			78		
ENOB Effective number of bits	F_{IN} = 10 MHz	LVDS interface	12.2	13.1		12.4	13.5		bits
SFDR Spurious free dynamic range	F_{IN} = 3 MHz			85			90		dBc
	F_{IN} = 10 MHz		77	85		78	88		
	F_{IN} = 25 MHz			83			83		
	F_{IN} = 30 MHz			80			79		
HD2 Second harmonic	F_{IN} = 3 MHz			90			94		dBc
	F_{IN} = 10 MHz		77	89		78	92		
	F_{IN} = 25 MHz			88			90		
	F_{IN} = 30 MHz			88			88		

(1) Note that after reset, the device is initialized to 1 dB fine gain setting. For SFDR and SNR performance across fine gains, see Typical Characteristics section.

ELECTRICAL CHARACTERISTICS (Continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, default fine gain (0 dB), internal reference mode, DDR LVDS interface, (1).
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Max Rated, *default fine gain (1 dB)*, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS5562			ADS5560			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
HD3 Third harmonic	F_{IN} = 3 MHz		85			90		dBc
	F_{IN} = 10 MHz	77	85		78	88		
	F_{IN} = 25 MHz		83			83		
	F_{IN} = 30 MHz		80			79		
Worst harmonic other than HD2, HD3	F_{IN} = 3 MHz		104			104		dBc
	F_{IN} = 10 MHz		102			102		
	F_{IN} = 25 MHz		100			101		
	F_{IN} = 30 MHz		100			101		
THD Total harmonic distortion	F_{IN} = 3 MHz		84			88		dBc
	F_{IN} = 10 MHz	75.5	83		76.5	86		
	F_{IN} = 25 MHz		82			81		
	F_{IN} = 30 MHz		80			78		
IMD Two-tone intermodulation distortion	F_{IN1} = 5 MHz, F_{IN2} = 10 MHz each tone -7 dBFS		92			98		dBFS
Voltage overload recovery time	Recovery to 1% for 6-dB overload		1			1		clock cycles

(1) Note that after reset, the device is initialized to 1 dB fine gain setting. For SFDR and SNR performance across fine gains, see Typical Characteristics section.

DIGITAL CHARACTERISTICS

DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1, AVDD = 3.0V to 3.6V, I_O = 3.5 mA, R_L = 100 Ω(1) (2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			33		µA
Low-level input current			-33		µA
Input capacitance			4		pF
DIGITAL OUTPUTS – CMOS MODE					
High-level output voltage			DRVDD		V
Low-level output voltage			0		V
Output capacitance	Capacitance inside the device from each output pin to ground		4		pF
DIGITAL OUTPUTS – LVDS MODE					
V_{ODH} High-level output voltage			+350		mV
V_{ODL} Low-level output voltage			-350		mV
V_{OCM} Output common-mode voltage			1.2		V
Output capacitance	Capacitance inside the device from each output pin to ground		4		pF

(1) All LVDS and CMOS specifications are characterized, but not tested at production.
(2) I_O refers to the LVDS buffer current setting; R_L is the differential load resistance between the LVDS output pair.

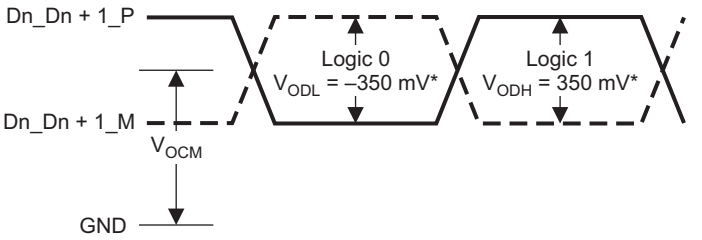


Figure 1. LVDS Output Voltage Levels

TIMING CHARACTERISTICS – LVDS AND CMOS MODES(1)

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 3.0 to 3.6V, Sampling frequency = 80 MSPS, sine wave input clock, 50% clock duty cycle, 1.5 V_{PP} clock amplitude, C_L = 5 pF(2) , no internal termination, I_O = 3.5 mA, R_L = 100 Ω (3)
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.0 to 3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay		0.5	1.2	2	ns
t_j	Aperture jitter	Sampling frequency = 80 MSPS		90		fs rms
		Sampling frequency = 40 MSPS		135		fs rms
	Wake-up time	Time to data stable (4) after coming out of STANDBY mode		60	200	µs
		Time to valid data after stopping and restarting the input clock		80		µs
	Latency			16		Clock cycles
DDR LVDS MODE(5)						
	LVDS bit clock duty cycle		47%	50%	53%	
t_{su}	Data setup time(6)	Data valid(7) to zero-crossing of CLKOUTP	2.0	3.0		ns
t_h	Data hold time(6)	Zero-crossing of CLKOUTP to data becoming invalid(7)	2.0	3.0		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	9.5	11	12.5	ns
t_r	Data rise time	Rise time measured from –100 mV to 100 mV	0.15	0.22	0.3	ns
t_f	Data fall time	Fall time measured from 100 mV to –100 mV	0.15	0.22	0.3	ns
t_r	Output clock rise time	Rise time measured from –100 mV to 100 mV	0.15	0.22	0.3	ns
t_f	Output clock fall time	Fall time measured from 100 mV to –100 mV	0.15	0.22	0.3	ns
t_{OE}	Output enable (OE) to data delay	Time to data valid after OE becomes active		700		ns
PARALLEL CMOS MODE						
	CMOS output clock duty cycle			50%		
t_{su}	Data setup time	Data valid(8) to 50% of CLKOUT rising edge	6.5	8.0		ns
t_h	Data hold time	50% of CLKOUT rising edge to data becoming invalid (8)	2.0	3.0		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to 50% of CLKOUT rising edge	6.3	7.8	9.3	ns
t_r	Data rise time	Rise time measured from 20% to 80% of DRVDD	1.0	1.5	2.0	ns
t_f	Data fall time	Fall time measured from 80% to 20% of DRVDD	1.0	1.5	2.0	ns
t_r	Output clock rise time	Rise time measured from 20% to 80% of DRVDD	0.7	1.0	1.2	ns
t_f	Output clock fall time	Fall time measured from 80% to 20% of DRVDD	1.2	1.5	1.8	ns
t_{OE}	Output enable (OE) to data delay	Time to data valid after OE becomes active		200		ns

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) C_L is the effective external single-ended load capacitance between each output pin and ground.
(3) Io refers to the LVDS buffer current setting; R_L is the differential load resistance between the LVDS output pair.
(4) Data stable is defined as the point at which the SNR is within 2dB of its normal value.
(5) Measurements are done with a transmission line of 100 Ω characteristic impedance between the device and the load.
(6) Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(7) Data valid refers to logic high of +100 mV and logic low of -100 mV.
(8) Data valid refers to logic high of 2.6 V and logic low of 0.66 V.

Table 2. Timing Characteristics at Lower Sampling Frequencies

Sampling Frequency, MSPS	t_{su},Setup time, ns			t_h,Hold time, ns			t_{PDI},Clock propagation delay, ns		
DDR LVDS									
	MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
65	**2.7**	**3.7**		**2.7**	**3.7**		**11.5**	**13**	**14.5**
40	5	6		5	6		16.5	18	19.5
20	8	11		8	11		30.5	32	33.5
Parallel CMOS									
65	8	9.5		3	4		7	8.5	10
40	14	15.5		6.5	7.5		8	9.5	11
20	14			6.5			5	10.5	15

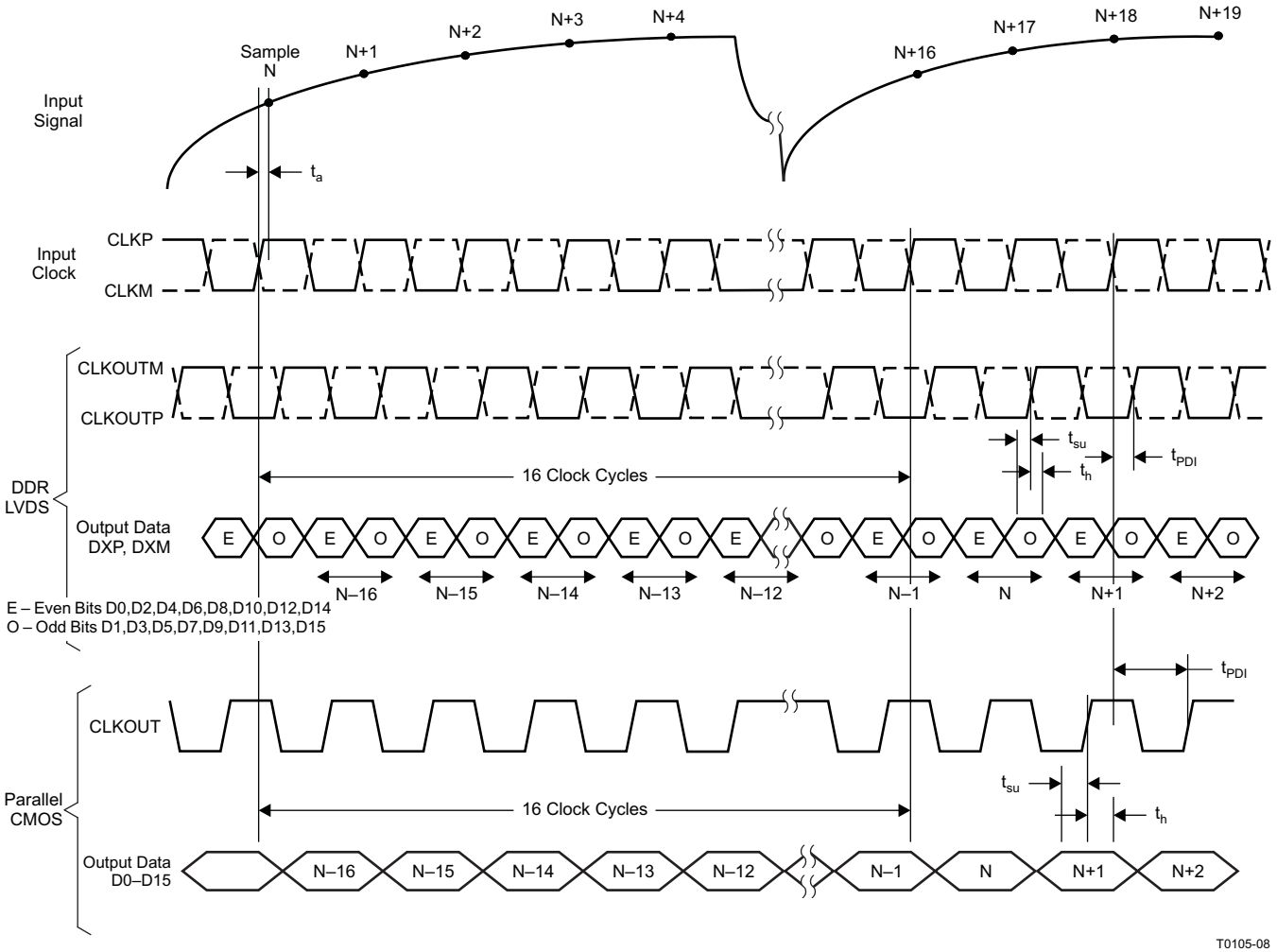
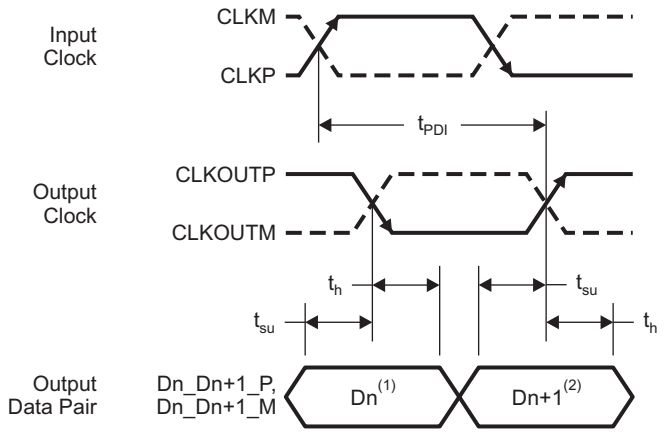


Figure 2. Latency



(1)Dn – Bits D0, D2, D4, D6, D8, D10, D12, D14
(2)Dn+1 – Bits D1, D3, D5, D7, D9, D11, D13, D15

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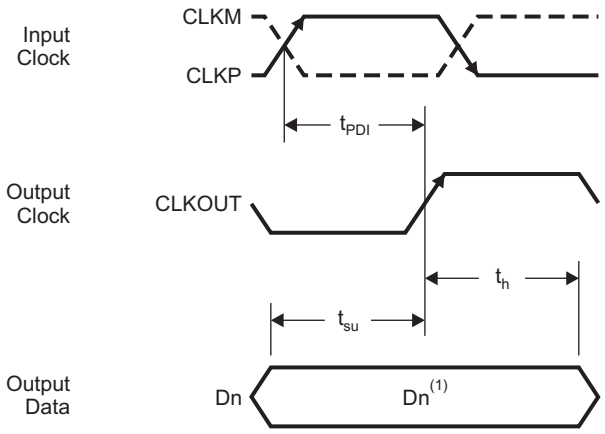
Figure 3. LVDS Mode Timing



(1)Dn – Bits D0–D15

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Figure 4. CMOS Mode Timing

DEVICE PROGRAMMING MODES

ADS556X offers flexibility with several programmable features that are easily configured.

The device can be configured independently using either parallel interface control or serial interface programming.

In addition, the device supports a third configuration mode, where both the parallel interface and the serial control registers are used. In this mode, the priority between the parallel and serial interfaces is determined by a priority table (Table 4). If this additional level of flexibility is not required, the user can select either the serial interface programming or the parallel interface control.

USING PARALLEL INTERFACE CONTROL ONLY

To control the device using parallel interface, keep RESET tied to **high** (DRVDD). Pins DFS, MODE, SEN, SCLK, and SDATA are used to directly control certain modes of the ADC. The device is configured by connecting the parallel pins to the correct voltage levels (as described in Table 5 to Table 9). There is no need to apply reset.

In this mode, SEN, SCLK, and SDATA function as parallel interface control pins. Frequently used functions are controlled in this mode—standby, selection between LVDS/CMOS output format, internal/external reference, two's complement/offset binary output format, and position of the output clock edge.

Table 3 has a description of the modes controlled by the parallel pins.

Table 3. Parallel Pin Definition

PIN	CONTROL MODES
DFS	DATA FORMAT and the LVDS/CMOS output interface
MODE	Internal or external reference
SEN	CLKOUT edge programmability
SCLK	LOW SPEED mode control for low sampling frequencies (≤ 30 MSPS)
SDATA	STANDBY mode – Global (ADC, internal references and output buffers are powered down)

USING SERIAL INTERFACE PROGRAMMING ONLY

To program using the serial interface, the internal registers must first be reset to their default values, and the RESET pin must be kept **low**. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on the RESET pin (of width greater than 10ns), or by a **high** setting on the <RST> bit (D1 in register 0x6C). The *serial interface section* describes the register programming and register reset in more detail.

Since the parallel pins DFS and MODE are not used in this mode, they must be tied to ground.

USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (DFS, MODE) can also be used to configure the device.

The serial registers must first be reset to their default values and the RESET pin must be kept **low**. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on RESET pin or by a **high** setting on the <RST> bit (D1 in register 0x6C). The *serial interface section* describes the register programming and register reset in more detail.

The parallel interface control pins DFS and MODE are used and their function is determined by the appropriate voltage levels as described in Table 8 and Table 9. The voltage levels are derived by using a resistor string as illustrated in Figure 5. Since some functions are controlled using both the parallel pins and serial registers, the priority between the two is determined by a priority table (Table 4).

Table 4. Priority Between Parallel Pins and Serial Registers

PIN	FUNCTIONS SUPPORTED	PRIORITY
MODE	Internal/External reference	When using the serial interface, bit <REF> (register 0x6D, bit D4) controls this mode, ONLY if the MODE pin is tied low.
DFS	DATA FORMAT	When using the serial interface, bit <DF> (register 0x63, bit D3) controls this mode, ONLY if the DFS pin is tied low.
	LVDS/CMOS	When using the serial interface, bit <ODI> (register 0x6C, bits D3-D4) controls LVDS/CMOS selection independent of the state of DFS pin, only if <ODI> is not programmed as 00. DFS pin controls LVDS/CMOS selection if <ODI> is programmed as 00.

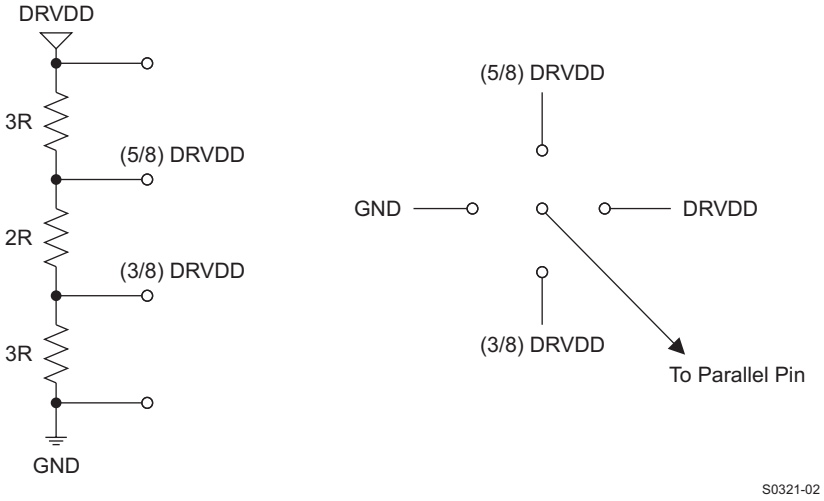


Figure 5. Simple Scheme to Configure Parallel Pins

DESCRIPTION OF PARALLEL PINS

Table 5. SCLK Control Pin

SCLK	DESCRIPTION
0	DEFAULT SPEED mode - Use for sampling frequencies > 25 MSPS, 3dB Gain.
DRVDD	LOW SPEED mode Enabled - Use for sampling frequencies ≤ 25 MSPS, 1dB Gain.

Table 6. SDATA Control Pin

SDATA	DESCRIPTION
0	Normal operation (Default)
DRVDD	STANDBY. This is a global power down, where ADC, internal references and the output buffers are powered down.

Table 7. SEN Control Pin

SEN	With CMOS interface
0	CLKOUT Rising edge later by (3/36)Ts CLKOUT Falling edge later by (3/36)Ts
(3/8)DRVDD	CLKOUT Rising edge later by (5/36)Ts CLKOUT Falling edge later by (5/36)Ts
(5/8)DRVDD	CLKOUT Rising edge earlier by (3/36)Ts CLKOUT Falling edge earlier by (3/36)Ts
DRVDD	Default CLKOUT position
	With LVDS interface
0	CLKOUT Rising edge later by (7/36)Ts CLKOUT Falling edge later by (6/36)Ts
(3/8)DRVDD	CLKOUT Rising edge later by (7/36)Ts CLKOUT Falling edge later by (6/36)Ts
(5/8)DRVDD	CLKOUT Rising edge later by (3/36)Ts CLKOUT Falling edge later by (3/36)Ts
DRVDD	Default CLKOUT position

Table 8. DFS Control Pin

DFS	DESCRIPTION
0	2's complement data and DDR LVDS output (Default)
(3/8)DRVDD	2's complement data and parallel CMOS output
(5/8)DRVDD	Offset binary data and parallel CMOS output
DRVDD	Offset binary data and DDR LVDS output

Table 9. MODE Control Pin

MODE	DESCRIPTION
0	Internal reference
(3/8)AVDD	External reference
(5/8)AVDD	External reference
AVDD	Internal reference

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed through the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock), SDATA (Serial Interface Data) and RESET. After device power-up, the internal registers must be reset to their default values by applying a high-going pulse on RESET (of width greater than 10 ns), or by a high setting on the <RST> bit (D1 in register 0x6C).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data is loaded in multiples of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits form the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

REGISTER INITIALIZATION

After power-up, the internal registers *must* be reset to their default values. This is done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10 ns) as shown in Figure 6.

   OR

2. By applying software reset. Using the serial interface, set the <RST> bit (D1 in register 0x6C) to **high**. This initializes the internal registers to their default values and then self-resets the <RST> bit to **low**. In this case the RESET pin is kept **low**.

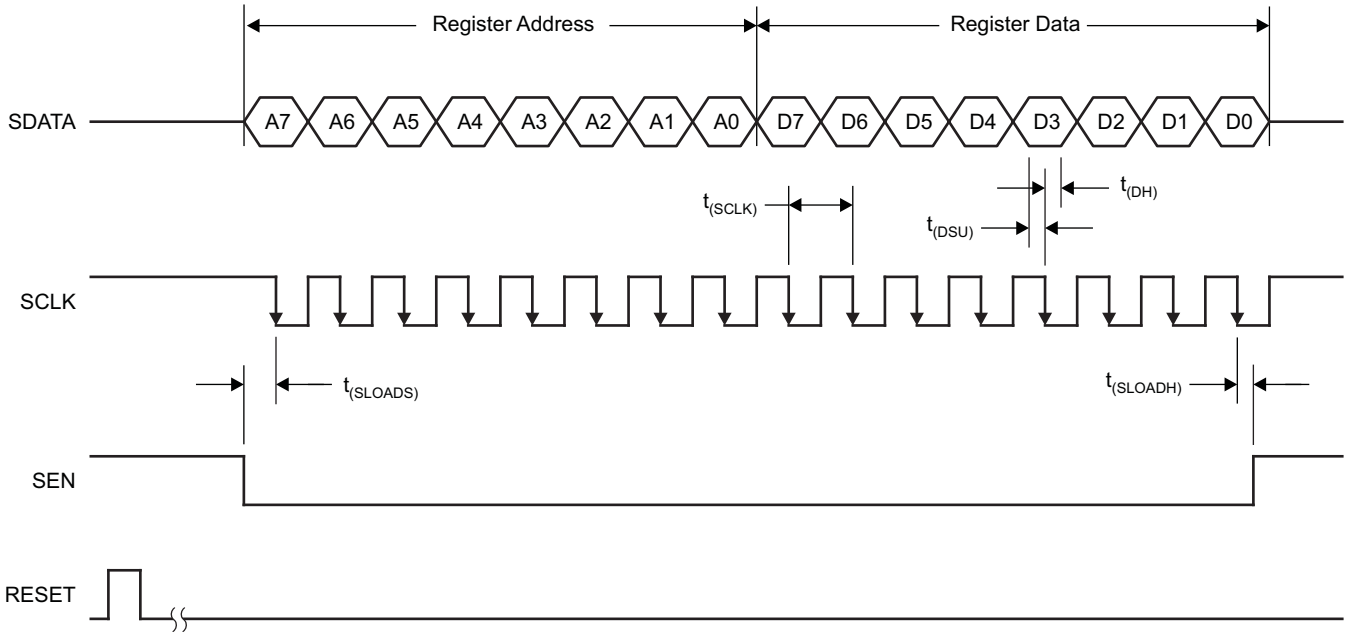


Figure 6. Serial Interface Timing Diagram

SERIAL INTERFACE TIMING CHARACTERISTICS

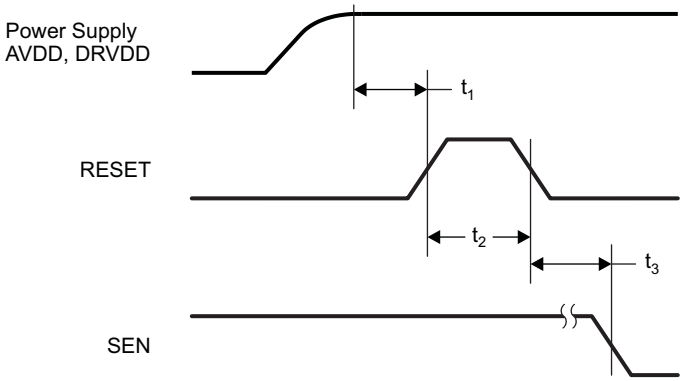
Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

RESET TIMING

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	5			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	25			ns
t_{PO}	Power-up time	Delay from power-up of AVDD and DRVDD to output stable		6.5		ms



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. If the pulse is greater than 1µs, the device could enter the parallel configuration mode briefly then return back to serial interface mode. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 7. Reset Timing Diagram

SERIAL REGISTER MAP

Table 10 gives a summary of all the modes that can be programmed through the serial interface.

Table 10. Summary of Functions Supported by Serial Interface(1) (2)

REGISTER ADDRESS IN HEX	REGISTER FUNCTIONS							
A7 - A0	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
5D								**<LF NOISE SUPPRESSION>**
62				**<CLKOUT POSN>** OUTPUT CLOCK POSITION PROGRAMMABILITY				
63	**<STBY>** GLOBAL POWER DOWN				**<DF>** DATA FORMAT - 2's COMP or OFFSET BINARY			**<LOW SPEED>** ENABLE LOW SAMPLING FREQUENCY OPERATION
65	**<TEST PATTERN>** – ALL 0S, ALL 1s, TOGGLE, RAMP, CUSTOM PATTERN							
68					**<GAIN>** FINE GAIN 0dB to 6dB, in 1dB steps			
69	**<CUSTOM A>** CUSTOM PATTERN (D7 TO D0)							
6A	**<CUSTOM B>** CUSTOM PATTERN (D15 TO D8)							
6C				**<ODI>** OUTPUT DATA INTERFACE DDR LVDS or PARALLEL CMOS				
6D				**<REF>** INTERNAL or EXTERNAL REFERENCE				
6E								**<RST>** SOFTWARE RESET
7E	**<DATA TERM>** INTERNAL TERMINATION – DATA OUTPUTS			**<CLKOUT TERM>** INTERNAL TERMINATION – OUTPUT CLOCK			**<LVDS CURR>** LVDS CURRENT PROGRAMMABILITY	
7F	**<CURR DOUBLE>** LVDS CURRENT DOUBLE							

(1) The unused bits in each register (shown by blank cells in above table) must be programmed as '0'.
(2) Multiple functions in a register can be programmed in a single write operation. See Serial Interface section for details.

DESCRIPTION OF SERIAL REGISTERS

Each register function is explained in detail below.

Table 11.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
5D								<LF NOISE SUPPRESSION>

D0	<LF NOISE SUPPRESSION> Low frequency noise suppression
0	Disable low frequency noise suppression
1	Enable low frequency noise suppression

Table 12.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
62				<CLKOUT POSN> OUTPUT CLOCK POSITION PROGRAMMABILITY				

D4 - D0	<CLKOUT POSN> Output Clock Position Programmability
00000	Register value after reset (corresponds to default CLKOUT position) Setup/hold timings with this clock position are specified in the timing characteristics table.
00001	Default CLKOUT position. Setup/hold timings with this clock position are specified in the timing characteristics table.
XX011	**CMOS** - Rising edge earlier by (3/36) Ts
	LVDS - Falling edge later by (3/36) Ts
XX101	**CMOS** - Rising edge later by (3/36) Ts
	LVDS - Falling edge later by (6/36) Ts
XX111	**CMOS** - Rising edge later by (5/36) Ts
	LVDS - Falling edge later by (6/36) Ts
01XX1	**CMOS** - Falling edge earlier by (3/36) Ts
	LVDS - Rising edge later by (3/36) Ts
10XX1	**CMOS** - Falling edge later by (3/36) Ts
	LVDS - Rising edge later by (7/36) Ts
11XX1	**CMOS** - Falling edge later by (5/36) Ts
	LVDS - Rising edge later by (7/36) Ts

Table 13.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
63	**<STBY>** GLOBAL POWER DOWN				**<DF>** DATA FORMAT 2's COMP or OFFSET BINARY			**<LOW SPEED>** ENABLE LOW SAMPLING FREQUENCY OPERATION

D3	<DF> Output Data Format
0	2's complement
1	Offset binary

D0	<LOW SPEED> Low Sampling Frequency Operation
0	DEFAULT SPEED mode (for Fs > 25 MSPS)
1	LOW SPEED mode eabled (for Fs ≤ 25 MSPS)

D7	<STBY> Global STANDBY
0	Normal operation
1	Global power down (includes ADC, internal references and output buffers)

Table 14.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
65	**<TEST PATTERNS>** — ALL 0S, ALL 1s, TOGGLE, RAMP, CUSTOM PATTERN							

D7 - D5	<TEST PATTERN> Outputs selected test pattern on data lines
000	Normal operation
001	All 0s
010	All 1s
011	Toggle pattern - alternate 1s and 0s on each data output and across data outputs
100	Ramp pattern - Output data ramps from 0x0000 to 0xFFFF by one code every clock cycle
101	Custom pattern - Outputs the custom pattern in CUSTOM PATTERN registers A and B
111	Unused

Table 15.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
68					**<GAIN>** FINE GAIN 0 dB to 6 dB, in 1 dB steps			

D3 - D0	<GAIN> Programmable Fine Gain
0XXX	1 dB
1000	0 dB
1001	1 dB, default register value after reset
1010	2 dB
1011	3 dB
1100	4 dB
1101	5 dB
1110	6 dB

Table 16.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
69	**<CUSTOM A>** CUSTOM PATTERN (D7 TO D0)							
6A	**<CUSTOM B>** CUSTOM PATTERN (D15 TO D8)							

Reg 69	D7 - D0	Program bits D7 to D0 of custom pattern
Reg 6A	D15 - D8	Program bits D15 to D8 of custom pattern

Table 17.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
6C				**<ODI>** OUTPUT DATA INTERFACE - DDR LVDS OR PARALLEL CMOS				

D4 - D3	<ODI> Output Interface
00	default after reset, state of DFS pin determines interface type. See Table 8.
01	DDR LVDS outputs, independent of state of DFS pin.
11	Parallel CMOS outputs, independent of state of DFS pin.

Table 18.

A7 - A0	D7	D6	D5	D4	D3	D2	D1	D0
6D				**<REF>** INTERNAL or EXTERNAL REFERENCE				

D4	<REF> Reference
0	Internal reference
1	External reference mode, force voltage on VCM to set reference.

Table 19.

A7 - A0	D7	D6	D5	D4	D3	D2	D1	D0
6E								**<RST>** SOFTWARE RESET

D0	<RST> Software resets the ADC
1	Resets all registers to default values

Table 20.

A7 - A0	D7	D6	D5	D4	D3	D2	D1	D0
7E	**<DATA TERM>** INTERNAL TERMINATION – DATA OUTPUTS			**<CLKOUT TERM>** INTERNAL TERMINATION – OUTPUT CLOCK			**<LVDS CURR>** LVDS CURRENT PROGRAMMABILITY	

D1 - D0	<LVDS CURR> LVDS Buffer Current Programmability
00	3.5 mA, default
01	2.5 mA
10	4.5 mA
11	1.75 mA

D4 - D2	<CLKOUT TERM> LVDS Buffer Internal Termination
000	No internal termination
001	325
010	200
011	125
100	170
101	120
110	100
111	75

D7 - D5	<DATA TERM> LVDS Buffer Internal Termination
000	No internal termination
001	325
010	200
011	125
100	170
101	120
110	100
111	75

Table 21.

A7 - A0	D7	D6	D5	D4	D3	D2	D1	D0
7F	**<CURR DOUBLE>** LVDS CURRENT DOUBLE							

D7 - D6	**<CURR DOUBLE> LVDS Buffer Internal Termination**
00	Value specified by <LVDS CURR>
01	2x data, 2x clockout currents
10	1x data, 2x clockout currents
11	2x data, 4x clockout currents

PIN CONFIGURATION (LVDS MODE)

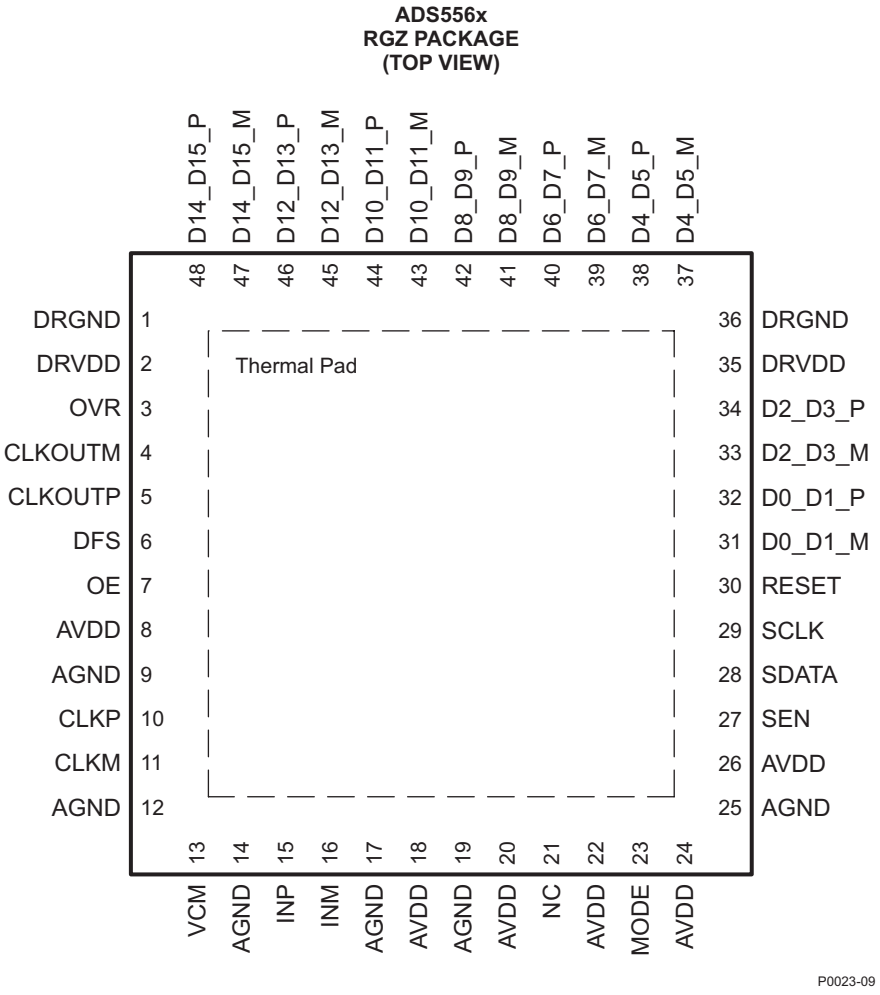


Figure 8. LVDS Mode Pinout

Table 22. PIN ASSIGNMENTS – LVDS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	8, 18, 20, 22, 24, 26	6
AGND	Analog ground	I	9, 12, 14, 17, 19, 25	6
CLKP, CLKM	Differential clock input	I	10, 11	2
INP, INM	Differential analog input	I	15, 16	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal reference.	I/O	13	1
RESET	Serial interface reset input. When using the serial interface, the user should apply a high-going pulse on this pin to reset the internal registers. When the serial interface is not used, the user should tie RESET permanently high. (SCLK, SDATA and SEN can be used as parallel pin controls). The pin has an internal 100-kΩ pull-down resistor to DRGND.	I	30	1

Table 22. PIN ASSIGNMENTS – LVDS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
SCLK	This pin functions as serial interface clock input when RESET is low. It functions as LOW SPEED MODE control when RESET is tied high. See Table 5 for detailed information. The pin has an internal 100-kΩ pull-down resistor to DRGND.	I	29	1
SDATA	This pin functions as serial interface data input when RESET is low. It functions as STANDBY control pin when RESET is tied high. See Table 6 for detailed information. The pin has an internal 100-kΩ pull-down resistor to DRGND.	I	28	1
SEN	This pin functions as serial interface enable input when RESET is low. It functions as CLKOUT edge programmability when RESET is tied high. See Table 7 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	27	1
OE	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	7	1
DFS	Data Format Select input. This pin sets the DATA FORMAT (Twos complement or Offset binary) and the LVDS/CMOS output mode type. See Table 8 for detailed information. The pin has an internal 100-kΩ pull-down resistor to DRGND.	I	6	1
MODE	Mode select input. This pin selects the Internal or External reference mode. See Table 9 for detailed information. The pin has an internal 100-kΩ pull-down resistor to AGND.	I	23	1
CLKOUTP	Differential output clock, true	O	5	1
CLKOUTM	Differential output clock, complement	O	4	1
D0_D1_P	Differential output data D0 and D1 multiplexed, true	O	32	1
D0_D1_M	Differential output data D0 and D1 multiplexed, complement.	O	31	1
D2_D3_P	Differential output data D2 and D3 multiplexed, true	O	34	1
D2_D3_M	Differential output data D2 and D3 multiplexed, complement	O	33	1
D4_D5_P	Differential output data D4 and D5 multiplexed, true	O	38	1
D4_D5_M	Differential output data D4 and D5 multiplexed, complement	O	37	1
D6_D7_P	Differential output data D6 and D7 multiplexed, true	O	40	1
D6_D7_M	Differential output data D6 and D7 multiplexed, complement	O	39	1
D8_D9_P	Differential output data D8 and D9 multiplexed, true	O	42	1
D8_D9_M	Differential output data D8 and D9 multiplexed, complement	O	41	1
D10_D11_P	Differential output data D10 and D11 multiplexed, true	O	44	1
D10_D11_M	Differential output data D10 and D11 multiplexed, complement	O	43	1
D12_D13_P	Differential output data D12 and D13 multiplexed, true	O	46	1
D12_D13_M	Differential output data D12 and D13 multiplexed, complement	O	45	1
D14_D15_P	Differential output data D14 and D15 multiplexed, true	O	48	1
D14_D15_M	Differential output data D14 and D15 multiplexed, complement	O	47	1
OVR	Out-of-range indicator, CMOS level signal	O	3	1
DRVDD	Digital and output buffer supply	I	2, 35	2
DRGND	Digital and output buffer ground	I	1, 36	2
PAD	Connect the PAD to the ground plane. See in application section.			1
NC	Do not connect	-	21	1

PIN CONFIGURATION (CMOS MODE)

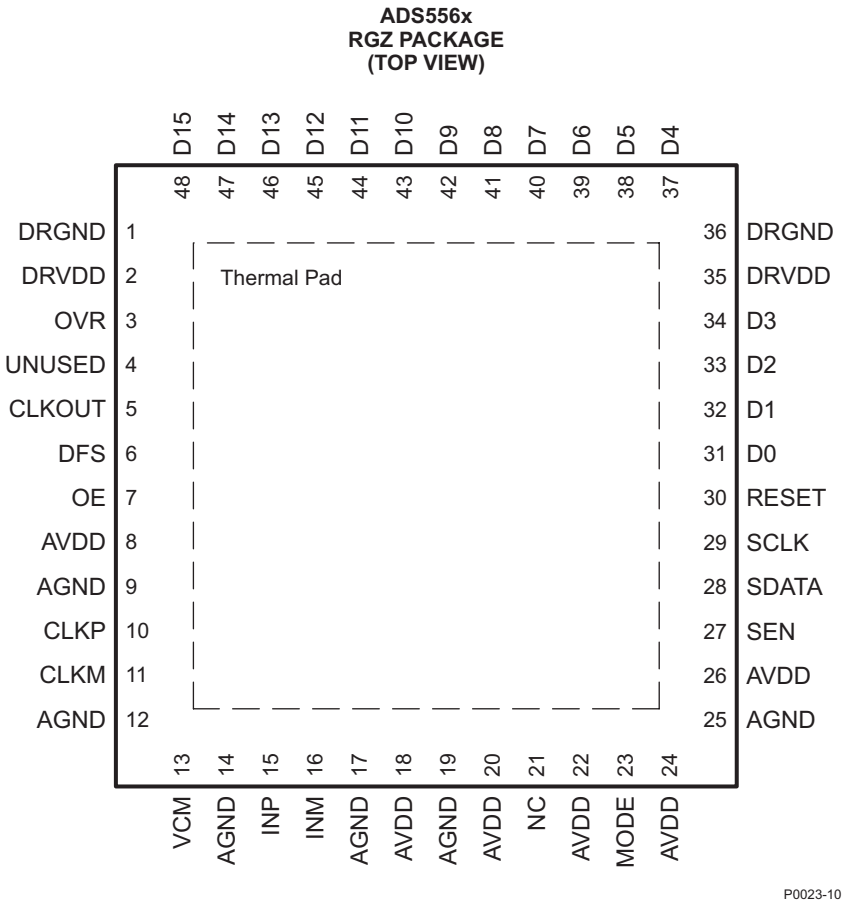


Figure 9. CMOS Mode Pinout

Table 23. PIN ASSIGNMENTS – CMOS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	8, 18, 20, 22, 24, 26	6
AGND	Analog ground	I	9, 12, 14, 17, 19, 25	6
CLKP, CLKM	Differential clock input	I	10, 11	2
INP, INM	Differential analog input	I	15, 16	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.	I/O	13	1
RESET	Serial interface reset input. When using the serial interface, the user should apply a high-going pulse on this pin to reset the internal registers. When the serial interface is not used, the user should tie RESET permanently high. (SCLK, SDATA and SEN can be used as parallel pin controls). The pin has an internal 100-kΩ pull-down resistor to DRGND.	I	30	1
SCLK	This pin functions as serial interface clock input when RESET is low. It functions as LOW SPEED MODE control when RESET is tied high. See Table 5 for detailed information. The pin has an internal 100-kΩ pull-down resistor to DRGND.	I	29	1

Table 23. PIN ASSIGNMENTS – CMOS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
SDATA	This pin functions as serial interface data input when RESET is low. It functions as STANDBY control pin when RESET is tied high. See Table 6 for detailed information. The pin has an internal 100-kΩ pull-down resistor to DRGND.	I	28	1
SEN	This pin functions as serial interface enable input when RESET is low. It functions as CLKOUT edge programmability when RESET is tied high. See Table 7 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	27	1
OE	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	7	1
DFS	Data Format Select input. This pin sets the DATA FORMAT (Twos complement or Offset binary) and the LVDS/CMOS output mode type. See Table 8 for detailed information. The pin has an internal 100-kΩ pull-down resistor to DRGND.	I	6	1
MODE	Mode select input. This pin selects the Internal or External reference mode. See Table 9 for detailed information. The pin has an internal 100-kΩ pull-down resistor to AGND.	I	23	1
CLKOUT	CMOS output clock	O	5	1
D0	CMOS output data D0	O	31	1
D1	CMOS output data D1	O	32	1
D2	CMOS output data D2	O	33	1
D3	CMOS output data D3	O	34	1
D4	CMOS output data D4	O	37	1
D5	CMOS output data D5	O	38	1
D6	CMOS output data D6	O	39	1
D7	CMOS output data D7	O	40	1
D8	CMOS output data D8	O	41	1
D9	CMOS output data D9	O	42	1
D10	CMOS output data D10	O	43	1
D11	CMOS output data D11	O	44	1
D12	CMOS output data D12	O	45	1
D13	CMOS output data D13	O	46	1
D14	CMOS output data D14	O	47	1
D15	CMOS output data D15	O	48	1
OVR	Out-of-range indicator, CMOS level signal	O	3	1
DRVDD	Digital and output buffer supply	I	2, 35	2
DRGND	Digital and output buffer ground	I	1, 36	2
UNUSED	Unused pin in CMOS mode	-	4	1
PAD	Connect the PAD to the ground plane. See in application section.			1
NC	Do not connect	-	21	1

TYPICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*, 32k Point FFT (unless otherwise noted)

ADS5562 - 80MSPS

FFT for 5 MHz, -1dBFS Input Signal

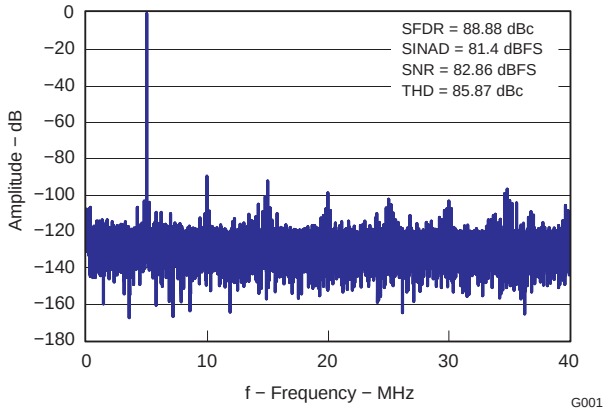


Figure 10.

FFT for 20 MHz, -1dBFS Input Signal

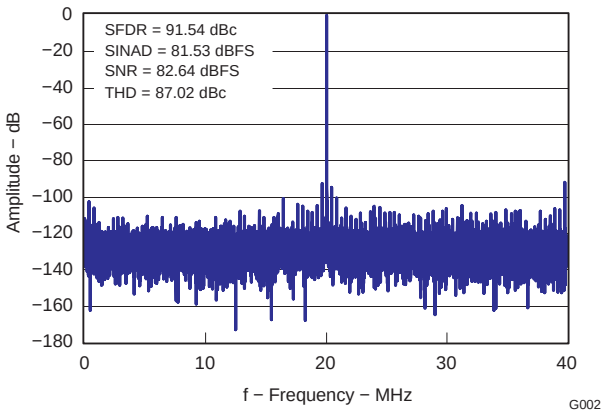


Figure 11.

FFT for 5 MHz, -80dBFS Input Signal (Small signal)

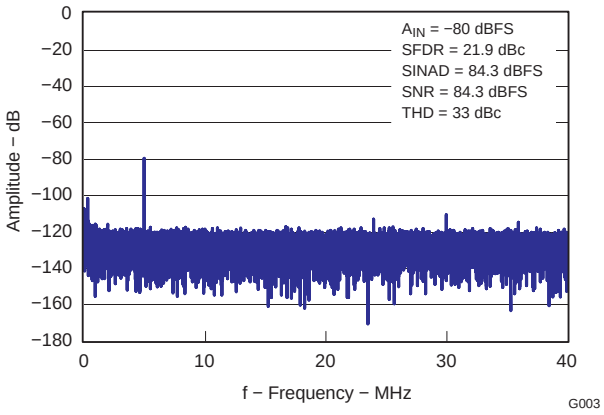


Figure 12.

Inter-modulation Distortion

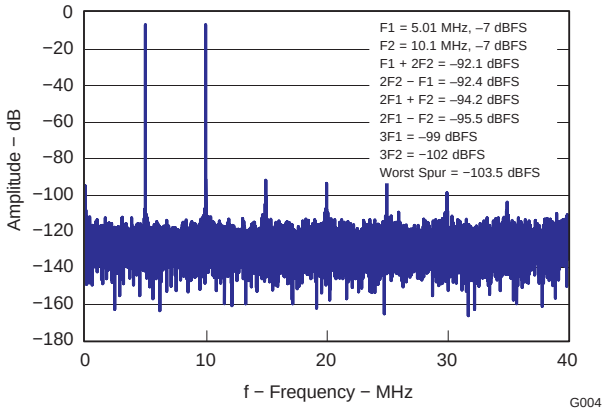


Figure 13.

SNR vs Fin, 0 dB gain

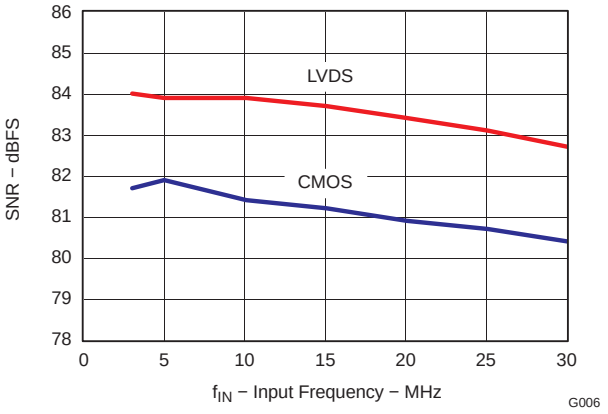


Figure 14.

SFDR vs Fin

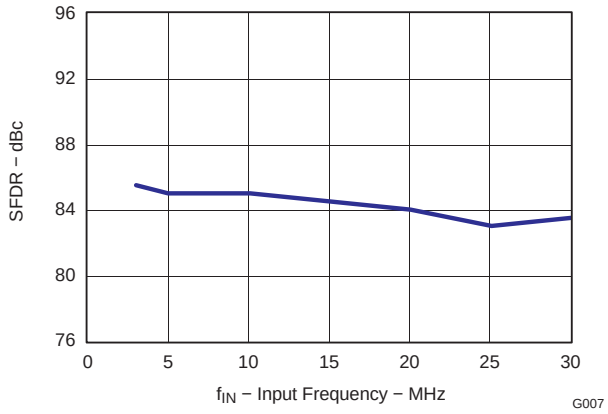


Figure 15.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*, 32k Point FFT (unless otherwise noted)

SFDR Across Fine Gain

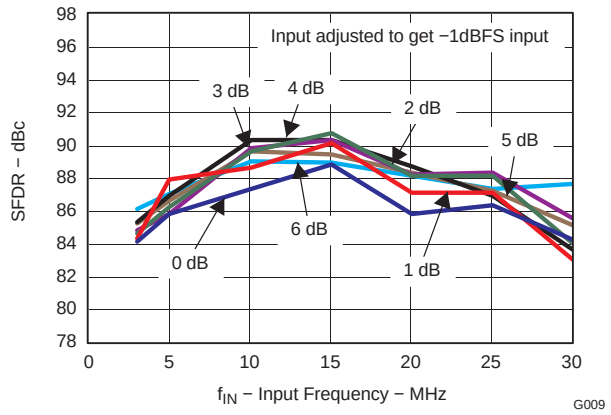


Figure 16.

SNR Across Fine Gain

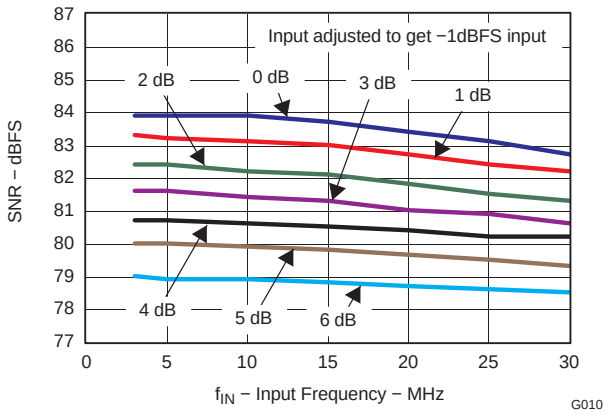


Figure 17.

Performance vs AVDD Supply

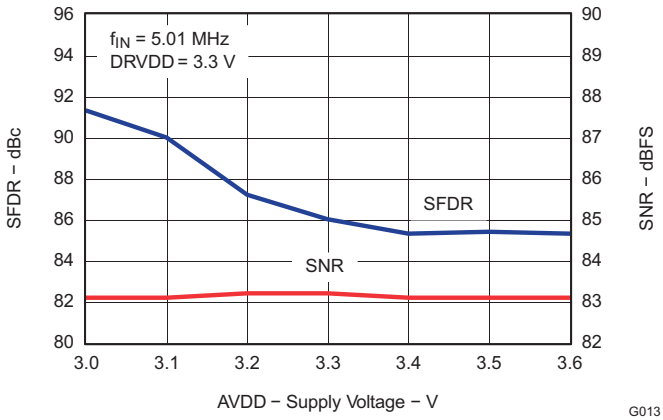


Figure 18.

Performance vs DRVDD Supply

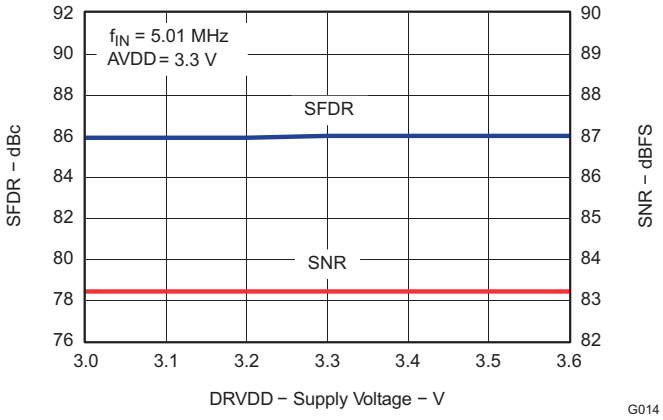


Figure 19.

Performance vs Temperature

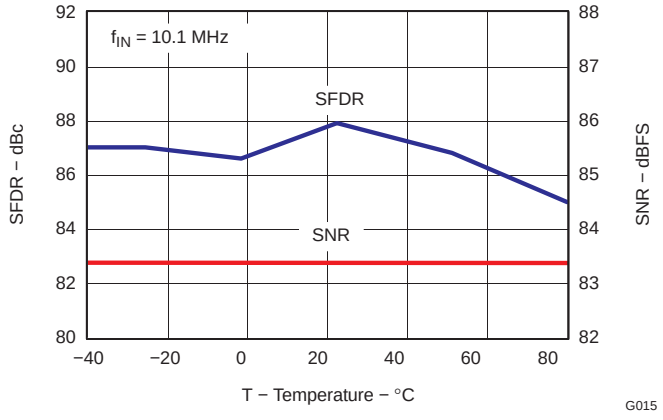


Figure 20.

Performance vs Input Amplitude, 0 dB gain

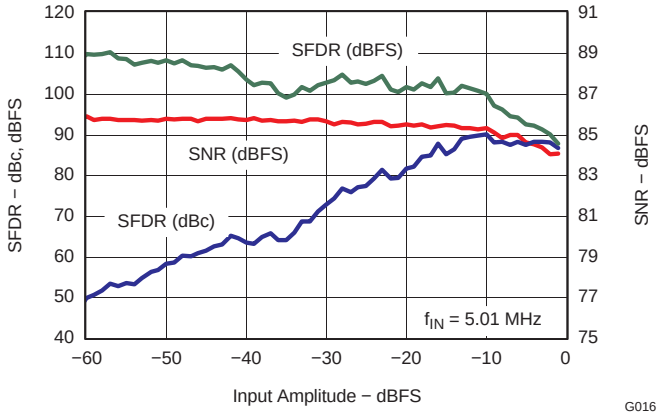


Figure 21.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*, 32k Point FFT (unless otherwise noted)

Performance vs Clock Amplitude

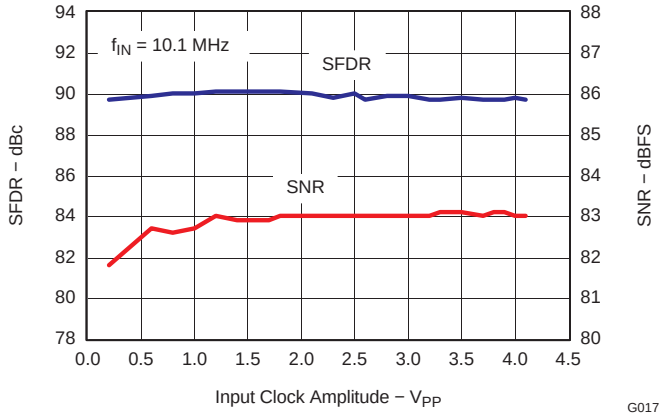


Figure 22.

Performance vs Clock Duty Cycle

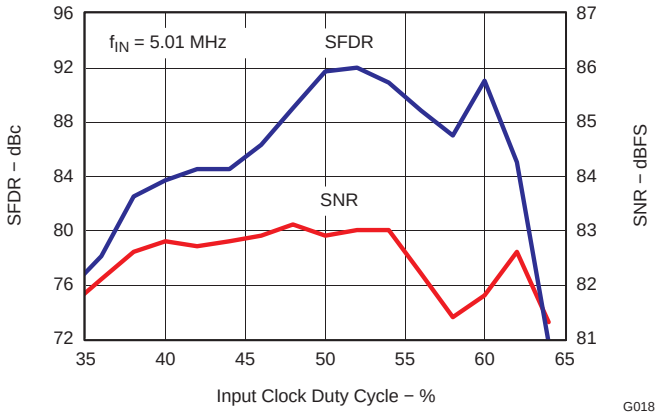


Figure 23.

Output Noise Histogram

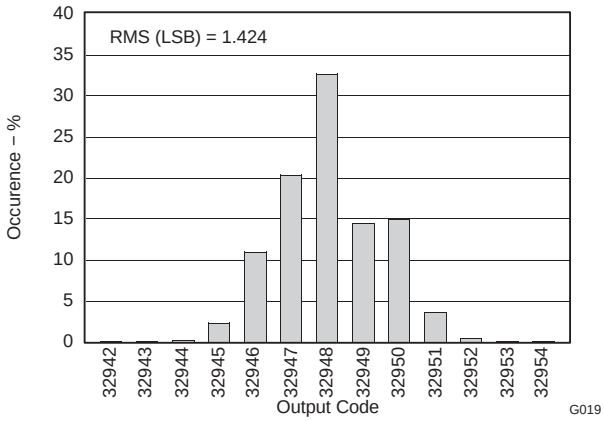


Figure 24.

Performance in External Reference Mode

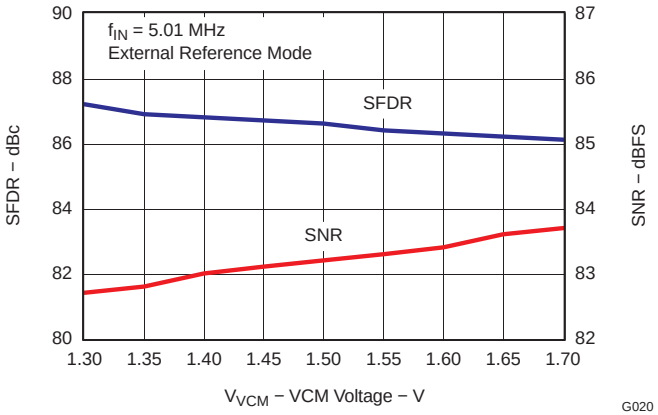


Figure 25.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*, 32k Point FFT (unless otherwise noted)

ADS5560 - 40MSPS

FFT for 5 MHz, -1dBFS Input Signal

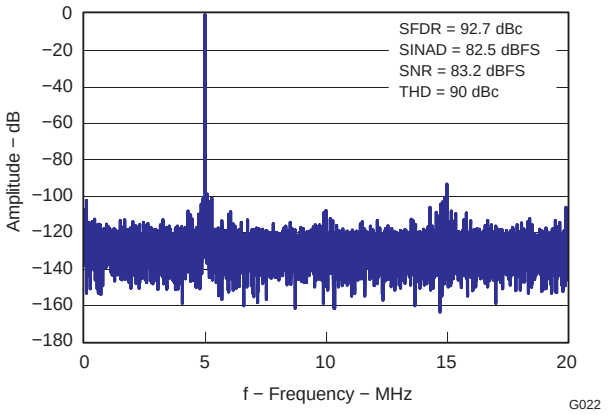


Figure 26.

FFT for 20 MHz, -1dBFS Input Signal

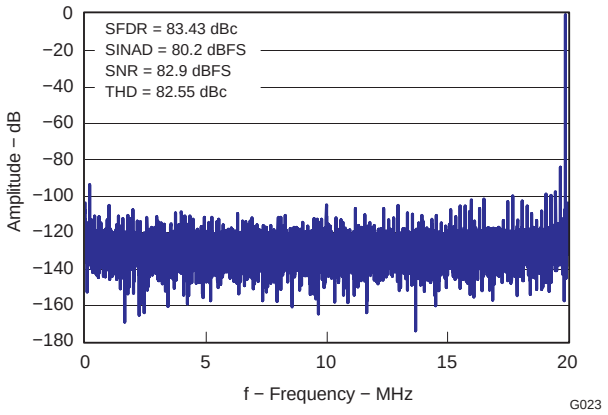


Figure 27.

FFT for 5 MHz, -80dBFS Input Signal

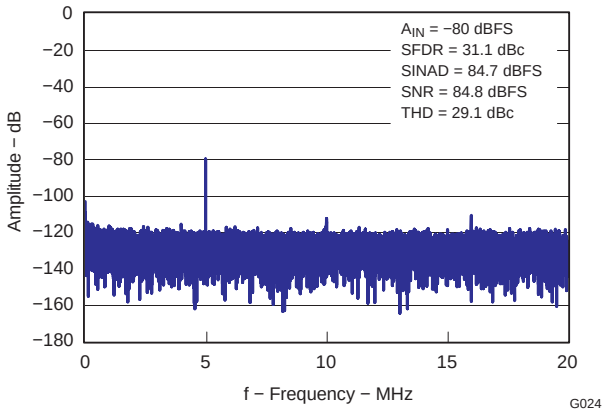


Figure 28.

Inter-modulation Distortion

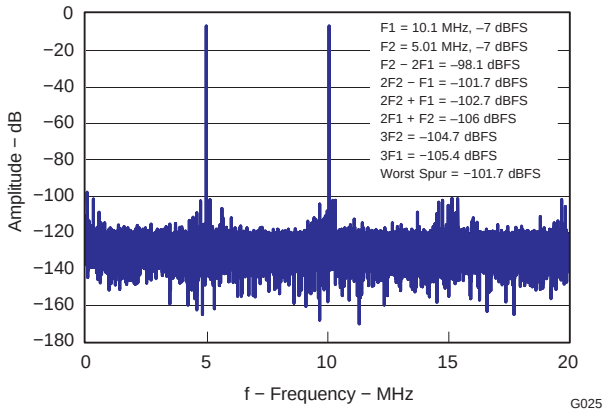


Figure 29.

SNR vs Fin, 0 dB gain

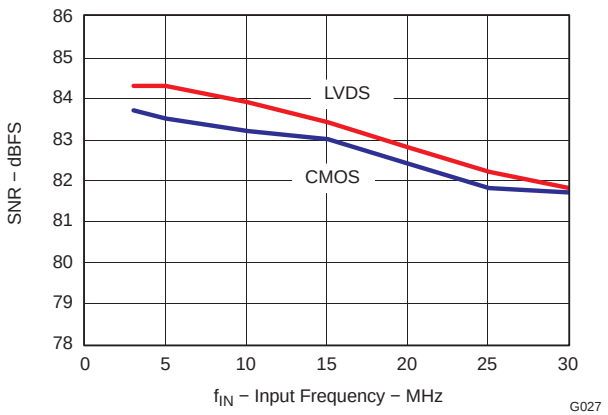


Figure 30.

SFDR vs Fin

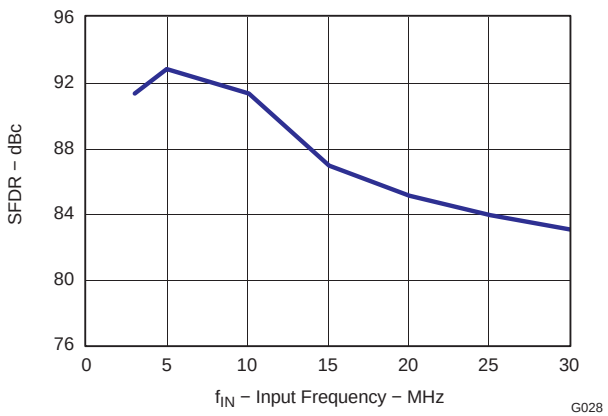


Figure 31.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*, 32k Point FFT (unless otherwise noted)

SFDR Across Fine Gain

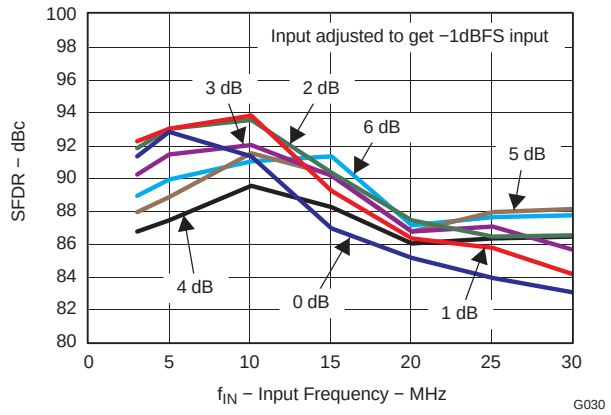


Figure 32.

SNR Across Fine Gain

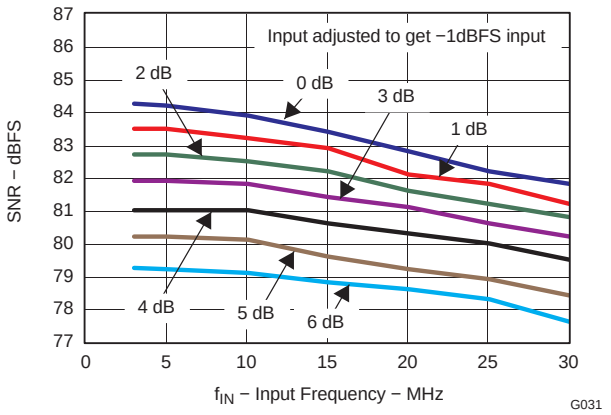


Figure 33.

Performance vs AVDD Supply

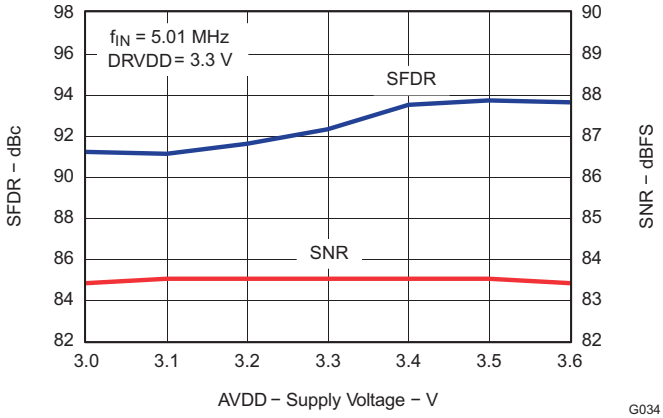


Figure 34.

Performance vs DRVDD Supply

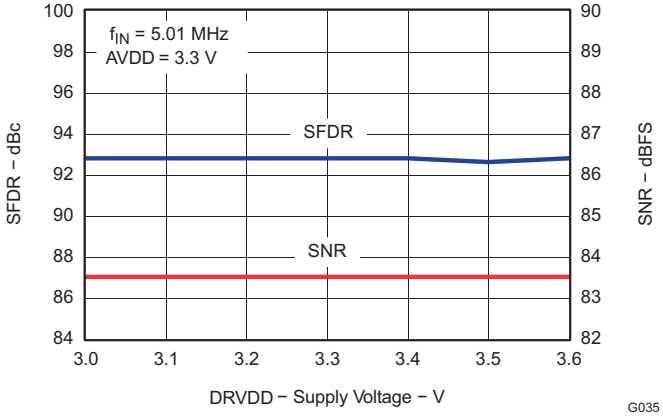


Figure 35.

Performance vs Temperature

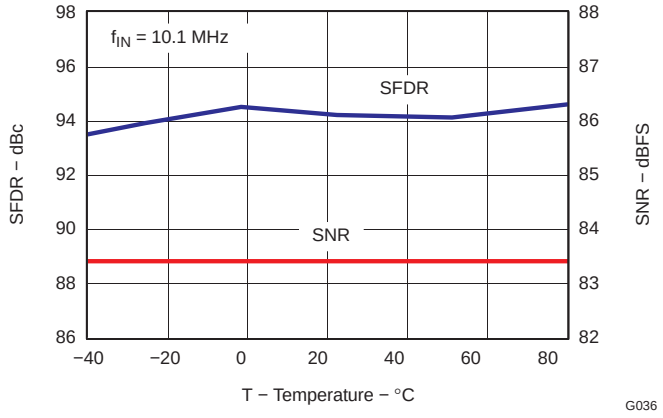


Figure 36.

Performance vs Input Amplitude, 0 dB gain

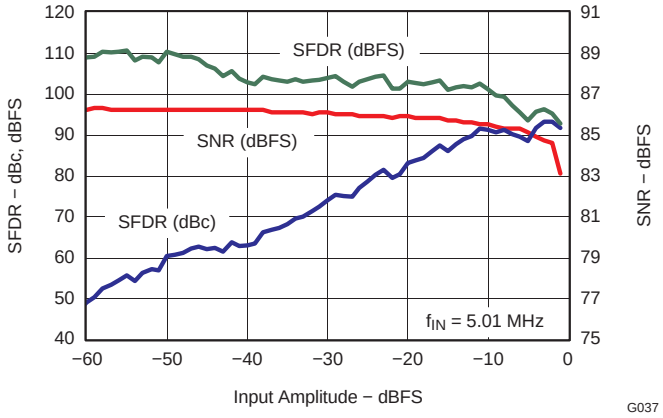


Figure 37.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*, 32k Point FFT (unless otherwise noted)

Performance vs Clock Amplitude

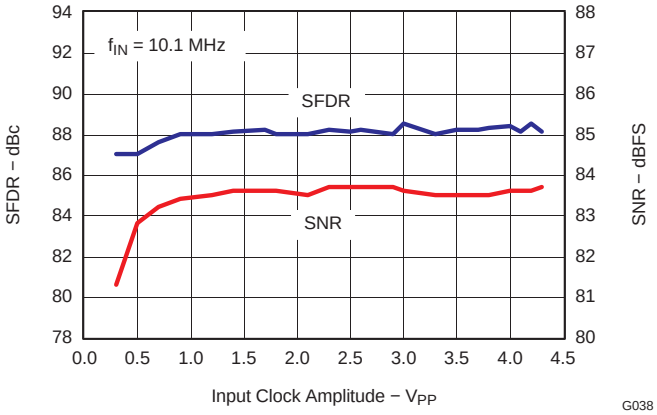


Figure 38.

Performance vs Clock Duty Cycle

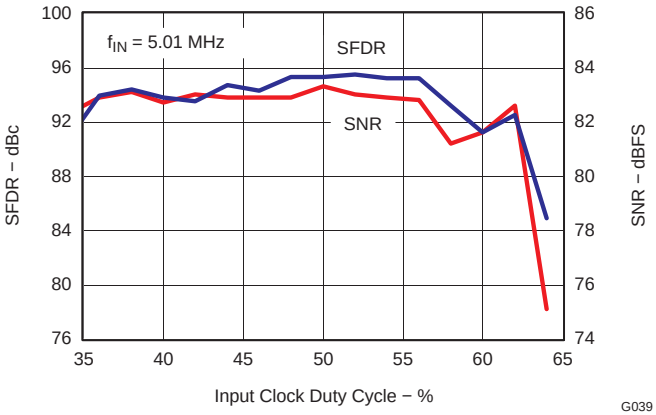


Figure 39.

Output Noise Histogram

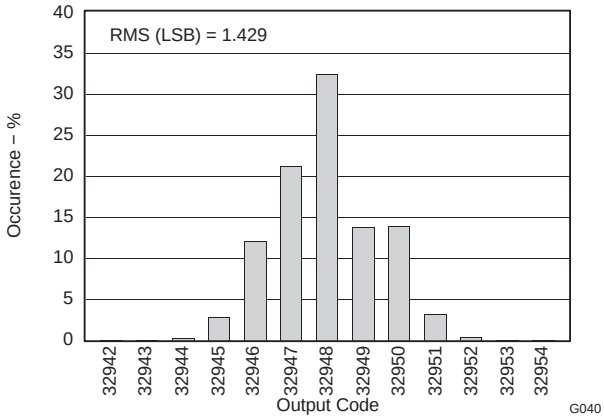


Figure 40.

Performance in External Reference Mode

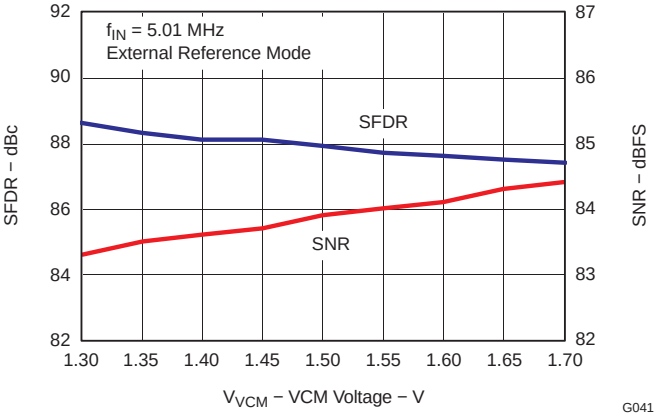


Figure 41.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*, 32k Point FFT (unless otherwise noted)

Valid Up to Max Clock Rate (ADS5562 or ADS5560)

CMRR vs Common-Mode Frequency

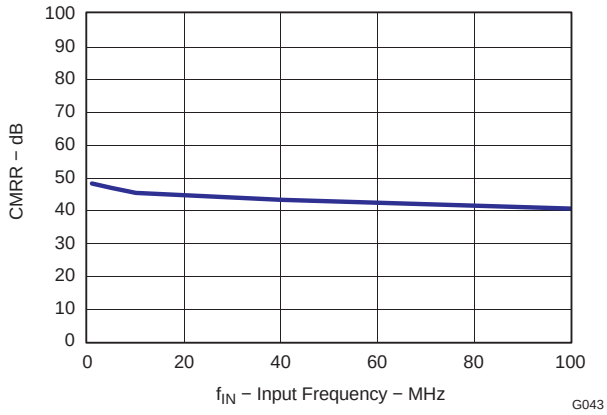


Figure 42.

Power Dissipation vs Sampling Frequency

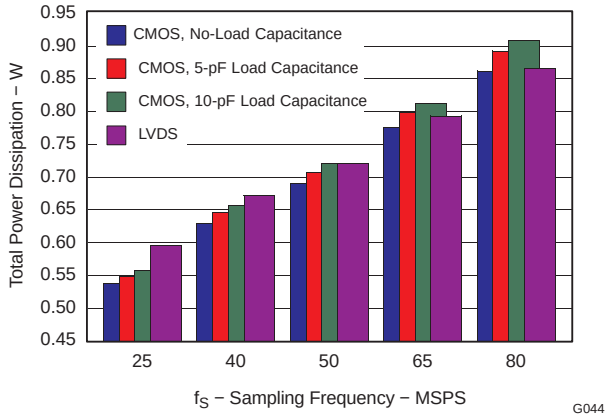


Figure 43.

TYPICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Max Rated, sine wave input clock, 1.5 V_{PP} clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1dB)*, 32k Point FFT (unless otherwise noted)

SFDR Contour, 0 dB Gain

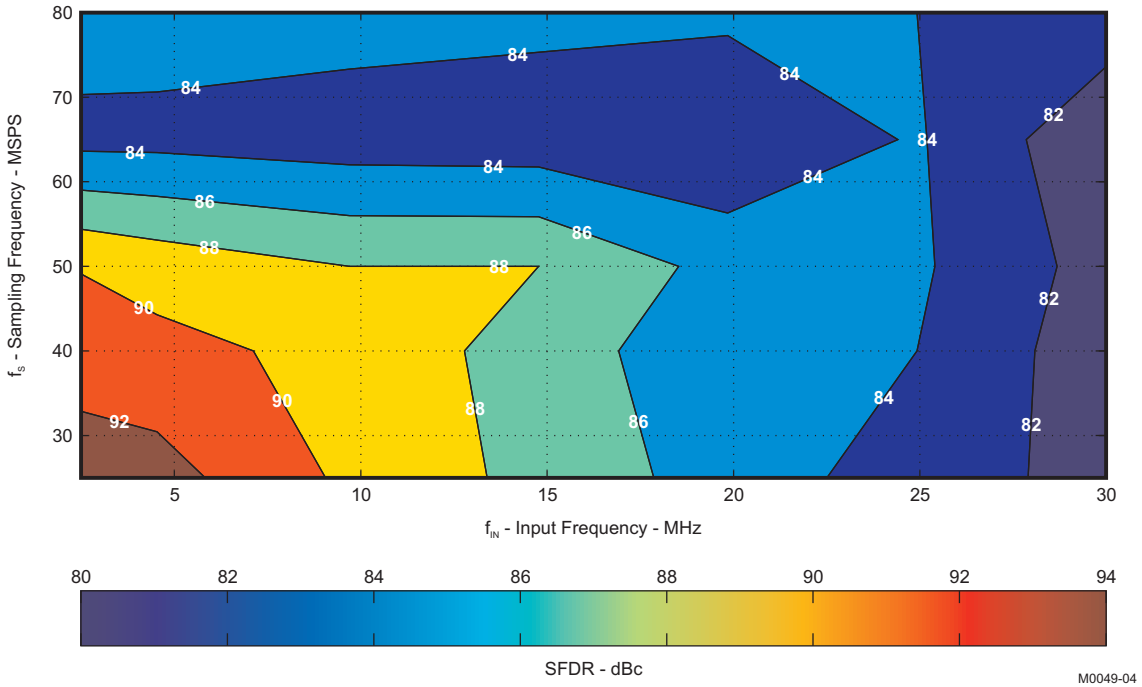


Figure 44.

SNR Contour, 0 dB Gain

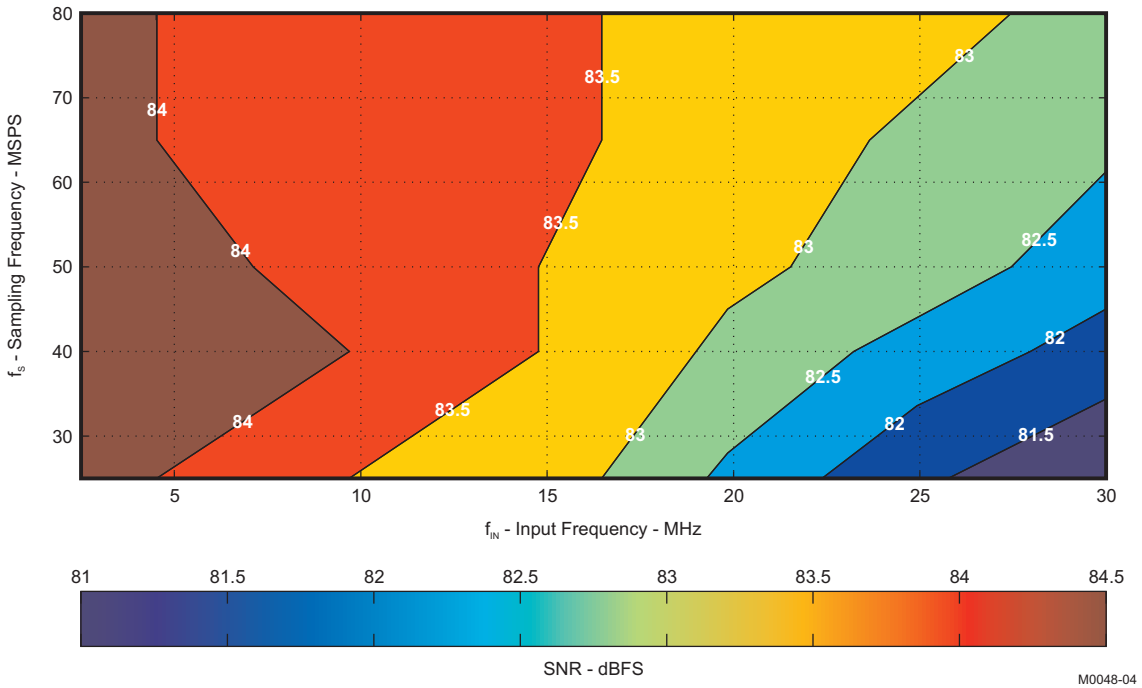


Figure 45.

APPLICATION INFORMATION

THEORY OF OPERATION

ADS556X is a high performance 16-bit A/D converter family with sampling rates up to 80 MSPS. It is based on switched capacitor technology and runs off a single 3.3-V supply. Once the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of small resolution stages. At every clock edge, the sample propagates through the pipeline resulting in a data latency of 16 clock cycles. The output is available as 16-bit data, in DDR LVDS or parallel CMOS and coded in either offset binary or binary 2's complement format.

Analog Input Circuit

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 46.

This differential topology results in good ac-performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V (VCM). For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.9 V and VCM – 0.9 V, resulting in a 3.6-V_{PP} differential input swing.

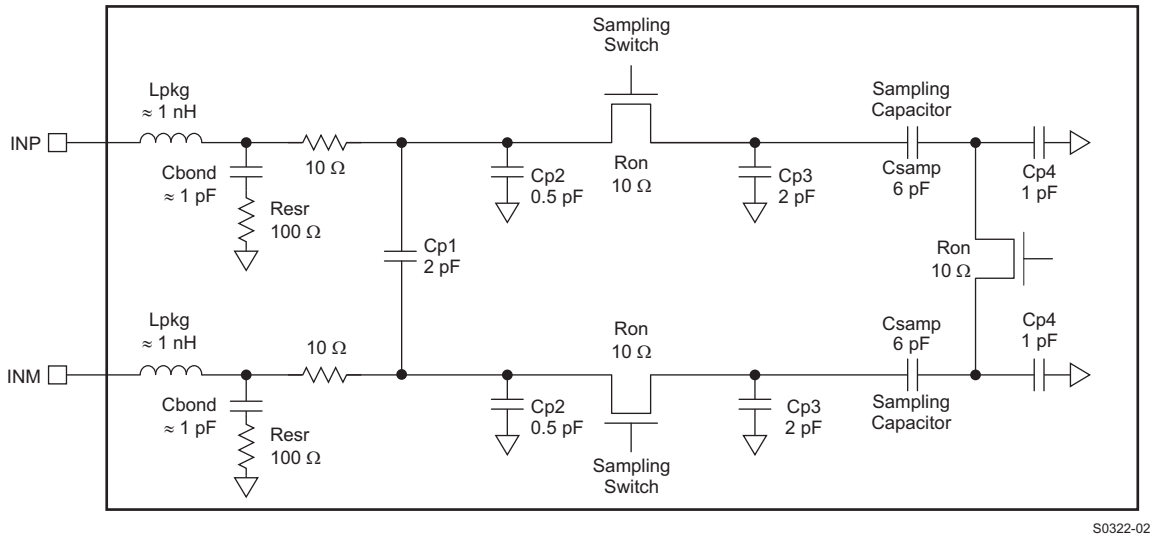


Figure 46. Input Stage

Drive Circuit Recommendations

For optimum performance, the analog inputs have to be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A resistor in series with each input pin (about 15 Ω) is recommended to damp out ringing caused by package parasitics. It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

Note that the device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. The filtering of the glitches can be improved further using an external R-C-R filter.

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 47 and Figure 48 show the impedance (Zin = Rin || Cin) looking into the ADC input pins.

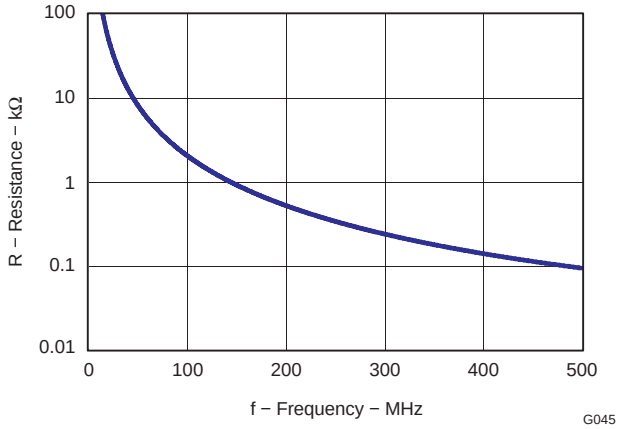


Figure 47. ADC Analog Input Resistance (Rin) Across Frequency

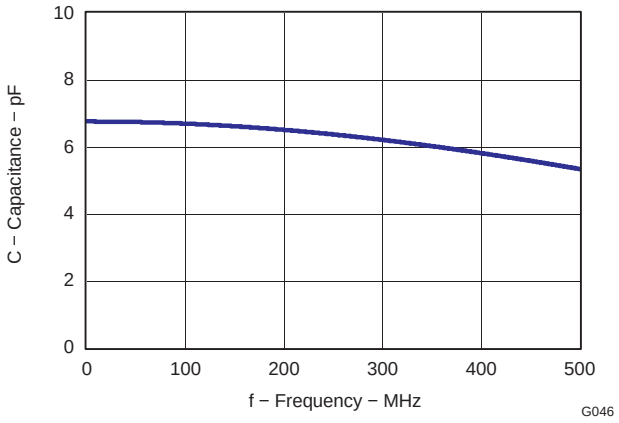


Figure 48. ADC Analog Input Capacitance (Cin) Across Frequency

Example Driving Circuit

An example input configuration using RF transformers is shown in Figure 49. Here, an external R-C-R filter using 22pF has been used. Together with the series inductor (39nH), this combination forms a filter and absorbs the sampling glitches. Due to the relatively large capacitor (22pF) in the R-C-R and the 15 ohms resistors in series with each input pin, this drive circuit has low bandwidth and is suited for low input frequencies.

Note that the drive circuit has been terminated by 50 ohms near the ADC side. The termination is accomplished by a 25 ohms resistor from each input to the 1.5V common-mode (VCM) from the device. This allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair may be required between the two transformers (enclosed by the dashed lines in Figure 49). The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side have to be chosen to get an effective 50 ohms (in the case of 50 ohms source impedance).

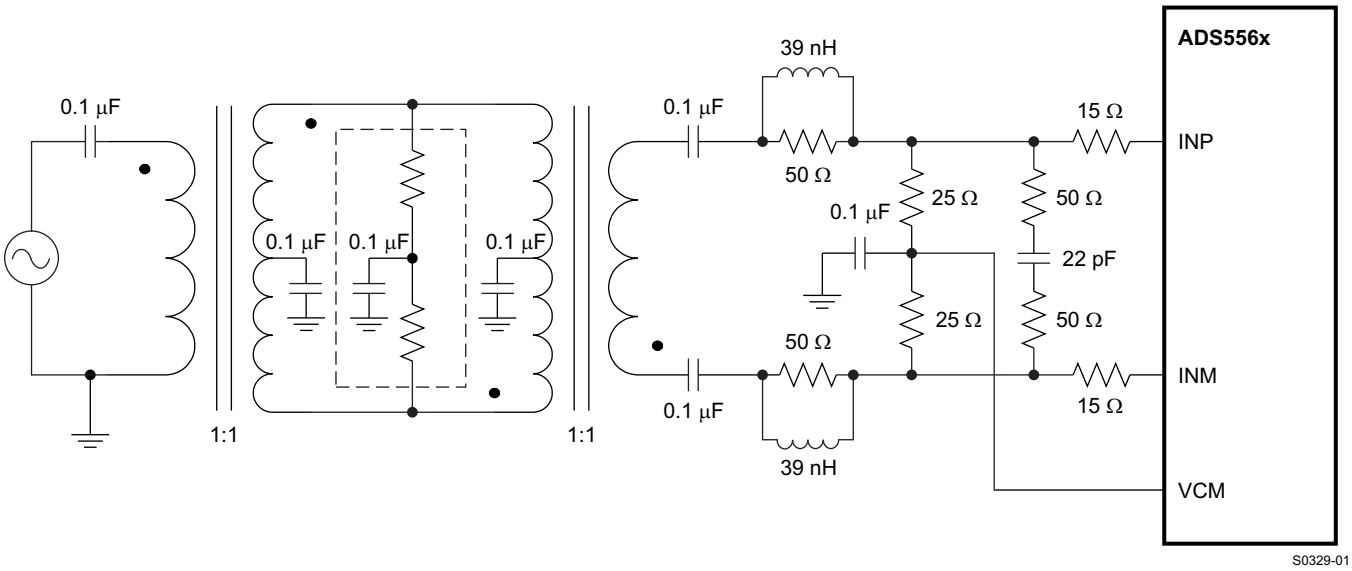


Figure 49. Drive Circuit Using RF transformers

Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1-µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. Each input pin of the ADC sinks a common-mode current in the order of 6uA/MSPS(about 1mA at 80 MSPS) from the external drive circuit.

Reference

ADS556X has built-in internal reference that does not require external components. Design schemes are used to linearize the converter load seen by the reference; this and the integration of the requisite reference capacitors on-chip eliminates the need for external decoupling capacitors. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by controlling the MODE pin 23 (see Table 9 for details) or by programming the serial interface register bit **<REF>**.

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 1. In this mode, the 1.5 V common-mode voltage to bias the input pins has to be generated externally.

$$\text{Full-scale differential input voltage, pp} = (\text{Voltage forced on VCM pin}) \times 2.67 \times G$$
$$\text{where } G = 10^{-(\text{Fine gain in dB}/20)} \quad (1)$$

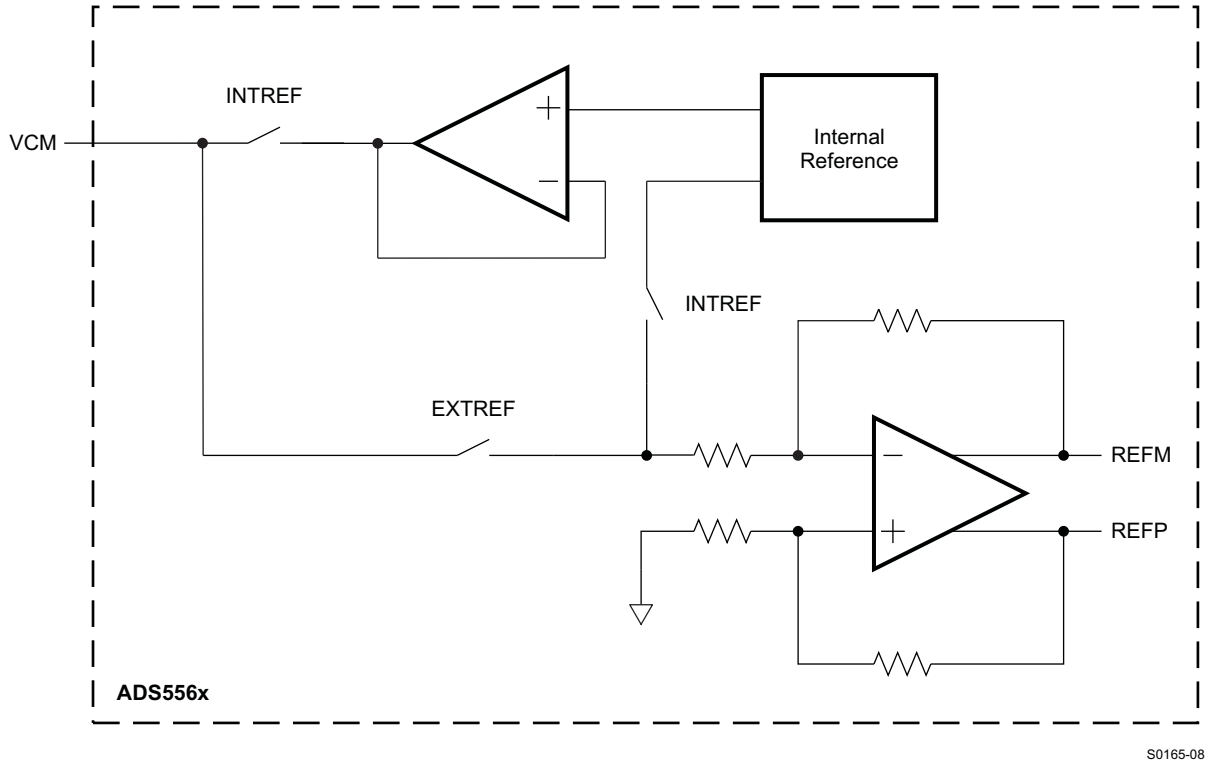


Figure 50. Reference Section

Programmable Fine Gain

ADS556X has programmable fine gain from 0 dB to 6dB in steps of 1 dB. The corresponding full-scale input range varies from $3.6V_{PP}$ down to $2V_{PP}$. The fine gain is useful, when lower full-scale input ranges are used to get SFDR improvement (See Figure 15 and Figure 31). This is accompanied by corresponding degradation in SNR (see Figure 16 and Figure 32). The gain can be programmed using the register bits **GAIN** (Table 15).

After reset, the device is initialized to 1 dB fine gain when configured as Serial Interface Mode. The gain of the device in Parallel Mode will depend on the voltage applied on the SCLK pin. See Table 5 for details.

Table 24. Full-scale Input Range Across Gains (Serial Interface Mode)

Gain, dB	Corresponding full-scale input range, Vpp
0	3.56 (1)
1, default after reset	3.56
2	3.20
3	2.85
4	2.55
5	2.27
6	2.00

(1) Note that with 0 dB gain, the full-scale input range continues to be 3.56Vpp. This means that the output code range will be 58409 LSBs (or 1dB below 65536).

Low Frequency Noise Suppression

The low-frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the low frequency band of DC to 1 MHz. Setting this mode shifts the low-frequency noise of the ADS556X to approximately (Fs/2), thereby moving the noise floor around dc to a much lower value. Register bit <LF NOISE SUPPRESSION> enables this mode. As Figure 52 shows, when the mode is enabled, the noise floor from DC to 1 MHz improves significantly. The low frequency noise components get shifted to the region around Fs/2 (Figure 53).

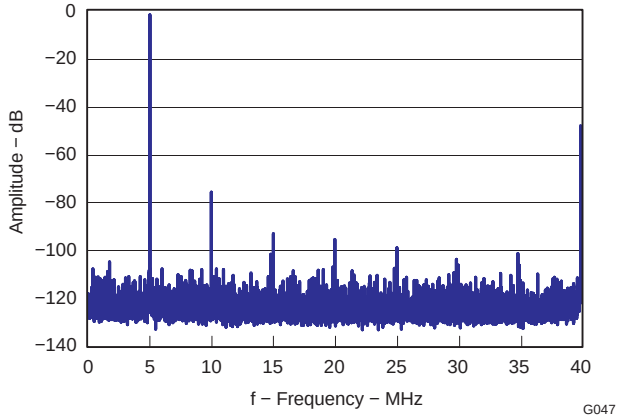


Figure 51. Spectrum with LF Noise Suppression Enabled (Fs=80 MSPS)

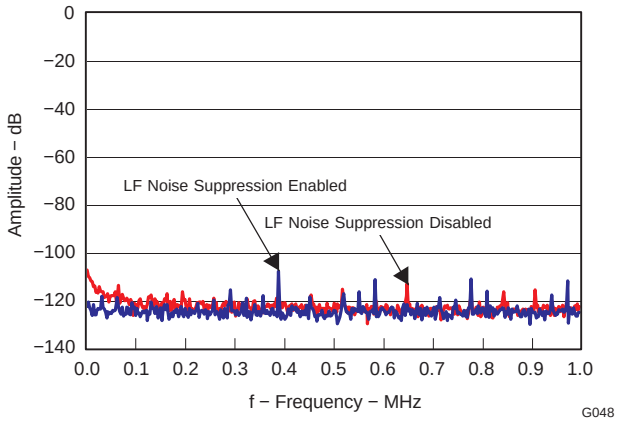


Figure 52. Zoomed Spectrum (dc to 1 MHz) with LF Noise Suppression Enabled (Fs=80 MSPS)

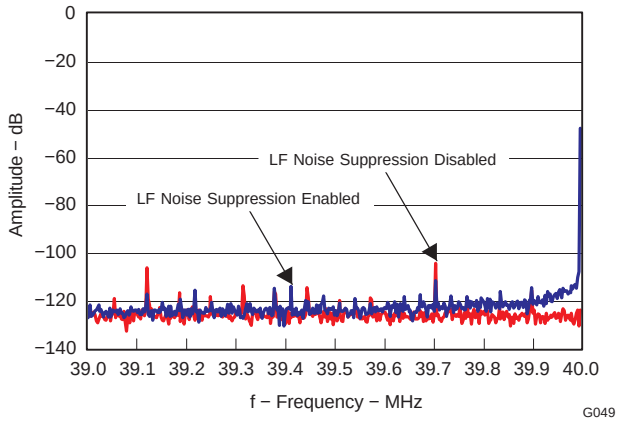


Figure 53. Zoomed Spectrum (39 to 40 MHz) with LF Noise Suppression Enabled (Fs=80 MSPS)

Low Sampling Frequency Operation

For best performance at high sampling frequencies, ADS556X uses a clock generator circuit to derive internal timing for the ADC. The clock generator operates from 80 MSPS down to 25 MSPS in the DEFAULT SPEED mode. The ADC enters this mode after applying reset (with serial interface configuration) or by tying SCLK pin to low (with parallel configuration).

For low sampling frequencies (below 25 MSPS), the ADC must be put in the LOW SPEED mode. This mode can be entered by

- setting the register bit <LOW SPEED> (Table 13) through the serial interface, OR
- tying the SCLK pin to high (see Table 5) using the parallel configuration.

Clock Input

ADS556X clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors that connect CLKP and CLKM to VCM, as shown in Figure 54. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS, and LVCMOS clock sources (Figure 55, Figure 56, Figure 57, and Figure 58).

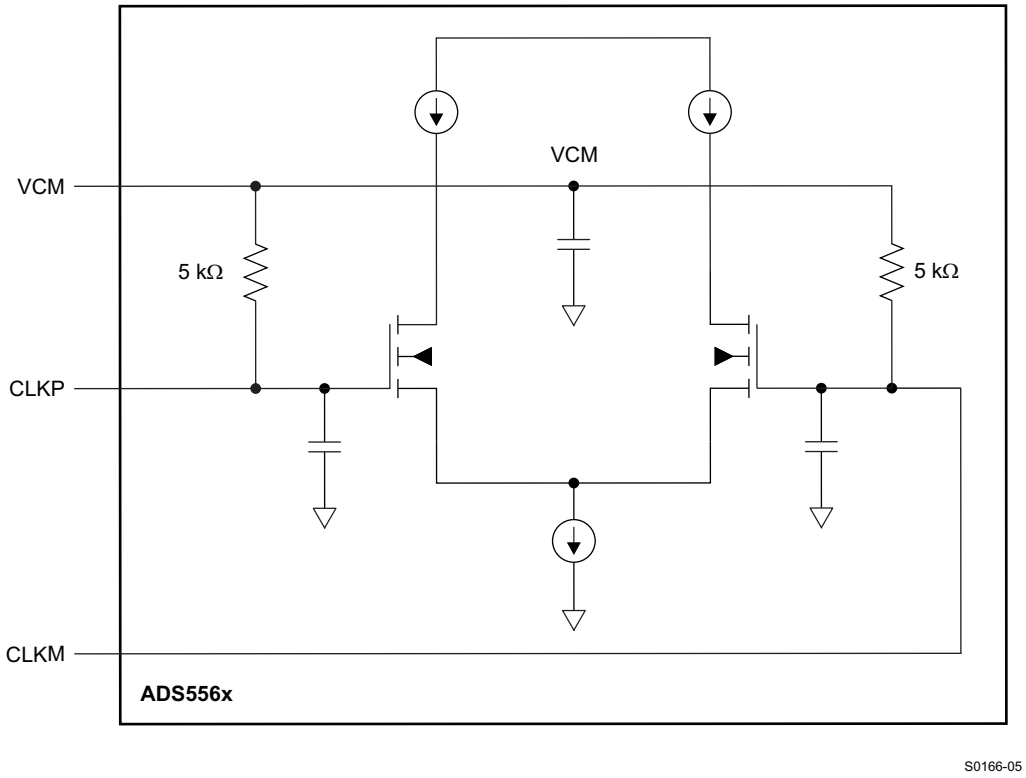


Figure 54. Clock Inputs

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input. Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with 0.1µF capacitor, as shown in Figure 58.

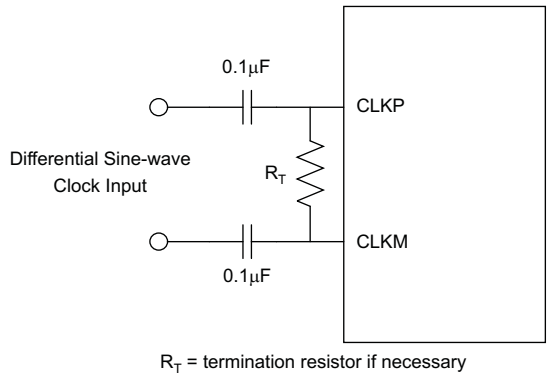


Figure 55. Differential Sine-Wave Clock Driving Circuit

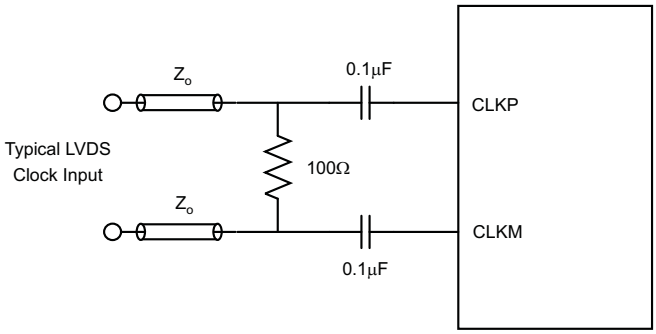


Figure 56. Typical LVDS Clock Driving Circuit

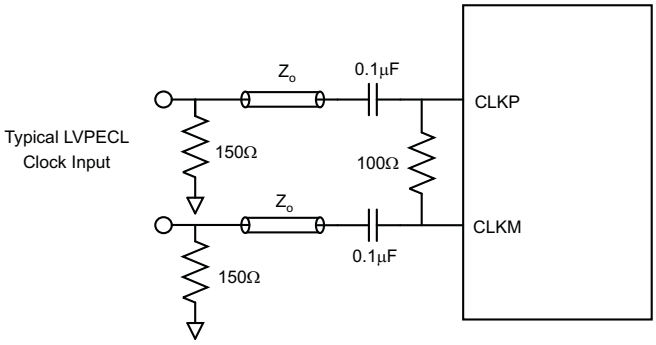


Figure 57. Typical LVPECL Clock Driving Circuit

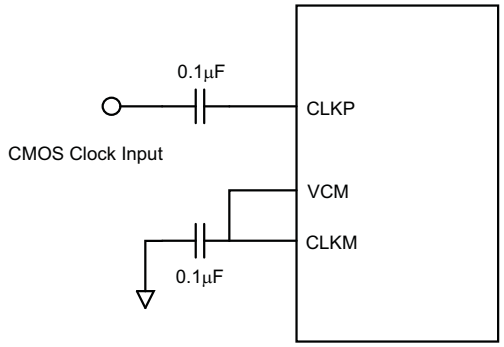


Figure 58. Typical LVCMOS Clock Driving Circuit

For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is little change in performance with a non-50% duty cycle clock input.

Power Down

ADS556X has three power-down modes – global STANDBY, output buffer disabled, and input clock stopped.

Global STANDBY

This mode can be initiated by controlling SDATA or by setting the register bit **<STBY>** through the serial interface. In this mode, the A/D converter, reference block and the output buffers are powered down resulting in reduced total power dissipation of about 155 mW. The wake-up time from global power down to valid data is typically 60 µs.

Output Buffer Disable

The output buffers can be disabled using OE pin in both the LVDS and CMOS modes. With the buffers disabled, the digital outputs are three-stated. The wake-up time from this mode to data becoming valid in normal mode is typically 700 ns in LVDS mode and 200 ns in CMOS mode.

Input Clock Stop

The converter enters this mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 125 mW and the wake-up time from this mode to data becoming valid in normal mode is typically 80 µs.

Power Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

Output Interface

ADS556X provides 16-bit data, an output clock synchronized with the data and an out-of-range indicator that goes high when the output reaches the full-scale limits. In addition, output enable control (OE) is provided to power down the output buffers and put the outputs in high-impedance state.

Two output interface options are available – Double Data Rate (DDR) LVDS and parallel CMOS. They can be selected using the DFS or the serial interface register bit **<ODI>** (see Table 8).

DDR LVDS Outputs

In this mode, the 16 data bits and the output clock are put out using LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair as shown in Figure 59, so there are 8 LVDS output pairs for the data bits and 1 LVDS output pair for the output clock.

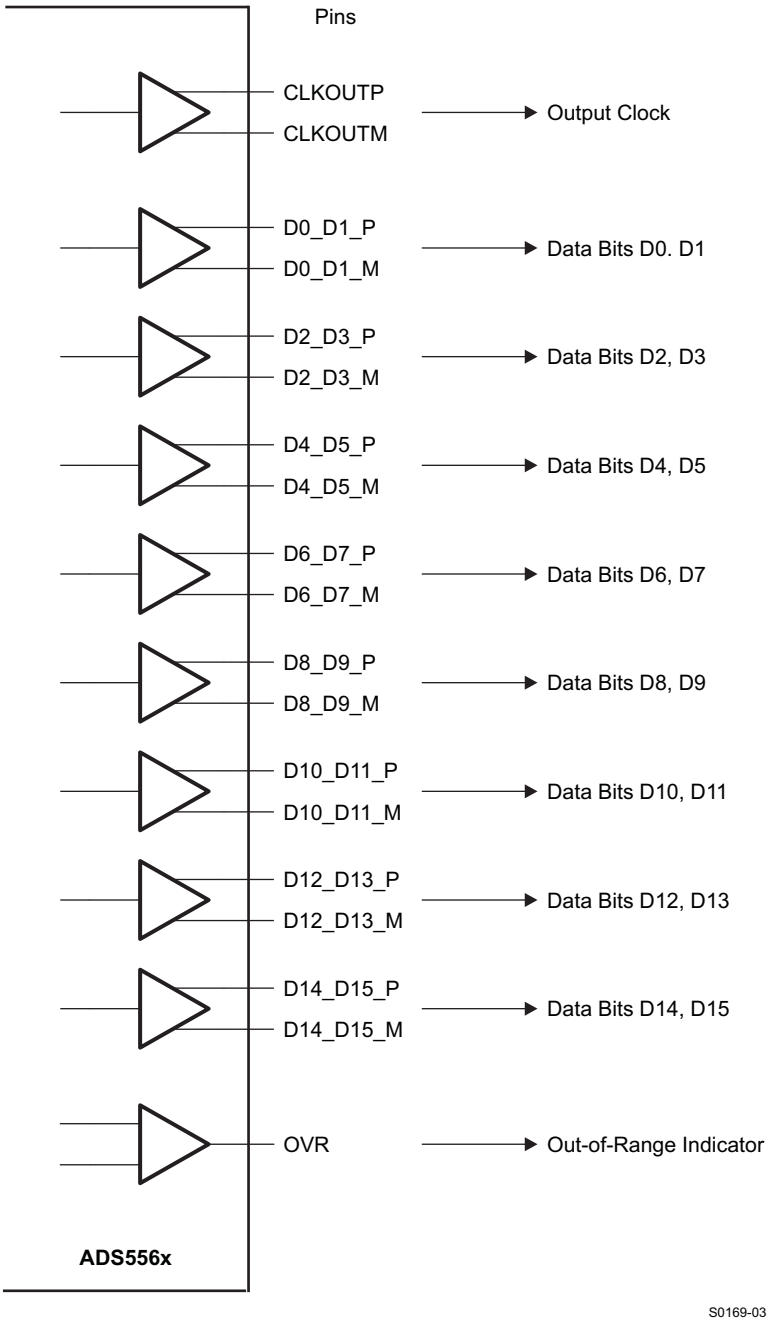


Figure 59. DDR LVDS Outputs

Even data bits (D0, D2...D14) are output at the falling edge of CLKOUTP and the odd data bits (D1, D3...D15) are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all the data bits (see Figure 60).

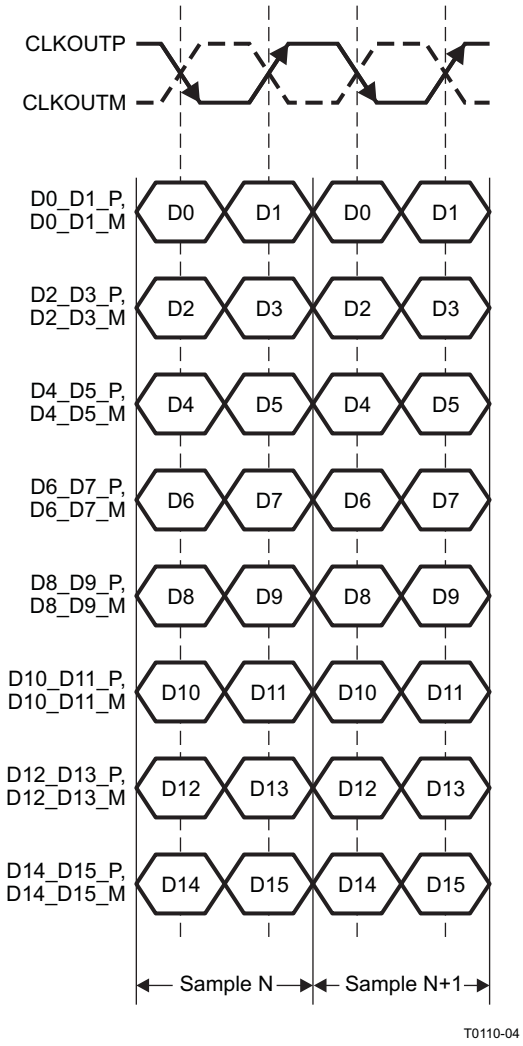


Figure 60. DDR LVDS Interface

LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. When terminated by 100 Ω, this results in logic HIGH of +350 mV and logic LOW of -350 mV. The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.95 mA using the serial interface. In addition, there exists a current double mode, where this current is doubled for the data and output clock buffers.

Both the buffer current programming and the current double mode can be done separately for the data buffers and the output clock buffer (register bits <LVDS CURR>).

LVDS Buffer Internal Termination

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. These termination resistances are available – 325, 200, and 175 Ω (nominal with ±20% variation). Any combination of these three terminations can be programmed; the effective termination will be the parallel combination of the selected resistances. This results in eight effective terminations from open (no termination) to 75 Ω.

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100 Ω internal and 100 Ω external termination, the voltage swing at the receiver end will be halved (compared to no internal termination). The terminations can be controlled using register bits <DATA TERM> and <CLKOUT TERM>.

The voltage swing can be restored by using the LVDS current double mode (register bit <CURR DOUBLE>).

Parallel CMOS

In this mode, the digital data and output clock are put out as 3.3-V CMOS voltage levels. Each data bit and the output clock is available on a separate pin in parallel. By default, the data outputs are valid during the rising edge of the output clock. The output clock is CLKOUT.

Output Clock Position Programmability

In both the LVDS and CMOS modes, the output clock can be moved around its default position. This can be done using SEN pin (as described in Table 7) or using the serial interface register bits **<CLKOUT POSN>** (Table 12).

Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using DFS pin or the serial interface register bit **<DFS>** (see Table 10). In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0xFFFF in offset binary output format, and 0x7FFF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x8000 in 2s complement output format.

Board Design Considerations

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital and clock sections of the board are cleanly partitioned. See the EVM User Guide (SLWU028) for details on layout and grounding.

Supply de-coupling

As ADS556X already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help to filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins. It is recommended to use separate supplies for the analog and digital supply pins to isolate digital switching noise from sensitive analog circuitry. In case only a single 3.3V supply is available, it should be routed first to AVDD. It can then be tapped and isolated with a ferrite bead (or inductor) with decoupling capacitor, before being routed to DRVDD.

Exposed thermal pad

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes QFN Layout Guidelines (SLOA122) and QFN/SON PCB Attachment (SLUA271).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Jitter

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Sample Rate

The maximum conversion rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Sample Rate

The minimum conversion rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10}\frac{P_S}{P_N} \quad (2)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10}\frac{P_S}{P_N + P_D} \quad (3)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (4)$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10}\frac{P_S}{P_N} \quad (5)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Voltage Overload Recovery

The number of clock cycles taken to recover to less than 1% error for a 6-dB overload on the analog inputs.

REVISION HISTORY

Changes from Original (May 2008) to Revision A **Page**

- Changed Programmable Fine Gain in FEATURES 1
- Added maximum gain to end of second paragraph of DESCRIPTION 1
- Changed Voltage between AVDD to DRVDD to Voltage between AVDD and DRVDD in ABS MAX RATINGS 3
- Added Voltage applied to analog input pins, INP, INM in ABS MAX RATINGS 3
- Added Voltage applied to analog input pins, CLKP, CLKM, MODE in ABS MAX RATINGS 3
- Added Voltage applied to analog input pins, RESET, SCLK, SDATA, SEN, OE, DFS in ABS MAX RATINGS 3
- Changed boundary between DEFAULT SPEED mode and LOW SPEED mode from 30 MSPS to 25 MSPS in RECOMMENDED OPERATING CONDITIONS 4
- Changed t_{ho} to t_h in header row of Table 2 10
- Added (of width greater than 10ns) in USING SERIAL INTERFACE PROGRAMMING ONLY section 12
- Added to Priority last row in Table 4 13
- Changed Parallel Interface Control description for SCLK Control Pin, (SCLK = 0, 3dB gain; SCLK = DRVDD, 1 dB gain) in Table 5 14
- Changed first pargraph in SERIAL INTERFACE section 14
- Added text to Note regarding RESET pulse requirement in Figure 7 16
- Changed SERIAL REGISTER MAP format 17
- Added text to Table 10 Note 17
- Changed Fs > 30 MSPS to Fs > 25 MSPS in <LOW SPEED> 19
- Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions 27
- Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions 28
- Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions 29
- Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions 30
- Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions 31
- Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions 32
- Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions 33
- Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions 34
- Changed Figure 49 37
- Added text to end of Programmable Fine Gain section 38
- Added (Serial Interface Mode) to Table 24 title 38
- Changed LOW SPEED mode boundary from 30 MSPS to 25 MSPS in Low Sampling Frequency Operation section 40
- Added text to Clock Input section 40
- Changed Clock Input section paragraphs and 4 illustrations 41

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5560IRGZ25	ACTIVE	VQFN	RGZ	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5560	Samples
ADS5560IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5560	Samples
ADS5560IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5560	Samples
ADS5562IRGZ25	ACTIVE	VQFN	RGZ	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5562	Samples
ADS5562IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5562	Samples
ADS5562IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ5562	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

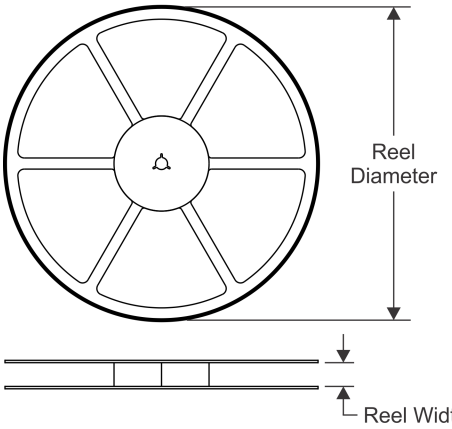
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

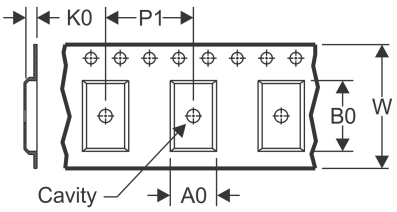
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

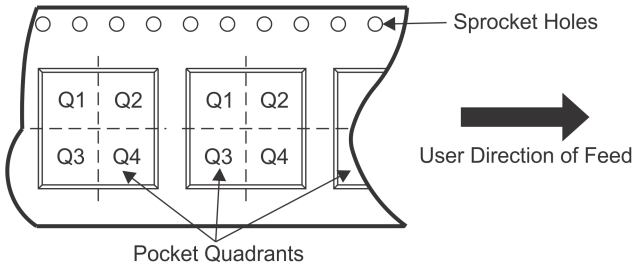


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

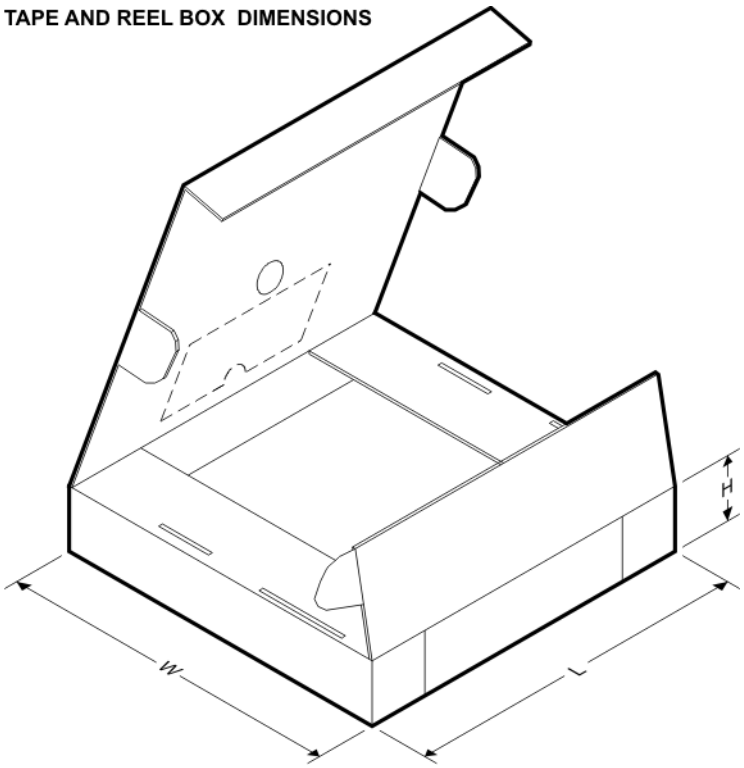
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5560IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS5560IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS5562IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS5562IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

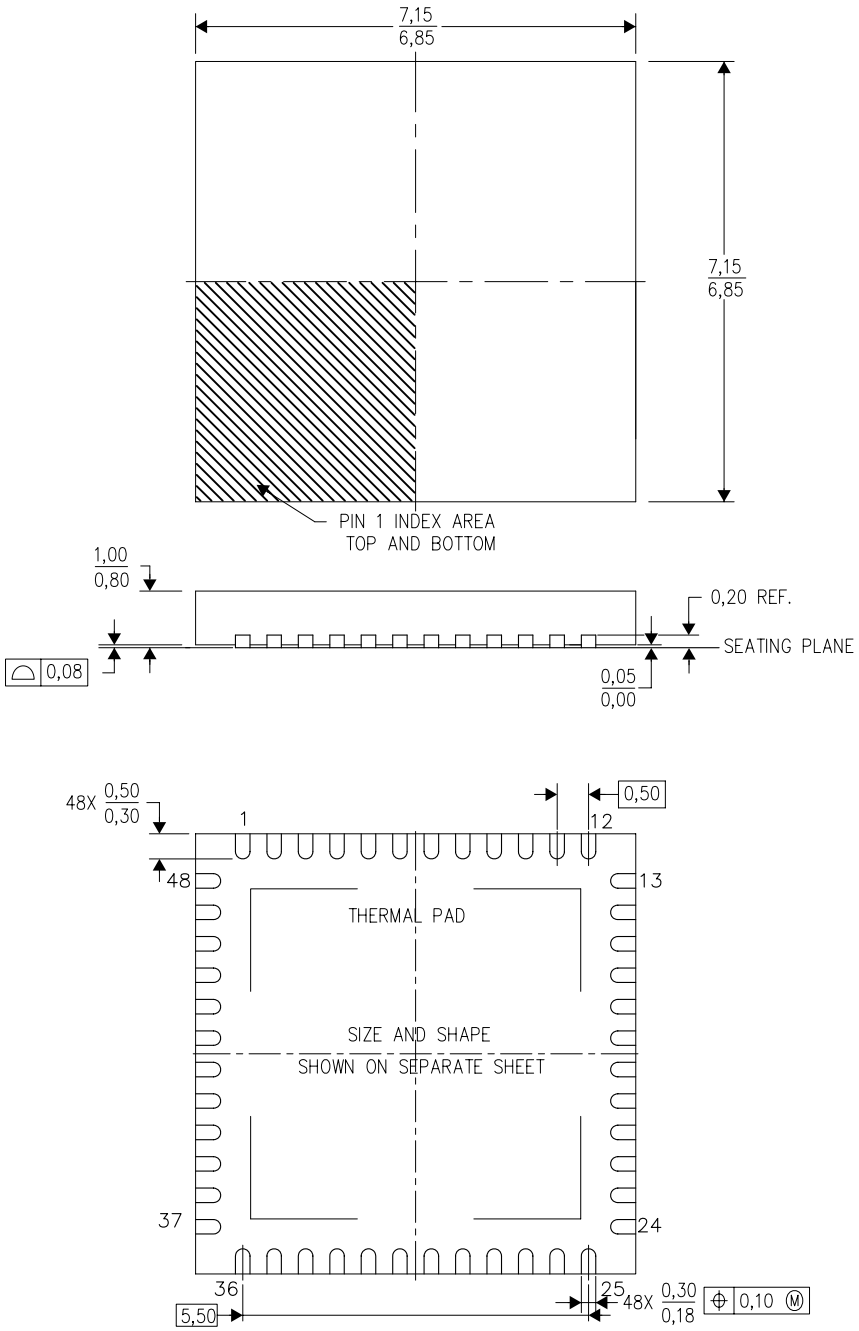
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5560IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS5560IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS5562IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS5562IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

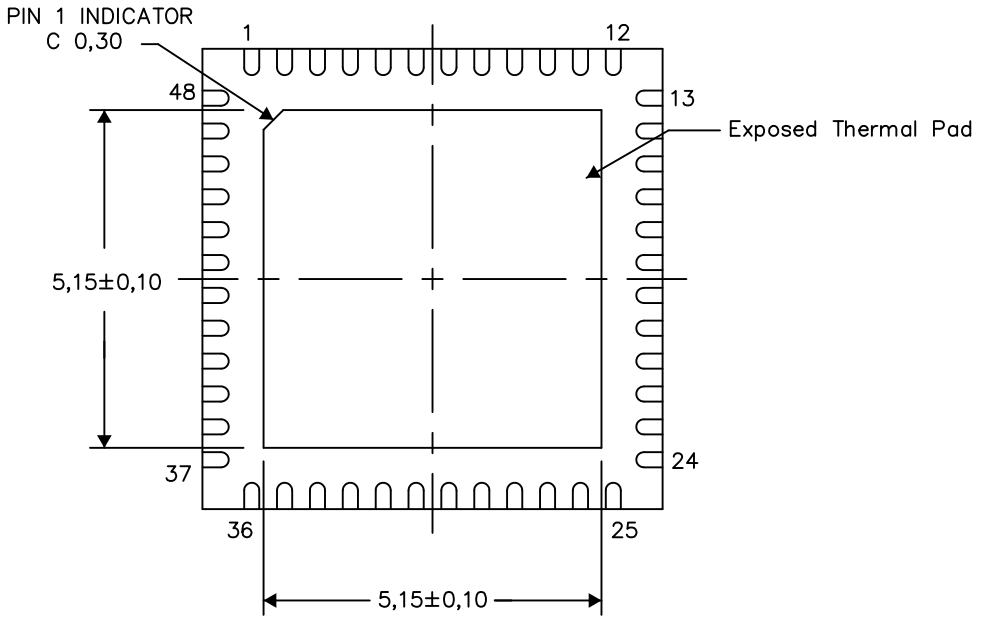
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



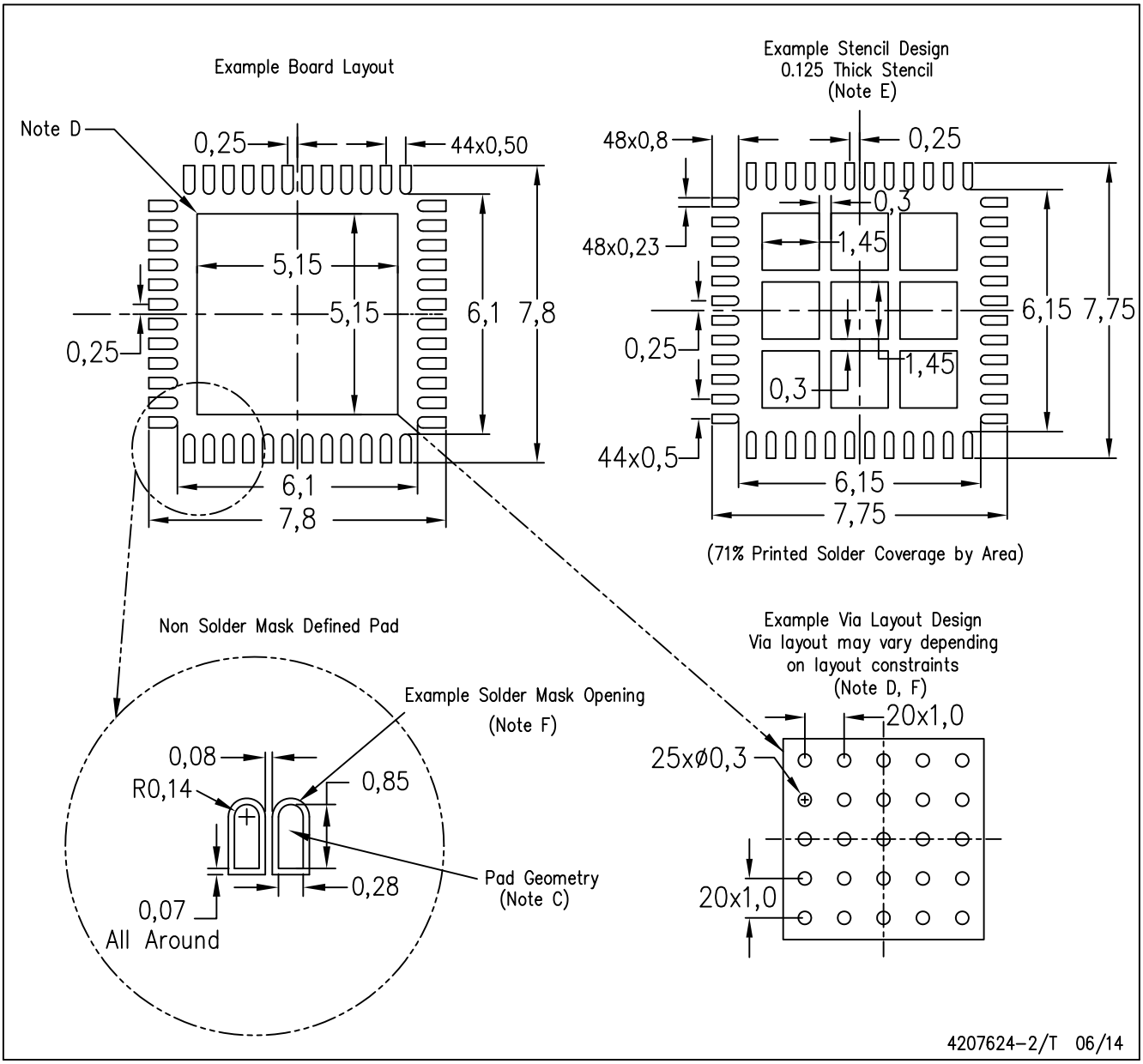
Bottom View

Exposed Thermal Pad Dimensions

4206354–2/Y 06/14

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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