

FEATURES

Ultrawideband frequency range: 100 MHz to 40 GHz

Attenuation range: 2 dB steps to 30 dB

Low insertion loss

1.7 dB to 18 GHz

2.2 dB to 26 GHz

3.5 dB to 40 GHz

Attenuation accuracy

±(0.1 + 2.0%) of attenuation state up to 18 GHz

±(0.2 + 2.5%) of attenuation state up to 26 GHz

±(0.5 + 10.0%) of attenuation state up to 40 GHz

Typical step error

±0.15 dB to 18 GHz

±0.20 dB to 26 GHz

±0.60 dB to 40 GHz

High input linearity

P0.1dB insertion loss state: 30 dBm

P0.1dB other attenuation states: 26 dBm

IP3: 50 dBm typical

High RF input power handling: 26 dBm average, 30 dBm peak

Tight distribution in relative phase

No low frequency spurious signals

SPI and parallel mode control, CMOS/LVTTL compatible

RF amplitude settling time (0.1 dB of final RF output): 230 ns

2.5 mm × 2.5 mm, 16-terminal LGA package

Pin compatible with [ADRF5721](#), low frequency cutoff version

APPLICATIONS

Industrial scanners

Test and instrumentation

Cellular infrastructure: 5G millimeter wave

Military radios, radars, electronic counter measures (ECMs)

Microwave radios and very small aperture terminals (VSATs)

GENERAL DESCRIPTION

The ADRF5731 is a silicon, 4-bit digital attenuator with a 30 dB attenuation control range in 2 dB steps.

This device operates from 100 MHz to 40 GHz with better than 3.5 dB of insertion loss. The ATTIN port of the ADRF5720 has a radio frequency (RF) input power handling capability of 26 dBm average and 30 dBm peak for all states.

The ADRF5731 requires a dual supply voltage of +3.3 V and -3.3 V. The device features serial peripheral interface (SPI), parallel mode control, and complementary metal-oxide semiconductor (CMOS)/low voltage transistor to transistor logic (LVTTL) compatible controls.

Rev. 0

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FUNCTIONAL BLOCK DIAGRAM

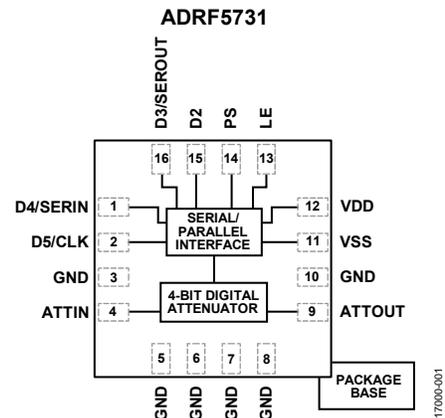


Figure 1.

The ADRF5731 is pin compatible with the [ADRF5721](#) low frequency cutoff version, which operates from 9 kHz to 40 GHz.

The ADRF5731 RF ports are designed to match a characteristic impedance of 50 Ω.

The ADRF5731 comes in a 16-terminal, 2.5 mm × 2.5 mm, RoHS compliant, land grid array (LGA) package and operates from -40°C to +105°C.

TABLE OF CONTENTS

Features	1	Input Power Compression and Third-Order Intercept.....	10
Applications.....	1	Theory of Operation	11
Functional Block Diagram	1	Power Supply.....	11
General Description	1	RF Input and Output	11
Revision History	2	Serial or Parallel Mode Selection	11
Specifications.....	3	Serial Mode Interface.....	12
Electrical Specifications.....	3	Using SEROUT	12
Timing Specifications	5	Parallel Mode Interface.....	13
Absolute Maximum Ratings	6	Applications Information	14
Thermal Resistance	6	Evaluation Board	14
Power Derating Curves.....	6	Probe Matrix Board	16
ESD Caution.....	6	Packaging and Ordering Information	17
Pin Configuration and Function Descriptions.....	7	Outline Dimensions.....	17
Interface Schematics.....	7	Ordering Guide	17
Typical Performance Characteristics	8		
Insertion Loss, Return Loss, State Error, Step Error, and Relative Phase.....	8		

REVISION HISTORY

9/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = -3.3 V, digital voltages = 0 V or VDD, case temperature (T_{CASE}) = 25°C, and a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	
FREQUENCY RANGE		100		40,000	MHz	
INSERTION LOSS (IL)	100 MHz to 10 GHz		1.3		dB	
	10 GHz to 18 GHz		1.7		dB	
	18 GHz to 26 GHz		2.2		dB	
	26 GHz to 35 GHz		2.8		dB	
	35 GHz to 40 GHz		3.5		dB	
RETURN LOSS	ATTIN and ATTOUT, all attenuation states					
	100 MHz to 10 GHz		22		dB	
	10 GHz to 18 GHz		22		dB	
	18 GHz to 26 GHz		16		dB	
	26 GHz to 35 GHz		15		dB	
35 GHz to 40 GHz		14		dB		
ATTENUATION	Range	Between minimum and maximum attenuation states	30		dB	
	Step Size	Between any successive attenuation states	2		dB	
	Accuracy	Referenced to insertion loss				
		100 MHz to 10 GHz		$\pm(0.05 + 1.0\%)$		dB
		10 GHz to 18 GHz		$\pm(0.1 + 2.0\%)$		dB
		18 GHz to 26 GHz		$\pm(0.2 + 2.5\%)$		dB
		26 GHz to 35 GHz		$\pm(0.2 + 6.0\%)$		dB
	35 GHz to 40 GHz		$\pm(0.5 + 10.0\%)$		dB	
	Step Error	Between any successive attenuation states				
		100 MHz to 10 GHz		± 0.05		dB
10 GHz to 18 GHz			± 0.15		dB	
18 GHz to 26 GHz			± 0.20		dB	
26 GHz to 35 GHz			± 0.35		dB	
35 GHz to 40 GHz		± 0.60		dB		
RELATIVE PHASE	Referenced to insertion loss					
	100 MHz to 10 GHz		15		Degrees	
	10 GHz to 18 GHz		25		Degrees	
	18 GHz to 26 GHz		40		Degrees	
	26 GHz to 35 GHz		55		Degrees	
35 GHz to 40 GHz		80		Degrees		
SWITCHING CHARACTERISTICS	All attenuation states at input power (P_{IN}) = 10 dBm					
	Rise and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output	35		ns	
	On and Off Time (t_{ON} and t_{OFF})	50% triggered control (CTL) to 90% of RF output	110		ns	
	RF Amplitude Settling Time	50% triggered CTL to 0.1 dB of final RF output	230		ns	
		50% triggered CTL to 0.05 dB of final RF output	250		ns	
	Overshoot		0.5		dB	
	Undershoot		-1		dB	
	RF Phase Settling Time	f = 5 GHz				
50% triggered CTL to 5° of final RF output		100		ns		
1°	50% triggered CTL to 1° of final RF output	125		ns		

TIMING SPECIFICATIONS

See Figure 24, Figure 25, and Figure 26 for the timing diagrams.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Minimum serial period, see Figure 24	70			ns
t_{CS}	Control setup time, see Figure 24	15			ns
t_{CH}	Control hold time, see Figure 24		20		ns
t_{LN}	LE setup time, see Figure 24	15			ns
t_{LEW}	Minimum LE pulse width, see Figure 24 and Figure 26		10		ns
t_{LES}	Minimum LE pulse spacing, see Figure 24		630		ns
t_{CKN}	Serial clock hold time from LE, see Figure 24		0		ns
t_{PH}	Hold time, see Figure 26		10		ns
t_{PS}	Setup time, see Figure 26		2		ns
t_{CO}	Clock to output (SEROUT) time, see Figure 25		20		ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Positive Supply Voltage (V_{DD})	-0.3 V to +3.6 V
Negative Supply Voltage (V_{SS})	-3.6 V to +0.3 V
Digital Control Input Voltage	-0.3 V to $V_{DD} + 0.3$ V
RF Input Power ¹ (f = 10 MHz to 30 GHz, $T_{CASE} = 85^{\circ}C^2$)	
ATTIN	
Steady State Average	27 dBm
Steady State Peak	31 dBm
Hot Switching Average	25 dBm
Hot Switching Peak	28 dBm
ATTOUT	
Steady State Average	19 dBm
Steady State Peak	22 dBm
Hot Switching Average	16 dBm
Hot Switching Peak	19 dBm
Temperature	
Junction (T_J)	135°C
Storage	-65°C to +150°C
Reflow	260°C
Continuous Power Dissipation (P_{DISS})	0.5 W
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	
ATTIN and ATTOUT Pins	500 V
Digital Pins	2000 V
Charged Device Model (CDM)	1250 V

¹ For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

² For 105°C operation, the power handling derates from the $T_{CASE} = 85^{\circ}C$ specifications by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-16-6	100	°C/W

POWER DERATING CURVES

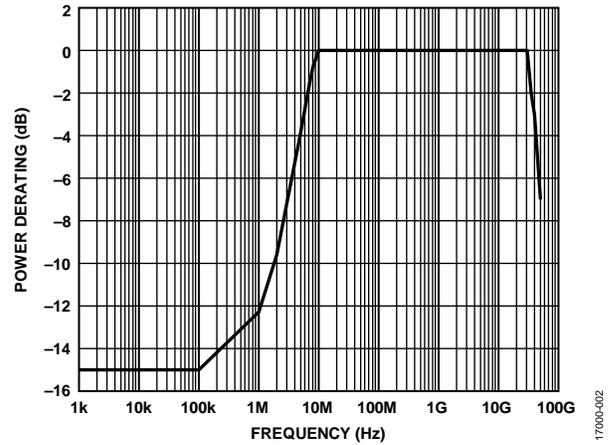


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE} = 85^{\circ}C$

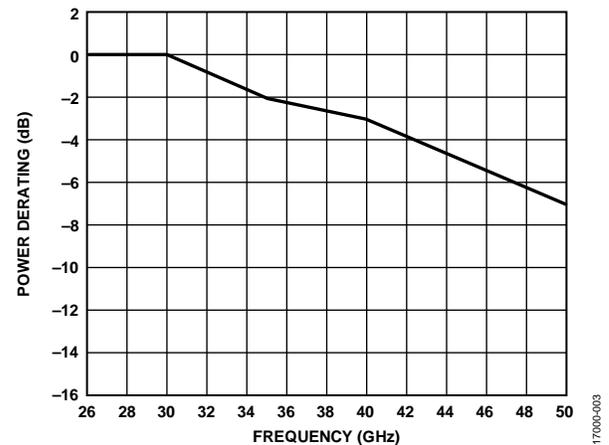


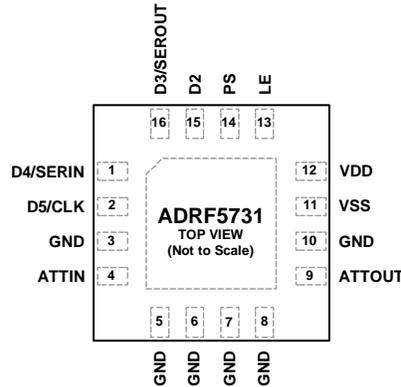
Figure 3. Power Derating vs. Frequency, High Frequency Detail, $T_{CASE} = 85^{\circ}C$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF AND DC GROUND OF THE PCB.

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D4/SERIN	Parallel Control Input for 8 dB Attenuator Bit (D4). Serial Data Input (SERIN). See the Theory of Operation section for more information.
2	D5/CLK	Parallel Control Input for 16 dB Attenuator Bit (D5). Serial Clock Input (CLK). See the Theory of Operation section for more information.
3, 5 to 8, 10	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
4	ATTIN	Attenuator Input. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is needed when the RF line potential is equal to 0 V dc.
9	ATTOUT	Attenuator Output. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is needed when the RF line potential is equal to 0 V dc.
11	VSS	Negative Supply Input.
12	VDD	Positive Supply Input.
13	LE	Latch Enable Input. See the Theory of Operation section for more information.
14	PS	Parallel or Serial Control Interface Selection Input. See the Theory of Operation section for more information.
15	D2	Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information.
16	D3/SEROUT	Parallel Control Input for 4 dB Attenuator Bit (D3). Serial Data Output (SEROUT). See the Theory of Operation section for more information.
17	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB.

INTERFACE SCHEMATICS

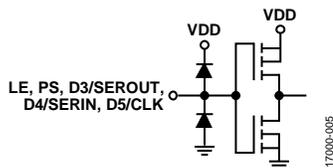


Figure 5. Digital Input Interface Schematic for LE, PS, D3/SEROUT, D4/SERIN, and D5/CLK

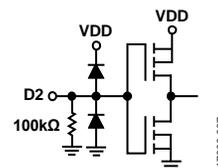


Figure 7. Digital Input Interface Schematic for D2

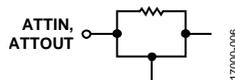


Figure 6. ATTIN and ATTOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

VDD = 3.3 V, VSS = -3.3 V, digital voltages = 0 V or VDD, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. Measured on probe matrix board using ground signal ground (GSG) probes close to the RF pins (ATTIN and ATTOUT). See the Applications Information section for details on evaluation and probe matrix boards.

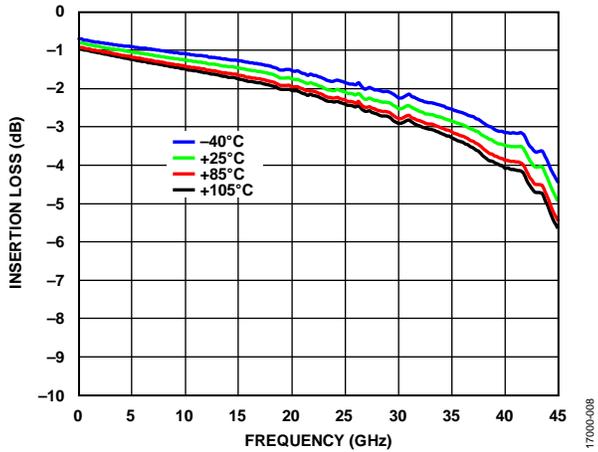


Figure 8. Insertion Loss vs. Frequency over Temperature

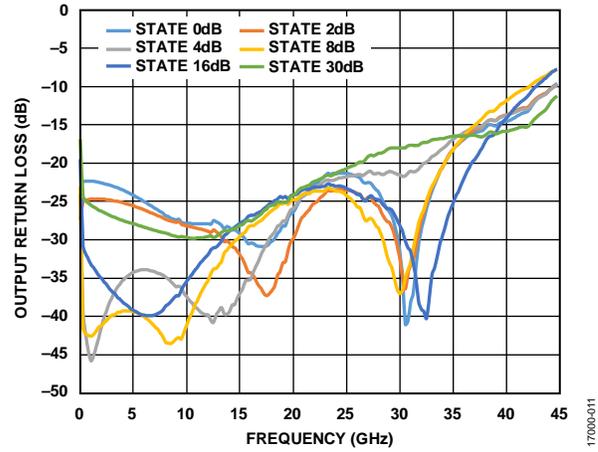


Figure 11. Output Return Loss vs. Frequency (Major States Only)

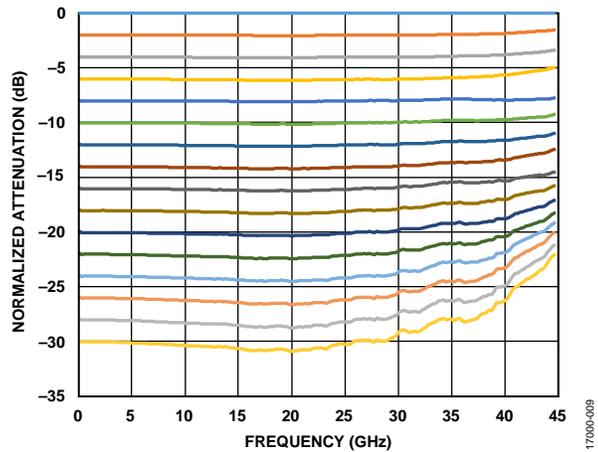


Figure 9. Normalized Attenuation vs. Frequency for All States at Room Temperature

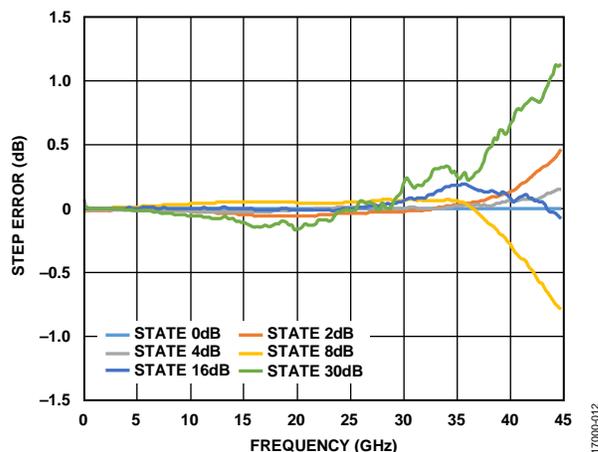


Figure 12. Step Error vs. Frequency (Major States Only)

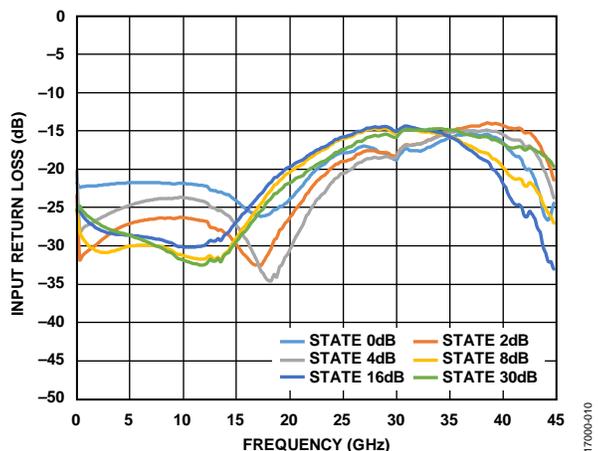


Figure 10. Input Return Loss vs. Frequency (Major States Only)

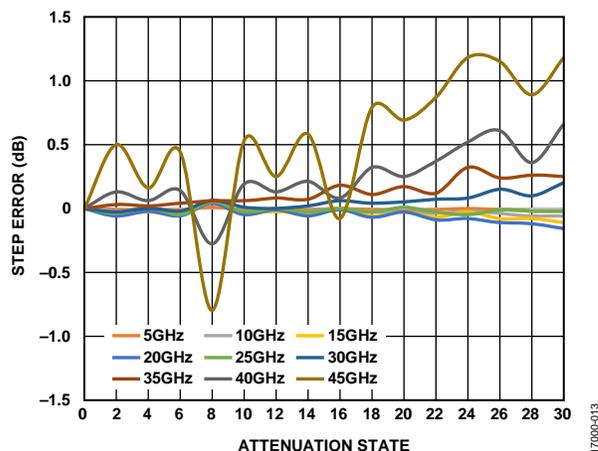


Figure 13. Step Error vs. Attenuation State over Frequency

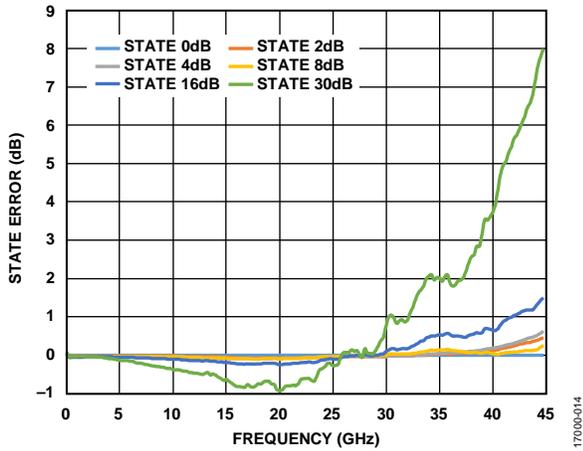


Figure 14. State Error vs. Frequency (Major States Only)

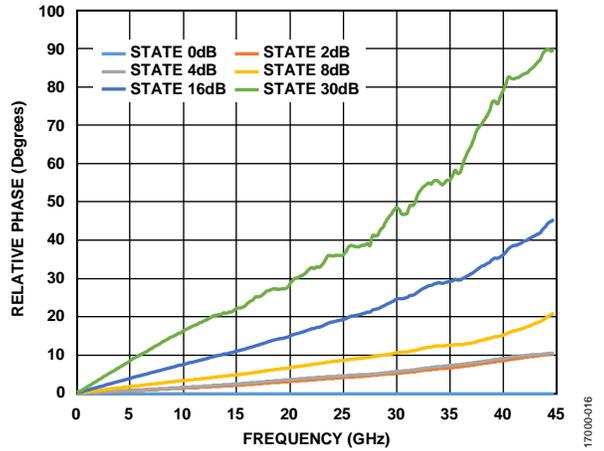


Figure 16. Relative Phase vs. Frequency (Major States Only)

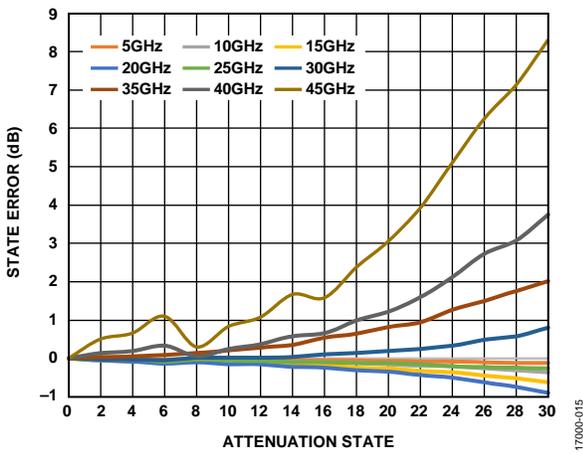


Figure 15. State Error vs. Attenuation State over Frequency

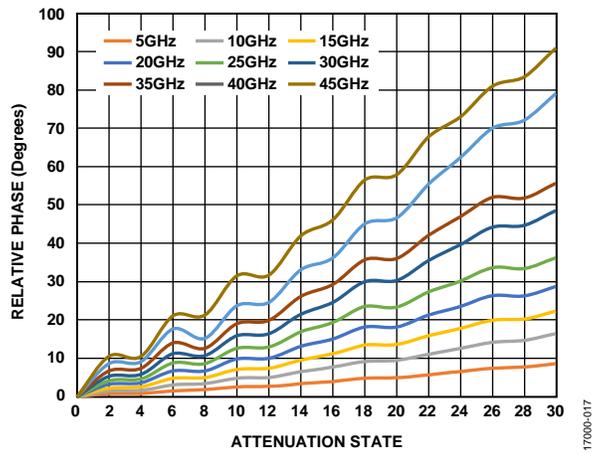


Figure 17. Relative Phase vs. Attenuation State over Frequency

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

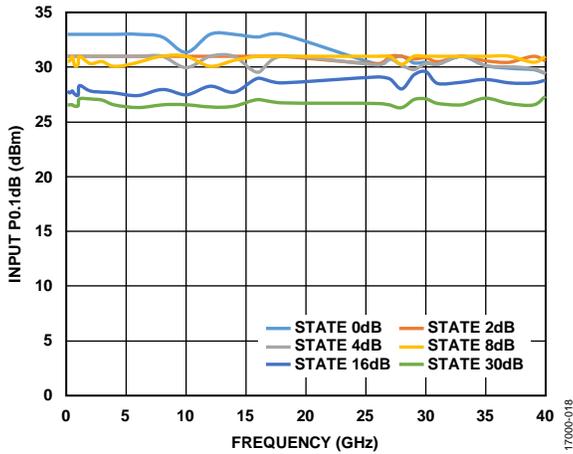


Figure 18. Input P0.1dB vs. Frequency (Major States Only)

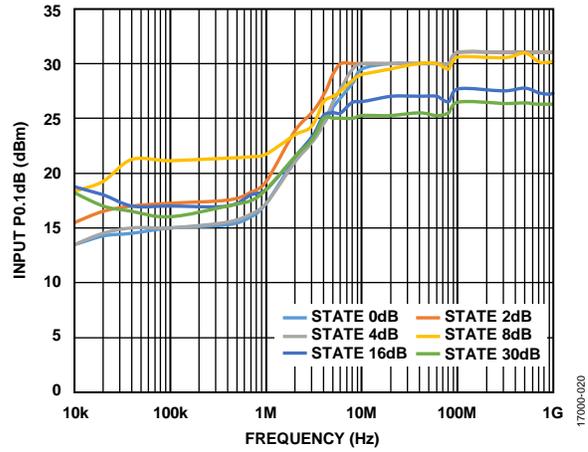


Figure 20. Input P0.1dB vs. Frequency (Major States Only), Low Frequency Detail

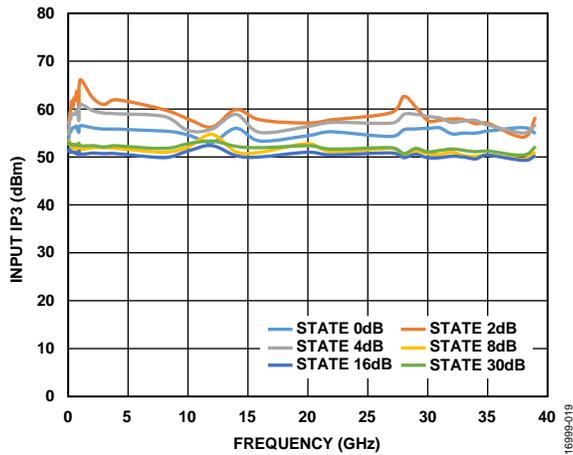


Figure 19. Input IP3 vs. Frequency (Major States Only)

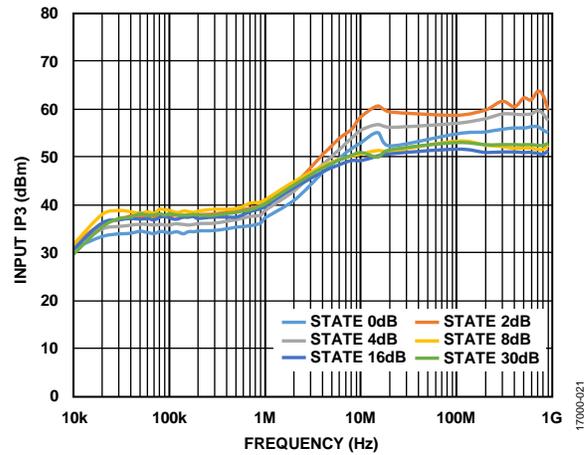


Figure 21. Input IP3 vs. Frequency (Major States Only), Low Frequency Detail

THEORY OF OPERATION

The ADRF5731 incorporates a 4-bit fixed attenuator array that offers an attenuation range of 30 dB in 2 dB steps. An integrated driver provides both serial and parallel mode control of the attenuator array (see Figure 22).

Note that when referring to a single function of a multifunction pin in this section, only the portion of the pin name that is relevant is mentioned. For full pin names of the multifunction pins, refer to the Pin Configuration and Function Descriptions section.

POWER SUPPLY

The ADRF5731 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Power up GND.
2. Power up VDD.
3. Power up VSS.
4. Apply the digital control inputs. The relative order of the digital control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
5. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power up sequence.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are dc-coupled to 0 V. DC blocking is not required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching components are not required.

The ADRF5731 supports bidirectional operation at a lower power level. The power handling of the ATTIN and ATTOUT ports are different. Therefore, the bidirectional power handling is defined by the ATTOUT port. Refer to the RF input power specifications in Table 1.

SERIAL OR PARALLEL MODE SELECTION

The ADRF5731 can be controlled in either serial or parallel mode by setting the PS pin to high or low, respectively (see Table 6).

Table 6. Mode Selection

PS	Control Mode
Low	Parallel
High	Serial

Table 7. Truth Table

Digital Control Input ¹						Attenuation State (dB)
D5	D4	D3	D2	D1	D0	
Low	Low	Low	Low	Don't care	Don't care	0 (reference)
Low	Low	Low	High	Don't care	Don't care	2
Low	Low	High	Low	Don't care	Don't care	4
Low	High	Low	Low	Don't care	Don't care	8
High	Low	Low	Low	Don't care	Don't care	16
High	High	High	High	Don't care	Don't care	30

¹ Any combination of the control voltage input states shown in Table 7 provides an attenuation equal to the sum of the bits selected.

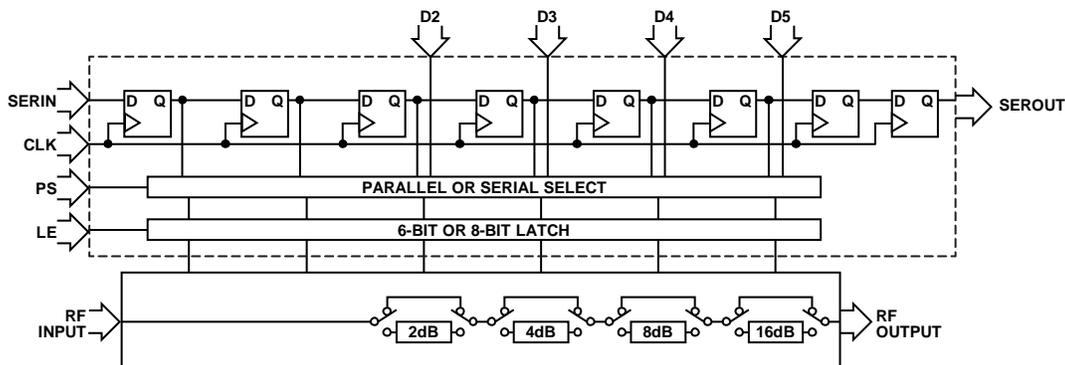


Figure 22. Simplified Circuit Diagram

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SERIAL MODE INTERFACE

The ADRF5731 supports a 3-wire SPI: serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when PS is set to high.

The ADRF5731 attenuation state is controlled by Bits[D5:D2]. Bit D0 and Bit D1 are don't care bits but must be input.

Therefore, at least a 6-bit SERIN must be used to control the attenuation states. If using an 8-bit word to control the state of the attenuator, [D7:D6] and [D1:D0] are don't care bits. It does not matter if these bits are held low or high. Refer to Table 7 and Figure 24 for additional information.

In serial mode, the SERIN data is clocked most significant bit (MSB) first on the rising CLK edges into the shift register. Then, LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new SERIN data into the shift register as CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 24 in conjunction with Table 2 and Table 7.

USING SEROUT

The ADRF5731 also features a serial data output, SEROUT. SEROUT outputs the serial input data at the eighth clock cycle and can control a cascaded attenuator using a single SPI bus. Figure 25 shows the serial output timing diagram.

When using the attenuator in a daisy-chain operation, 8-bit SERIN data must be used due to the 8-clock cycle delay between SERIN and SEROUT.

It is optional to use a 1 kΩ resistor between SEROUT on the first attenuator and SERIN of the next attenuator to filter the signal (see Figure 23).

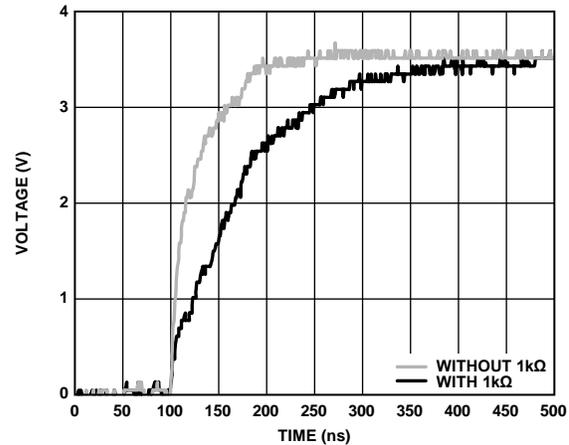


Figure 23. Using a Resistor on SEROUT

17000-023

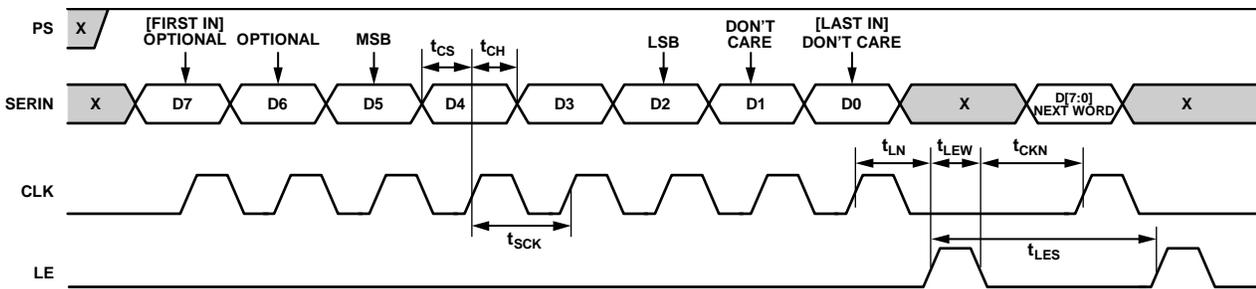


Figure 24. Serial Control Timing Diagram

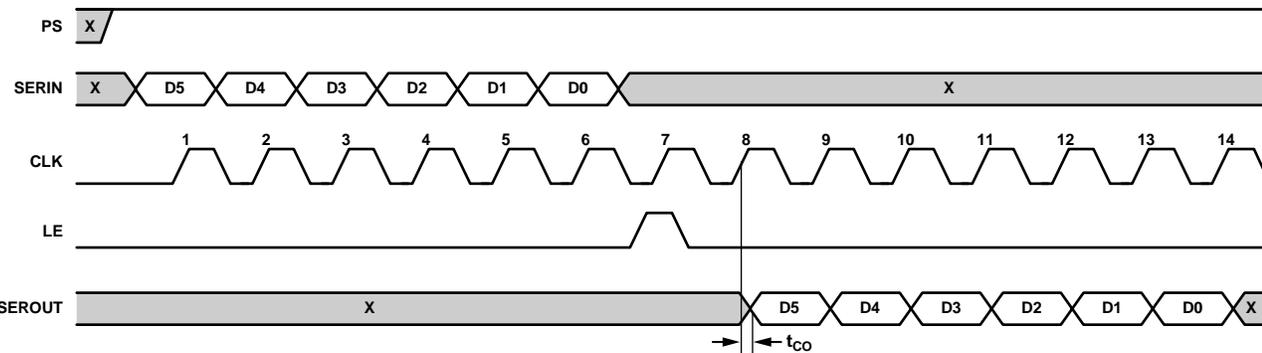


Figure 25. Serial Output Timing Diagram

17000-024

17000-025

PARALLEL MODE INTERFACE

The ADRF5731 has four digital control inputs, D2 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 7. The parallel control interface is activated when PS is set to low.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode, keep the LE pin high. To change the attenuation state, use the control voltage inputs (D2 to D5) directly. This mode is ideal for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, keep the LE pin low when changing the control voltage inputs (D2 to D5) to set the attenuation state. When the desired state is set, toggle LE high to transfer the 4-bit data to the bypass switches of the attenuator array and then toggle LE low to latch the change into the device until the next desired attenuation change (see Figure 26 in conjunction with Table 2).

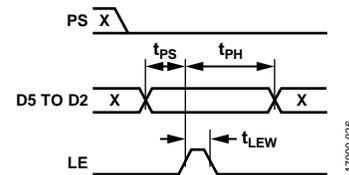


Figure 26. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

EVALUATION BOARD

The [ADRF5731-EVALZ](#) is a 4-layer evaluation board. The top and bottom copper layer are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) and are separated by dielectric materials. The stackup for this evaluation board is shown in Figure 27.

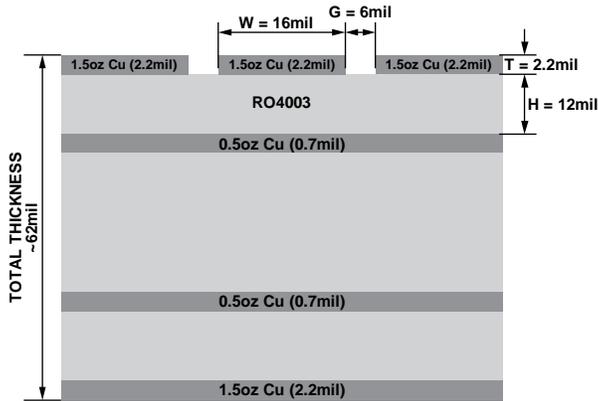


Figure 27. Evaluation Board Stackup, Cross Sectional View

All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 12 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a trace width of 16 mil and ground clearance of 6 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Thru calibration can be used to calibrate out the board loss effects from the [ADRF5731-EVALZ](#) evaluation board measurements to determine the device performance at the pins of the IC. Figure 28 shows the typical board loss (THRU) for the [ADRF5731-EVALZ](#) evaluation board at room temperature, the embedded insertion loss, and the de-embedded insertion loss for the ADRF5731.

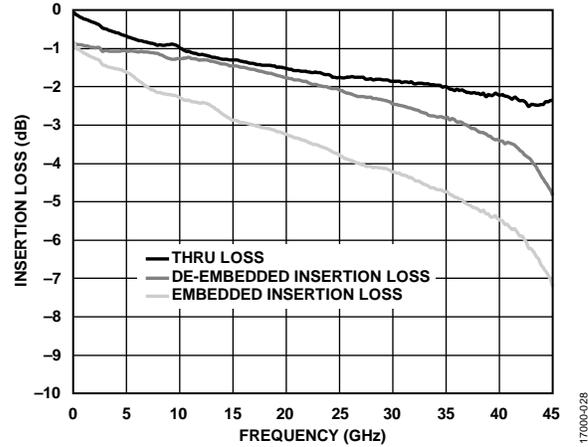


Figure 28. Insertion Loss vs. Frequency

Figure 29 shows the actual [ADRF5731-EVALZ](#) evaluation board with component placement.

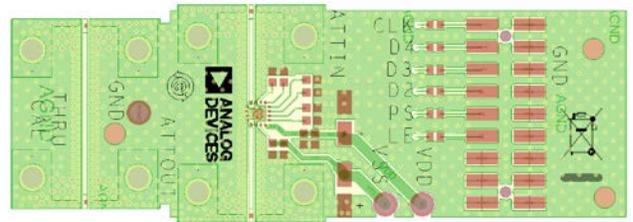


Figure 29. Evaluation Board Layout, Top View

Two power supply ports are connected to the VDD and VSS test points, TP1 and TP2, and the ground reference is connected to the GND test point, TP4. On the supply traces, VDD and VSS, use a 100 pF bypass capacitor to filter high frequency noise. Additionally, unpopulated components positions are available for applying extra bypass capacitors.

All the digital control pins are connected through digital signal traces to the 2 × 9-pin header, P1. There are provisions for a resistor capacitor (RC) filter that helps eliminate dc-coupled noise. The ADRF5731 was evaluated without an external RC filter, the series resistors are 0 Ω, and shunt capacitors are unpopulated on the evaluation board.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines to the 2.4 mm RF launchers, J1 and J2, respectively. These high frequency RF launchers are connected by contact and are not soldered onto the board.

A thru calibration line connects the unpopulated J3 and J4 launchers. This transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

The schematic of the [ADRF5731-EVALZ](#) evaluation board is shown in Figure 30.

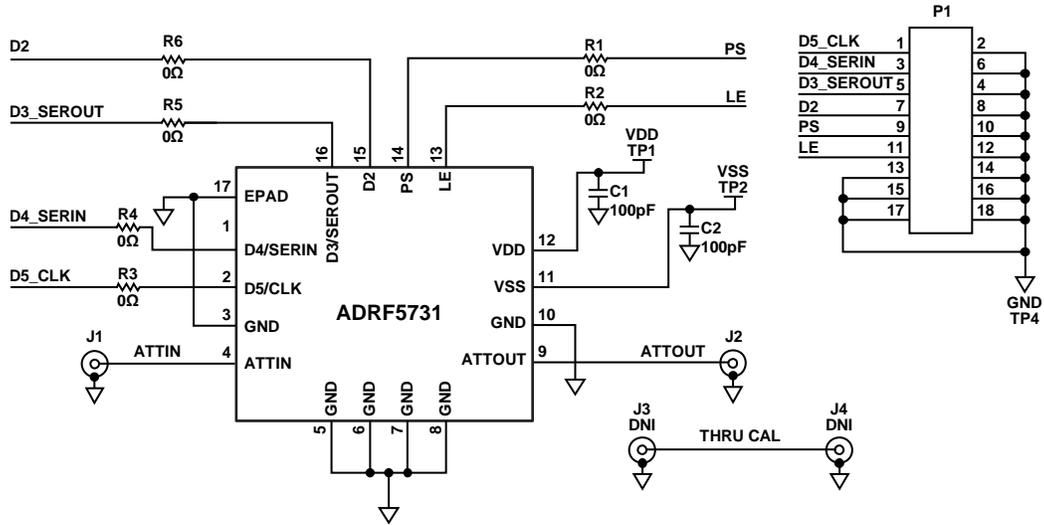


Figure 30. Evaluation Board Schematic

17000-030

Table 8. Evaluation Board Components

Component	Default Value	Description
C1, C2	100 pF	Capacitors, C0402 package
J1, J2	Not applicable	2.4 mm end launch connectors (Southwest Microwave: 1492-04A-6)
P1	Not applicable	2 × 9-pin header
R1 to R6	0 Ω	Resistors, 0402 package
TP1, TP2, TP4	Not applicable	Through hole mount test points
U1	ADRF5731	ADRF5731 digital attenuator, Analog Devices, Inc.

PROBE MATRIX BOARD

The probe matrix board is a 4-layer board. Similar to the evaluation board, the probe matrix board also uses a 12 mil Rogers RO4003 dielectric. The top and bottom copper layers are 1.5 oz (2.2 mil) plated to 1.5 oz (2.2 mil). The RF transmission lines are designed using a CPWG model with a width of 16 mil and ground spacing of 6 mil to have a characteristic impedance of 50 Ω.

Figure 31 and Figure 32 show the cross sectional view and the top view of the board, respectively. Measurements are made using GSG probes at close proximity to the RF pins (ATTIN and ATTOUT). Unlike the evaluation board, probing reduces reflections caused by mismatch arising from connectors, cables, and board layout, resulting in a more accurate measurement of the device performance.

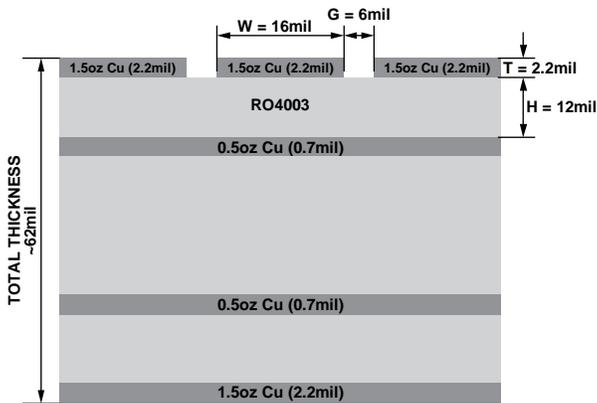


Figure 31. Probe Matrix Board (Cross Sectional View)

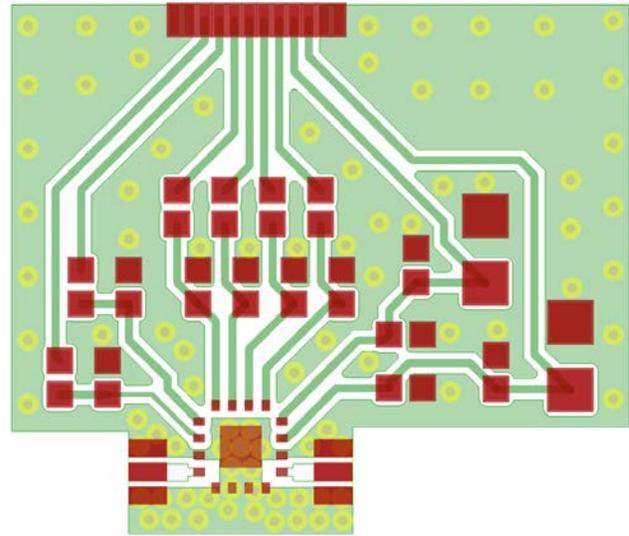


Figure 32. Probe Matrix Board Layout (Top View)

The probe matrix board includes a thru reflect line (TRL) calibration kit, allowing board loss de-embedding. The actual board duplicates the same layout in matrix form to assemble multiple devices at one time. Figure 33 is a detailed image of the trace to pin transition with corresponding dimensions. All S parameters were measured on this board.

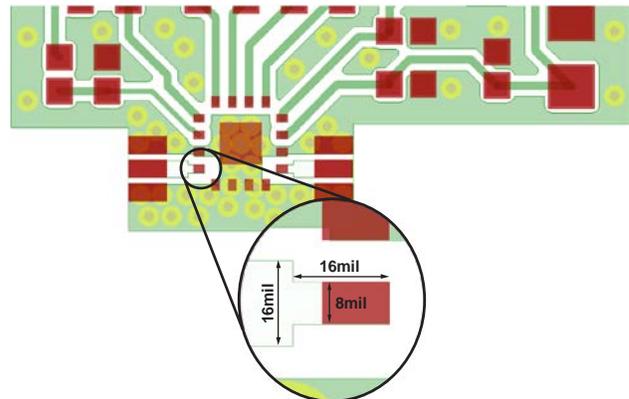


Figure 33. Probe Board Layout Dimensions (Top View)

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

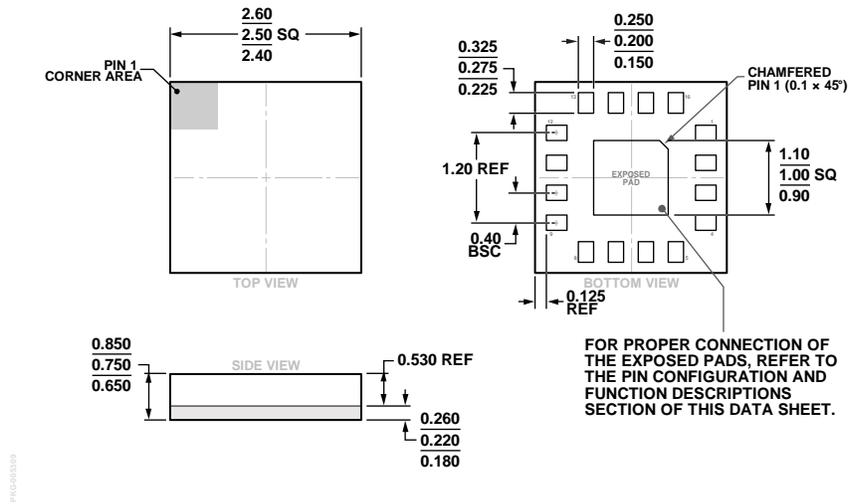


Figure 34. 16-Terminal Land Grid Array [LGA]
 2.5 mm × 2.5 mm Body and 0.75 mm Package Height
 (CC-16-6)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Marking Code
ADRF5731BCCZN	-40°C to +105°C	16-Terminal Land Grid Array [LGA]	CC-16-6	31
ADRF5731BCCZN-R7	-40°C to +105°C	16-Terminal Land Grid Array [LGA]	CC-16-6	31
ADRF5731-EVALZ		Evaluation Board		

¹ Z = RoHS Compliant Part.