24 GHz to 44 GHz, Wideband, Microwave Upconverter

Data Sheet

ADMV1013

FEATURES

- Wideband RF input frequency range: 24 GHz to 44 GHz
- 2 upconversion modes
  - Direct conversion from baseband I/Q to RF
  - Single-sideband upconversion from real IF
- LO input frequency range: 5.4 GHz to 10.25 GHz
- LO quadrupler for up to 41 GHz
- Matched 50 Ω single-ended RF output and IF inputs
- Option between matched 100 Ω balanced or 50 Ω single-ended LO inputs
- 100 Ω balanced baseband inputs
- Sideband suppression and carrier feedthrough optimization
- Variable attenuator for transceiver power control
- Programmable via 4-wire SPI interface
- 40-terminal land grid array package (LGA)

APPLICATIONS

- Point to point microwave radios
- Radar, electronic warfare systems
- Instrumentation, automatic test equipment (ATE)

FUNCTIONAL BLOCK DIAGRAM

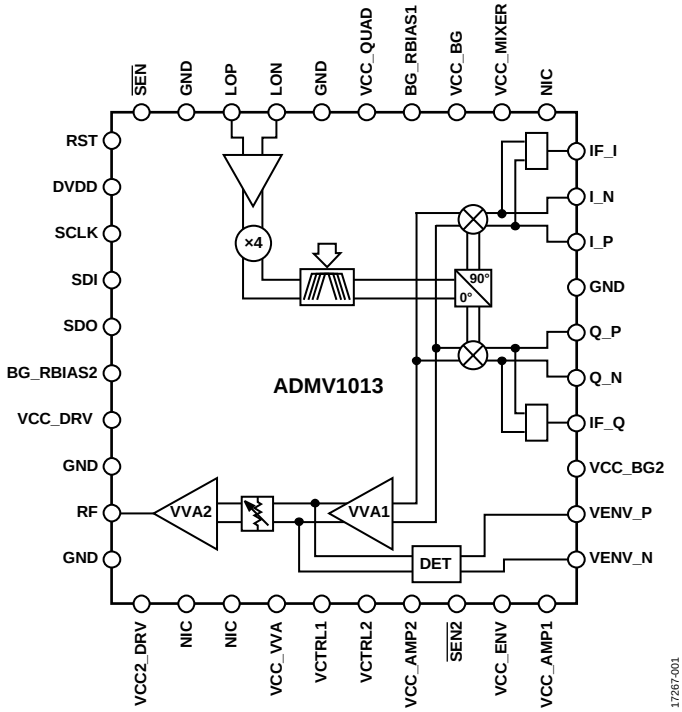

Figure 1.

GENERAL DESCRIPTION

The ADMV1013 is a wideband, microwave upconverter optimized for point to point microwave radio designs operating in the 24 GHz to 44 GHz radio frequency (RF) range.

The upconverter offers two modes of frequency translation. The device is capable of direct conversion to RF from baseband in-phase quadrature (I/Q) input signals, as well as single-sideband (SSB) upconversion from complex intermediate frequency (IF) inputs. The baseband I/Q input path can be disabled and modulated complex IF signals, anywhere from 0.8 GHz to 6.0 GHz, can be inserted in the IF path and upconverted to 24 GHz to 44 GHz while suppressing the unwanted sideband by typically better than 26 dBc. The serial port interface (SPI) allows adjustment of the quadrature phase and mixer gate voltage to allow optimum sideband suppression and local oscillator (LO) nulling. In addition, the SPI interface allows powering down the output envelope detector to reduce power consumption.

The ADMV1013 upconverter comes in a 40-terminal land grid array package (LGA) package. The ADMV1013 operates over the −40°C to +85°C case temperature range.

Rev. A

Document Feedback

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Serial Port Register Timing ... 5
Absolute Maximum Ratings ... 6
Thermal Resistance ... 6
ESD Caution ... 6
Pin Configuration and Function Descriptions ... 7
Typical Performance Characteristics ... 9
I/Q Mode ... 9
IF Mode ... 14
Envelope Detector Performance ... 19
Return Loss ... 21
M × N Spurious Performance ... 24
Theory of Operation ... 25
Start-Up Sequence ... 25
Baseband Quadrature Modulation (I/Q Mode) ... 25
Single-Sideband Upconversion (IF Mode) ... 25
LO Input Path ... 25
Sideband Suppression Optimization ... 25
Carrier Feedthrough Nulling ... 26
Envelope Detector ... 26
Power Down and Reset ... 26
Serial Port Interface (SPI) ... 26
Applications Information ... 28
Baseband Quadrature Modulation from Low Frequencies ... 28
Performance at Different Quad Filter Settings ... 28
VVA Temperature Compensation ... 28
Performance Between Differential vs. Single-Ended LO Input ... 29
Performance Across RF Frequency at Fixed Input Frequencies ... 30
Performance Across Common-Mode Voltage in I/Q Mode 31
Operating VCTRL1 and VCTRL2 Independently ... 31
Recommended Land Pattern ... 33
Evaluation Board Information ... 33
Register Summary ... 34
Register Details ... 35
Outline Dimensions ... 39
Ordering Guide ... 39

REVISION HISTORY

4/2019—Rev. 0 to Rev. A

Changes to Figure 1 ... 1
Changes to Frequency Ranges Parameter, Table 1 ... 3
Changes to Thermal Resistance Section ... 6
Changes to Figure 3 ... 7
Changes to Table 5 ... 8
Changes to Figure 50 Caption ... 16
Changes to Figure 58 Caption ... 18
Change to Return Loss and Isolation Section ... 21
Moved Figure 70; Renumbered Sequentially ... 21
Moved Figure 72 ... 22
Moved Figure 77 ... 22
Moved Figure 80 ... 23
Changes to M × N Spurious Performance Section, I/Q Mode Section, and IF Mode Section ... 24
Changes to Start-Up Sequence Section ... 25

12/2018—Revision 0: Initial Version

SPECIFICATIONS

IF and I/Q amplitude = −20 dBm, VCC_DRV = VCC2_DRV = VCC_AMP2 = VCC_ENV = VCC_AMP1 = VCC_BG2 = VCC_MIXER = VCC_BG = VCC_QUAD = 3.3 V, DVDD = VCC_VVA = 1.8 V, T_A = 25°C, and set Register 0x0A to 0xE700, unless otherwise noted.

Measurements in IF mode performed with a 90° hybrid, Register 0x03, Bit 7 = 1, IF input frequency (f_{IF}) = 3.5 GHz.

Measurements in I/Q mode are measured as a composite of the I and Q channel performance, common-mode voltage (V_{CM}) = 0 V, Register 0x03, Bit 7 = 0, and Register 0x05, Bits[6:0] = 0x051, unless otherwise noted. I/Q baseband frequency (f_{BB}) = 100 MHz.

VCTRL1 = VCTRL2. V_{CTRL} is the attenuation voltage at the VCTRL1 and VCTRL2 pins. V_{CTRL} =1800 mV, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGES					
RF Output		24		44	GHz
LO Input		5.4		10.25	GHz
LO Quadrupler		21.6		41	GHz
IF Input		0.8		6.0	GHz
Baseband (BB) I/Q Input		DC		6.0	GHz
LO AMPLITUDE RANGE		−6	0	+6	dBm
I/Q MODULATOR PERFORMANCE					
Conversion Gain	At maximum gain				
24 GHz to 40 GHz	f_{BB} ≤ 3.5 GHz	18	23		dB
	6 GHz > f_{BB} > 3.5 GHz		21		
40 GHz to 44 GHz			19		dB
Voltage Variable Attenuator (VVA) Control Range			35		dB
Single-Sideband (SSB) Noise Figure	At maximum gain				
24 GHz to 40 GHz			18		dB
40 GHz to 44 GHz			19		dB
Output Third-Order Intercept (IP3)	At maximum gain				
24 GHz to 40 GHz		20	23		dBm
40 GHz to 44 GHz			22		dBm
Output 1 dB Compression Point (P1dB)	At maximum gain				
24 GHz to 40 GHz		10	13		dBm
40 GHz to 44 GHz			12		dBm
Sideband Rejection (SBR)	24 GHz to 44 GHz, at maximum gain				
Uncalibrated			32		dBc
IF SINGLE-SIDEBAND UPCONVERSION PERFORMANCE					
Conversion Gain	At maximum gain				
24 GHz to 40 GHz	f_{IF} ≤ 3.5 GHz	13	18		dB
	6 GHz > f_{IF} > 3.5 GHz		12		
40 GHz to 44 GHz			14		dB
VVA Control Range			35		dB
SSB Noise Figure	At maximum gain				
24 GHz to 40 GHz			25		dB
40 GHz to 44 GHz			28		dB
Output IP3	At maximum gain				
24 GHz to 40 GHz		20	23		dBm
40 GHz to 44 GHz			22		dBm
Output P1dB	At maximum gain				
24 GHz to 40 GHz		10	13		dBm
40 GHz to 44 GHz			12		dBm
SBR	24 GHz to 44 GHz, at maximum gain				
Uncalibrated			26		dBc
Calibrated	Calibrated using LOAMP_PH_ADJ_Q_FINE and LOAMP_PH_ADJ_I_FINE bits		36		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ENVELOPE DETECTOR PERFORMANCE					
Output Level	For optimum performance				
Minimum			−45		dBm
Maximum			−20		dBm
Envelope Bandwidth	Measured with two tones with total power output (P_{OUT}) at RF = 10 dBm				
3 dB	RF frequency (f_{RF}) = 28 GHz		350		MHz
10 dB	f_{RF} = 28 GHz		1		GHz
RETURN LOSS					
RF Output	50 Ω single-ended		−8		dB
LO Input	100 Ω differential		−12		dB
IF Input	50 Ω single-ended		−12		dB
BB Input	100 Ω differential		−10		dB
BB I/Q Input Impedance			100		Ω
LEAKAGE	At maximum gain				
Fundamental LO to RF			−80		dBm
4 × LO to RF					
5.4 GHz to 6.8 GHz LO	Uncalibrated		−12		dBm
6.8 GHz to 10.25 GHz LO	Uncalibrated		−20		dBm
5.4 GHz to 10.25 GHz LO	Calibrated using MXER_OFF_ADJ_I_N, MXER_OFF_ADJ_I_P, MXER_OFF_ADJ_Q_N, MXER_OFF_ADJ_Q_P bits at V_{CTRL} = 1800 mV, IF mode		−45		dBm
5 × LO to RF			−55		dBm
Fundamental LO to IF			−70		dBm
Fundamental LO to I/Q			−75		dBm
LOGIC INPUTS					
Input Voltage Range					
High, V_{INH}		DVDD − 0.4		1.8	V
Low, V_{INL}		0		0.4	V
Input Current, I_{INH}/I_{INL}			100		µA
Input Capacitance, C_{IN}			3		pF
LOGIC OUTPUTS					
Output Voltage Range					
High, V_{OH}		DVDD − 0.4		1.8	V
Low, V_{OL}		0		0.4	V
Output High Current, I_{OH}				500	µA
POWER INTERFACE					
VCC_DRV, VCC2_DRV, VCC_AMP2, VCC_ENV, VCC_AMP1, VCC_BG2, VCC_MIXER, VCC_BG, VCC_QUAD		3.15	3.3	3.45	V
3.3 V Supply Current	V_{CTRL} = 1.8 V, no IF and I/Q or LO input signal		550		mA
DVDD, VCC_VVA		1.7	1.8	1.9	V
1.8 V Supply Current	V_{CTRL} = 1.8 V, no IF and I/Q or LO input signal		3		mA
Total Power Consumption			1.9		W
Power-Down			77	136	mW

SERIAL PORT REGISTER TIMING

Table 2.

Parameter	Description	Min	Typ	Max	Unit
$t_{SDI, SETUP}$	Data to clock setup time	10			ns
$t_{SDI, HOLD}$	Data to clock hold time	10			ns
$t_{SCLK, HIGH}$	Clock high duration	40 to 60			%
$t_{SCLK, LOW}$	Clock low duration	40 to 60			%
$t_{SCLK, \overline{SEN}/\overline{SEN2}\_SETUP}$	Clock to $\overline{SEN}/\overline{SEN2}$ setup time	30			ns
$t_{SCLK, DOT}$	Clock to data out transition time			10	ns
$t_{SCLK, DOV}$	Clock to data out valid time			10	ns
$t_{SCLK, \overline{SEN}/\overline{SEN2}\_INACTIVE}$	Clock to $\overline{SEN}/\overline{SEN2}$ inactive	20			ns
$t_{\overline{SEN}/\overline{SEN2}\_INACTIVE}$	Inactive $\overline{SEN}/\overline{SEN2}$ (between two operations)	80			ns

Timing Diagram

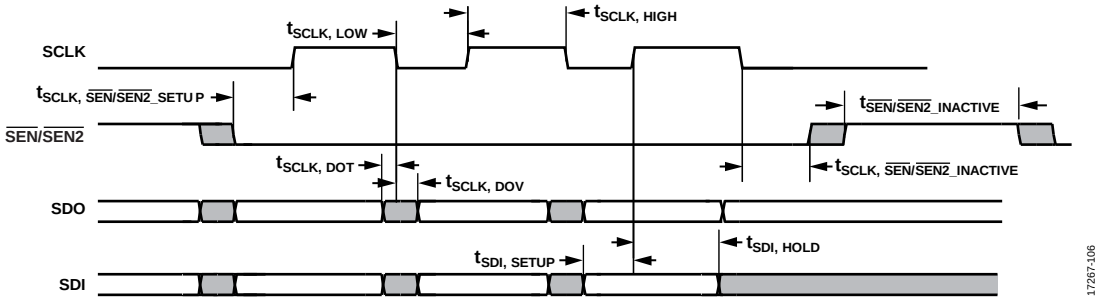

Figure 2. Serial Port Register Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	
VCC_DRV, VCC2_DRV, VCC_AMP2, VCC_ENV, VCC_AMP1, VCC_BG2, VCC_BG, VCC_MIXER	4.3 V
DVDD, VCC_VVA	2.3 V
IF Input Power	5 dBm
I/Q Input Power	5 dBm
LO Input Power	9 dBm
Maximum Junction Temperature	125°C
Maximum Power Dissipation[1]	2.9 W
Lifetime at Maximum Junction Temperature (T_J)	1 ×10^6 hours
Operating Case Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering 60 sec)	260°C
Moisture Sensitivity Level (MSL) Rating[2]	MSL3
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	1250 V
Field Induced Charged Device Model (FICDM)	750 V

[1] The maximum power dissipation is a theoretical number calculated by $(T_J - 85°C)/\theta_{JC\_TOP}$.
[2] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

θ_{JA} and θ_{JC} must only be used to compare thermal performance of different packages if all test conditions listed are similar to JEDEC specifications. Instead, Ψ_{JT} and Ψ_{JB} can be used to calculate the junction temperature of the device using the following equations:

$T_J = (P \times \Psi_{JT}) + T_{Top}$ (Equation 1)

T_{Top}: Refers to package top temperature (°C). T_{Top} is measured at the top-center of the package.

Ψ_{JT}: Refers to junction-to-top thermal characterization number.

P: Refers to total power dissipation in the chip (W).

$T_J = (P \times \Psi_{JB}) + T_{Board}$ (Equation 2)

T_{Board}: Refers to board temperature measured on the mid-point of the longest side of the package no more than 1 mm from the edge of the package body (°C).

Ψ_{JB}: Refers to junction-to-board thermal characterization number.

P: Refers to total power dissipation in the chip (W).

As stated in JEDEC51-12, Equation 1 and Equation 2 must only be used when no heat sink/heat spreader is present. When a heat sink/heat spreader is added, estimating and calculating junction temperature can be achieved using θ_{JC_TOP}.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC_TOP}[3]	θ_{JB}[4]	Ψ_{JT}[5]	Ψ_{JB}[6]	Unit
CC-40-5	28	13.8	11.1	6.4	13.8	°C/W

[1] The thermal resistance values specified in Table 4 are simulated based on JEDEC specifications, unless specified otherwise, and must be used in compliance with JESD51-12.
[2] θ_{JA} is the junction to ambient thermal resistance in a natural convection, JEDEC environment.
[3] θ_{JC_TOP} is the junction to case (top) JEDEC thermal resistance.
[4] θ_{JB} is the junction to board JEDEC thermal resistance.
[5] Ψ_{JT} is the junction to top JEDEC thermal characterization parameter.
[6] Ψ_{JB} is the junction to board JEDEC thermal characterization parameter.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

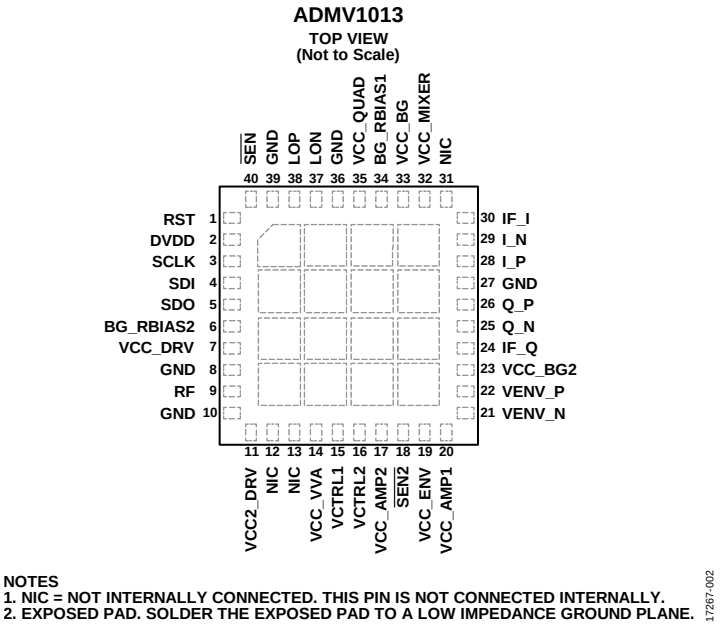

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RST	SPI Reset. Connect this pin to logic high for normal operation. The SPI logic is 1.8 V.
2	DVDD	1.8 V SPI Digital Supply.
3	SCLK	SPI Clock Digital Input.
4	SDI	SPI Serial Data Input.
5	SDO	SPI Serial Data Output.
6	BG_RBIAS2	Voltage Gain Amplifier (VGA) Chip Band Gap Circuit, External High Precision Resistor. Place a 1.1 kΩ, high precision resistor shunt to ground close to this pin.
7	VCC_DRV	3.3 V Power Supply for RF Driver. Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
8, 10, 27, 36, 39	GND	Ground.
9	RF	RF Output. This pin is dc-coupled internally to GND and matched to 50 Ω single ended.
11	VCC2_DRV	3.3 V Power Supply for RF Predriver. Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
12, 13, 31	NIC	Not Internally Connected. This pin is not connected internally.
14	VCC_VVA	1.8 V Power Supply for VVA Control Circuit. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
15	VCTRL1	RF Voltage Variable Attenuator 1 (VVA1) Control Voltage. Place a 1 kΩ series resistor with this pin.
16	VCTRL2	RF Voltage Variable Attenuator 2 (VVA2) Control Voltage. Place a 1 kΩ series resistor with this pin.
17	VCC_AMP2	3.3 V Power Supply for RF Amplifier 2 (AMP2). Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
18	$\overline{\text{SEN2}}$	SPI Serial Enable for VGA Chip. Connect this pin with Pin 40 ($\overline{\text{SEN}}$).
19	VCC_ENV	3.3 V Power Supply for Envelope Detector. Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
20	VCC_AMP1	3.3 V Power Supply for RF Amplifier 1 (AMP1). Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
21	VENV_N	Negative Differential Envelope Detector Output.
22	VENV_P	Positive Differential Envelope Detector Output.
23	VCC_BG2	3.3 V Power Supply for VGA Chip Band Gap Circuit. Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
24, 30	IF_Q, IF_I	IF Single-Ended Complex Inputs. These pins are internally ac-coupled. When in IF mode, Pin 25 (Q_P), Pin 26 (Q_N), Pin 28 (I_P), and Pin 29 (I_N) must be kept floating.
25, 26	Q_N, Q_P	Differential Baseband Q Inputs. These pins are dc-coupled. Do not connect these pins in IF mode.
28, 29	I_P, I_N	Differential Baseband I Inputs. These pins are dc-coupled. Do not connect these pins in IF mode.

Pin No.	Mnemonic	Description
32	VCC_MIXER	3.3 V Power Supply for Mixer. Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
33	VCC_BG	3.3 V Power Supply for Mixer Chip Band Gap Circuit. Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
34	BG_RBIAS1	Mixer Chip Band Gap Circuit, External High Precision Resistor. Place a 1.1 kΩ, high precision resistor shunt to ground close to this pin.
35	VCC_QUAD	3.3 V Power Supply for Quadruppler. Place a 100 pF, a 0.01 µF, and a 10 µF capacitor close to this pin.
37, 38	LON, LOP	Negative and Positive Differential Local Oscillator Input. This pin is dc-coupled internally to ground and matched to 100 Ω differential or 50 Ω single ended. If using the LO as single ended, terminate the unused LO port with 50 Ω impedance to ground.
40	$\overline{\text{SEN}}$	SPI Serial Enable for Mixer Chip. Connect this pin with Pin 18 ($\overline{\text{SEN2}}$).
	EPAD	Exposed Pad. Solder the exposed pad to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

I/Q MODE

I/Q amplitude = −20 dBm, VCC_DRV = VCC2_DRV = VCC_AMP2 = VCC_ENV = VCC_AMP1 = VCC_BG2 = VCC_MIXER = VCC_BG = VCC_QUAD = 3.3 V, DVDD = VCC_VVA = 1.8 V, T_A = 25°C, and set Register 0x0A to 0xE700, unless otherwise noted. VCTRL1 = VCTRL2. V_{CTRL} is the attenuation voltage at the VCTRL1 and VCTRL2 pins. V_{CTRL} = 1800 mV, unless otherwise specified. Measurements in I/Q mode are measured as a composite of the I and Q channel performance, V_{CM} = 0 V, Register 0x03, Bit 7 = 0, and Register 0x05, Bits[6:0] = 0x051, unless otherwise noted. I/Q f_{BB} = 100 MHz.

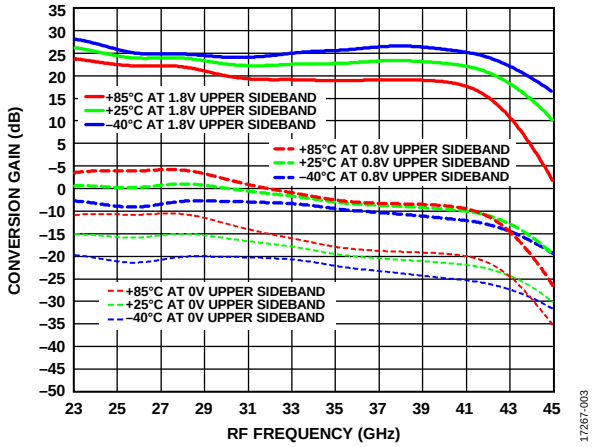

Figure 4. Conversion Gain vs. RF Frequency (f_{RF}) at Three Different Gain Settings for Various Temperatures, f_{BB} = 100 MHz (Upper Sideband)

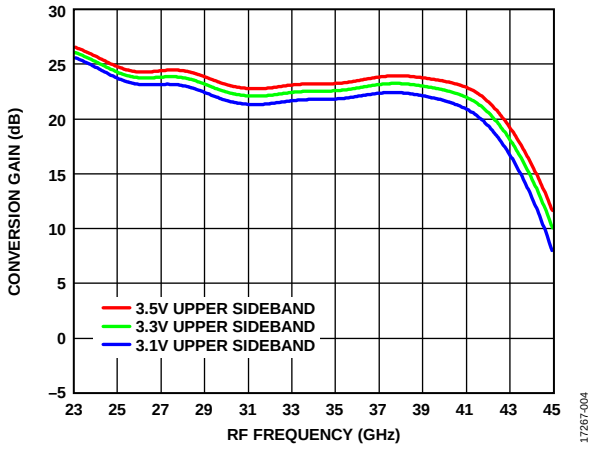

Figure 5. Conversion Gain vs. RF Frequency at for Various Supply Voltages, f_{BB} = 100 MHz (Upper Sideband)

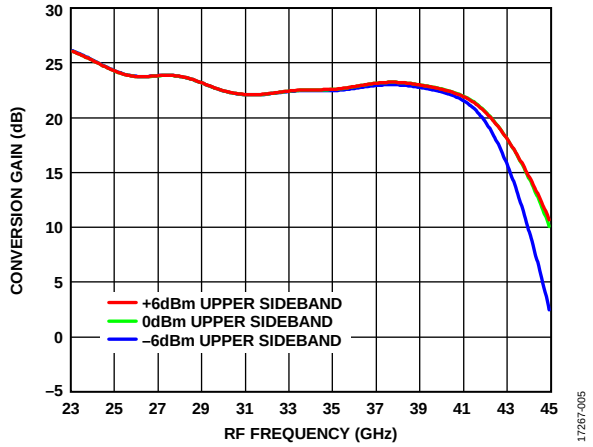

Figure 6. Conversion Gain vs. RF Frequency at for Various LO Inputs, f_{BB} = 100 MHz (Upper Sideband)

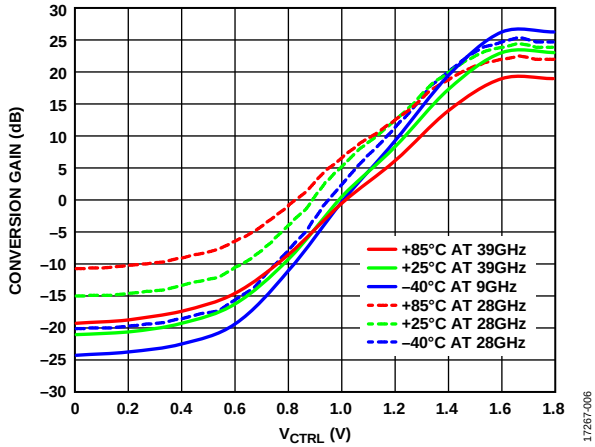

Figure 7. Conversion Gain vs. V_{CTRL} at Various Temperatures and f_{RF} = 28 GHz and 39 GHz, f_{BB} = 100 MHz

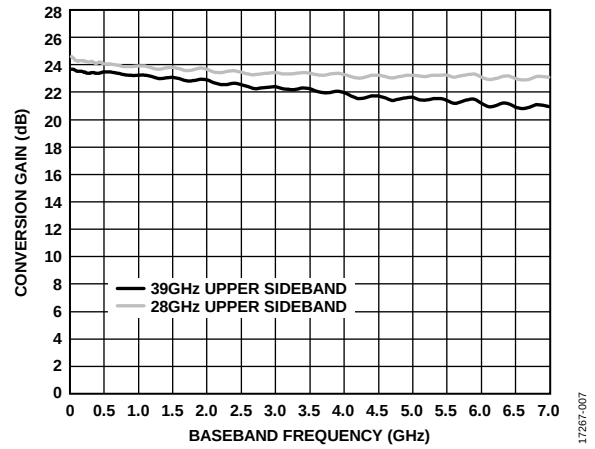

Figure 8. Conversion Gain vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Upper Sideband)

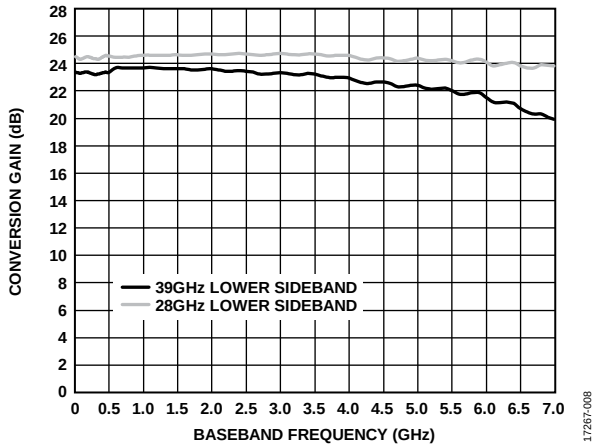

Figure 9. Conversion Gain vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Lower Sideband)

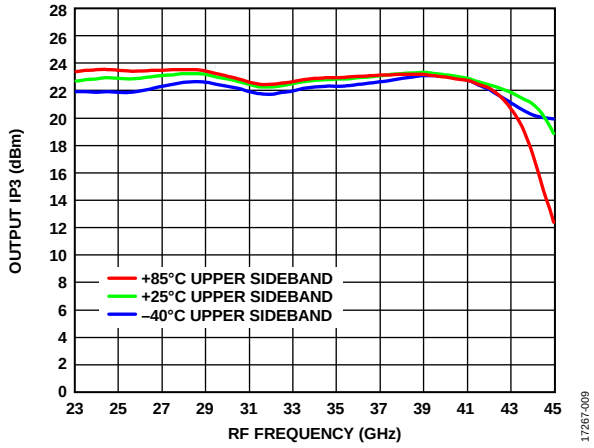

Figure 10. Output IP3 vs. RF Frequency at Maximum Gain for Various Temperatures, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)

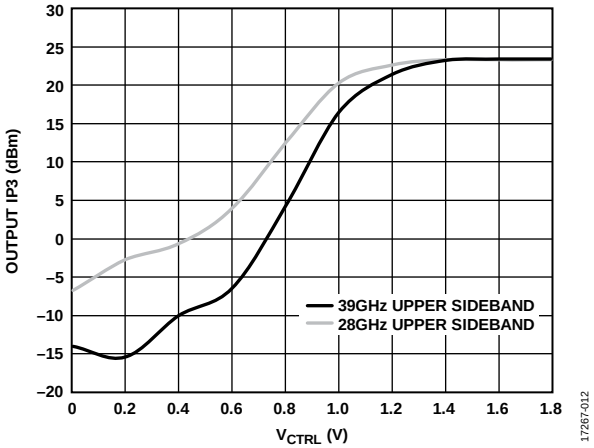

Figure 13. Output IP3 vs. V_{CTRL}, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz at f_{RF} = 28 GHz and 39 GHz (Upper Sideband)

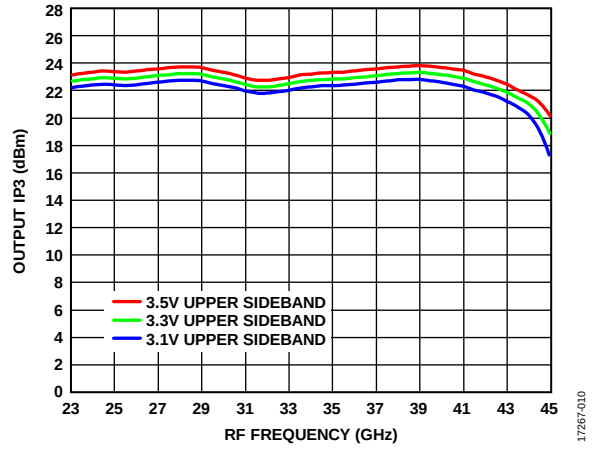

Figure 11. Output IP3 vs. RF Frequency at Maximum Gain for Supply Voltages, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)

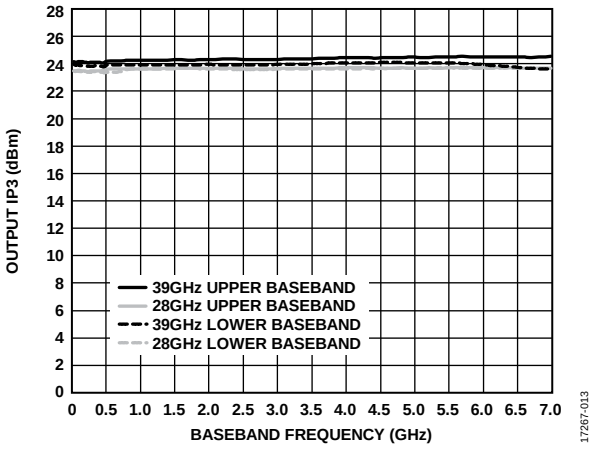

Figure 14. Output IP3 vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz at Maximum Gain, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing (Upper Sideband and Lower Sideband)

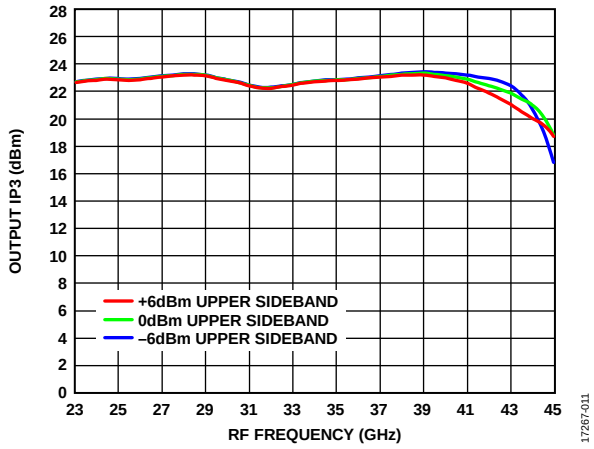

Figure 12. Output IP3 vs. RF Frequency at Maximum Gain for Various LO Inputs, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)

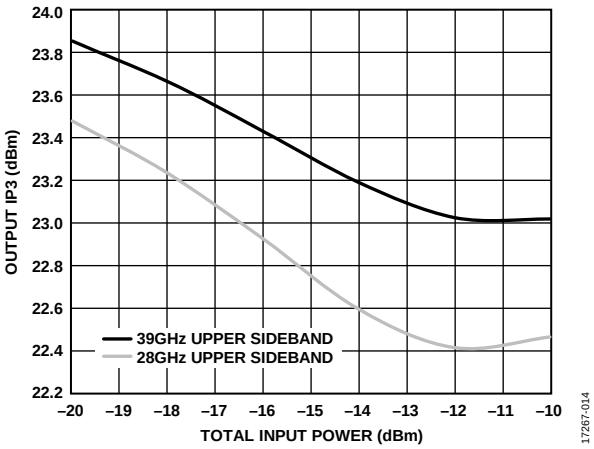

Figure 15. Output IP3 vs. Total Input Power at 20 MHz Spacing, f_{BB} = 100 MHz, f_{RF} = 28 GHz and 39 GHz (Upper Sideband)

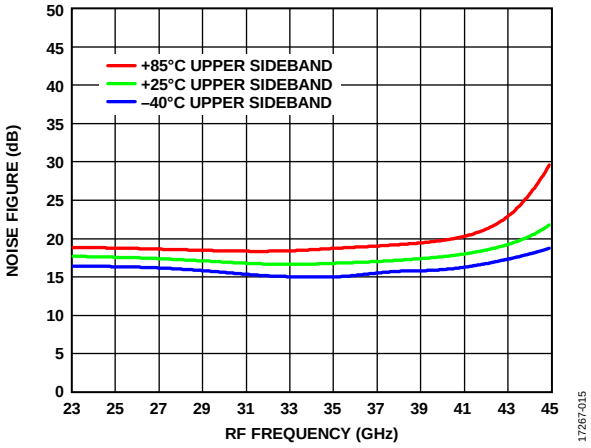

Figure 16. Noise Figure vs. RF Frequency at Maximum Gain for Various Temperatures, f_{BB} = 100 MHz (Upper Sideband)

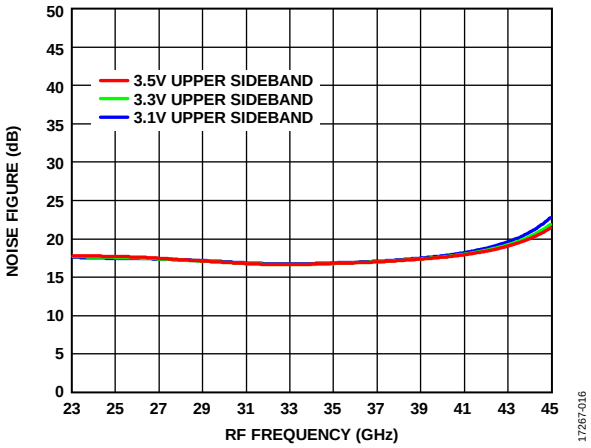

Figure 17. Noise Figure vs. RF Frequency for Various Supply Voltages, f_{BB} = 100 MHz (Upper Sideband)

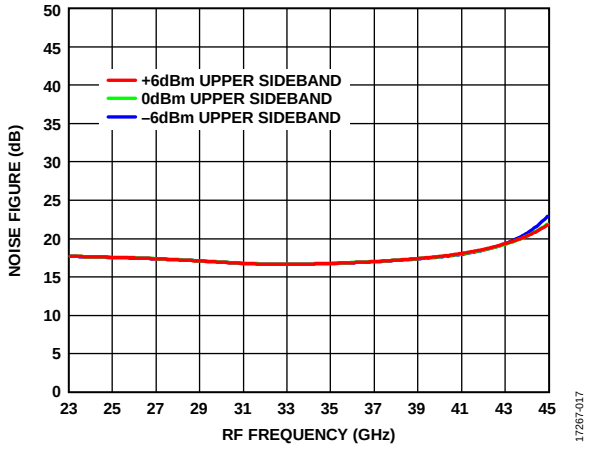

Figure 18. Noise Figure vs. RF Frequency for Various LO Inputs, f_{BB} = 100 MHz (Upper Sideband)

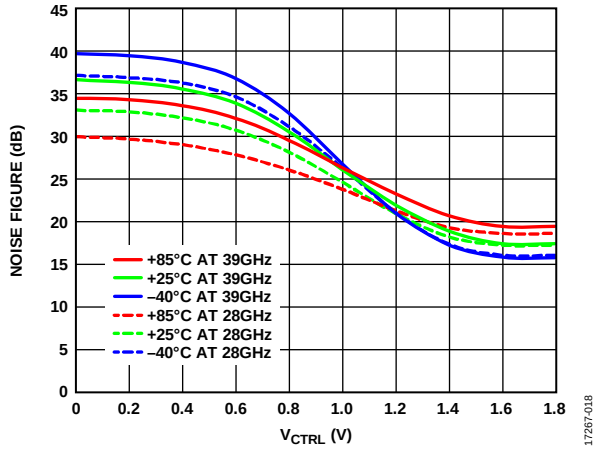

Figure 19. Noise Figure vs. V_{CTRL} for Various Temperatures at f_{RF} = 28 GHz 39 GHz, f_{BB} = 100 MHz

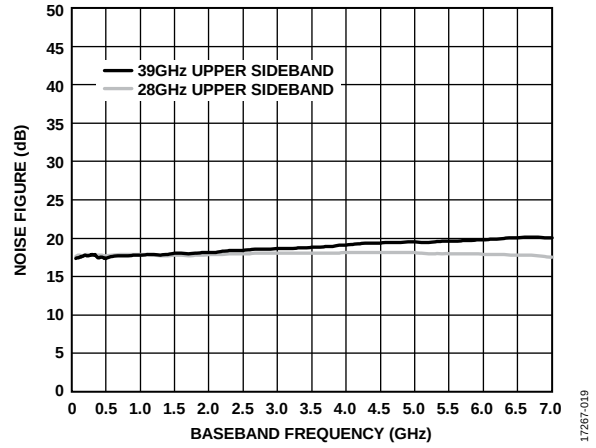

Figure 20. Noise Figure vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Upper Sideband)

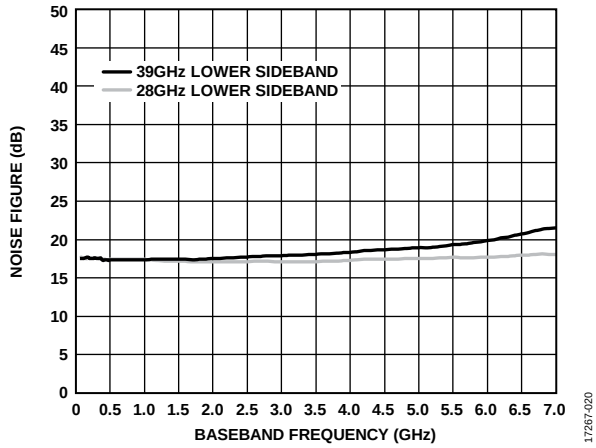

Figure 21. Noise Figure vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Lower Sideband)

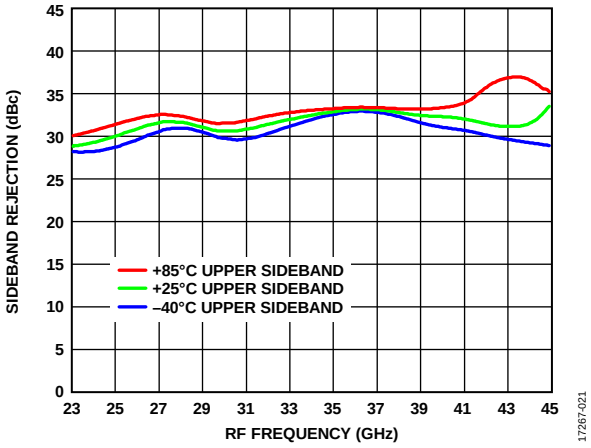

Figure 22. Sideband Rejection vs. RF Frequency at Maximum Gain for Various Temperatures, f_{BB} = 100 MHz (Upper Sideband)

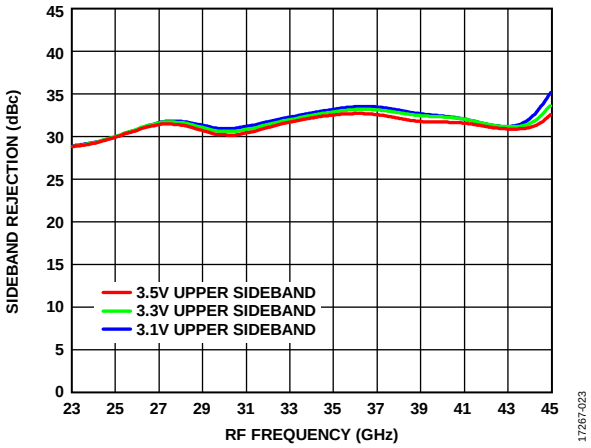

Figure 23. Sideband Rejection vs. RF Frequency at for Various Supply Voltages, f_{BB} = 100 MHz (Upper Sideband)

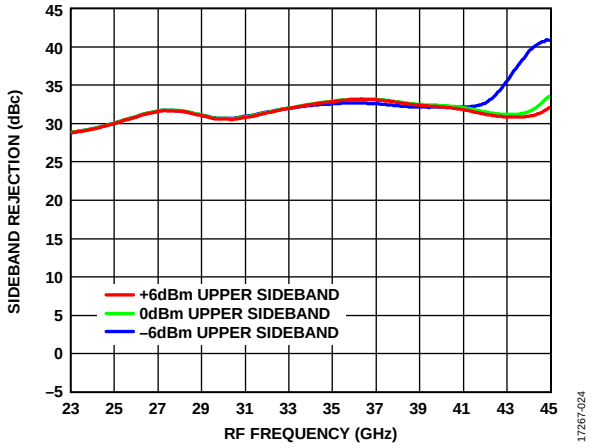

Figure 24. Sideband Rejection vs. RF Frequency for Various LO Inputs, f_{BB} = 100 MHz (Upper Sideband)

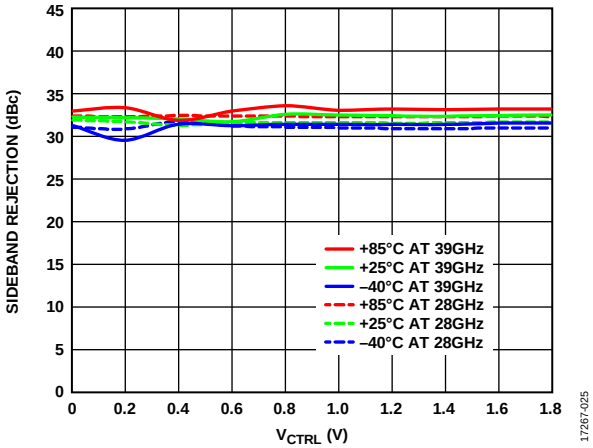

Figure 25. Sideband Rejection vs. V_{CTRL} for Various Temperatures at f_{RF} = 28 GHz and 39 GHz, f_{BB} = 100 MHz

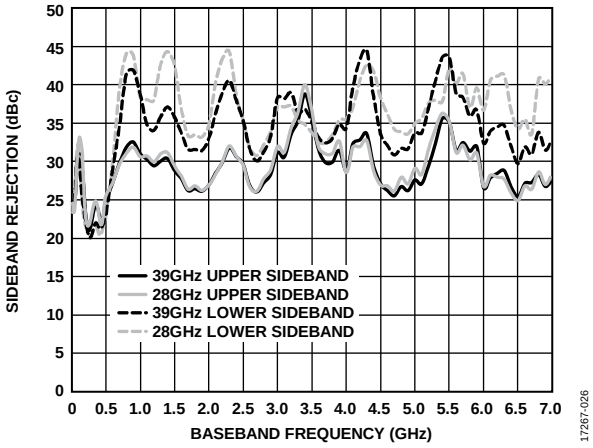

Figure 26. Sideband Rejection vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)

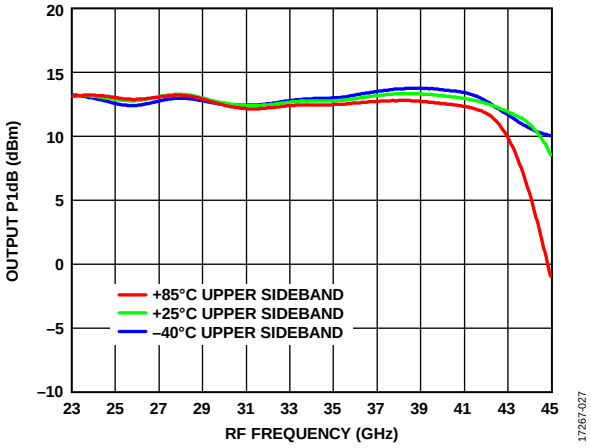

Figure 27. Output P1dB vs. RF Frequency at Maximum Gain for Various Temperatures, f_{BB} = 100 MHz (Upper Sideband)

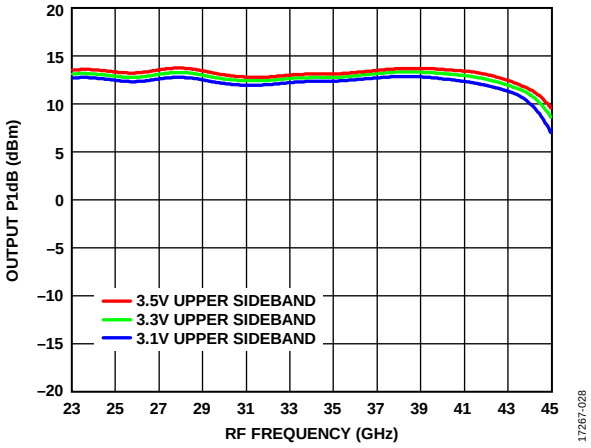

Figure 28. Output P1dB vs. RF Frequency for Various Supply Voltages, f_{BB} = 100 MHz (Upper Sideband)

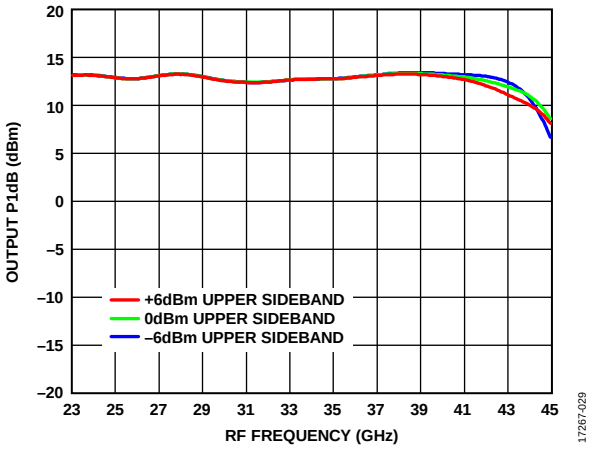

Figure 29. Output P1dB vs. RF Frequency for Various LO Inputs, f_{BB} = 100 MHz (Upper Sideband)

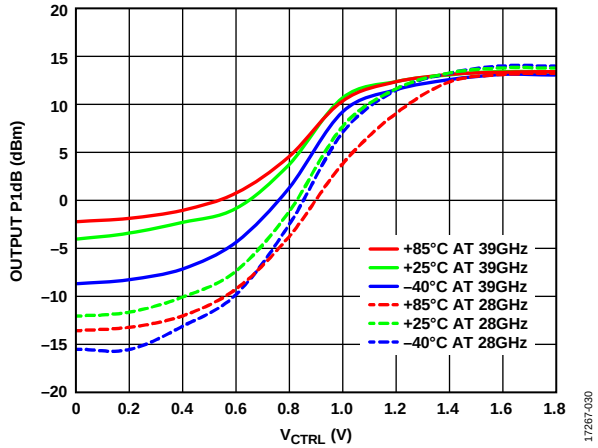

Figure 30. Output P1dB vs. V_{CTRL} for Various Temperatures at f_{RF} = 28 GHz and 39 GHz, f_{BB} = 100 MHz

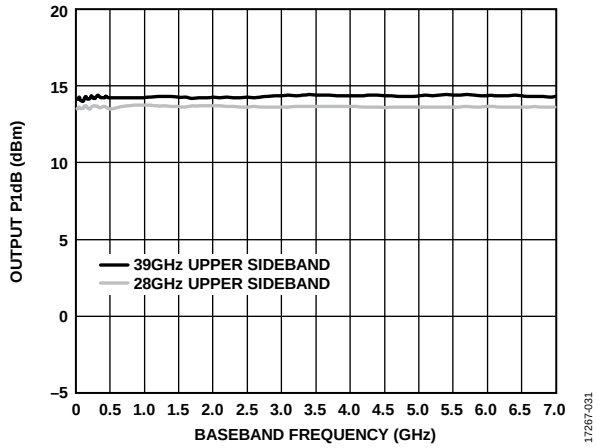

Figure 31. Output P1dB vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Upper Sideband)

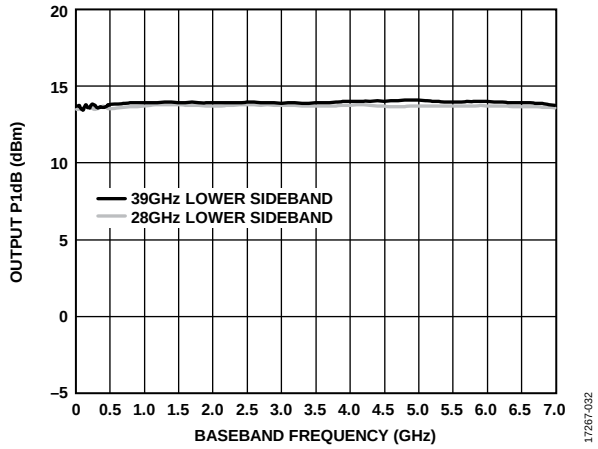

Figure 32. Output P1dB vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Lower Sideband)

IF MODE

IF amplitude = −20 dBm, VCC_DRV = VCC2_DRV = VCC_AMP2 = VCC_ENV = VCC_AMP1 = VCC_BG2 = VCC_MIXER = VCC_BG = VCC_QUAD = 3.3 V, DVDD = VCC_VVA = 1.8 V, T_A = 25°C, and set Register 0x0A to 0xE700, unless otherwise noted. VCTRL1 = VCTRL2. V_{CTRL} is the attenuation voltage at the VCTRL1 and VCTRL2 pins. V_{CTRL} = 1800 mV, unless otherwise specified. Measurements in IF mode performed with a 90° hybrid, Register 0x03, Bit 7 = 1, and f_{IF} = 3.5 GHz.

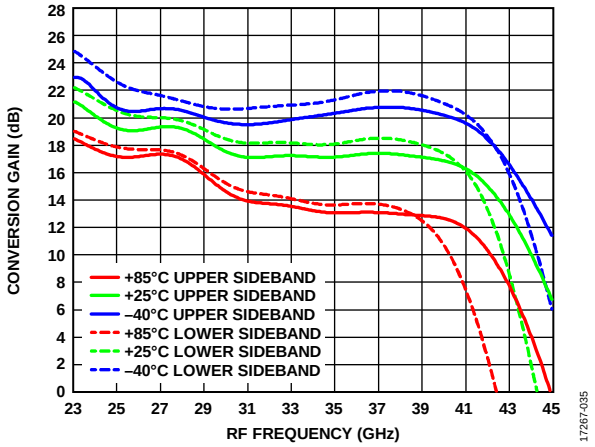

Figure 33. Conversion Gain vs. RF Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

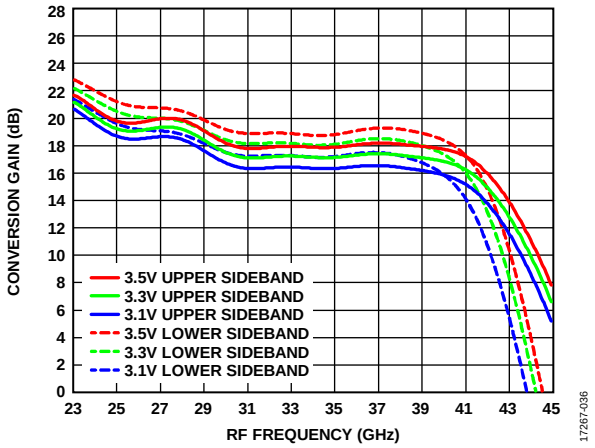

Figure 34. Conversion Gain vs. RF Frequency at Maximum Gain for Various Supply Voltages, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

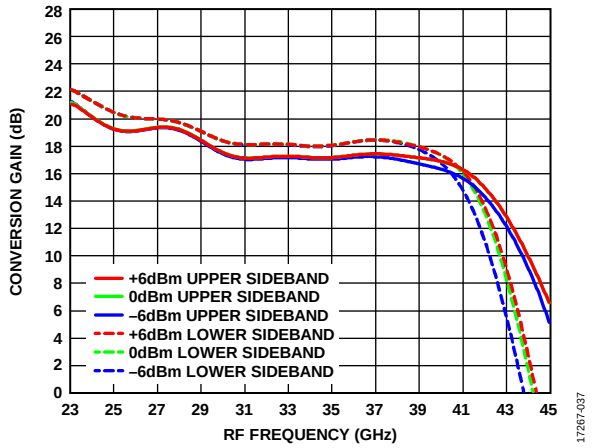

Figure 35. Conversion Gain vs. RF Frequency at Maximum Gain for Various LO Inputs, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

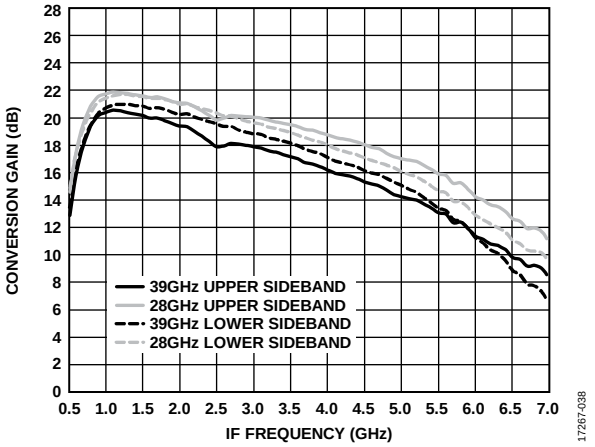

Figure 36. Conversion Gain vs. IF Frequency at f_{RF} = 28 GHz and 39 GHz at Maximum Gain (Upper Sideband and Lower Sideband)

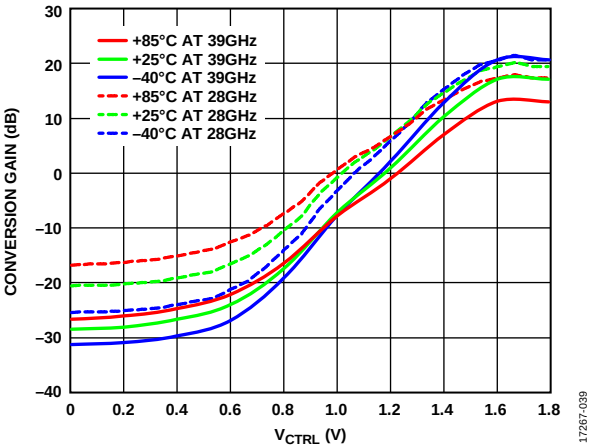

Figure 37. Conversion Gain vs. V_{CTRL} at Various Temperatures at f_{RF} = 28 GHz and 39 GHz, f_{IF} = 3.5 GHz (Upper Sideband)

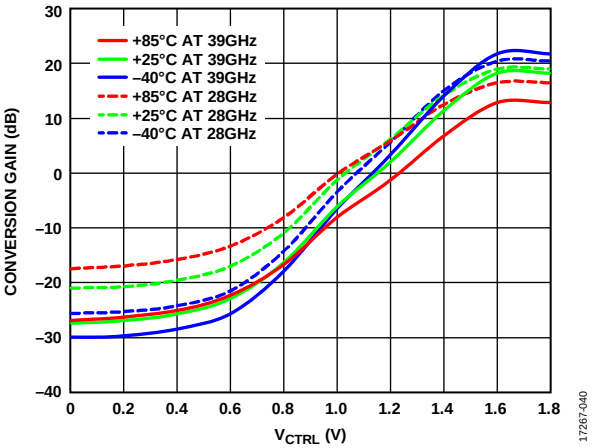

Figure 38. Conversion Gain vs. V_{CTRL} at Various Temperatures at f_{RF} = 28 GHz and 39 GHz, f_{IF} = 3.5 GHz (Lower Sideband)

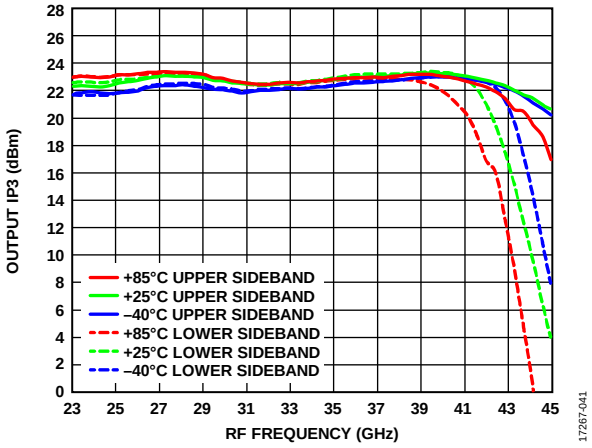

Figure 39. Output IP3 vs. RF Frequency at Maximum Gain for Various Temperatures, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

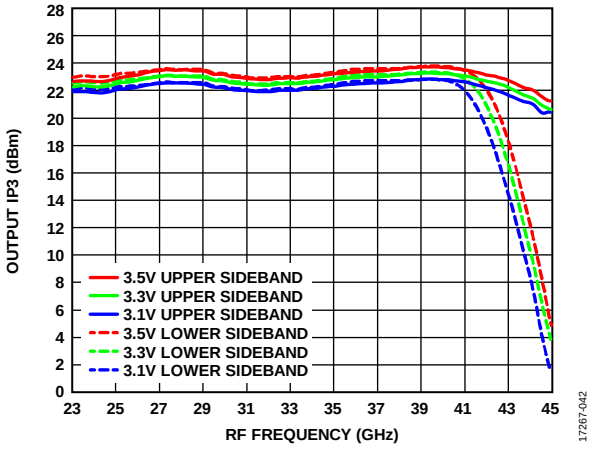

Figure 40. Output IP3 vs. RF Frequency at Maximum Gain for Various Supply Voltages, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

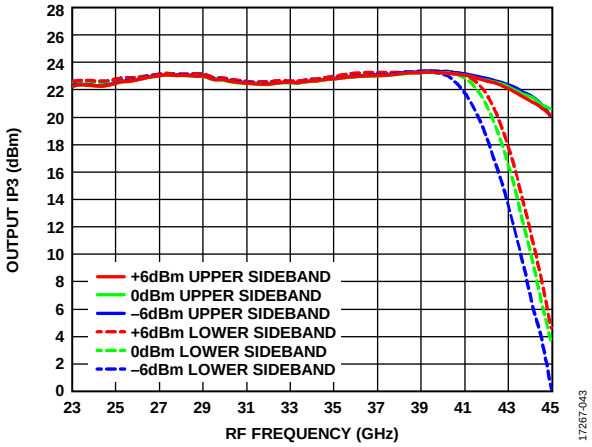

Figure 41. Output IP3 vs. RF Frequency at Maximum Gain for Various LO Inputs, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

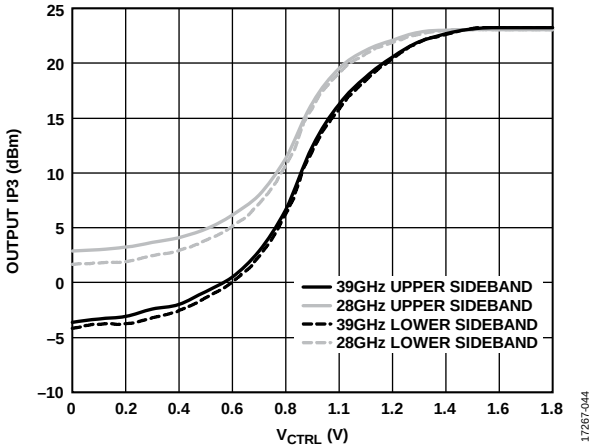

Figure 42. Output IP3 vs. V_{CTRL} at f_{RF} = 28 GHz and 39 GHz, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

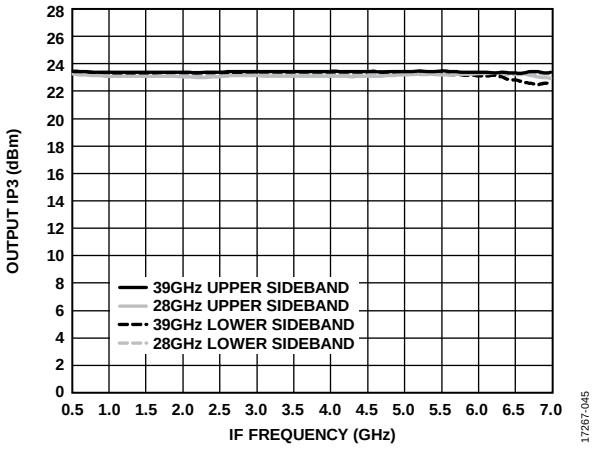

Figure 43. Output IP3 vs. IF Frequency at f_{RF} = 28 GHz and 39 GHz at Maximum Gain, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing (Upper Sideband and Lower Sideband)

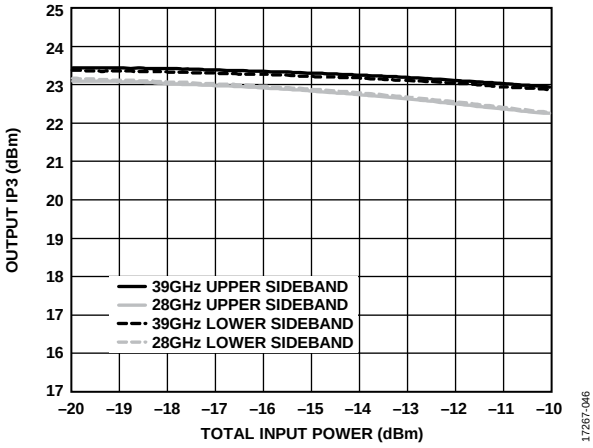

Figure 44. Output IP3 vs. Total Input Power at f_{RF} = 28 GHz and 39 GHz at 20 MHz Spacing, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

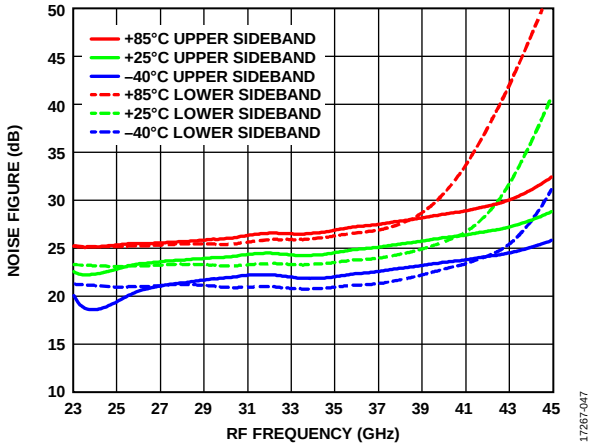

Figure 45. Noise Figure vs. RF Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

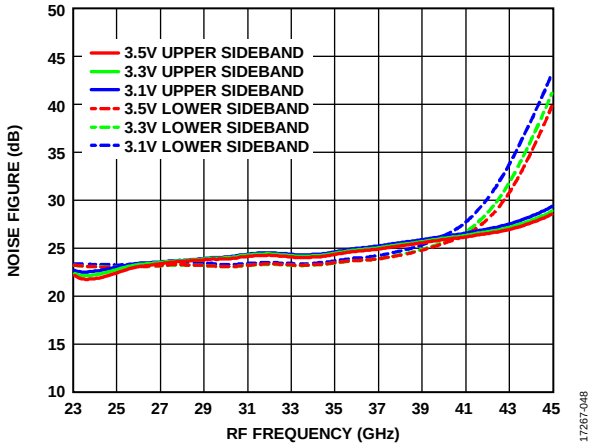

Figure 46. Noise Figure vs. RF Frequency at Maximum Gain for Various Supply Voltages, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

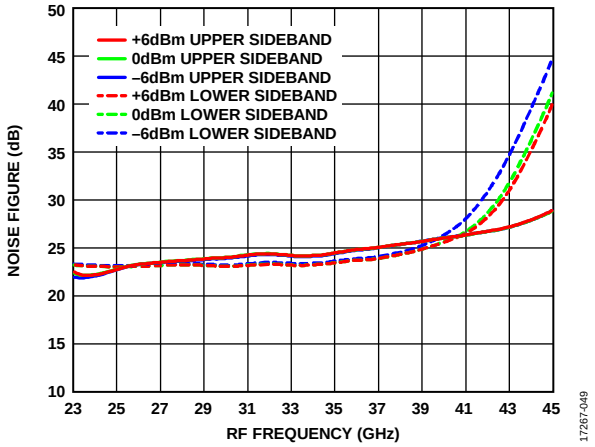

Figure 47. Noise Figure vs. RF Frequency at Maximum Gain for Various LO Inputs, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

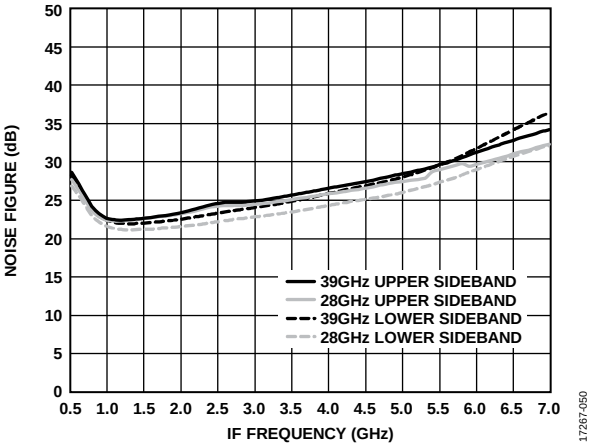

Figure 48. Noise Figure vs. IF Frequency at f_{RF} = 28 GHz and 39 GHz at Maximum Gain (Upper Sideband and Lower Sideband)

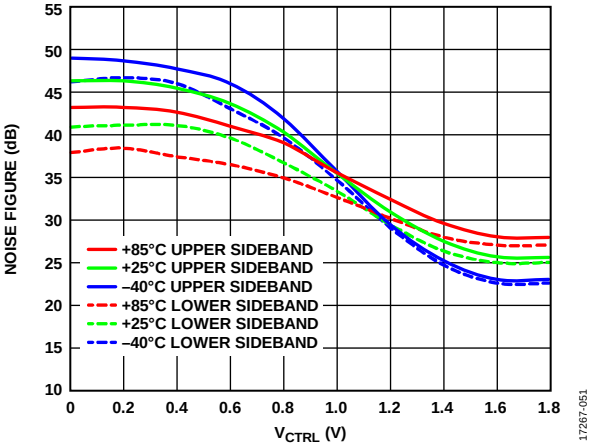

Figure 49. Noise Figure vs. V_{CTRL} at Various Temperatures, f_{IF} = 3.5 GHz, (Upper Sideband and Lower Sideband)

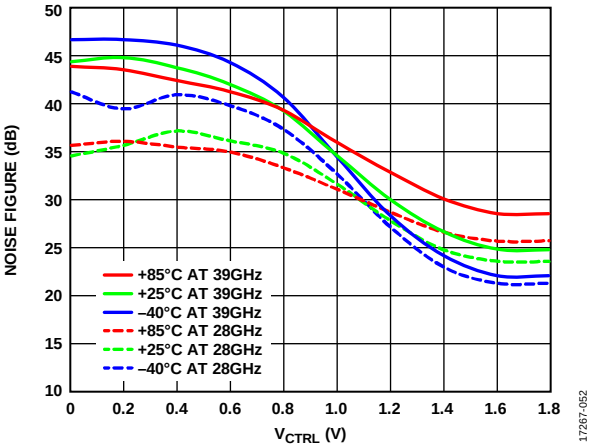

Figure 50. Noise Figure vs. V_{CTRL} for Various Temperatures at f_{RF} = 28 GHz and 39 GHz, f_{IF} = 3.5 GHz (Lower Sideband)

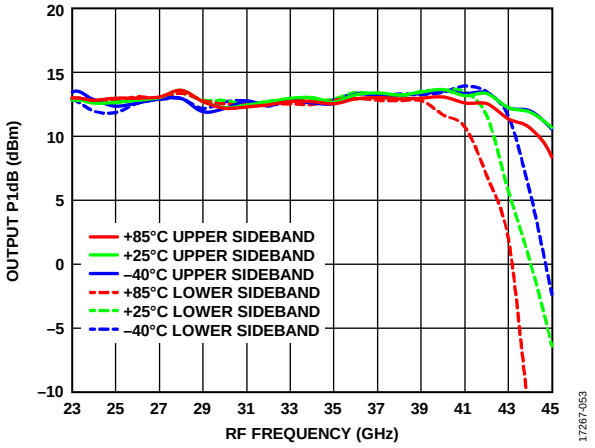

Figure 51. Output P1dB vs. RF Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

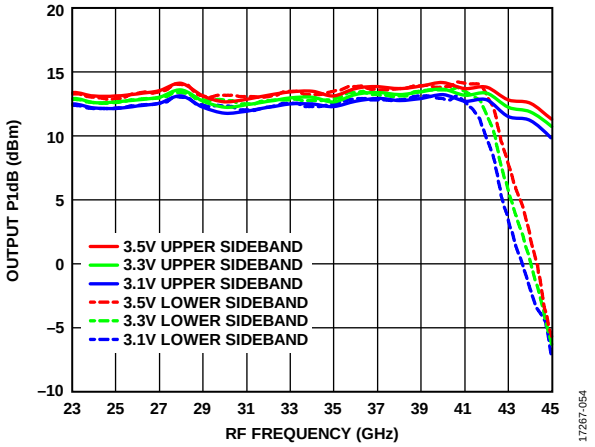

Figure 52. Output P1dB vs. RF Frequency at Maximum Gain for Various Supply Voltages, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

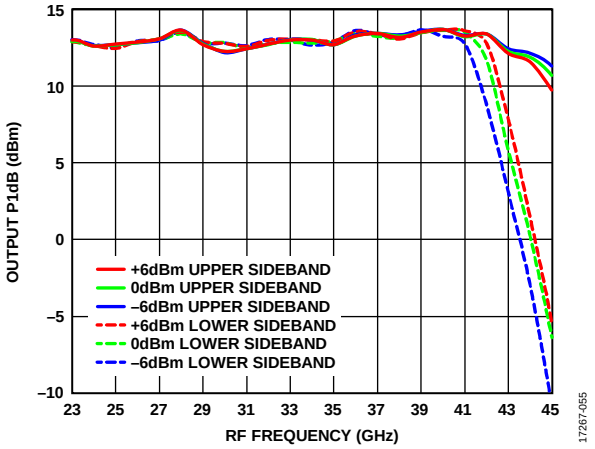

Figure 53. Output P1dB vs. RF Frequency at Maximum Gain for Various LO Inputs, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

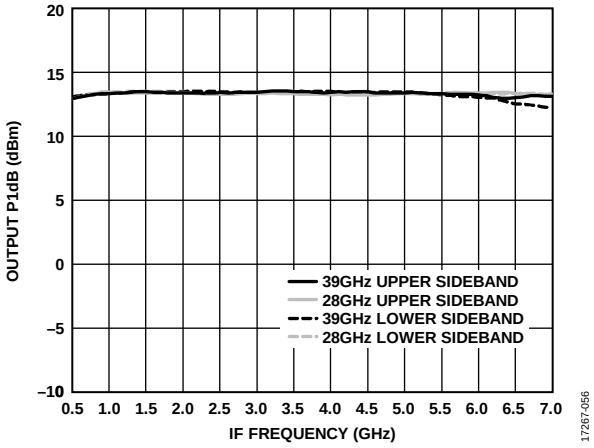

Figure 54. Output P1dB vs. IF Frequency at f_{RF} = 28 GHz and 39 GHz at Maximum Gain (Upper Sideband and Lower Sideband)

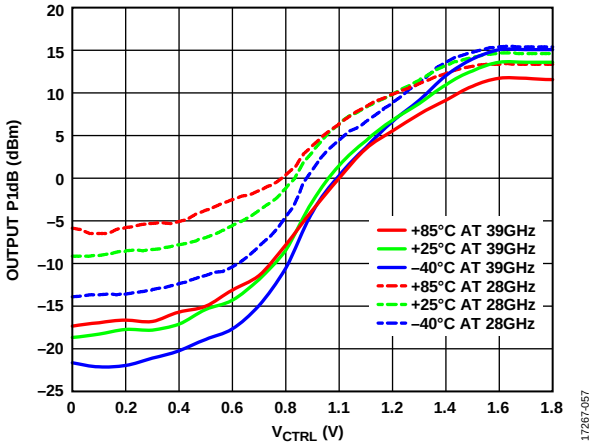

Figure 55. Output P1dB vs. V_{CTRL} for Various Temperatures at f_{RF} = 28 GHz and 39 GHz, f_{IF} = 3.5 GHz (Upper Sideband)

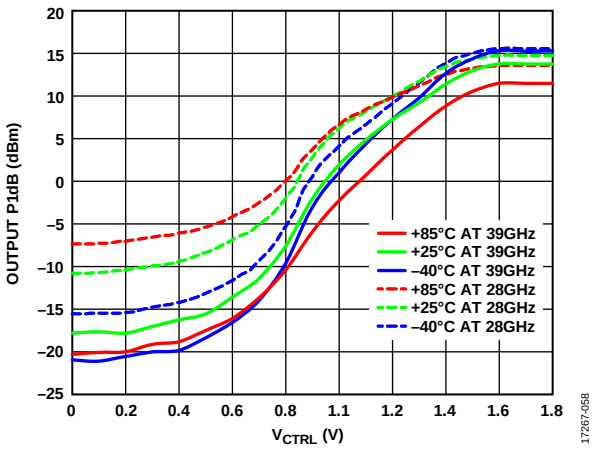

Figure 56. Output P1dB vs. V_{CTRL} for Various Temperatures at f_{RF} = 28 GHz and 39 GHz, f_{IF} = 3.5 GHz (Lower Sideband)

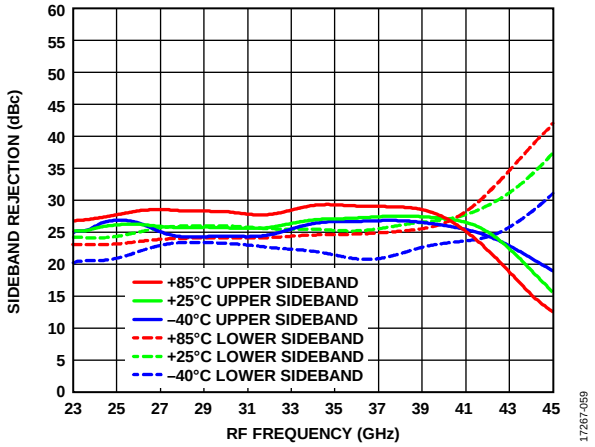

Figure 57. Sideband Rejection vs. RF Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz, Uncalibrated (Upper Sideband and Lower Sideband)

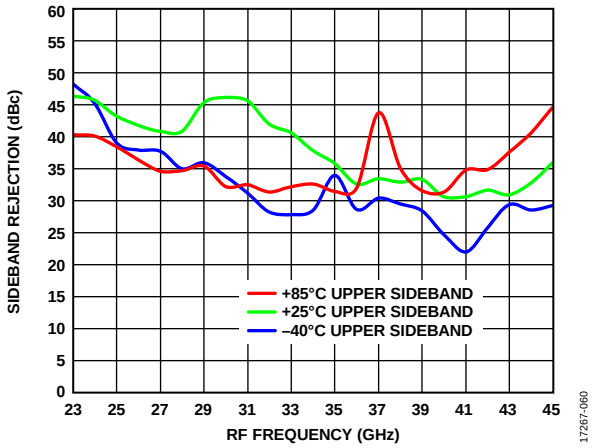

Figure 58. Sideband Rejection vs. RF Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz, Calibrated at 25°C (Upper Sideband). Note: Calibrated Using LOAMP_PH_ADJ_ Q_FINE and LOAMP_PH_ADJ_I_FINE Bits

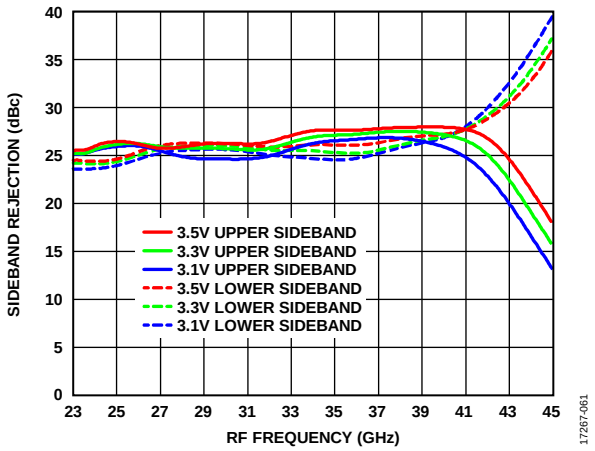

Figure 59. Sideband Rejection vs. RF Frequency at Maximum Gain for Various Supply Voltages, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

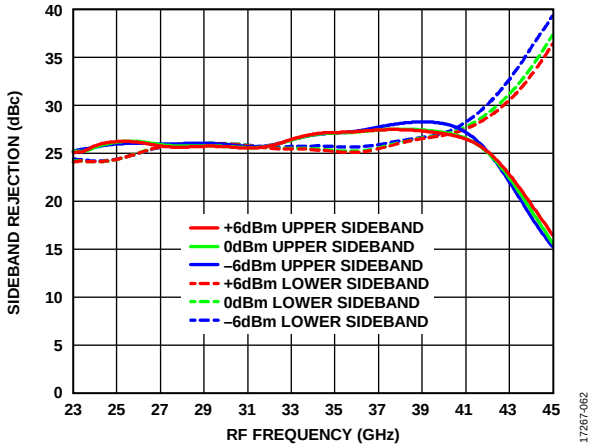

Figure 60. Sideband Rejection vs. RF Frequency at Maximum Gain for Various LO Inputs, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

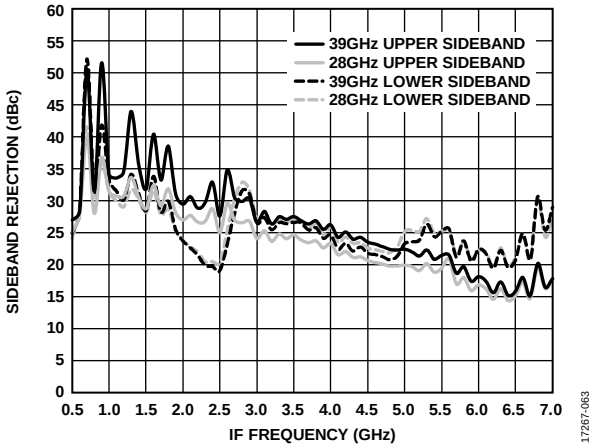

Figure 61. Sideband Rejection vs. IF Frequency at f_{RF} = 28 GHz and 39 GHz at Maximum Gain (Upper Sideband and Lower Sideband)

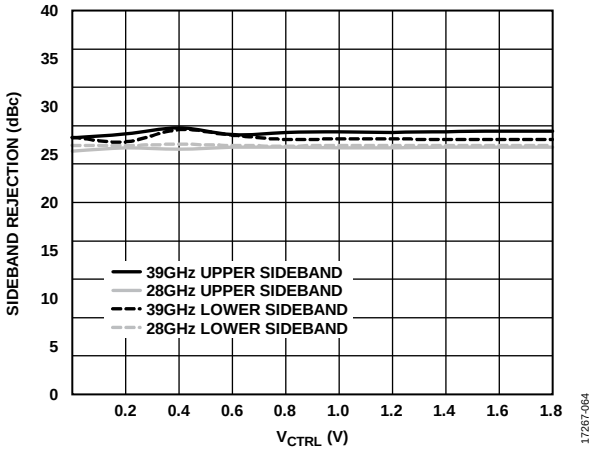

Figure 62. Sideband Rejection vs. V_{CTRL} at f_{RF} = 28 GHz and 39 GHz, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

ENVELOPE DETECTOR PERFORMANCE

IF and I/Q amplitude = −20 dBm, VCC_DRV = VCC2_DRV = VCC_AMP2 = VCC_ENV = VCC_AMP1 = VCC_BG2 = VCC_MIXER = VCC_BG = VCC_QUAD = 3.3 V, DVDD = VCC_VVA = 1.8 V, T_A = 25°C, and set Register 0x0A to 0xE700, unless otherwise noted.

Measurements in IF mode performed with a 90° hybrid, Register 0x03, Bit 7 = 1, IF f_{IF} = 3.5 GHz.

Measurements in I/Q mode are measured as a composite of the I and Q channel performance, V_{CM} = 0 V, Register 0x03, Bit 7 = 0, and Register 0x05, Bits[6:0] = 0x051, unless otherwise noted. I/Q f_{BB} = 100 MHz.

VCTRL1 = VCTRL2. V_{CTRL} is the attenuation voltage at the VCTRL1 and VCTRL2 pins. V_{CTRL} = 1800 mV, unless otherwise specified.

Envelope detector measurements made with Register 0x03, Bit 5 = 1.

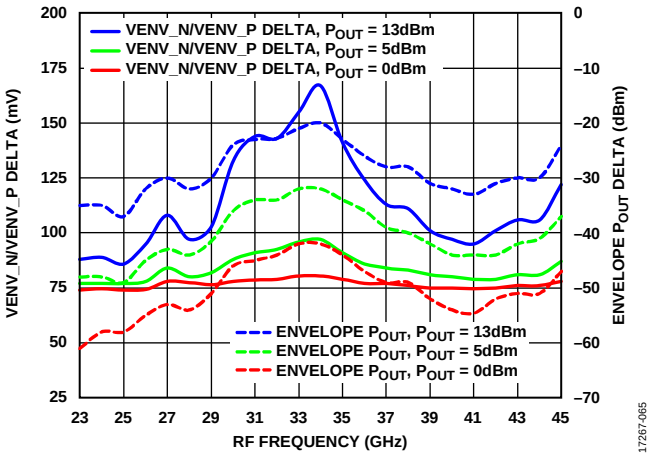

Figure 63. VENV_N/VENV_P Delta and Envelope P_{OUT} Delta vs. RF Frequency at Various Output Power Levels, Envelope Frequency = 100 MHz, V_{CTRL} = 1800 mV, T_A = 25°C, LO = 0 dBm, IF = 2 GHz (Upper Sideband)

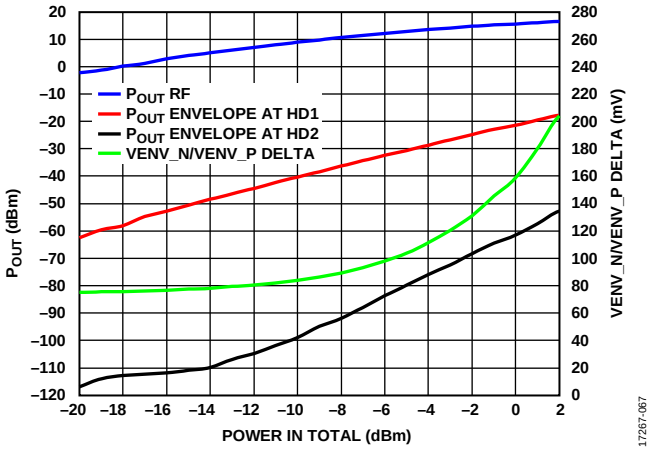

Figure 65. P_{OUT} and VENV_N/VENV_P Delta vs. Power In Total for P_{OUT} RF, P_{OUT} Envelope HD1, P_{OUT} Envelope HD2, and VENV_N/VENV_P Delta, Measurements Performed with Two Tones with 100 MHz Separation, f_{RF} = 28 GHz, V_{CTRL} = 1800 mV

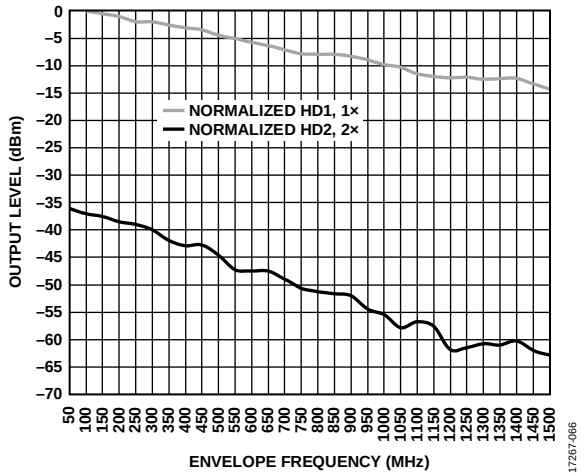

Figure 64. Output Level vs. Envelope Frequency for Normalized Harmonic Distortion (HD1), 1× and Normalized Harmonic Distortion(HD2), 2×, f_{RF} = 28 GHz, LO = 0 dBm at 25°C, HD1 and HD2 Measurement Performed with Two Tones with Delta Equal to Envelope Frequency, HD2 Normalized to HD1 Level at 50 MHz

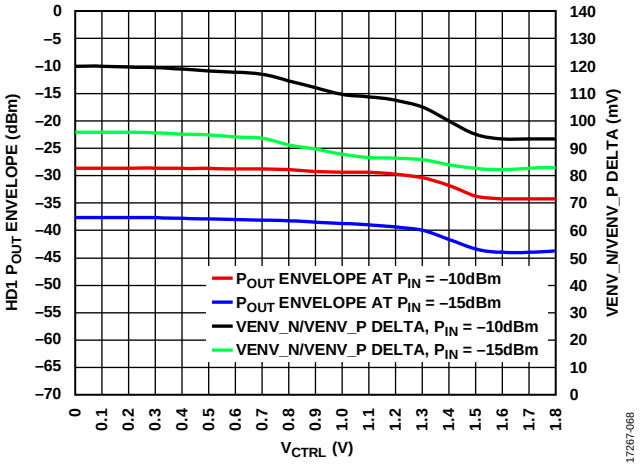

Figure 66. HD1 P_{OUT} Envelope and VENV_N/VENV_P Delta vs. V_{CTRL} at Various Total Input Power (P_{IN}) Levels, Measurements Performed at 28 GHz with Two Input Tones with Separation of 100 MHz

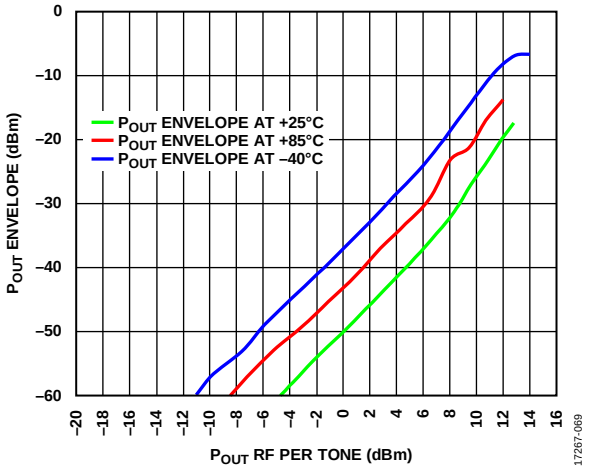

Figure 67. P_{OUT} Envelope vs. P_{OUT} RF per Tone at Various Temperatures at f_{RF} = 33 GHz, Measurement Performed at 3.5 GHz IF with Two Tones at 100 MHz Spacing, V_{CTRL} = 1800 mV

RETURN LOSS AND ISOLATION

IF and I/Q amplitude = −20 dBm, VCC_DRV = VCC2_DRV = VCC_AMP2 = VCC_ENV = VCC_AMP1 = VCC_BG2 = VCC_MIXER = VCC_BG = VCC_QUAD = 3.3 V, DVDD = VCC_VVA = 1.8 V, T_A = 25°C, and set Register 0x0A to 0xE700, unless otherwise noted.

Measurements in IF mode performed with a 90° hybrid, Register 0x03, Bit 7 = 1, and f_{IF} = 3.5 GHz.

Measurements in I/Q mode are measured as a composite of the I and Q channel performance, V_{CM} = 0 V, Register 0x03, Bit 7 = 0, and Register 0x05, Bits[6:0] = 0x051, unless otherwise noted. I/Q f_{BB} = 100 MHz.

VCTRL1 = VCTRL2. V_{CTRL} is the attenuation voltage at the VCTRL1 and VCTRL2 pins. V_{CTRL} = 1800 mV, unless otherwise specified.

Envelope detector measurements made with Register 0x03, Bit 5 = 1.

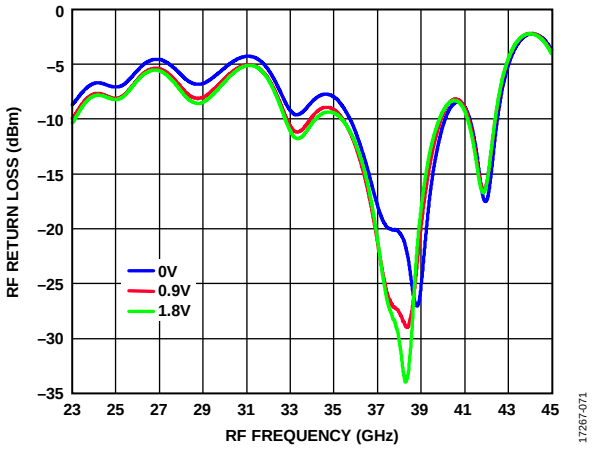

Figure 68. RF Return Loss vs. RF Frequency at Various V_{CTRL} Voltages

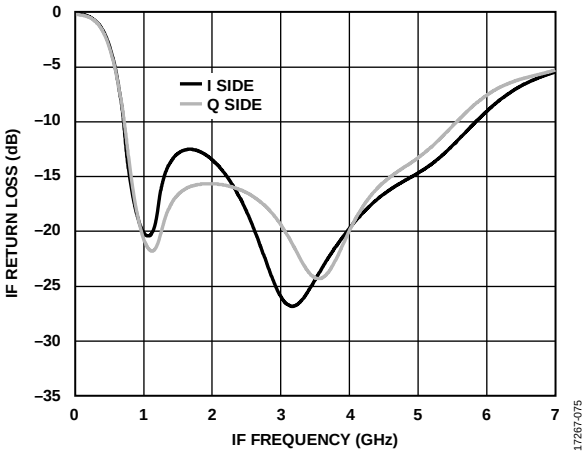

Figure 70. IF Return Loss vs. IF Frequency (Taken Without Hybrid)

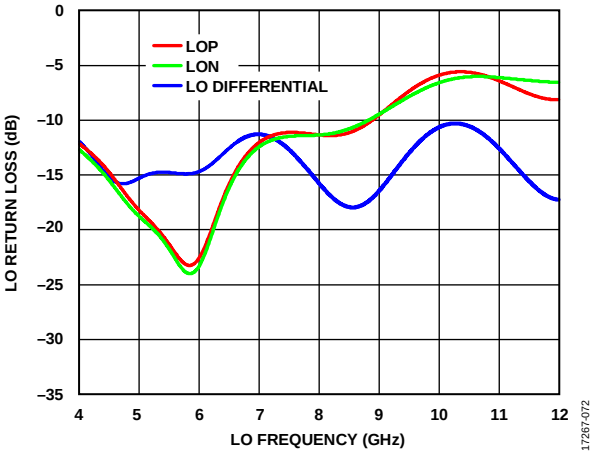

Figure 69. LO Return Loss vs. LO Frequency

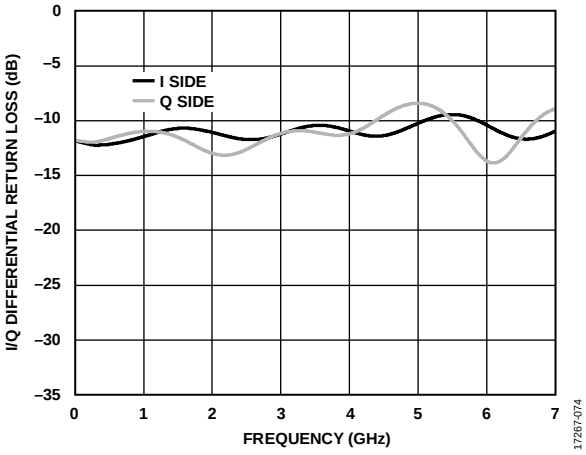

Figure 71. I/Q Differential Return Loss vs. Frequency (Taken Without Hybrids or Baluns)

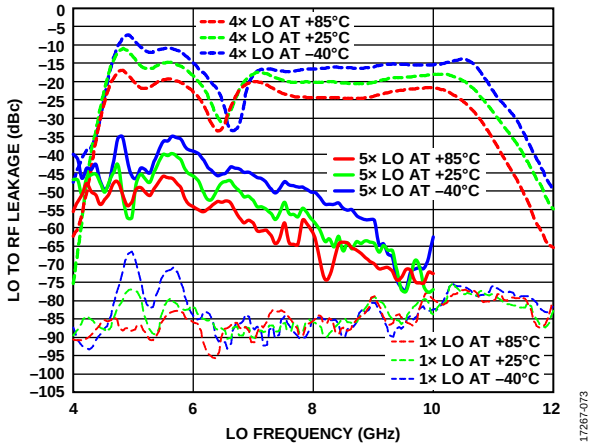

Figure 72. LO to RF Leakage vs. LO Frequency for 4× LO, 5× LO, and 1× LO at Various Temperatures (Uncalibrated)

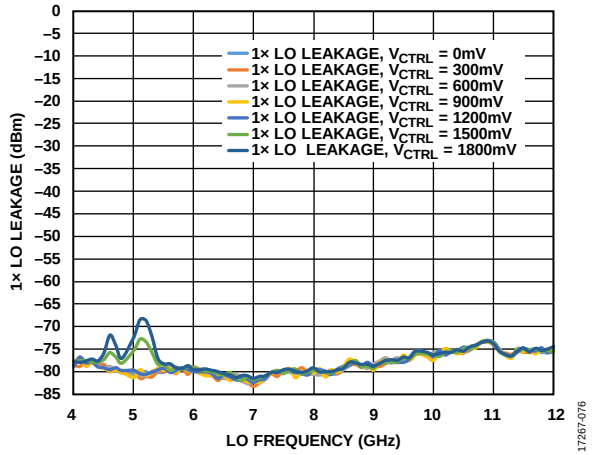

Figure 73. 1× LO Leakage vs. LO Frequency at Different V_{CTRL} Settings (Uncalibrated)

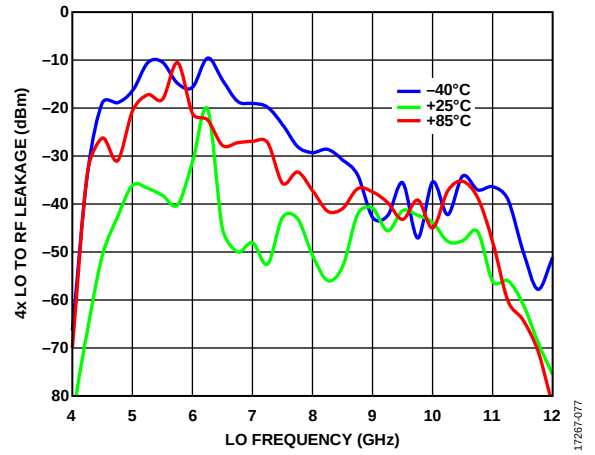

Figure 74. 4× LO to RF Leakage vs. LO Frequency at Various Temperatures (Calibrated). Note: Calibrated at Each Frequency Using MXER_OFF_ADJ_I_N, MXER_OFF_ADJ_I_P, MXER_OFF_ADJ_Q_N, and MXER_OFF_ADJ_Q_P Bits at T_A = 25°C

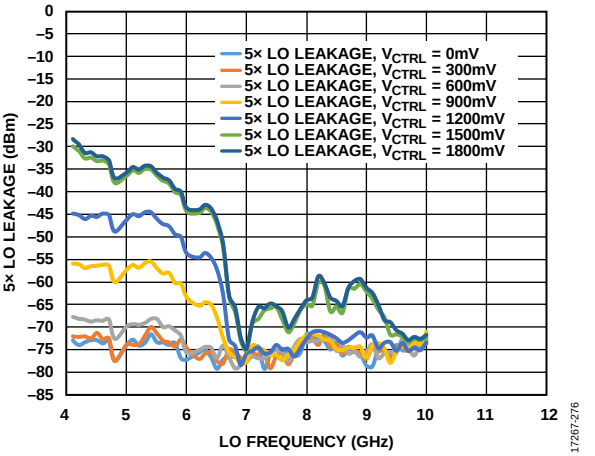

Figure 75. 5× LO Leakage vs. LO Frequency at Different V_{CTRL} Settings (Uncalibrated)

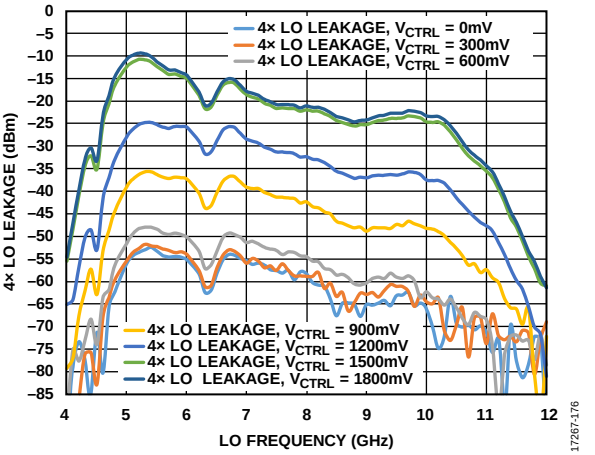

Figure 76. 4× LO Leakage vs. LO Frequency at Different V_{CTRL} Settings (Uncalibrated)

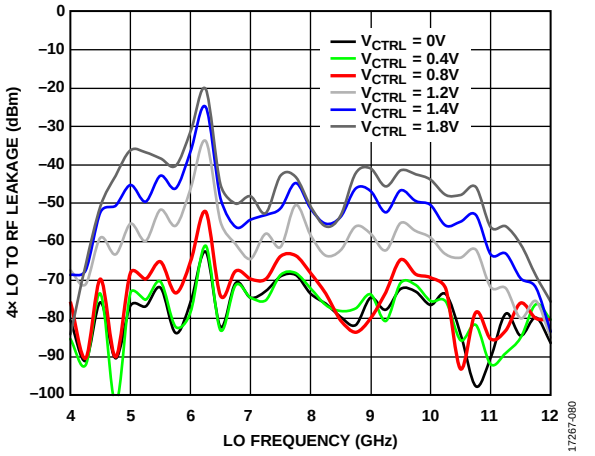

Figure 77. 4× LO to RF Leakage vs. LO Frequency at Various V_{CTRL} (Calibrated) Note: Calibrated at Each Frequency Using MXER_OFF_ADJ_I_N, MXER_OFF_ADJ_I_P, MXER_OFF_ADJ_Q_N, and MXER_OFF_ADJ_Q_P Bits at V_{CTRL} = 1800 mV

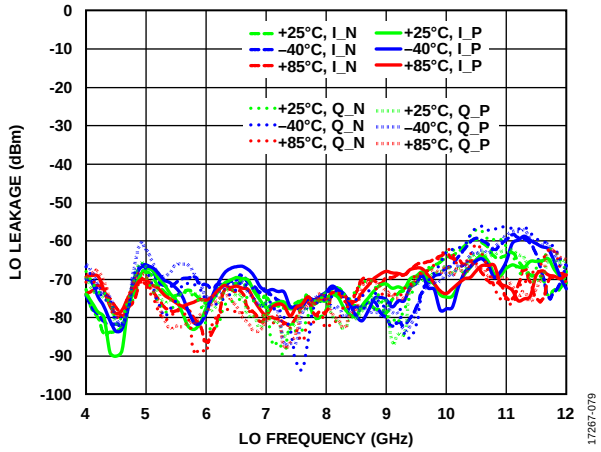

Figure 78. LO Leakage vs. LO Frequency at Various Temperatures at I_N, I_P, Q_N, and Q_P (Taken Without Hybrid(s))

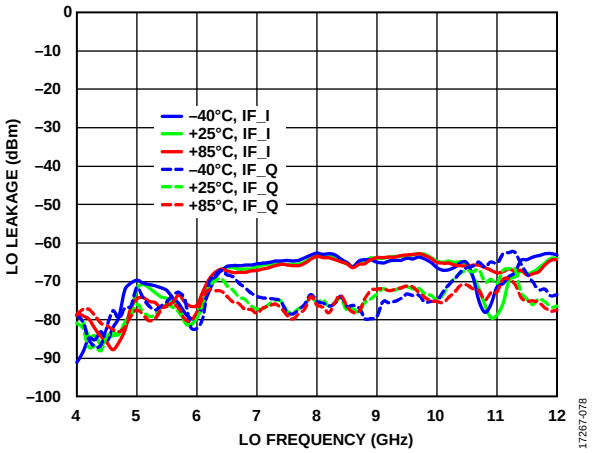

Figure 80. LO Leakage vs. LO Frequency at Various Temperatures at IF_I and IF_Q Ports(Taken Without Hybrid)

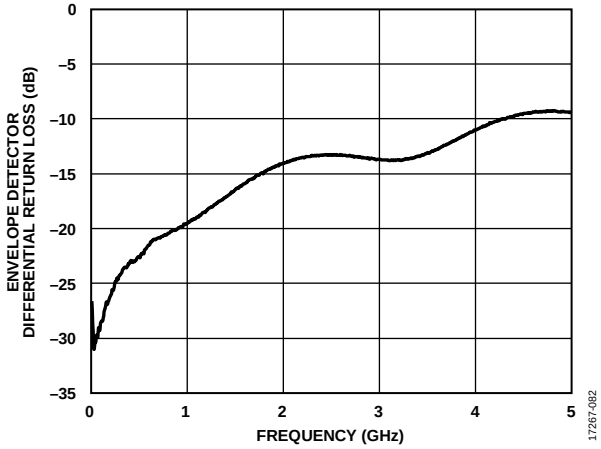

Figure 79. Envelope Detector Differential Return Loss vs. Frequency

M × N SPURIOUS PERFORMANCE

Mixer spurious products are measured in dBc from the RF output power level. Spurious frequencies are calculated by

$$|(M \times IF) + (N \times LO)| \text{ (for IF Mode)}$$

$$|(M \times IQ) + (N \times LO)| \text{ (for IQ Mode)}$$

N/A means not applicable. Blank cells in the spurious performance tables indicate that the frequency is above 50 GHz and is not measured. REF stands for reference RF output signal.

The LO frequencies are referred from the frequencies applied to the ADMV1013. IF and I/Q amplitude = −20 dBm.

VCC_DRV = VCC2_DRV = VCC_AMP2 = VCC_ENV = VCC_AMP1 = VCC_BG2 = VCC_MIXER = VCC_BG = VCC_QUAD = 3.3 V, DVDD = VCC_VVA = 1.8 V, T_A = 25°C, and set Register 0x0A to 0xE700, unless otherwise noted.

Measurements in IF mode performed with a 90° hybrid, Register 0x03, Bit 7 = 1, and f_{IF} = 3.5 GHz.

Measurements in I/Q mode are measured as a composite of the I and Q channel performance, V_{CM} = 0 V, Register 0x03, Bit 7 = 0, and Register 0x05, Bits[6:0] = 0x051, unless otherwise noted. I/Q f_{BB} = 100 MHz.

VCTRL1 = VCTRL2. V_{CTRL} is the attenuation voltage at the VCTRL1 and VCTRL2 pins. V_{CTRL} = 1800 mV, unless otherwise specified.

I/Q Mode

f_{BB} = 100 MHz at −20 dBm, LO = 6.975 GHz at +6 dBm.

		N × LO							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
M × IQ	**−2**	93	105	103	122	79	109	89	108
	−1	93	95	85	57	26	65	53	110
	0	N/A	80	72	53	20	61	35	73
	+1	93	96	74	32	REF	41	37	84
	+2	93	107	86	91	57	89	91	83

f_{BB} = 100 MHz at −20 dBm, LO = 9.725 GHz at +6 dBm, and f_{RF} = 39 GHz.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IQ	**−2**	97	116	95	116	89	113
	−1	101	100	37	62	26	90
	0	N/A	77	40	63	20	77
	+1	97	91	18	36	REF	68
	+2	101	118	80	99	64	103

IF Mode

f_{IF} = 3.5 GHz at −20 dBm, LO = 6.125 GHz at +6 dBm, and f_{RF} = 28 GHz.

		N × LO								
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
M × IF	**−2**	76	117	120	109	77	92	90	84	45
	−1	68	90	80	77	23	46	56	53	44
	0	N/A	71	71	26	9	34	24	20	30
	+1	76	92	58	18	REF	24	32	61	
	+2	68	84	75	70	58	80	82	75	

f_{IF} = 3.5 GHz at −20 dBm, LO = 8.875 GHz at +6 dBm, and f_{RF} = 39 GHz.

		N × LO						
		0	**1**	**2**	**3**	**4**	**5**	**6**
M × IF	**−2**	83	132	109	96	68	99	107
	−1	69	95	76	54	25	57	83
	0	N/A	69	44	53	16	52	
	+1	83	89	24	33	REF	58	
	+2	69	114	93	98	75		

f_{IF} = 3.5 GHz at −20 dBm, LO = 7.875 GHz at +6 dBm, and f_{RF} = 28 GHz.

		N × LO							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
M × IF	**−2**	82	140	115	107	69	99	97	95
	−1	65	120	91	41	REF	47	46	
	0	N/A	82	75	52	23	49	56	
	+1	82	94	60	70	26	75		
	+2	65	120	107	111	93	115		

f_{IF} = 3.5 GHz at −20 dBm, LO = 10.5 GHz at +6 dBm, and f_{RF} = 39 GHz.

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**−2**	96	122	99	91	70	94
	−1	80	85	28	26	REF	64
	0	N/A	83	34	43	16	
	+1	97	95	45	49	41	
	+2	79	113	88	103	102	

THEORY OF OPERATION

The ADMV1013 is a wideband microwave upconverter optimized for microwave radio designs operating in the 24 GHz to 44 GHz RF frequency range. See Figure 1 for a functional block diagram of the device. The ADMV1013 digital settings are controlled via the SPI. The ADMV1013 has two modes of operation:

- Baseband quadrature modulation (I/Q mode)
- Single-sideband upconversion (IF mode)

START-UP SEQUENCE

To use the voltage control RF VVA1 and RF VVA2, the VCC_VVA (1.8 V) supply must be on. The VCTRL1 pin and VCTRL2 pin control the gain of the RF VVA1 and the RF VVA2. Similarly, to use the SPI control, it is necessary to first turn on DVDD and then perform a hard reset by toggling the RST pin to logic low and then to logic high.

The ADMV1013 SPI settings require the default settings to be changed during startup for optimum performance.

Set Register 0x0A to 0xE700 after each power-up or reset.

BASEBAND QUADRATURE MODULATION (I/Q MODE)

In I/Q mode, the input impedance of the baseband pins (I_P, I_N, Q_P, and Q_N) are 100 Ω differential. These inputs can be loaded with a dc-coupled 100 Ω differential load. I_P and I_N are the differential baseband I inputs, and Q_P and Q_N are the differential baseband Q inputs. These inputs can operate from a V_{CM} of 0 V to 2.6 V. The baseband I/Q ports can operate from dc to 6.0 GHz at each I and Q channel.

To set the ADMV1013 in I/Q mode, set MIXER_IF_EN bit (Register 0x03, Bit 7) to 0.

When changing the external V_{CM}, the internal mixer gate voltage also must be changed. To make this change, set the MIXER_VGATE bits (Register 0x05, Bits[6:0]). The MIXER_VGATE value follows the V_{CM} such as, that for a 0 V to 1.8 V V_{CM}, MIXER_VGATE = 23.89 V_{CM} + 81, and for a >1.8 V to 2.6 V V_{CM}, MIXER_VGATE = 23.75 V_{CM} + 1.25.

SINGLE-SIDEBAND UPCONVERSION (IF MODE)

The ADMV1013 features the ability to upconvert a real IF input anywhere from 0.8 GHz to 6.0 GHz while suppressing the unwanted sideband by typically better than 26 dBc. The IF inputs are quadrature to each other, 50 Ω single ended, and are internally dc-coupled. IF_I and IF_Q are the quadrature IF inputs. An external 90° hybrid is required to select the appropriate sideband. To configure the ADMV1013 in IF mode, set the MIXER_IF_EN bit (Register 0x03, Bit 7) to 1. The MIXER_IF_EN bit defaults to IF mode on SPI startup and reset.

In addition, the baseband pins (I_P, I_N, Q_P, and Q_N) must see an open load for optimum performance in IF mode.

LO INPUT PATH

The LO input path operates from 5.4 GHz to 10.25 GHz with an LO amplitude range of −6 dBm to +6 dBm. The LO has an internal quadrupler (×4) and a programmable band-pass filter. The LO band-pass filter is programmable using the QUAD_FILTERS bits (Register 0x09, Bits[3:0]). See the Performance at Different Quad Filter Settings section for more information on the QUAD_FILTERS settings.

The LO path can operate either differentially or single ended. LOP and LON are the inputs to the LO path. The LO path can switch from differential to single-ended operation by setting the QUAD_SE_MODE bits (Register 0x09, Bits[9:6]). See the Performance Between Differential vs. Single-Ended LO Input section for more information. When using the LO as single ended, the unused LO input pin must be terminated with a 50 Ω load.

Figure 81 shows a block diagram of the LO path.

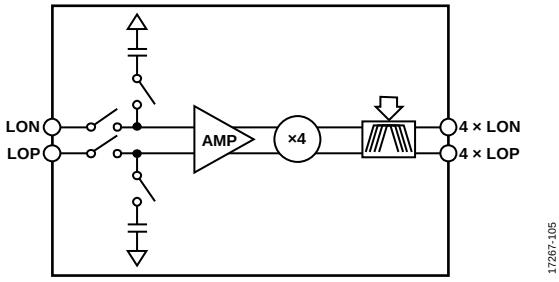

Figure 81. LO Path Block Diagram

Enable the quadrupler by setting the QUAD_PD bits (Register 0x03, Bits[13:11]) to 0x0. To power down the quadrupler, set these bits to 0x7.

SIDEBAND SUPPRESSION OPTIMIZATION

Unwanted sideband can be upconverted from the quadrature error by generating the quadrature LO signals and the external quadrature inputs. Deviation from ideal quadrature (that is, total sideband rejection and no sideband tone upconverts) on these signals limits the amount of achievable sideband rejection.

The ADMV1013 offers approximately 25° of quadrature phase adjustment in the LO path quadrature signals to suppress the sideband. Make these adjustments through the LOAMP_PH_ADJ_I_FINE bits (Register 0x05, Bits[13:7]) and the LOAMP_PH_ADJ_Q_FINE bits (Register 0x06, Bits[13:7]). These bits reject the unwanted sideband signal. To achieve the required sideband suppression, it may be necessary to adjust the amplitude difference between the quadrature inputs, as well externally.

In I/Q mode, the recommendation is to adjust the sideband suppression through the external transceiver digital-to-analog converter (DAC).

CARRIER FEEDTHROUGH NULLING

Carrier feedthrough results from minute dc offsets that occur on the internal mixer. In an I/Q modulator, nonzero differential offsets mix with the LO and result in carrier feedthrough to the RF output. In addition to this effect, some of the signal power at the LO input couples directly to the RF output (this may be because of the bond wire to bond wire coupling or coupling through the silicon substrate). The net carrier feedthrough at the RF output is the vector combination of the signals that appear at the output because of these two effects.

The ADMV1013 offers, in IF mode, LO feedthrough offset calibration adjustment in the LO path. Make these adjustments through the MXER_OFF_ADJ_I_N bits (Register 0x07, Bits[8:2], the MXER_OFF_ADJ_I_P bits (Register 0x07, Bits[15:9]), the MXER_OFF_ADJ_Q_N bits (Register 0x08, Bits[8:2]), and the MXER_OFF_ADJ_Q_P bits (Register 0x08, Bits[15:9] in order to reject the unwanted LO signal.

For I/Q mode, the LO feedthrough offset amplitude and phase calibration optimization can be adjusted externally through a transceiver DAC.

ENVELOPE DETECTOR

The ADMV1013 features an envelope detector with a pseudo differential voltage output. The envelope detector output pins are VENV_P and VENV_N. The ADMV1013 turns on with the envelope detector turned off. To turn on the envelope detector, set the DET_EN bit (Bit 5, Register 0x03). The differential voltage output of the envelope detector rises linearly to the square of the input envelope voltage to the detector. The detector output ranges from −45 dBm to −20 dBm when the input two tone power ranges from −20 dBm to 0 dBm. The envelope detector has 350 MHz, 3 dB envelope bandwidth and 1 GHz, 10 dB envelope bandwidth. The envelope detector precedes the VVA and the output driver of the ADMV1013.

POWER DOWN AND RESET

The SPI of the ADMV1013 allows the user to power down the device circuits and reduce power consumption to typically 77 mW. To turn off the entire chip, set the BG_PD bit (Register 0x03, Bit 10) to 1. In addition, individual blocks of the circuit can be powered down individually. To power down the quadrupler, set the QUAD_PD bits (Register 0x03, Bits[13:11]) to 0x7. To power down the VGA, set the VGA_PD bit (Register 0x03, Bit 15) to 1. To power down the mixer, set the MIXER_PD bit (Register 0x03, Bit 14) to 1. To power down the detector, set the DET_EN bit (Register 0x03, Bit 5) to 0.

SERIAL PORT INTERFACE (SPI)

The SPI of the ADMV1013 allows the user to configure the device for specific functions or operations via a 4-wire SPI port. This interface provides users with added flexibility and customization. The SPI consists of four control lines: SCLK, SDI, SDO, and active low chip select lines, $\overline{\text{SEN}}$/$\overline{\text{SEN2}}$. $\overline{\text{SEN}}$ and $\overline{\text{SEN2}}$ must be connected together.

The ADMV1013 protocol consists of a write/read bit followed by six register address bits, 16 data bits, and a parity bit. Both the address and data fields are organized MSB first and end with the LSB. For a write, set the first bit to 0. For a read, set the first bit to 1.

The write cycle sampling must be performed on the rising edge. The 16 bits of the serial write data are shifted in, MSB to lower sideband. The ADMV1013 input logic level for the write cycle supports a 1.8 V interface.

For a read cycle, up to 16 bits of serial read data are shifted out, MSB first. After the 16 bits of data shift out, the parity bit shifts out. The output logic level for a read cycle is 1.8 V.

The parity bit always follows the direction of the data. If parity is not used, the transmitting end transmits zero instead of parity. The parity is odd, which means that the total number of ones transmitted during a command, including the read/write bit, the address bit, the data bit, and the parity bit, must be odd.

Figure 82 and Figure 83 show the SPI write and read protocol, respectively.

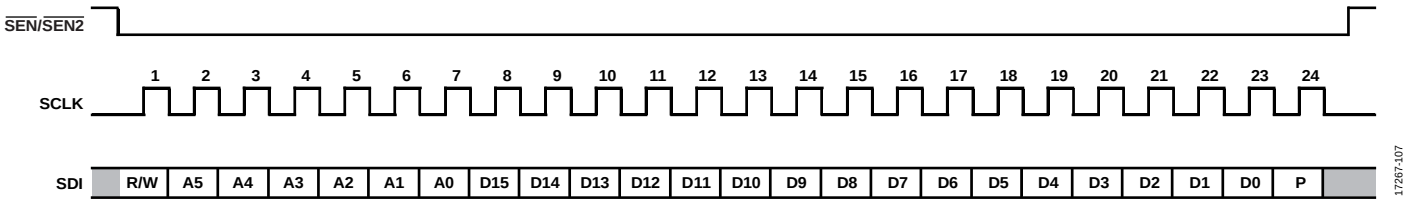

Figure 82. SPI Write Timing Diagram

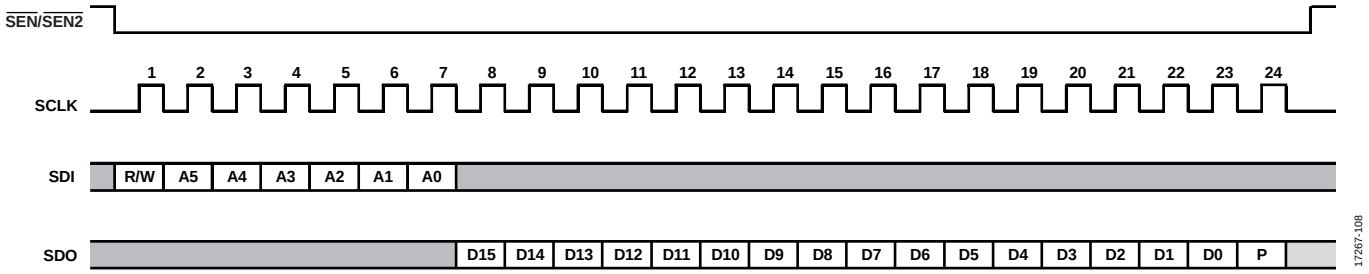

Figure 83. SPI Read Timing Diagram

APPLICATIONS INFORMATION

BASEBAND QUADRATURE MODULATION FROM LOW FREQUENCIES

Figure 84 shows the I/Q mode performance at low baseband input frequencies. The measurements were performed at 28 GHz, −10 dBm input power, V_{CM} = 0 V, Register 0x03, Bit 7 = 0, 0 dBm LO input power, and T_A = 25°C.

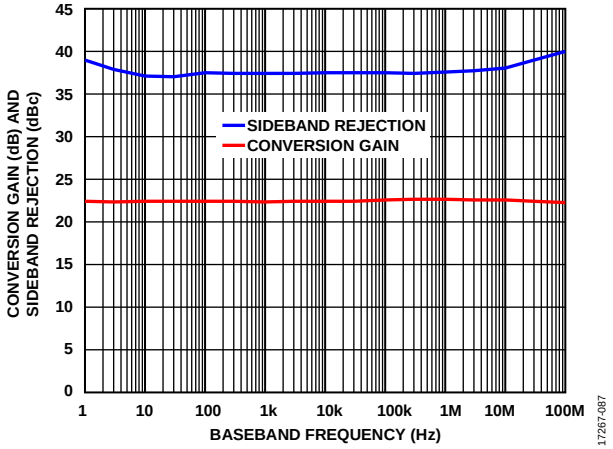

Figure 84. Conversion Gain and Sideband Rejection vs. Baseband Frequency

PERFORMANCE AT DIFFERENT QUAD FILTER SETTINGS

Figure 85 shows the conversion gain vs. RF frequency in IF mode at T_A = 25°C and LO input power = 0 dBm for different QUAD_FILTERS settings.

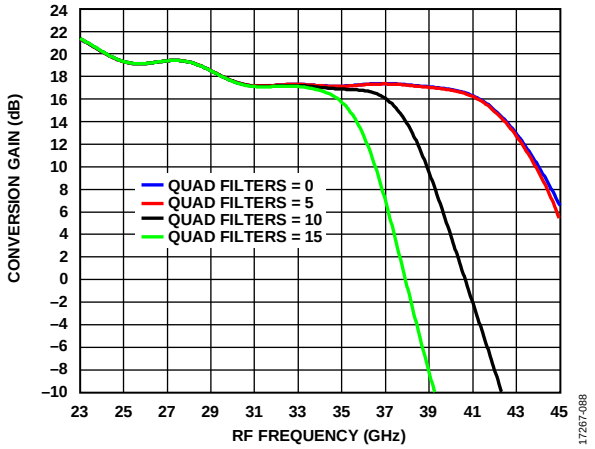

Figure 85. Conversion Gain vs. RF Frequency for Four Different QUAD_FILTERS Settings, f_{IF} = 3.5 GHz (Upper Sideband)

Figure 86 shows the 4× LO to RF leakage vs. 4× LO frequency at different quad filter settings.

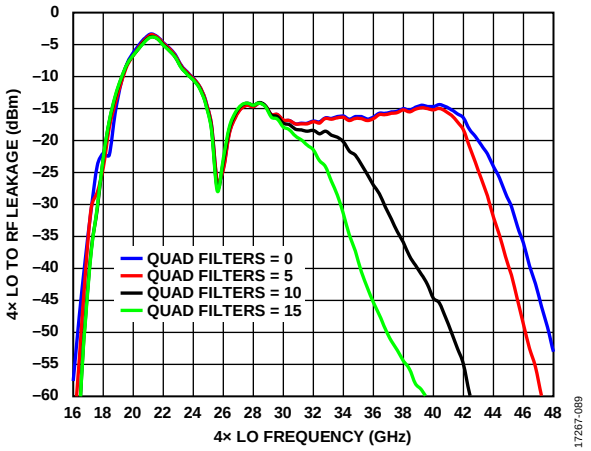

Figure 86.4× LO to RF Leakage vs. 4× LO Frequency for Four Different QUAD_FILTERS Settings

VVA TEMPERATURE COMPENSATION

Figure 87 shows the conversion gain vs. RF frequency at two different Register 0x0A settings, the recommended setting (0xE700) and a setting for higher gain, and three different temperatures for IF mode. The recommended value suggested in the Start-Up Sequence section provides the least variation in conversion gain over temperature. If the priority is to increase the conversion gain, Register 0x0A can be set to 0xFA00. However, at this value, the conversion gain variation over temperature can increase by 2 dB.

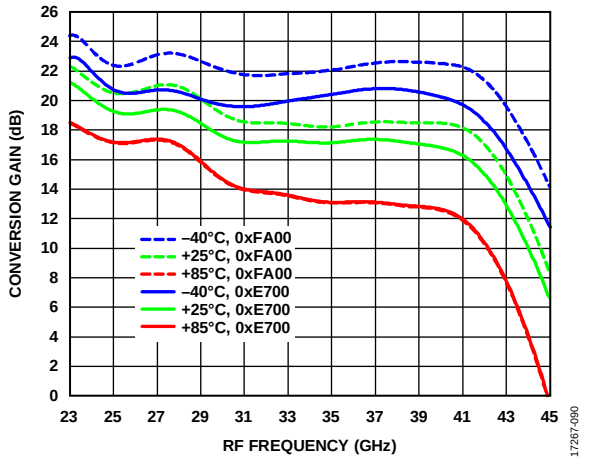

Figure 87. Conversion Gain vs. RF Frequency at Maximum Gain for Various Temperatures and Register 0x0A Settings (Recommended and Higher Gain Setting), f_{IF} = 3.5 GHz

Figure 88 shows the conversion gain vs. RF frequency at two different Register 0x0A settings, the recommended setting and the default setting, and three different temperatures for IF mode. The default values provides slightly less gain and a larger gain variation across temperature compared to the recommended setting.

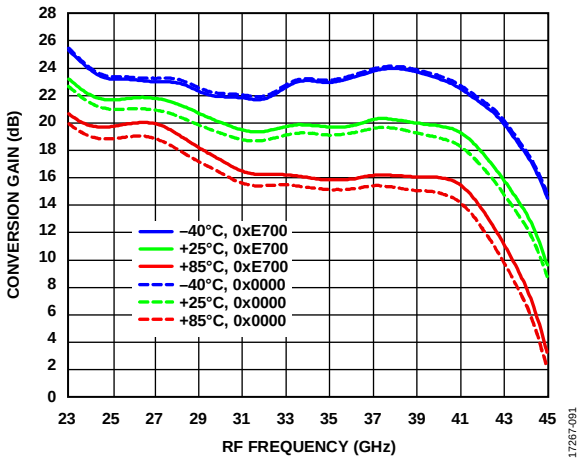

Figure 88. Conversion Gain vs. RF Frequency at Maximum Gain for Various Temperatures and Register 0x0A Settings (Default and Recommended Register 0x0A Settings), f_{IF} = 2 GHz

PERFORMANCE BETWEEN DIFFERENTIAL vs. SINGLE-ENDED LO INPUT

Figure 89 to Figure 91 show the conversion gain, output IP3, and sideband rejection performance for operating the ADMV1013 LO input as differential vs. single ended. The measurements were performed with 0 dBm LO input power, IF mode, with an IF frequency of 3.5 GHz, upper sideband, and T_A = 25°C.

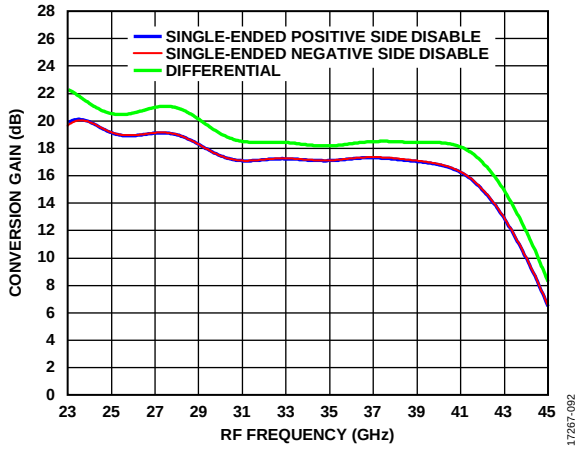

Figure 89. Conversion Gain vs. RF Frequency for Three Different LO Mode Settings, f_{IF} = 3.5 GHz (Upper Sideband)

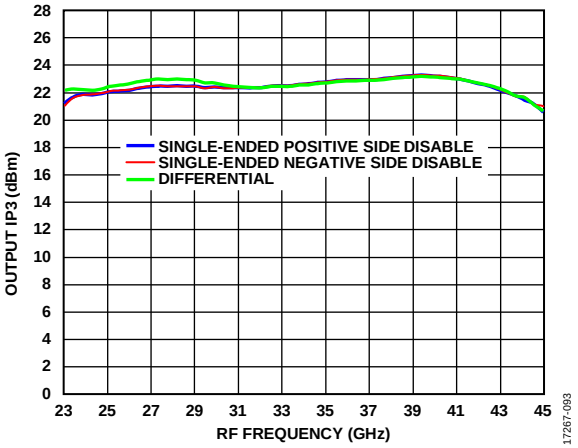

Figure 90. Output IP3 vs. RF Frequency for Three Different LO Mode Settings, RF Amplitude = –20 dBm per Tone at 20 MHz Spacing, f_{IF} = 3.5 GHz (Upper Sideband)

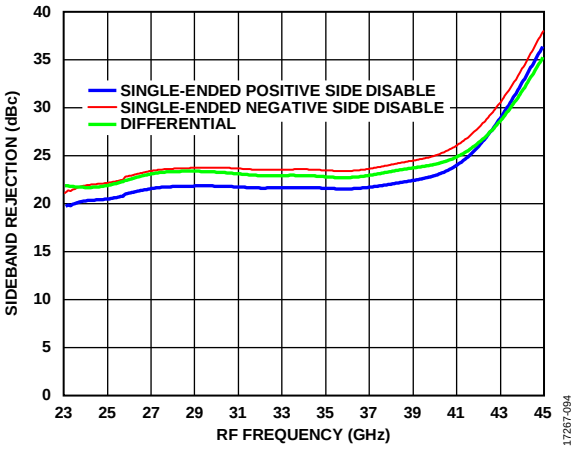

Figure 91. Sideband Rejection vs. RF Frequency for Three Different LO Mode Settings, RF Amplitude = –30 dBm per Tone at 20 MHz Spacing, f_{IF} = 3.5 GHz (Upper Sideband)

PERFORMANCE ACROSS RF FREQUENCY AT FIXED INPUT FREQUENCIES

The ADMV1013 quadrupler operates from 21.6 GHz to 41 GHz. When using the lower sideband, the conversion gain starts rolling off gradually after the quadrupler frequency reaches 41 GHz. When using the upper sideband, the conversion gain starts rolling off when the quadrupler frequency is 21.6 GHz.

Figure 92 and Figure 93 show the conversion gain vs. RF frequency in IF mode for fixed IF frequencies (T_A = 25°C, LO = 0 dBm) for the upper sideband and lower sideband, respectively.

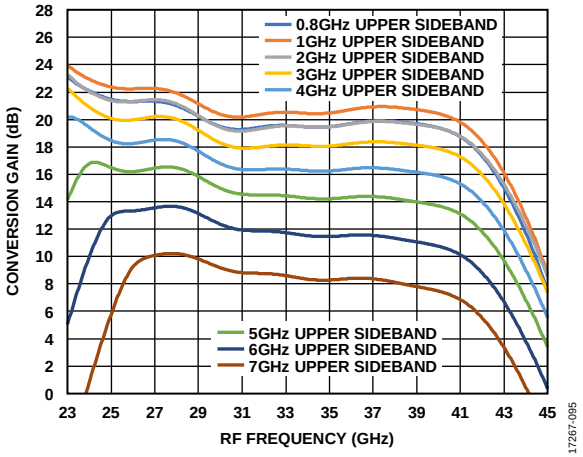

Figure 92. Conversion Gain vs. RF Frequency for Multiple IF Frequency Settings (Upper Sideband)

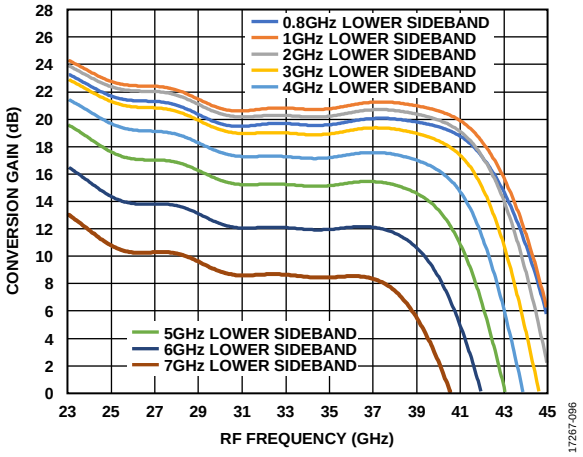

Figure 93. Conversion Gain vs. RF Frequency at Multiple IF Frequency Settings (Lower Sideband)

Figure 94 and Figure 95 show the conversion gain vs. RF frequency in I/Q mode for multiple baseband (BB) frequencies (T_A = 25°C, LO = 0 dBm) for upper sideband and lower sideband, respectively.

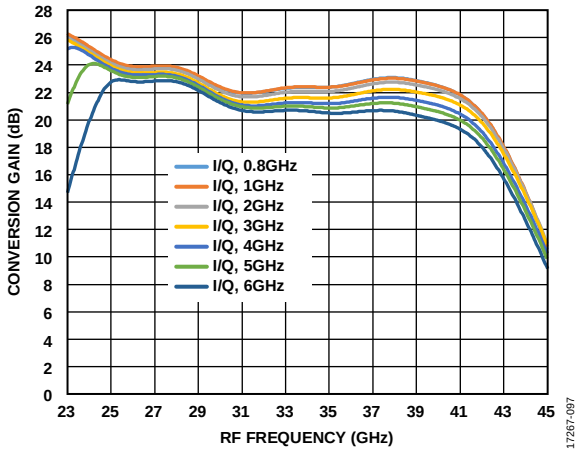

Figure 94. Conversion Gain vs. RF Frequency for Multiple Baseband Frequency Settings (Upper Sideband)

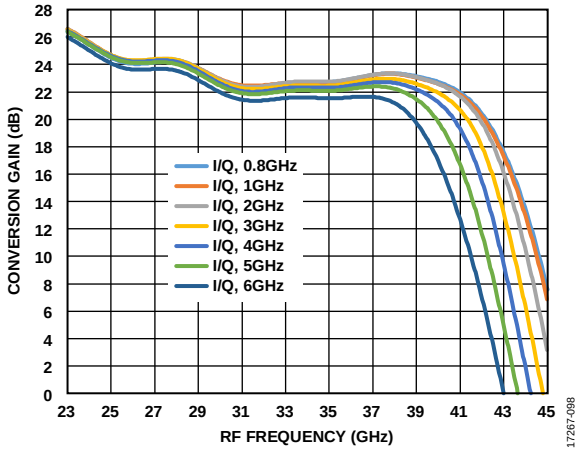

Figure 95. Conversion Gain vs. RF Frequency at Multiple Baseband Frequency Settings (Lower Sideband)

PERFORMANCE ACROSS COMMON-MODE VOLTAGE IN I/Q MODE

Figure 96, Figure 97, and Figure 98 show the performance at various common-mode voltages in I/Q mode. For each common-mode voltage, the mixer gate voltage was changed based on the equation described in the Baseband Quadrature Modulation (I/Q Mode) section.

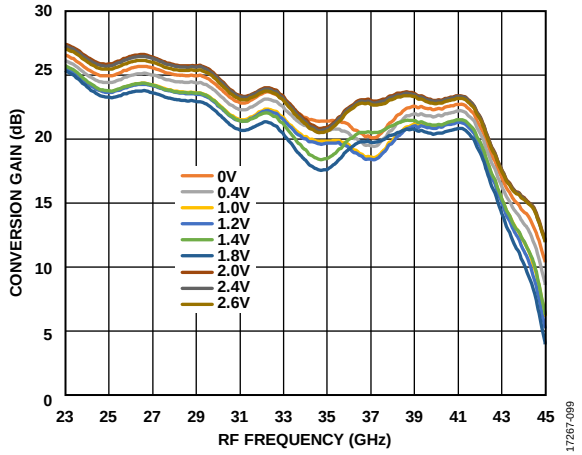

Figure 96. Conversion Gain vs. RF Frequency at Multiple Common-Mode Voltages in I/Q Mode (f_{BB} = 100 MHz, LO = 0 dBm, T_A = 25°C)

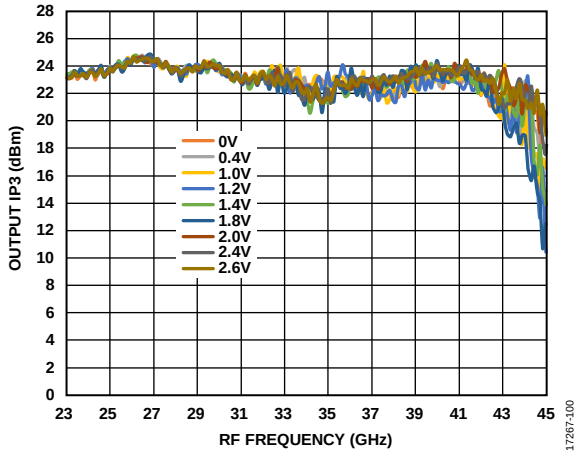

Figure 97. Output IP3 vs. RF Frequency at Multiple Common-Mode Voltages in I/Q Mode (f_{BB} = 100 MHz, LO = 0 dBm, T_A = 25°C)

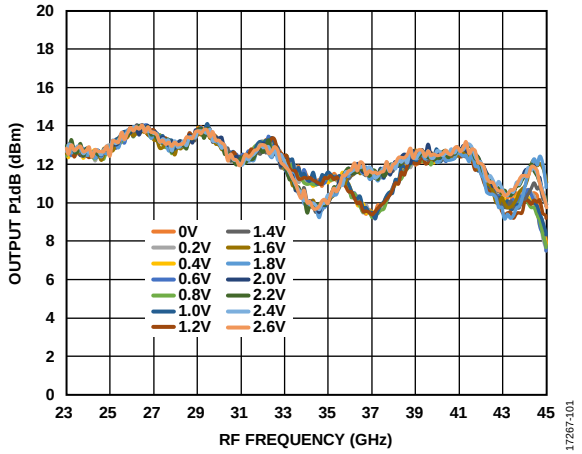

Figure 98. Output P1dB vs. RF Frequency at Multiple Common-Mode Voltages in I/Q Mode (f_{BB} = 100 MHz, LO = 0 dBm, T_A = 25°C)

OPERATING VCTRL1 AND VCTRL2 INDEPENDENTLY

The data shown in the Specifications section and the Typical Performance Characteristics section is based on the VCTRL1 and VCTRL2 voltages being equal. Finer gain regulation can be obtained if VCTRL1 and VCTRL2 are used separately. Operating VCTRL1 and VCTRL2 also allows either maintaining IP3 or noise figure performance while attenuating the RF output.

Figure 99, Figure 102, and Figure 105 show the conversion gain, input IP3, and noise figure vs. the RF frequency, respectively (IF = 2 GHz, upper sideband, LO = 0 dBm at T_A = 25°C), when VCTRL1 is equal to VCTRL2.

Figure 100, Figure 103, and Figure 106 show the conversion gain, input IP3, and noise figure vs. the RF frequency, respectively (IF = 2 GHz, upper sideband, LO = 0 dBm at T_A = 25°C), when VCTRL2 is held at a minimum attenuation and VCTRL1 is changed.

Figure 101, Figure 104, and Figure 107 show the conversion gain, input IP3, and noise figure vs. the RF frequency, respectively (IF = 2 GHz, upper sideband, LO = 0 dBm at T_A = 25°C), when VCTRL1 is held at minimum attenuation and VCTRL2 is changed.

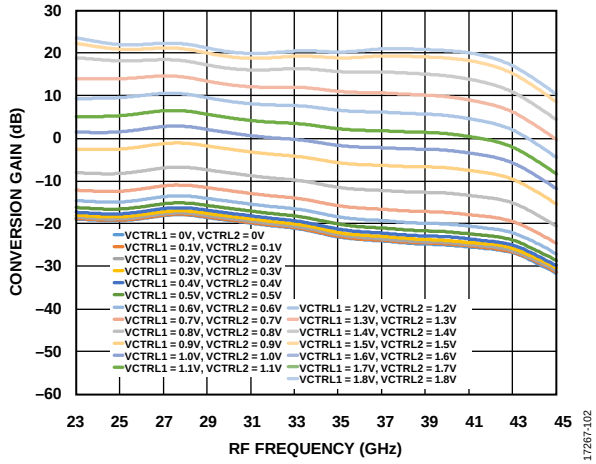

Figure 99. Conversion Gain vs. RF Frequency at Various V_{CTRL} Voltages (VCTRL1 = VCTRL2), IF Mode, IF Frequency = 2 GHz, Upper Sideband

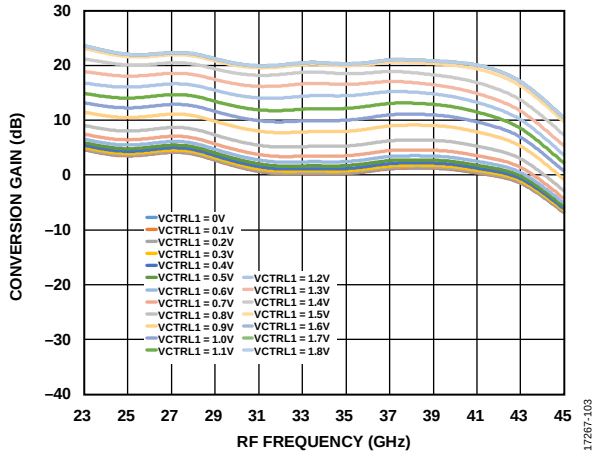

Figure 100. Conversion Gain vs. RF Frequency at Various VCTRL1 Voltages (VCTRL2 = 1.8 V), IF Mode, IF Frequency = 2 GHz, Upper Sideband

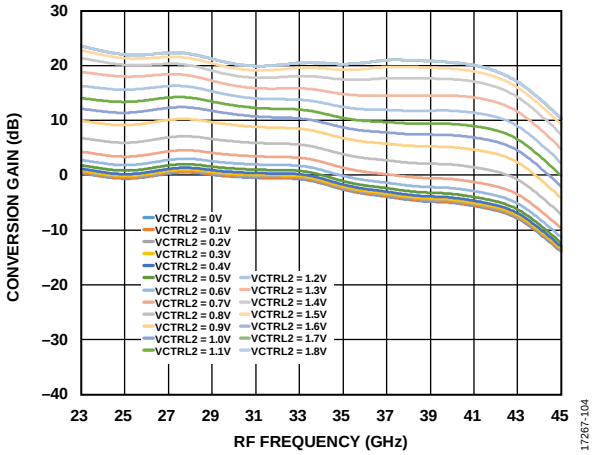

Figure 101. Conversion Gain vs. RF Frequency at Various VCTRL2 Voltages (VCTRL1 = 1.8 V), IF Mode, IF Frequency = 2 GHz, Upper Sideband

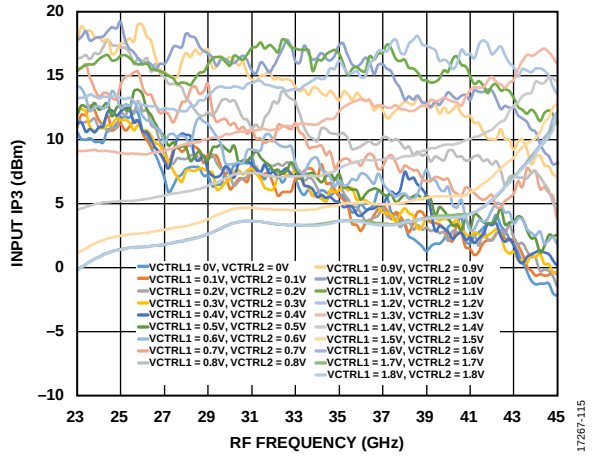

Figure 102. Input IP3 vs. RF Frequency at Various V_{CTRL} Voltages (VCTRL1 = VCTRL2), I IF Mode, IF Frequency = 2 GHz, Upper Sideband

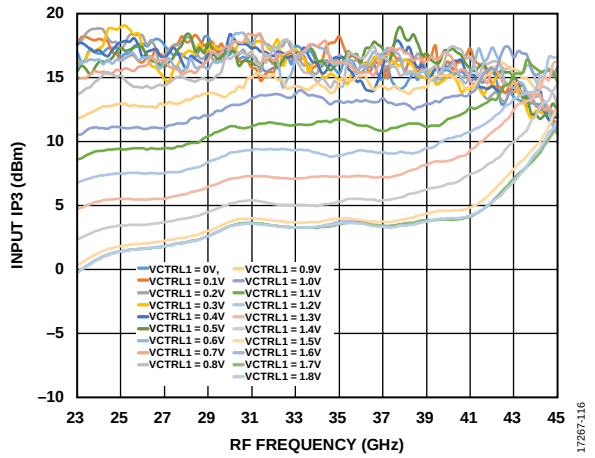

Figure 103. Input IP3 vs. RF Frequency at Various VCTRL1 Voltages (VCTRL2 = 1.8 V), IF Mode, IF Frequency = 2 GHz, Upper Sideband

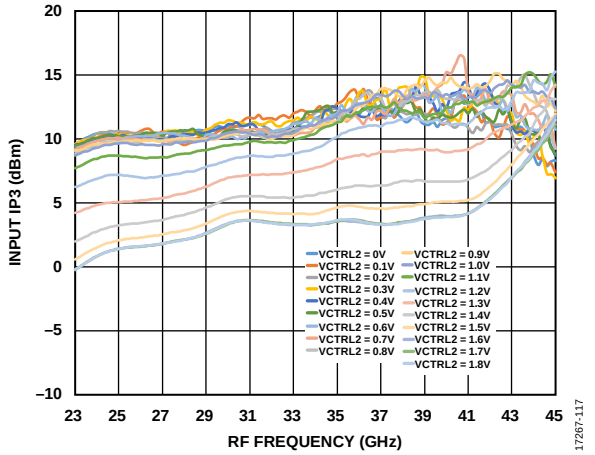

Figure 104. Input IP3 vs. RF Frequency at Various VCTRL2 Voltages (VCTRL1 = 1.8 V), IF Mode, IF Frequency = 2 GHz, Upper Sideband

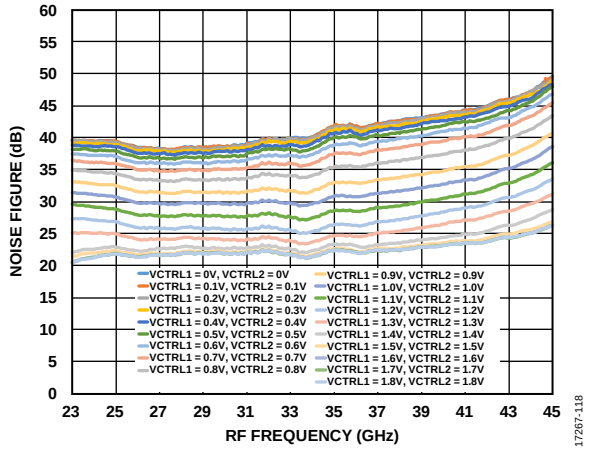

Figure 105. Noise Figure vs. RF Frequency at Various V_{CTRL} Voltages (VCTRL1 = VCTRL2), IF Mode, IF Frequency = 2 GHz, Upper Sideband

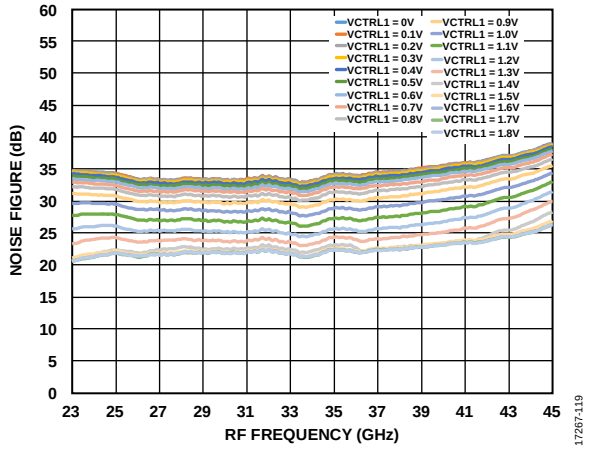

Figure 106. Noise Figure vs. RF Frequency at Various VCTRL1 Voltages (VCTRL2 = 1.8 V), IF Mode, IF Frequency = 2 GHz, Upper Sideband

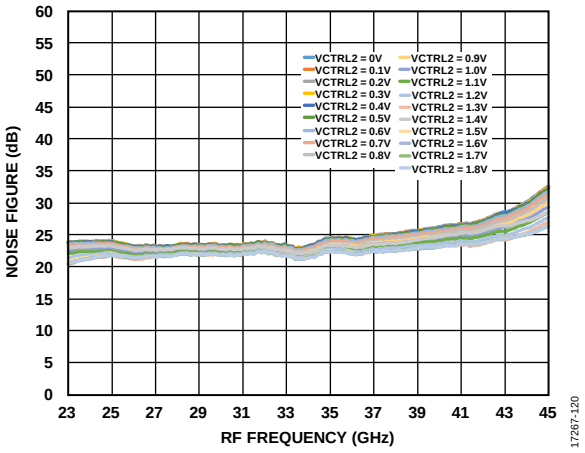

Figure 107. Noise Figure vs. RF Frequency at Various VCTRL2 Voltages (VCTRL1 = 1.8 V), IF Mode, IF Frequency = 2 GHz, Upper Sideband

RECOMMENDED LAND PATTERN

Solder the exposed pad on the underside of the ADMV1013 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package.

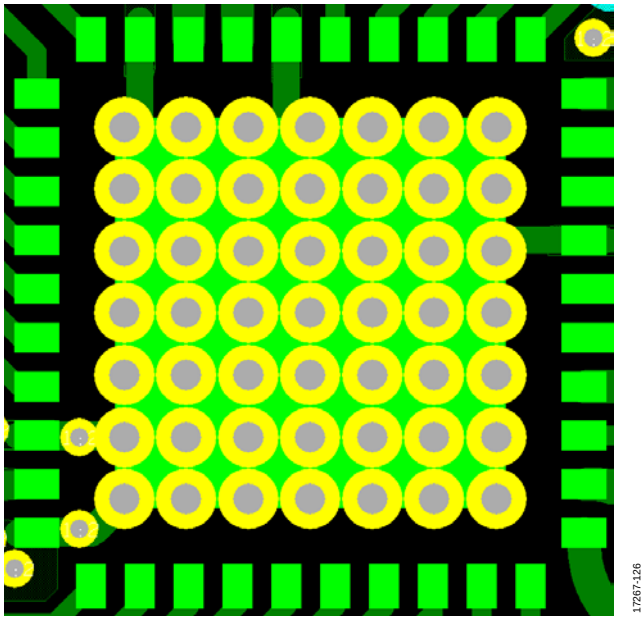

Figure 108. Evaluation Board Layout for the LGA Package

EVALUATION BOARD INFORMATION

For more information about the ADMV1013 evaluation board, refer to the ADMV1013-EVALZ user guide.

REGISTER SUMMARY

Table 6.

Reg. (Hex)	Register Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	R/W
00	SPI_CONTROL	[15:8]	PARITY_EN	SPI_SOFT_RESET	RESERVED		CHIP_ID				0x00A4	R/W
		[7:0]	CHIP_ID				REVISION					
01	ALARM	[15:8]	PARITY_ERROR	TOO_FEW_ERRORS	TOO_MANY_ERRORS	ADDRESS_RANGE_ERROR	RESERVED				0x0000	R
		[7:0]	RESERVED									
02	ALARM_MASKS	[15:8]	PARITY_ERROR_MASK	TOO_FEW_ERRORS_MASK	TOO_MANY_ERRORS_MASK	ADDRESS_RANGE_ERROR_MASK	RESERVED				0xFFFF	R/W
		[7:0]	RESERVED									
03	ENABLE	[15:8]	VGA_PD	MIXER_PD	QUAD_PD			BG_PD	RESERVED		0x01D7	R/W
		[7:0]	MIXER_IF_EN	RESERVED	DET_EN	RESERVED						
05	LO_AMP_I	[15:8]	RESERVED		LOAMP_PH_ADJ_I_FINE						0x5051	R/W
		[7:0]	LOAMP_PH_ADJ_I_FINE	MIXER_VGATE								
06	LO_AMP_Q	[15:8]	RESERVED		LOAMP_PH_ADJ_Q_FINE						0x5000	R/W
		[7:0]	LOAMP_PH_ADJ_Q_FINE	RESERVED								
07	OFFSET_ADJUST_I	[15:8]	MXER_OFF_ADJ_I_P							MXER_OFF_ADJ_I_N	0xFFFC	R/W
		[7:0]	MXER_OFF_ADJ_I_N						RESERVED			
08	OFFSET_ADJUST_Q	[15:8]	MXER_OFF_ADJ_Q_P							MXER_OFF_ADJ_Q_N	0xFFFC	R/W
		[7:0]	MXER_OFF_ADJ_Q_N[5:0]						RESERVED			
09	QUAD	[15:8]	RESERVED						QUAD_SE_MODE		0x5700	R/W
		[7:0]	QUAD_SE_MODE		RESERVED		QUAD_FILTERS					
0A	VVA_TEMPERATURE_COMPENSATION	[15:8]	VVA_TEMPERATURE_COMPENSATION								0x0000	R/W
		[7:0]	VVA_TEMPERATURE_COMPENSATION									

REGISTER DETAILS

Address: 0x00, Reset: 0x00A4, Name: SPI_CONTROL

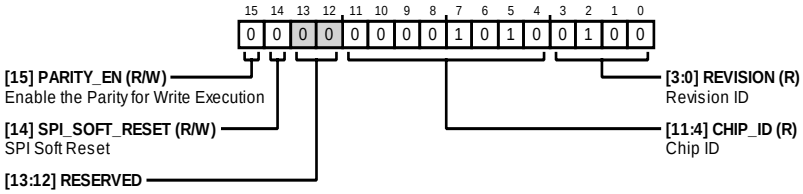

Table 7. Bit Descriptions for SPI_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
15	PARITY_EN		Enable the Parity for Write Execution	0x0	R/W
14	SPI_SOFT_RESET		SPI Soft Reset	0x0	R/W
[13:12]	RESERVED		Reserved	0x0	R
[11:4]	CHIP_ID		Chip ID	0xA	R
[3:0]	REVISION		Revision ID	0x4	R

Address: 0x01, Reset: 0x0000, Name: ALARM

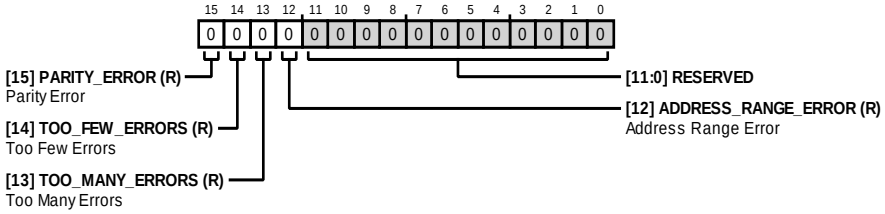

Table 8. Bit Descriptions for ALARM

Bits	Bit Name	Settings	Description	Reset	Access
15	PARITY_ERROR		Parity Error	0x0	R
14	TOO_FEW_ERRORS		Too Few Errors	0x0	R
13	TOO_MANY_ERRORS		Too Many Errors	0x0	R
12	ADDRESS_RANGE_ERRO R		Address Range Error	0x0	R
[11:0]	RESERVED		Reserved	0x0	R

Address: 0x02, Reset: 0xFFFF, Name: ALARM_MASKS

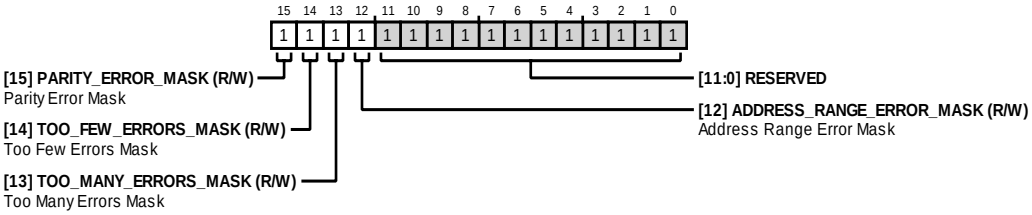

Table 9. Bit Descriptions for ALARM_MASKS

Bits	Bit Name	Settings	Description	Reset	Access
15	PARITY_ERROR_MASK		Parity Error Mask	0x1	R/W
14	TOO_FEW_ERRORS_MASK		Too Few Errors Mask	0x1	R/W
13	TOO_MANY_ERRORS_MASK		Too Many Errors Mask	0x1	R/W
12	ADDRESS_RANGE_ERROR_MASK		Address Range Error Mask	0x1	R/W
[11:0]	RESERVED		Reserved	0xFFF	R

Address: 0x03, Reset: 0x01D7, Name: ENABLE

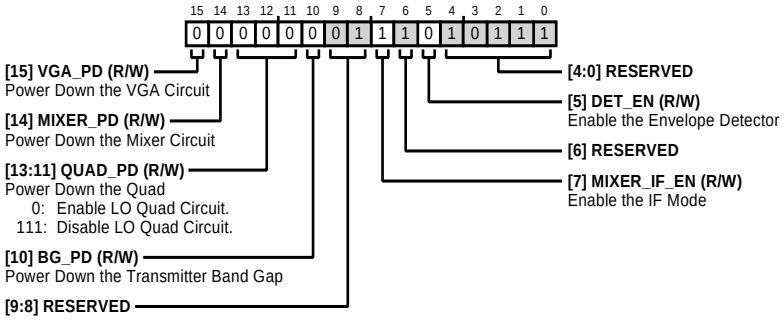

Table 10. Bit Descriptions for ENABLE

Bits	Bit Name	Settings	Description	Reset	Access
15	VGA_PD		Power Down the VGA Circuit	0x0	R/W
14	MIXER_PD		Power Down the Mixer Circuit	0x0	R/W
[13:11]	QUAD_PD		Power Down the Quad	0x0	R/W
		000	Enable LO Quad Circuit		
		111	Disable LO Quad Circuit		
10	BG_PD		Power Down the Transmitter Band Gap	0x0	R/W
[9:8]	RESERVED		Reserved	0x0	R
7	MIXER_IF_EN		Enable the IF Mode	0x1	R/W
6	RESERVED		Reserved	0x1	R
5	DET_EN		Enable the Envelope Detector	0x0	R/W
[4:0]	RESERVED		Reserved	0x17	R

Address: 0x05, Reset: 0x5051, Name: LO_AMP_I

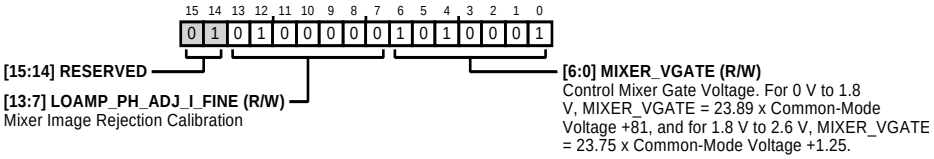

Table 11. Bit Descriptions for LO_AMP_I

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	RESERVED		Reserved.	0x1	R
[13:7]	LOAMP_PH_ADJ_I_FINE		Mixer Image Rejection Calibration.	0x20	R/W
[6:0]	MIXER_VGATE		Control Mixer Gate Voltage. For 0 V to 1.8 V, MIXER_VGATE = 23.89 × Common-Mode Voltage + 81, and for 1.8 V to 2.6 V, MIXER_VGATE = 23.75 × Common-Mode Voltage + 1.25.	0x51	R/W

Address: 0x06, Reset: 0x5000, Name: LO_AMP_Q

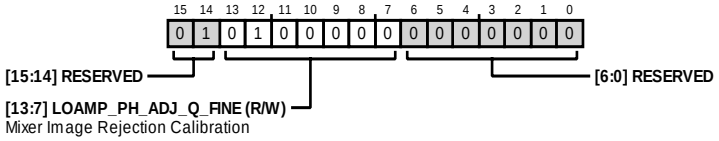

Table 12. Bit Descriptions for LO_AMP_Q

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	RESERVED		Reserved	0x1	R
[13:7]	LOAMP_PH_ADJ_Q_FINE		Mixer Image Rejection Calibration	0x20	R/W
[6:0]	RESERVED		Reserved	0x0	R

Address: 0x07, Reset: 0xFFFC, Name: OFFSET_ADJUST_I

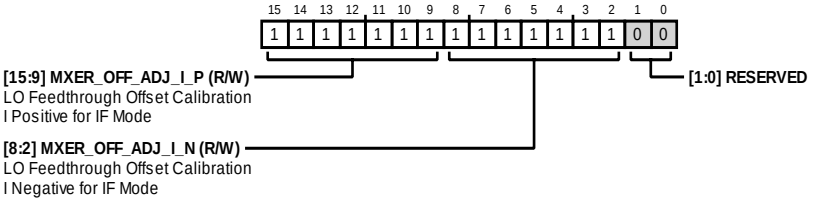

Table 13. Bit Descriptions for OFFSET_ADJUST_I

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	MXER_OFF_ADJ_I_P		LO Feedthrough Offset Calibration I Positive for IF Mode	0x7F	R/W
[8:2]	MXER_OFF_ADJ_I_N		LO Feedthrough Offset Calibration I Negative for IF Mode	0x7F	R/W
[1:0]	RESERVED		Reserved	0x0	R

Address: 0x08, Reset: 0xFFFC, Name: OFFSET_ADJUST_Q

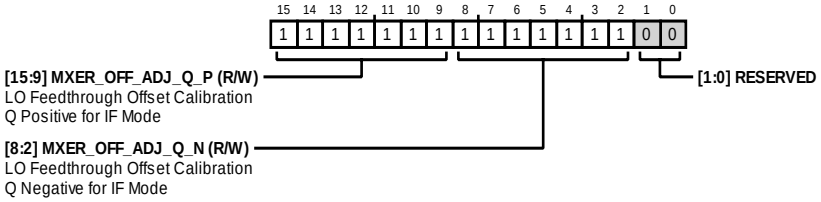

Table 14. Bit Descriptions for OFFSET_ADJUST_Q

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	MXER_OFF_ADJ_Q_P		LO Feedthrough Offset Calibration Q Positive for IF Mode	0x7F	R/W
[8:2]	MXER_OFF_ADJ_Q_N		LO Feedthrough Offset Calibration Q Negative for IF Mode	0x7F	R/W
[1:0]	RESERVED		Reserved	0x0	R

Address: 0x09, Reset: 0x5700, Name: QUAD

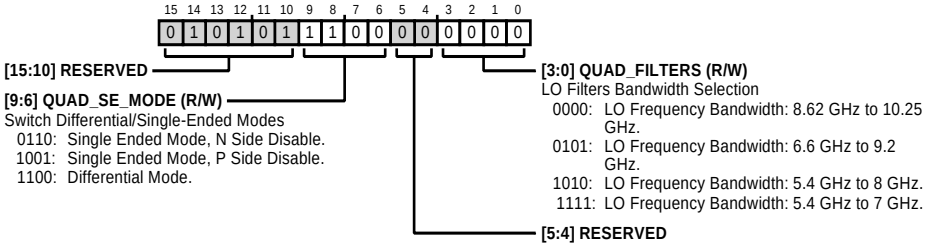

Table 15. Bit Descriptions for QUAD

Bits	Bit Name	Settings	Description	Reset	Access
[15:10]	RESERVED		Reserved.	0x15	R
[9:6]	QUAD_SE_MODE		Switch Differential/Single-Ended Modes.	0xC	R/W
		0110	Single-Ended Mode, Negative Side Disable.		
		1001	Single-Ended Mode, Positive Side Disable.		
		1100	Differential Mode.		
[5:4]	RESERVED		Reserved.	0x0	R
[3:0]	QUAD_FILTERS		LO Filters Bandwidth Selection.	0x0	R/W
		0000	LO Frequency Bandwidth: 8.62 GHz to 10.25 GHz.		
		0101	LO Frequency Bandwidth: 6.6 GHz to 9.2 GHz.		
		1010	LO Frequency Bandwidth: 5.4 GHz to 8 GHz.		
		1111	LO Frequency Bandwidth: 5.4 GHz to 7 GHz.		

Address: 0x0A, Reset: 0x0000, Name: VVA_TEMPERATURE_COMPENSATION

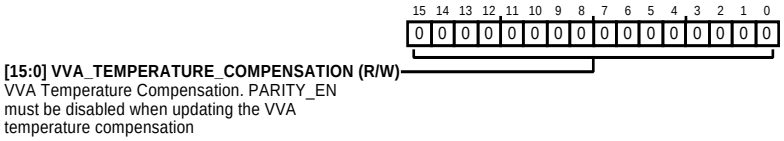

Table 16. Bit Descriptions for VVA_TEMPERATURE_COMPENSATION

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	VVA_TEMPERATURE_COMPENSATION		VVA Temperature Compensation. PARITY_EN must be disabled when updating the VVA temperature compensation. Set to 0xE700 on startup.	0x0	R/W

OUTLINE DIMENSIONS

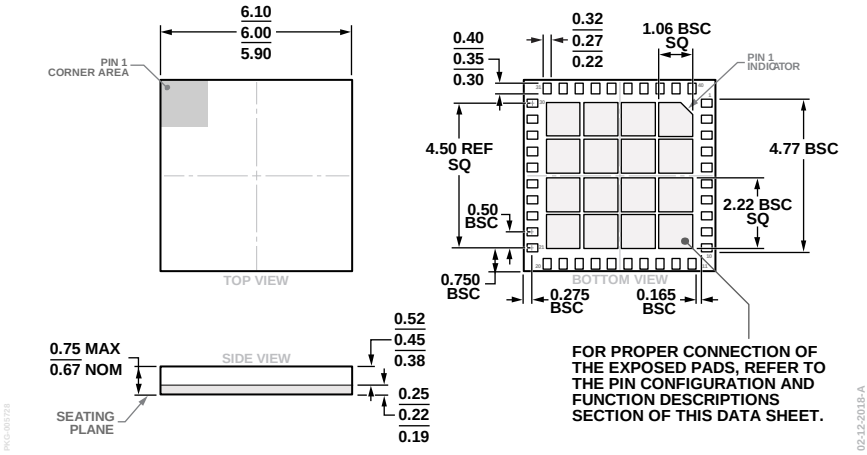

Figure 109. 40-Terminal Land Grid Array Package [LGA]
6 mm × 6 mm Body and 0.67 mm Package Height
(CC-40-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADMV1013ACCZ	−40°C to +85°C	40-Terminal Land Grid Array Package [LGA]	CC-40-5
ADMV1013ACCZ-R7	−40°C to +85°C	40-Terminal Land Grid Array Package [LGA]	CC-40-5
ADMV1013-EVALZ		Evaluation Board	

[1] Z = RoHS-Compliant Part.