50 MHz to 4 GHz TruPwr™ Detector

ADL5501

FEATURES

True rms response
Excellent temperature stability
Up to 30 dB input dynamic range at 4 GHz
50 Ω input impedance
1.25 V rms, 15 dBm, maximum input
Single-supply operation: 2.7 V to 5.5 V
Low power: 3.3 mW at 3 V supply
RoHS-compliant

APPLICATIONS

Measurement of CDMA2000-, W-CDMA-, and QPSK-/QAM-based OFDM, and other complex modulation waveforms
RF transmitter or receiver power measurement

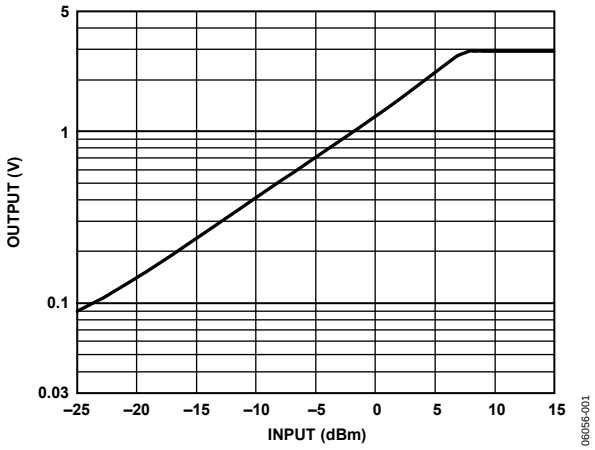

Figure 1. Output vs. Input Level, Supply 3 V, Frequency 1.9 GHz

GENERAL DESCRIPTION

The ADL5501 is a mean-responding power detector for use in high frequency receiver and transmitter signal chains from 50 MHz to 4 GHz. It is easy to apply, requiring only a single supply between 2.7 V and 5.5 V and a power supply decoupling capacitor. The input is internally ac-coupled and has a nominal input impedance of 50 Ω. The output is a linear-responding dc voltage with a conversion gain of 6.3 V/V rms at 900 MHz.

The ADL5501 is intended for true power measurement of simple and complex waveforms. The device is particularly useful for measuring high crest factor (high peak-to-rms ratio) signals, such as CDMA-, CDMA2000-, W-CDMA-, and QPSK-/QAM-based OFDM waveforms. The on-chip modulation filter provides adequate averaging for most waveforms.

The on-chip, 100 Ω series resistance at the output, combined with an external shunt capacitor, creates a low-pass filter response that reduces the residual ripple in the dc output voltage. For more complex waveforms, an external capacitor at the FLTR pin can be used for supplementary signal demodulation.

The ADL5501 offers excellent temperature stability across a 30 dB range and near 0 dB measurement error across temperature over the top portion of the dynamic range. In addition to its temperature stability, the ADL5501 offers low process variations that further reduce calibration complexity.

The ADL5501 operates from −40°C to +85°C and is available in a small 6-lead SC-70 package. It is fabricated on a proprietary high f_T silicon bipolar process.

FUNCTIONAL BLOCK DIAGRAM

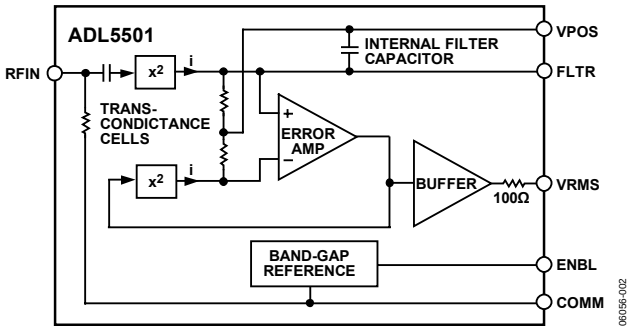

Figure 2.

Rev. 0

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REVISION HISTORY

9/06—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 3.0 V, C_{FLTR} = Open, C_{OUT} = 100 nF, unless otherwise specified.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
FREQUENCY RANGE	Input RFIN	50		4000	MHz
RMS CONVERSION (f = 50 MHz)	Input RFIN to Output VRMS				
Input Impedance			88||6.5		Ω||pF
Input Return Loss			11.0		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±1 dB Error[2]	V_S = 3 V		25		dB
	V_S = 5 V		26		dB
±2 dB Error[2]	V_S = 3 V		32		dB
	V_S = 5 V		35		dB
Maximum Input Level	±1 dB error[2]		+8		dBm
Minimum Input Level	±1 dB error[2]		−18		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		4.5		V/V rms
Output Intercept[3]			0.03		V
Output Voltage—High Power In	P_{IN} = 5 dBm, 400 mV rms		1.81		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, +20 mV rms		0.11		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0039		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0037		dB/°C
RMS CONVERSION (f = 100 MHz)	Input RFIN to Output VRMS				
Input Impedance			79||3.6		Ω||pF
Input Return Loss			12.4		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[4]	Delta from 25°C, V_S = 5 V		28		dB
±0.25 dB Error[2]	V_S = 3 V		19		dB
	V_S = 5 V		20		dB
±1 dB Error[2]	V_S = 3 V		23		dB
	V_S = 5 V		27		dB
±2 dB Error[2]	V_S = 3 V		26		dB
	V_S = 5 V		30		dB
Maximum Input Level	±1 dB error[2]		+6		dBm
Minimum Input Level	±1 dB error[2]		−18		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		6.1		V/V rms
	V_S = 5 V	5.6		7.8	V/V rms
Output Intercept[3]			0.03		V
	V_S = 5 V	−0.02		+0.1	V
Output Voltage—High Power In	P_{IN} = 5 dBm, 400 mV rms		2.47		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, +20 mV rms		0.13		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0028		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0018		dB/°C

Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 450 MHz)	Input RFIN to Output VRMS				
Input Impedance			65||1.4		Ω||pF
Input Return Loss			15.5		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[4]	Delta from 25°C, V_S = 5 V		32		dB
±0.25 dB Error[2]	V_S = 3 V		20		dB
	V_S = 5 V		24		dB
±1 dB Error[2]	V_S = 3 V		25		dB
	V_S = 5 V		29		dB
±2 dB Error[2]	V_S = 3 V		28		dB
	V_S = 5 V		33		dB
Maximum Input Level	±1 dB error[2]		+5		dBm
Minimum Input Level	±1 dB error[2]		−20		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		7.1		V/V rms
Output Intercept[3]			0.03		V
Output Voltage—High Power In	P_{IN} = 5 dBm, 400 mV rms		2.81		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, +20 mV rms		0.15		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0016		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0002		dB/°C
RMS CONVERSION (f = 900 MHz)	Input RFIN to Output VRMS				
Input Impedance			55||0.9		Ω||pF
Input Return Loss			17		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[4]	Delta from 25°C, V_S = 5 V		33		dB
±0.25 dB Error[2]	V_S = 3 V		20		dB
	V_S = 5 V		23		dB
±1 dB Error[2]	V_S = 3 V		24		dB
	V_S = 5 V		27		dB
±2 dB Error[2]	V_S = 3 V		27		dB
	V_S = 5 V		30		dB
Maximum Input Level	±1 dB error[2]		+6		dBm
Minimum Input Level	±1 dB error[2]		−18		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		6.3		V/V rms
Output Intercept[3]			0.03		V
Output Voltage—High Power In	P_{IN} = 5 dBm, 400 mV rms		2.53		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, +20 mV rms		0.14		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ +85°C		0.0019		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0002		dB/°C

Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 1900 MHz)	Input RFIN to Output VRMS				
Input Impedance			36||0.4		Ω||pF
Input Return Loss			14.5		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[4]	Delta from 25°C, V_S = 5 V		32		dB
±0.25 dB Error[2]	V_S = 3 V		5		dB
	V_S = 5 V		7		dB
±1 dB Error[2]	V_S = 3 V		25		dB
	V_S = 5 V		29		dB
±2 dB Error[2]	V_S = 3 V		28		dB
	V_S = 5 V		32		dB
Maximum Input Level	±1 dB error[2]		+7		dBm
Minimum Input Level	±1 dB error[2]		−19		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		5.5		V/V rms
Output Intercept[3]			0.02		V
Output Voltage—High Power In	P_{IN} = 5 dBm, 400 mV rms		2.20		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, +20 mV rms		0.12		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0031		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0034		dB/°C
RMS CONVERSION (f = 2350 MHz)	Input RFIN to Output VRMS				
Input Impedance			32||0.3		Ω||pF
Input Return Loss			13.5		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[4]	Delta from 25°C, V_S = 5 V		8		dB
±0.25 dB Error[2]	V_S = 3 V		4		dB
	V_S = 5 V		7		dB
±1 dB Error[2]	V_S = 3 V		25		dB
	V_S = 5 V		29		dB
±2 dB Error[2]	V_S = 3 V		29		dB
	V_S = 5 V		32		dB
Maximum Input Level	±1 dB error[2]		+8		dBm
Minimum Input Level	±1 dB error[2]		−18		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		5.0		V/V rms
Output Intercept[3]			0.02		V
Output Voltage—High Power In	P_{IN} = 5 dBm, 400 mV rms		2.00		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, +20 mV rms		0.10		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0032		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0044		dB/°C

Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 2700 MHz)	Input RFIN to Output VRMS				
Input Impedance			31||−0.1		Ω||pF
Input Return Loss			12.5		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[4]	Delta from 25°C, V_S = 5 V		5		dB
±0.25 dB Error[2]	V_S = 3 V		3		dB
	V_S = 5 V		7		dB
±1 dB Error[2]	V_S = 3 V		25		dB
	V_S = 5 V		30		dB
±2 dB Error[2]	V_S = 3 V		28		dB
	V_S = 5 V		33		dB
Maximum Input Level	±1 dB error[2]		+8		dBm
Minimum Input Level	±1 dB error[2]		−17		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		4.6		V/V rms
Output Intercept[3]			0.02		V
Output Voltage—High Power In	P_{IN} = 5 dBm, 400 mV rms		1.84		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, +20 mV rms		0.09		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0034		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0049		dB/°C
RMS CONVERSION (f = 4000 MHz)	Input RFIN to Output VRMS				
Input Impedance			36||−0.4		Ω||pF
Input Return Loss			11.8		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[4]	Delta from 25°C, V_S = 5 V		5		dB
±0.25 dB Error[2]	V_S = 3 V		4		dB
	V_S = 5 V		5		dB
±1 dB Error[2]	V_S = 3 V		28		dB
	V_S = 5 V		31		dB
±2 dB Error[2]	V_S = 3 V		30		dB
	V_S = 5 V		33		dB
Maximum Input Level	±1 dB error[2]		+10		dBm
Minimum Input Level	±1 dB error[2]		−18		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		3.8		V/V rms
Output Intercept[3]			0.01		V
Output Voltage—High Power In	P_{IN} = 5 dBm, 400 mV rms		1.53		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, +20 mV rms		0.07		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0019		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0043		dB/°C
OUTPUT OFFSET	No signal at RFIN		50	150	mV
ENABLE INTERFACE	Pin ENBL				
Logic Level to Enable Power, HI Condition	2.7 V ≤ V_S ≤ 5.5 V, −40°C < T_A < +85°C	1.8		V_{POS}	V
Input Current when HI	2.7 V at ENBL, −40°C ≤ T_A ≤ +85°C		0.05	0.1	µA
Logic Level to Disable Power, LO Condition	2.7 V ≤ V_S ≤ 5.5 V, −40°C < T_A < +85°C	−0.5		+0.5	V
Power-Up Response Time[5]	C_{FLTR} = C_{OUT} = Open, 0 dBm at RFIN		6		µs
	C_{FLTR} = 1 nF, C_{OUT} = Open, 0 dBm at RFIN		21		µs
	C_{FLTR} = Open, C_{OUT} = 100 nF, 0 dBm at RFIN		28		µs

Parameter	Condition	Min	Typ	Max	Unit
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	2.7		5.5	V
Quiescent Current	No signal at RFIN[6]		1.1		mA
Total Supply Current When Disabled	No signal at RFIN, ENBL Input LO		0.1	<10	µA

[1] The available output swing, and hence, the dynamic range, is altered by the supply voltage; see Figure 8.
[2] Error referred to best-fit line at 25°C.
[3] Calculated using linear regression.
[4] Error referred to delta from 25°C response; see Figure 13, Figure 14, Figure 15, Figure 19, Figure 20, and Figure 21.
[5] The response time is measured from 10% to 90% of settling level; see Figure 30.
[6] Supply current is input-level dependent; see Figure 6.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage V_S	5.5 V
VRMS	0 V, V_S
RFIN	1.25 V rms
Equivalent Power, re 50 Ω	15 dBm
Internal Power Dissipation	80 mW
θ_{JA} (SC-70)	494°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

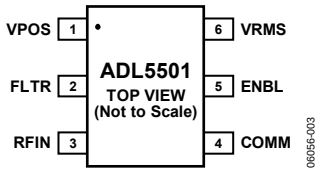


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPOS	Supply Voltage Pin. Operational range 2.7 V to 5.5 V.
2	FLTR	Square-Domain Filter Pin. Connection for an external capacitor to lower the corner frequency of the square-domain (or modulation) filter. Capacitor is connected between FLTR and V_S and forms a low-pass filter with an 8 kΩ on-chip resistor. The on-chip capacitor provides filtering with an approximate 100 kHz corner frequency. For simple waveforms, no further filtering of the demodulated signal is required.
3	RFIN	Signal Input Pin. Internally ac-coupled after internal termination resistance. Nominal 50 Ω input impedance.
4	COMM	Device Ground Pin.
5	ENBL	Enable Pin. Connect pin to V_S for normal operation. Connect pin to ground for disable mode for a supply current less than 1 μA.
6	VRMS	Output Pin. Rail-to-rail voltage output with limited 3 mA current drive capability. The output has an internal 100 Ω series resistance. High resistive loads are recommended to preserve output swing.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5.0 V, C_{FLTR} = open, C_{OUT} = 100 nF, Colors: black = +25°C, blue = −40°C, red = +85°C, unless otherwise noted.

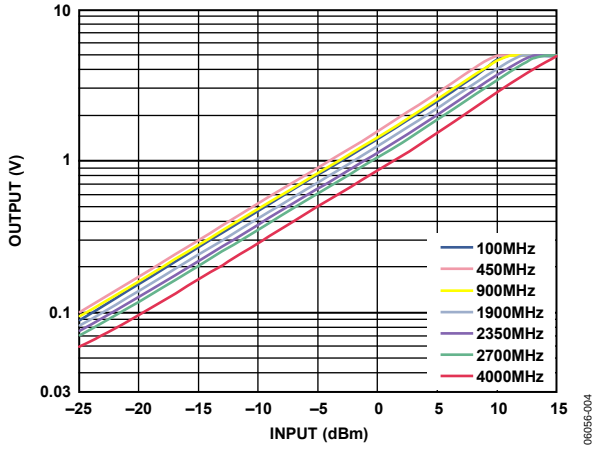


Figure 4. Output vs. Input Level; Frequencies100 MHz, 450 MHz, 900 MHz,1900 MHz, 2350 MHz, 2700 MHz, and 4000 MHz; Supply 5.0 V

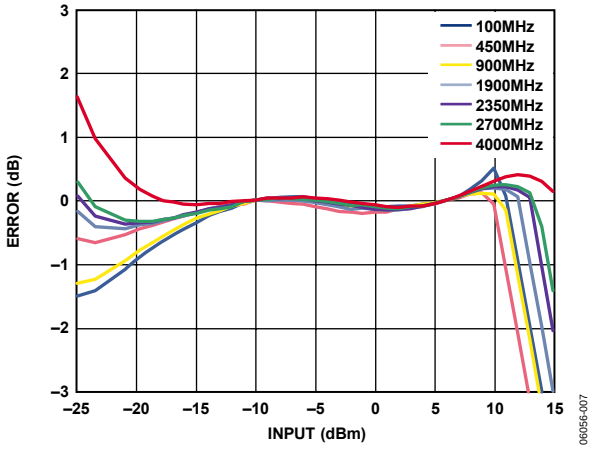


Figure 7. Linearity Error vs. Input Level; Frequencies 100 MHz, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, and 4000 MHz; Supply 5.0 V

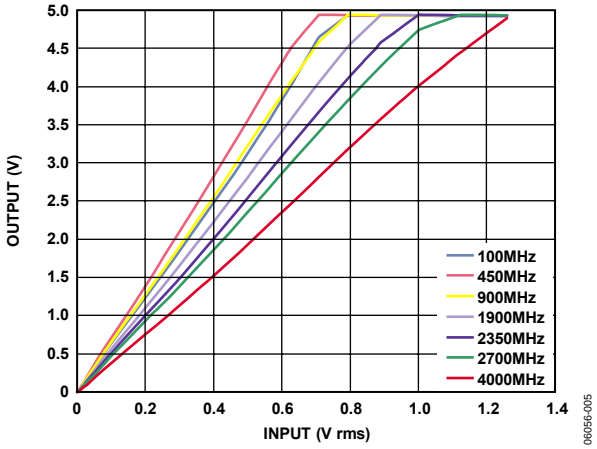


Figure 5. Output vs. Input Level (Linear Scale); Frequencies 100 MHz, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, and 4000 MHz; Supply 5.0 V

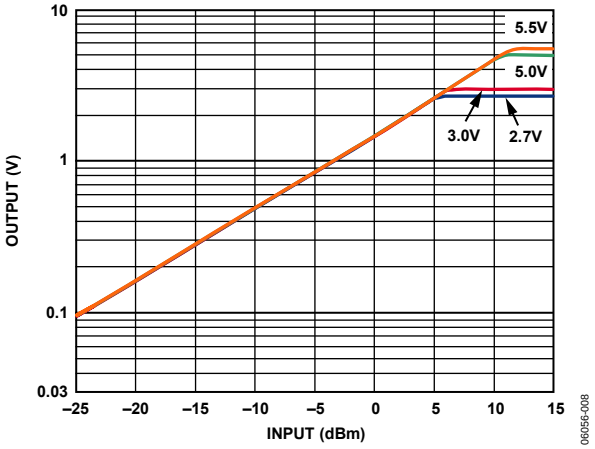


Figure 8. Output vs. Input Level; Supply 2.7 V, 3.0 V, 5.0 V, and 5.5 V; Frequency 900 MHz

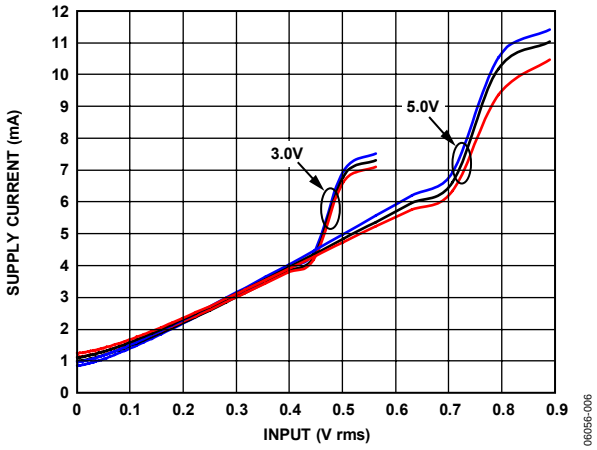


Figure 6. Supply Current vs. Input Level; Supplies 3.0 V and 5.0 V; Temperatures −40°C, +25°C, and +85°C

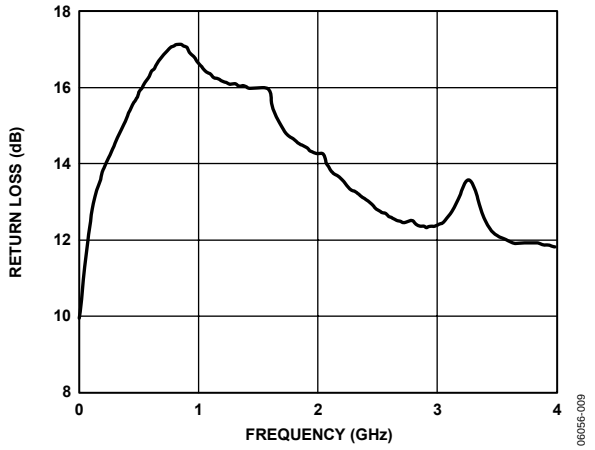


Figure 9. Return Loss vs. Frequency

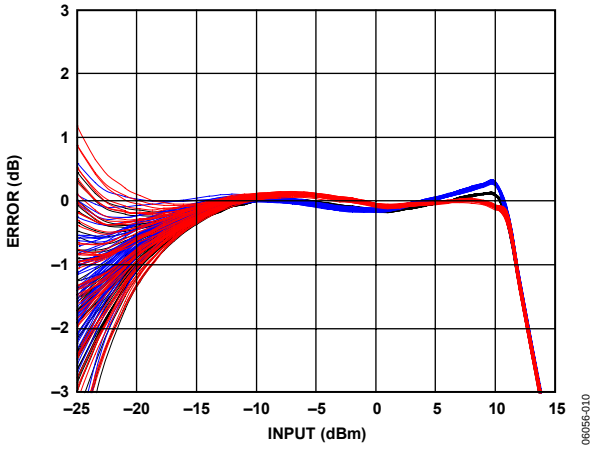


Figure 10. Temperature Drift Distributions for 50 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference; Frequency 900 MHz; Supply 5.0 V

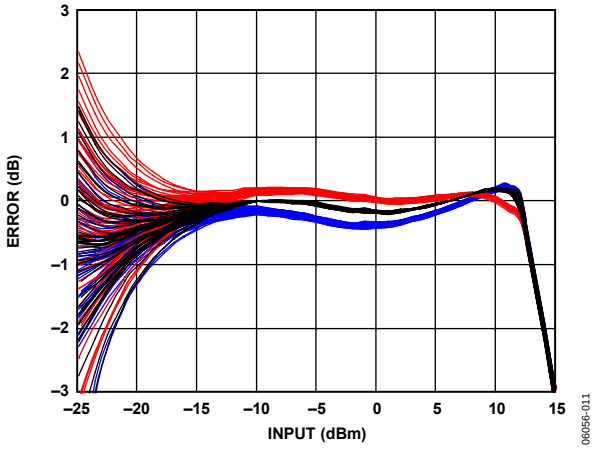


Figure 11. Temperature Drift Distributions for 50 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference; Frequency 1900 MHz; Supply 5.0 V

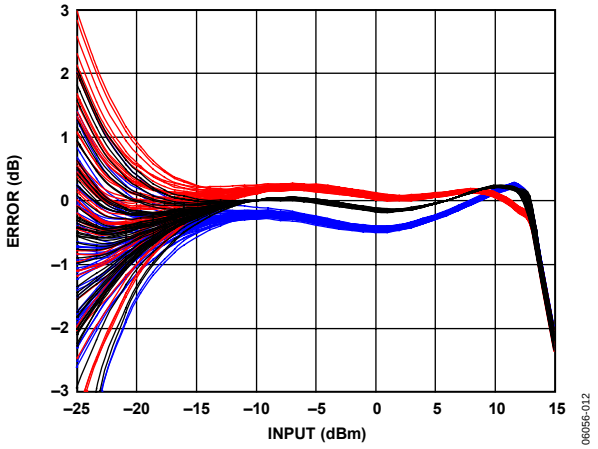


Figure 12. Temperature Drift Distributions for 50 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference; Frequency 2350 MHz; Supply 5.0 V

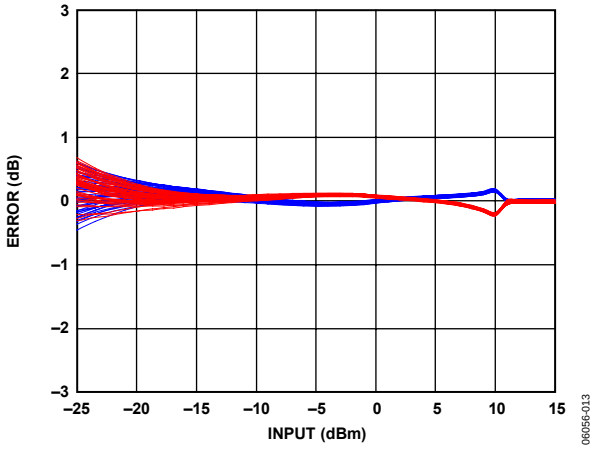


Figure 13. Output Delta from 25°C Output Voltage for 50 Devices at −40°C and +85°C, Frequency 900 MHz, Supply 5.0 V

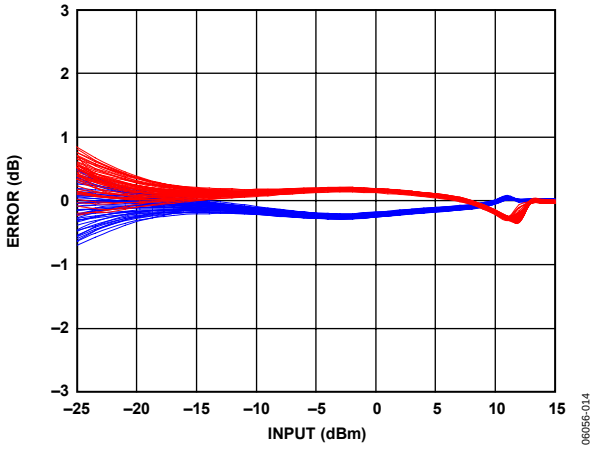


Figure 14. Output Delta from 25°C Output Voltage for 50 Devices at −40°C and +85°C, Frequency 1900 MHz, Supply 5.0 V

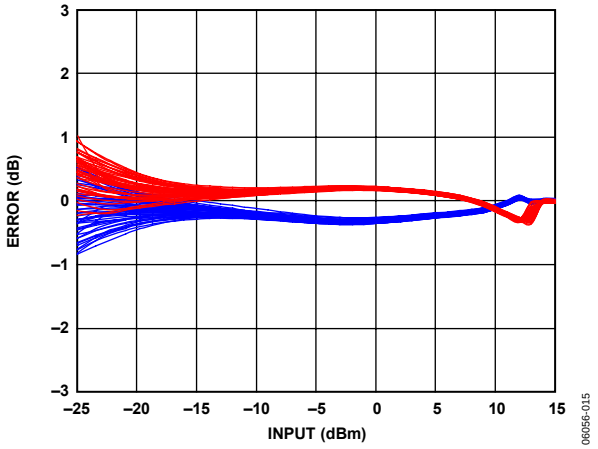


Figure 15. Output Delta from 25°C Output Voltage for 50 Devices at −40°C and +85°C, Frequency 2350 MHz, Supply 5.0 V

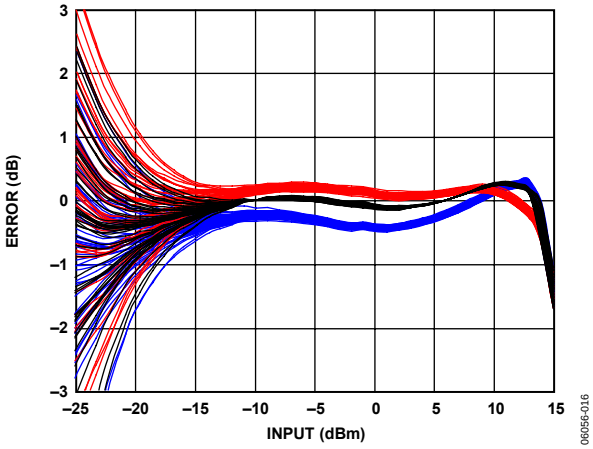


Figure 16. Temperature Drift Distributions for 50 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference; Frequency 2700 MHz; Supply 5.0 V

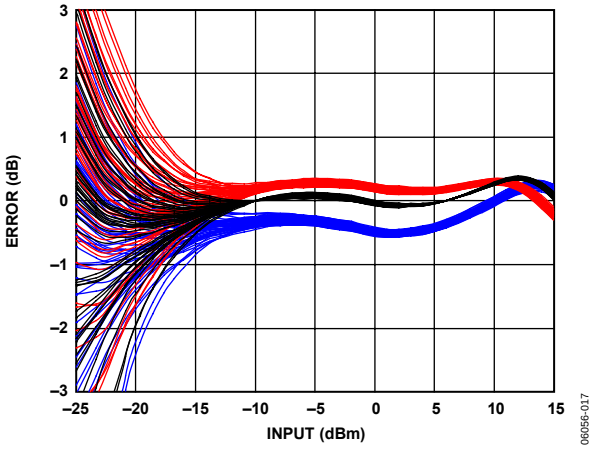


Figure 17. Temperature Drift Distributions for 50 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference; Frequency 3500 MHz; Supply 5.0 V

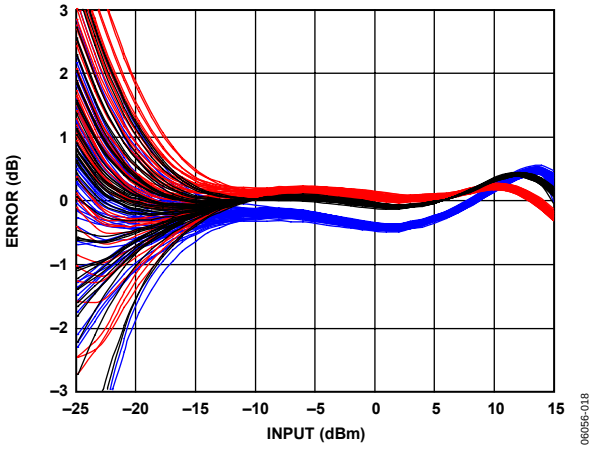


Figure 18. Temperature Drift Distributions for 50 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference; Frequency 4000 MHz; Supply 5.0 V

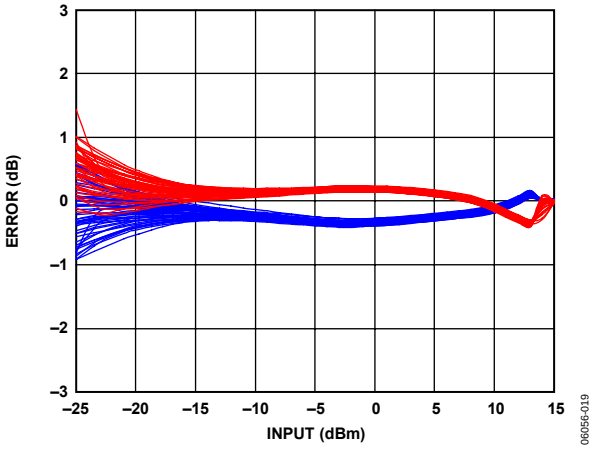


Figure 19. Output Delta from 25°C Output Voltage for 50 Devices at −40°C and +85°C, Frequency 2700 MHz, Supply 5.0 V

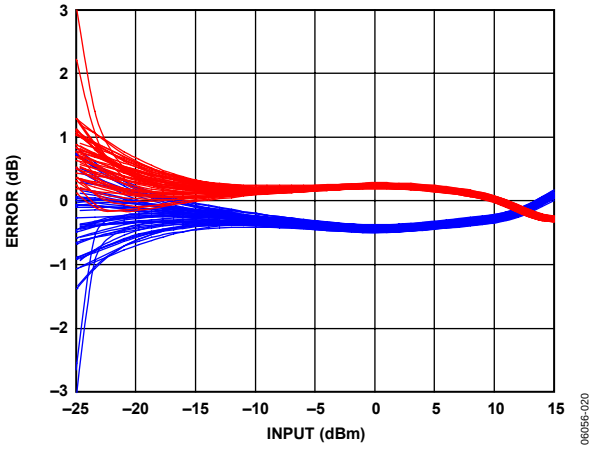


Figure 20. Output Delta from 25°C Output Voltage for 50 Devices at −40°C and +85°C, Frequency 3500 MHz, Supply 5.0 V

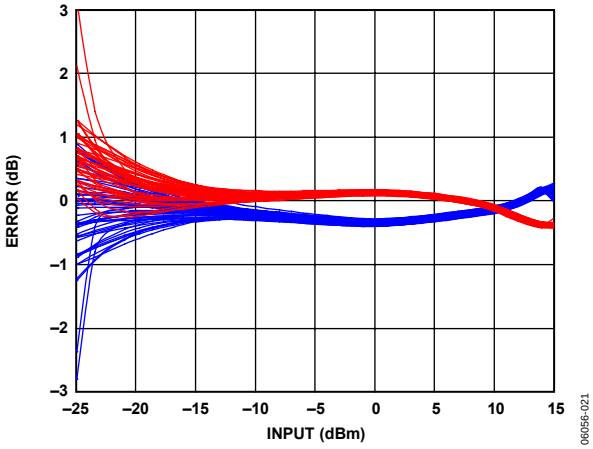


Figure 21. Output Delta from 25°C Output Voltage for 50 Devices at −40°C and +85°C, Frequency 4000 MHz, Supply 5.0 V

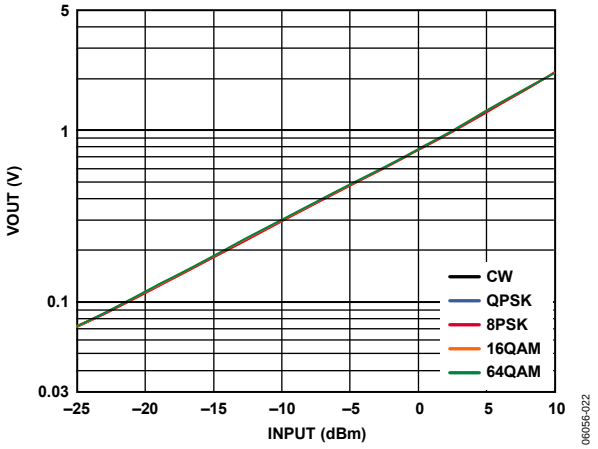


Figure 22. Output vs. Input Level with Different Waveforms, 10 MHz Signal BW for All Modulated Signals, Supply 5.0 V, Frequency 1900 MHz

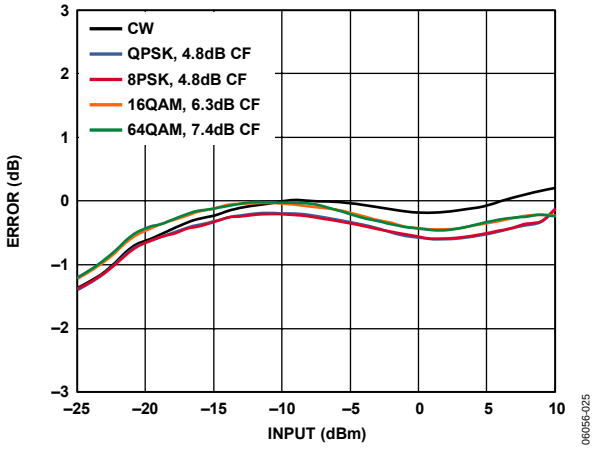


Figure 25. Error from CW Linear Reference vs. Input with Different Waveforms, 10 MHz Signal BW for All Modulated Signals, Supply 5.0 V, Frequency 1900 MHz

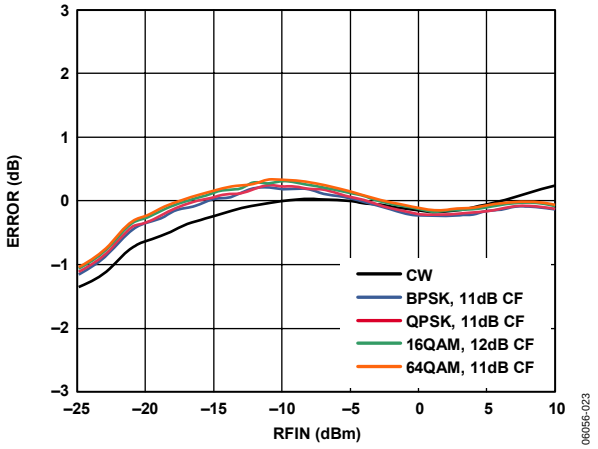


Figure 23. Error from CW Linear Reference vs. Input Level for Various 802.16 OFDM Waveforms at 2.35 GHz, 10 MHz Signal BW, and 256 Subcarriers for All Modulated Signals, Supply 5.0 V

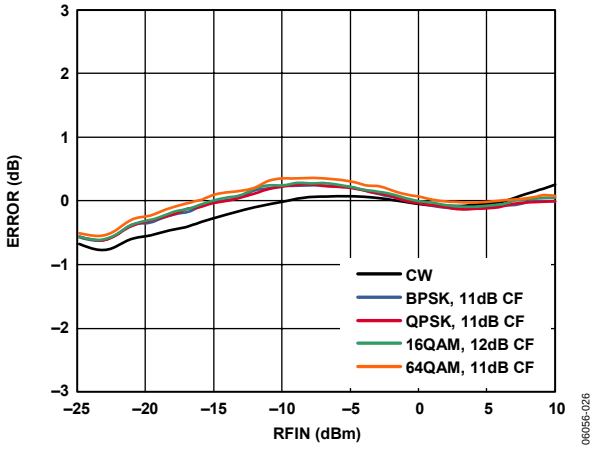


Figure 26. Error from CW Linear Reference vs. Input Level for Various 802.16 OFDM Waveforms at 3.5 GHz, 10 MHz Signal BW, and 256 Subcarriers for All Modulated Signals, Supply 5.0 V

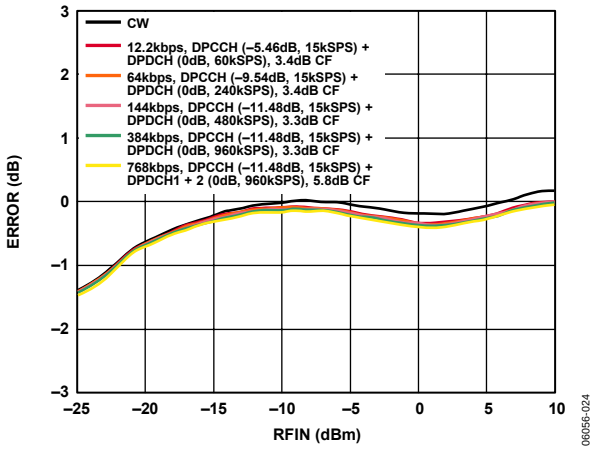


Figure 24. Error from CW Linear Reference vs. Input with Various W-CDMA Up Link Waveforms at 1900 MHz, C_{FLTR} = Open, C_{OUT} = 100 nF

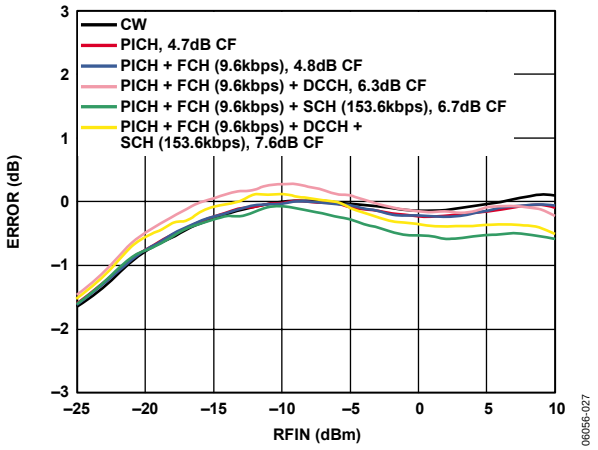


Figure 27. Error from CW Linear Reference vs. Input with Various CDMA2000 Reverse Link Waveforms at 900 MHz, C_{FLTR} = 1 nF, C_{OUT} = 100 nF

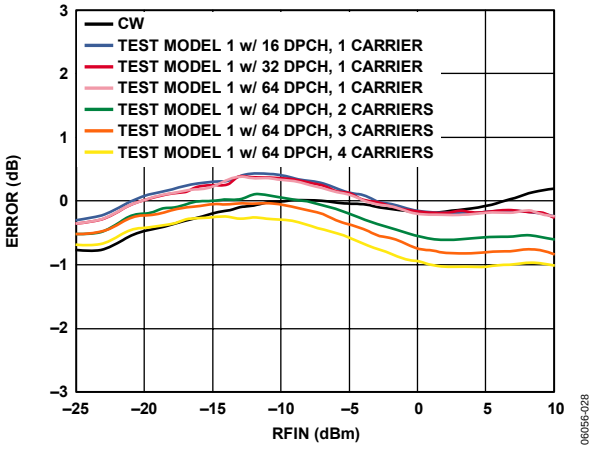


Figure 28. Error from CW Linear Reference vs. Input with Various WCDMA Down Link Waveforms at 2140 MHz, C_{FLTR} = 1 nF, C_{OUT} = 100 nF

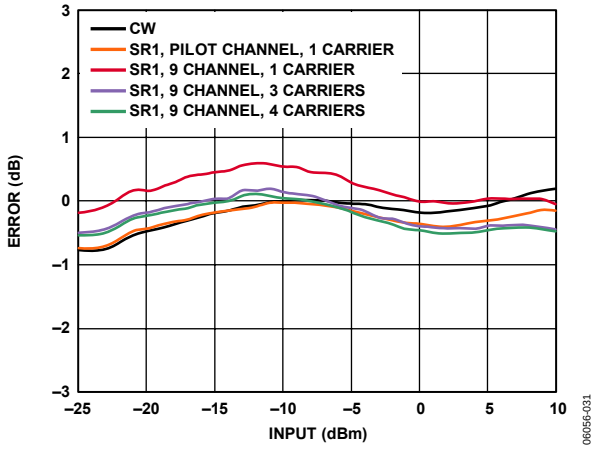


Figure 31. Error from CW Linear Reference vs. Input with Various CDMA2000 Fwd Link Waveforms at 2140 MHz, C_{FLTR} = 1 nF, C_{OUT} = 100 nF

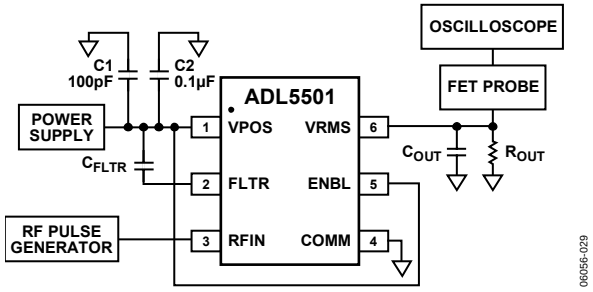


Figure 29. Hardware Configuration for Output Response to RF Input Pulse

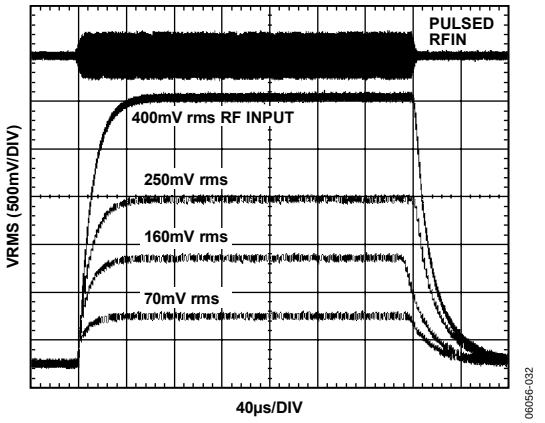


Figure 32. Output Response to Various RF Input Pulse Levels, Supply 3 V, Frequency 900 MHz, C_{FLTR} = 1 nF, C_{OUT} = Open, R_{OUT} = Open

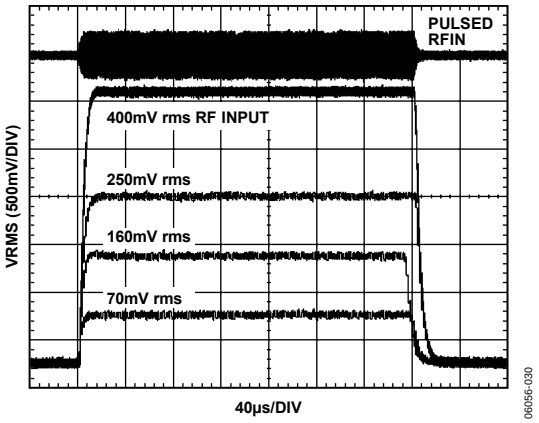


Figure 30. Output Response to Various RF Input Pulse Levels, Supply 3 V, Frequency 900 MHz, C_{FLTR} = Open, C_{OUT} = Open, R_{OUT} = Open

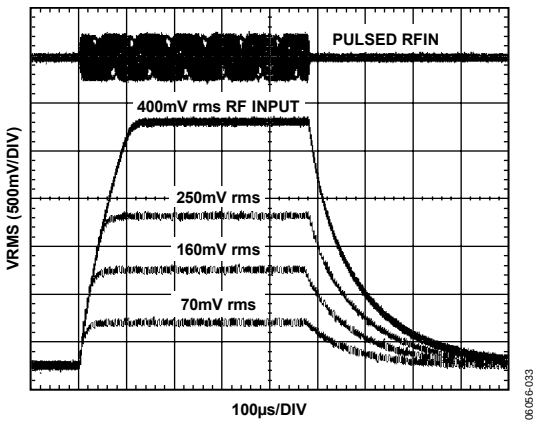


Figure 33. Output Response to Various RF Input Pulse Levels, Supply 3 V, Frequency 900 MHz, C_{FLTR} = Open, C_{OUT} = 0.1 µF, R_{OUT} = 1 kΩ

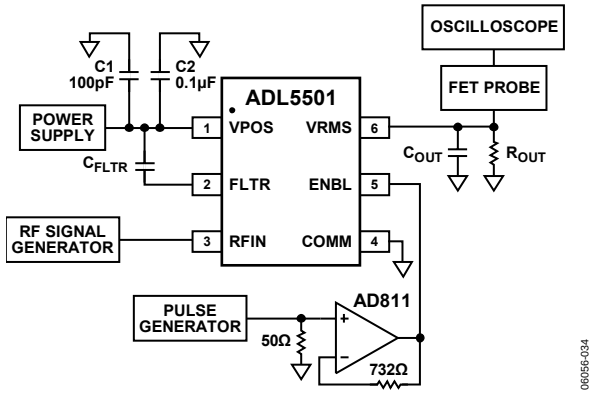


Figure 34. Hardware Configuration for Output Response to Enable Gating Measurements

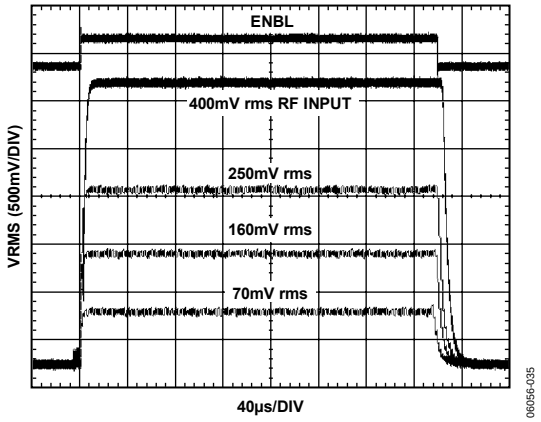


Figure 35. Output Response to Enable Gating at Various RF Input Levels, Supply 3 V, Frequency 900 MHz, C_{FLTR} = Open, C_{OUT} = Open, R_{OUT} = Open

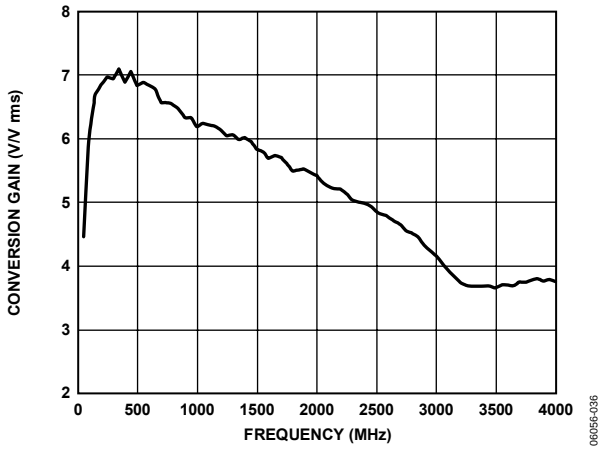


Figure 36. Conversion Gain vs. Frequency, Supply 5 V

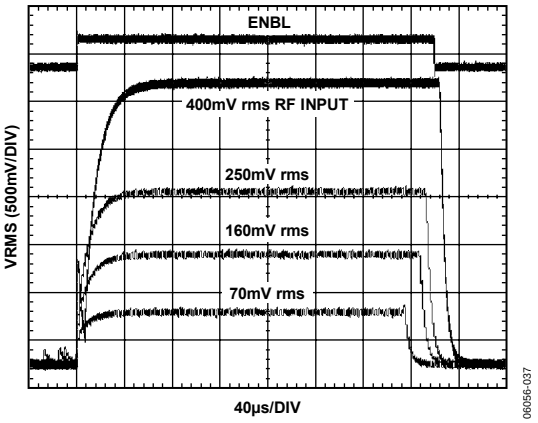


Figure 37. Output Response to Enable Gating at Various RF Input Levels, Supply 3 V, Frequency 900 MHz, C_{FLTR} = 1 nF, C_{OUT} = Open, R_{OUT} = Open

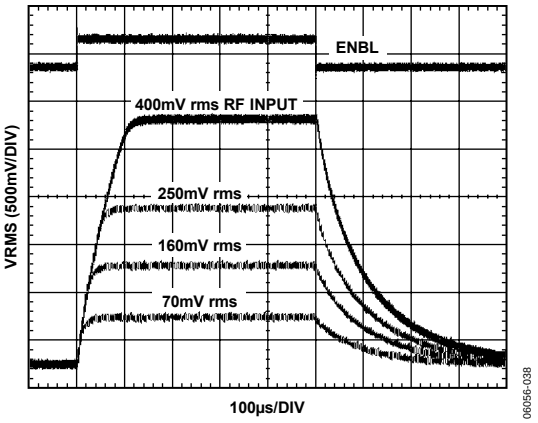


Figure 38. Output Response to Enable Gating at Various RF Input Levels, Supply 3 V, Frequency 900 MHz, C_{FLTR} = Open, C_{OUT} = 0.1 µF, R_{OUT} = 1 kΩ

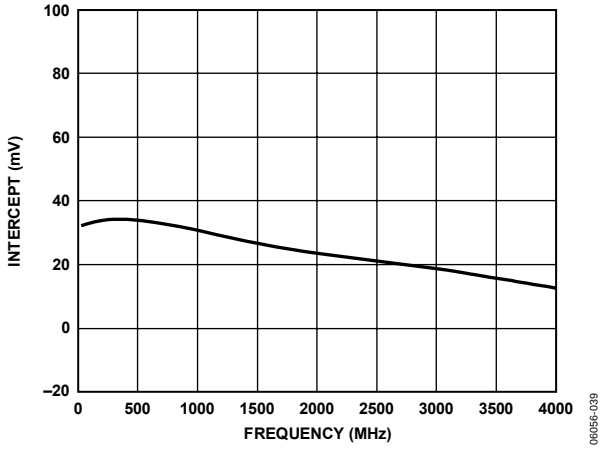


Figure 39. Intercept vs. Frequency, Supply 5 V

CIRCUIT DESCRIPTION

The ADL5501 is an rms-responding (mean power) detector that provides an approach to the exact measurement of RF power that is independent of waveform. It achieves this function by using a proprietary technique in which the outputs of two identical squaring cells are balanced by the action of a high gain error amplifier.

The signal to be measured is applied to the input of the first squaring cell through the input matching network. The input is matched to offer a broadband 50 Ω input impedance from 50 MHz to 4 GHz. The input matching network has a high-pass corner frequency of approximately 70 MHz.

The ADL5501 responds to the voltage, V_{IN}, at its input by squaring this voltage to generate a current proportional to V_{IN}^2. This current is applied to an internal load resistor in parallel with a capacitor, followed by a low-pass filter, which extracts the mean of V_{IN}^2. Although essentially voltage responding, the associated input impedance calibrates this port in terms of equivalent power. Therefore, 1 mW corresponds to a voltage input of 224 mV rms referenced to 50 Ω. Because both the squaring cell input impedance and the input matching network are frequency dependent, the conversion gain is a function of signal frequency.

The voltage across the low-pass filter, whose frequency can be arbitrarily low, is applied to one input of an error-sensing amplifier. A second identical voltage-squaring cell is used to close a negative feedback loop around this error amplifier. This second cell is driven by a fraction of the quasi-dc output voltage of the ADL5501. When the voltage at the input of the second squaring cell is equal to the rms value of V_{IN}, the loop is in a stable state, and the output then represents the rms value of the input.

By completing the feedback path through a second squaring cell, identical to the one receiving the signal to be measured, several benefits arise. First, scaling effects in these cells cancel; therefore, the overall calibration can be accurate, even though the open-loop response of the squaring cells taken separately need not be. Note that in implementing rms-dc conversion, no reference voltage enters into the closed-loop scaling. Second, the tracking in the responses of the dual cells remains very close over temperature, leading to excellent stability of calibration.

The squaring cells have very wide bandwidth with an intrinsic response from dc to microwave. However, the dynamic range of such a system is small, due in part to the much larger dynamic range at the output of the squaring cells. There are practical limitations to the accuracy of sensing very small error signals at the bottom end of the dynamic range, arising from small random offsets that limit the attainable accuracy at small inputs.

On the other hand, the squaring cells in the ADL5501 have a Class AB aspect; the peak input is not limited by its quiescent bias condition but is determined mainly by the eventual loss of square-law conformance. Consequently, the top end of their response range occurs at a large input level (approximately 700 mV rms), while preserving a reasonably accurate square-law response. The maximum usable range is, in practice, limited by the output swing. The rail-to-rail output stage can swing from a few millivolts above ground to within 100 mV below the supply. An example of the output induced limit, given a conversion gain of 6.3 V/V rms at 900 MHz and assuming a maximum output of 2.9 V with a 3 V supply, has a maximum input of 2.9 V rms/6.3 or 460 mV rms.

FILTERING

An important aspect of rms-dc conversion is the need for averaging (the function is root-mean-square). The on-chip averaging in the square domain has a corner frequency of approximately 100 kHz and is sufficient for common modulation signals, such as CDMA-, WCDMA-, and QPSK-/QAM-based OFDM (for example, WLAN and WiMAX).

For more complex RF waveforms (with modulation components extending down into the kilohertz region), more filtering is necessary to supplement the on-chip, low-pass filter. For this reason, the FLTR pin is provided; a capacitor attached between this pin and VPOS can extend the averaging time to very low frequencies.

Adequate filtering ensures the accuracy of the rms measurement; however, some ripple or ac residual can still be present on the dc output. To reduce this ripple, an external shunt capacitor can be used at the output to form a low-pass filter with the on-chip, 100 Ω resistance (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section).

APPLICATIONS

BASIC CONNECTIONS

Figure 40 shows the basic connections for the ADL5501. The device is powered by a single supply of between 2.7 V and 5.5 V, with a quiescent current of 1.1 mA. The VPOS pin is decoupled using 100 pF and 0.1 µF capacitors.

The ADL5501 RF input does not require external termination components because it is internally matched for an overall broadband input impedance of 50 Ω.

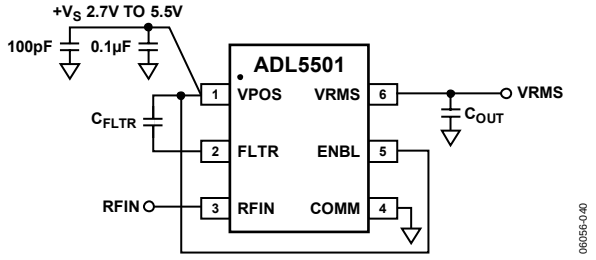


Figure 40. Basic Connections for ADL5501

OUTPUT SWING

At 900 MHz, the output voltage is nominally 6.3 times the input rms voltage (a conversion gain of 6.3 V/V rms). The output voltage swings from near ground to 4.9 V on a 5.0 V supply.

Figure 41 shows the output swing of the ADL5501 to a CW input for various supply voltages. It is clear from Figure 41 that operating the device at lower supply voltages reduces the dynamic range as the output headroom decreases.

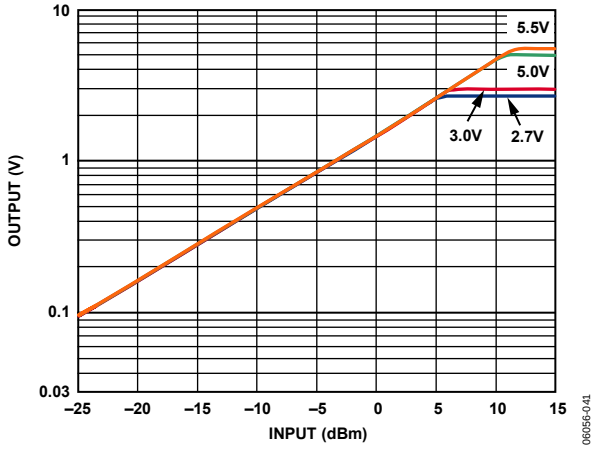


Figure 41. Output Swing for Supply Voltages of 2.7 V, 3.0 V, 5.0 V, and 5.5 V

LINEARITY

Because the ADL5501 is a linear-responding device, plots of output voltage vs. input voltage result in a straight line. It is more useful to plot the error on a logarithmic scale, as shown in Figure 42. The deviation of the plot for the ideal straight-line characteristic is caused by output clipping at the high end and by signal offsets at the low end. However, it should be noted that offsets at the low end can be either positive or negative; therefore, this plot could also trend upwards at the low end. Figure 10 through Figure 12 and Figure 16 through Figure 18 show error distributions for a large population of devices at specific frequencies.

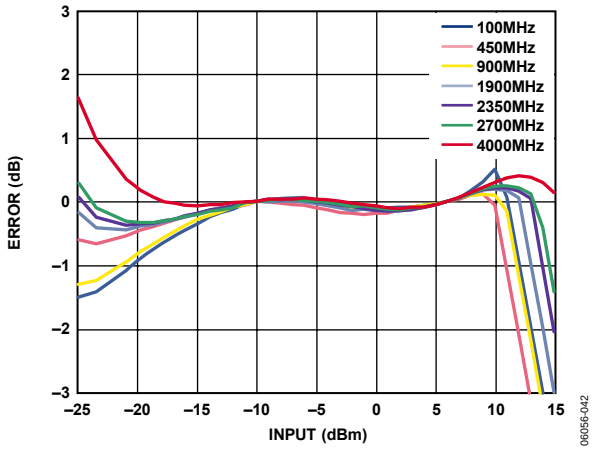


Figure 42. Representative Unit, Error in dB vs. Input Level, V_S = 5.0 V

It is also apparent in Figure 42 that the error plot tends to shift to the right with increasing frequency. The squaring cell has an input impedance that decreases with frequency. The matching network compensates for the change and maintains the input impedance at a nominal 50 Ω. The result is a decrease in the actual voltage across the squaring cell as the frequency increases, reducing the conversion gain. Similarly, conversion gain is less at frequencies near 100 MHz because of the small on-chip coupling capacitor.

INPUT COUPLING USING A SERIES RESISTOR

Figure 43 shows a technique for coupling the input signal into the ADL5501 that can be applicable where the input signal is much larger than the input range of the ADL5501. A series resistor combines with the input impedance of the ADL5501 to attenuate the input signal. Because this series resistor forms a divider with the frequency dependent input impedance, the apparent gain changes greatly with frequency. However, this method has the advantage of very little power being tapped off in RF power transmission applications. If the resistor is large compared to the transmission line's impedance, the VSWR of the system is relatively unaffected.

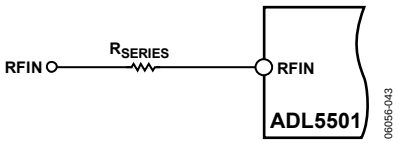


Figure 43. Attenuating the Input Signal

The resistive tap or series resistance, R_{SERIES}, can expressed as

$$R_{SERIES} = R_{IN}\,(1 - 10^{ATTN/20})/(10^{ATTN/20}) \quad (1)$$

where:

R_{IN} is the input impedance of RFIN.

ATTN is the desired attenuation factor in dB.

For example, if a power amplifier with a maximum output power of +28 dBm is matched to the ADL5501 input at +5 dBm, then a −23 dB attenuation factor is required. At 900 MHz, the input resistance, R_{IN}, is 55 Ω.

$$R_{SERIES} = (55\ \Omega)(1 - 10^{-23/20})/(10^{-23/20}) = 722\ \Omega \quad (2)$$

Thus, for an attenuation of −23 dB, a series resistance of approximately 722 Ω is needed.

MULTIPLE RF INPUTS

Figure 44 shows a technique for combining multiple RF input signals to the ADL5501. Some applications can share a single detector for multiple bands. Three 16.5 Ω resistors in a T-network combine the three 50 Ω terminations (including the ADL5501). The broadband resistive combiner ensures each port of the T-network sees a 50 Ω termination. Because there are only 6 dB of isolation from one port of the combiner to the other ports, only one band should be active at a time.

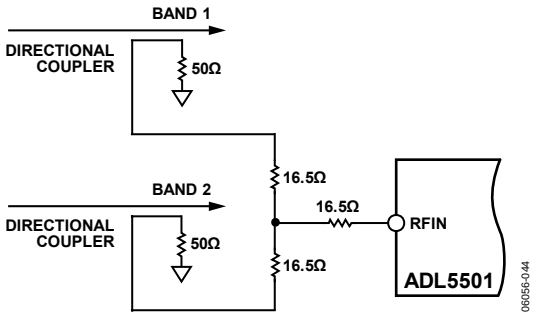


Figure 44. Combining Multiple RF Input Signals

SELECTING THE SQUARE-DOMAIN FILTER AND OUTPUT LOW-PASS FILTER

The internal filter capacitor of the ADL5501 provides averaging in the square domain but leaves some residual ac on the output. Signals with high peak-to-average ratios, such as W-CDMA or CDMA2000, can produce ac-residual levels on the ADL5501 dc output. To reduce the effects of these low frequency components in the waveforms, some additional filtering is required.

The square-domain filter capacitance of the ADL5501 can be augmented by connecting a capacitor between Pin 2 (FLTR) and Pin 1 (VPOS). In addition, the output of the ADL5501 can be filtered directly by placing a capacitor between VRMS (Pin 6) and ground. The combination of the on-chip, 100 Ω output series resistance and the external shunt capacitor forms a low-pass filter to reduce the residual ac.

Table 4 shows the effect of several capacitor values for various communications standards with high peak-to-average ratios along with the residual ripple at the output, in peak-to-peak and rms volts. Note that large load capacitances increase the turn-on and pulse response times (see Figure 30, Figure 32, Figure 33, Figure 35, Figure 37, and Figure 38). For more information on the effects of the filter capacitances on the response, see the Power Consumption, Enable, and Power-On/-Off Response Time section.

Table 4. Waveform and Output Filter Effects on Residual AC

Waveform	C_{FILT}, C_{OUT}	Output	Residual AC	
		V dc	mV p-p	mV rms
64QAM (7.4 dB CF)	1 nF, Open	0.5	83	11
		1.0	175	21
		2.0	394	47
	Open, 0.1 µF	0.5	49	5.5
		1.0	98	11
		2.0	212	23
	1 nF, 0.1 µF	0.5	45	5.5
		1.0	93	11
		2.0	200	24
W-CDMA RL (3.4 dB CF)	1 nF, Open	0.5	6.4	0.8
		1.0	19	2.6
		2.0	52	6.6
	Open, 0.1 µF	0.5	4.5	0.6
		1.0	16	2.2
		2.0	36	4.9
	1 nF, 0.1 µF	0.5	3.1	0.5
		1.0	9.6	1.4
		2.0	27	3.9
CDMA2000 DL (6.7 dB CF)	1 nF, Open	0.5	67	8.6
		1.0	148	19
		2.0	339	43
	Open, 0.1 µF	0.5	28	3.9
		1.0	56	7.9
		2.0	119	17
	1 nF, 0.1 µF	0.5	26	3.7
		1.0	52	7.7
		2.0	116	17
W-CDMA UL TM1-64, 1 CR	1 nF, Open	0.5	204	32
		1.0	396	64
		2.0	840	140
	Open, 0.1 µF	0.5	60	11
		1.0	112	21
		2.0	227	42
	1 nF, 0.1 µF	0.5	56	11
		1.0	114	21
		2.0	243	45

POWER CONSUMPTION, ENABLE, AND POWER-ON/-OFF RESPONSE TIME

The quiescent current consumption of the ADL5501 varies with the size of the input signal from approximately 1.1 mA for no signal up to 6.2 mA at an input level of 0.7 V rms (10 dBm, re 50 Ω). If the input is driven beyond this point, the supply current increases sharply (as shown in Figure 6). There is little variation in quiescent current with power supply voltage.

The ADL5501 can be disabled either by pulling the ENBL (Pin 5) to COMM (Pin 4) or by removing the supply power to the device. Disabling the device via the ENBL function reduces the leakage current to less than 1 µA.

If the input of the ADL5501 is driven while the device is disabled (ENBL = COMM), the leakage current of less than 1 µA increases as a function of input level. When the device is disabled, the output impedance increases to approximately 33.5 kΩ.

The turn-on time and pulse response is strongly influenced by the size of the square-domain filter and output shunt capacitor. Figure 45 shows a plot of the output response to an RF pulse on the RFIN pin, with a 0.1 µF output filter capacitor and no square-domain filter capacitor. The falling edge is particularly dependent on the output shunt capacitance, as shown in Figure 45.

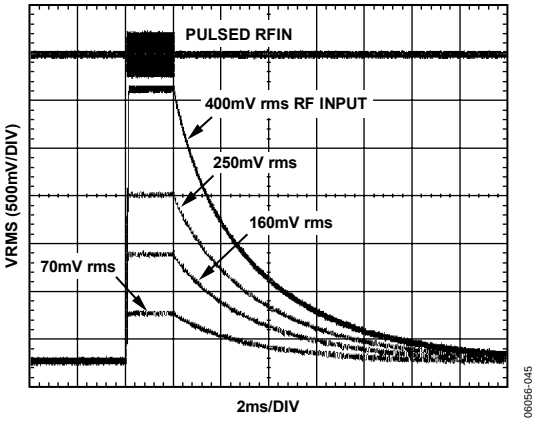


Figure 45. Output Response to Various RF Input Pulse Levels, Supply 3 V, Frequency 900 MHz, Square-Domain Filter Open, Output Filter 0.1 µF

To improve the falling edge of the enable and pulse responses, a resistor can be placed in parallel with the output shunt capacitor. The added resistance helps to discharge the output filter capacitor. Although this method reduces the power-off time, the added load resistor also attenuates the output (see the Output Drive Capability and Buffering section).

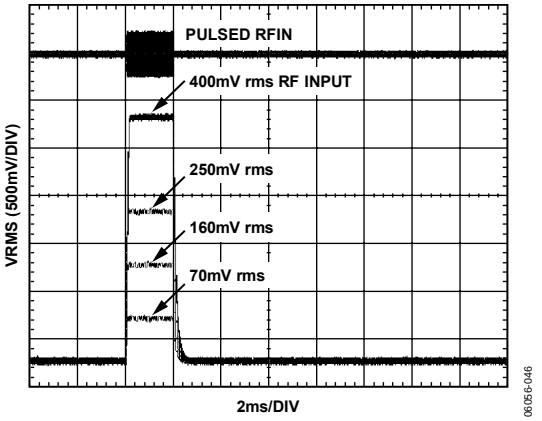


Figure 46. Output Response to Various RF Input Pulse Levels, Supply 3 V, Frequency 900 MHz, Square-Domain Filter Open, Output Filter 0.1 µF with Parallel 1 kΩ

The square-domain filter improves the rms accuracy for high crest factors (see the Selecting the Square-Domain Filter and Output Low-Pass Filter), but it can hinder the response time. For optimum response time and low ac residual, both the square-domain filter and the output filter should be used.

The square-domain filter at FLTR can be reduced to improve response time, and the remaining ac residual can be decreased by using the output filter, which has a smaller time constant.

OUTPUT DRIVE CAPABILITY AND BUFFERING

The ADL5501 is capable of sourcing an output current of approximately 3 mA. The output current is sourced through the on-chip, 100 Ω series resistor; therefore, any load resistor forms a voltage divider with this on-chip resistance.

It is recommended that the ADL5501 drive high resistive loads to preserve output swing. If an application requires driving a low resistance load, a simple buffering circuit can be used, as shown in Figure 49. Similar circuits can be used to increase or decrease the nominal conversion gain (see Figure 47 and Figure 48). In Figure 48, the AD8031 buffers a resistive divider to give half of the slope. In Figure 47, the op amp gain of two doubles the slope. Using other resistor values, the slope can be changed to an arbitrary value. The AD8031 rail-to-rail op amp, used in these examples, can swing from 50 mV to 4.95 V on a single 5 V supply and operates at supply voltages down to 2.7 V. If high output current is required (>10 mA), the AD8051, which also has rail-to-rail capability, can be used down to a supply voltage of 3 V. It can deliver up to 45 mA of output current.

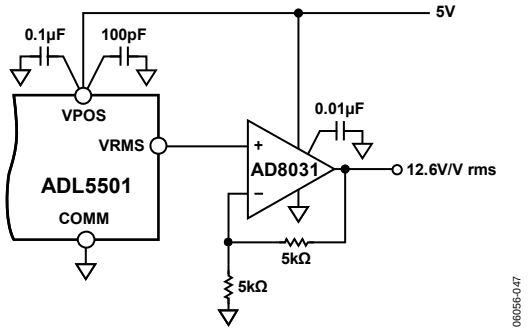


Figure 47. Output Buffering Options, Slope of 12.6 V/V rms at 900 MHz

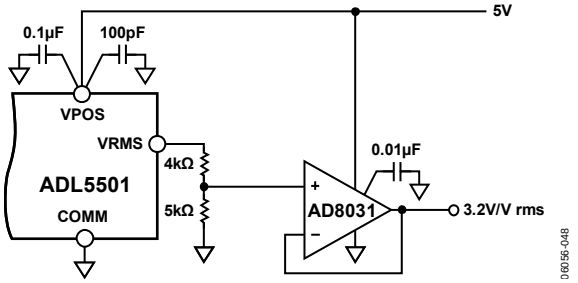


Figure 48. Output Buffering Options, Slope of 3.2 V/V rms at 900 MHz

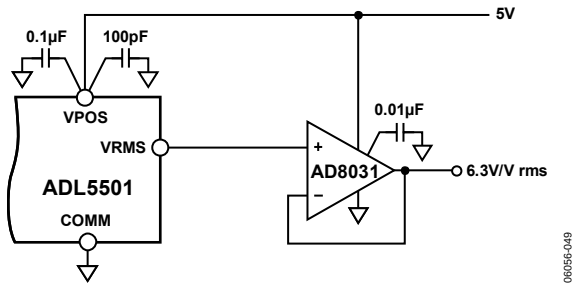


Figure 49. Output Buffering Options, Slope of 6.3 V/V rms at 900 MHz

VRMS OUTPUT OFFSET

The ADL5501 has a ±1 dB error detection range of about 30 dB, as shown in Figure 10 to Figure 12 and Figure 16 to Figure 18. The error is referred to the best-fit line defined in the linear region of the output response. Below an input power of −20 dBm, the response is no longer linear and begins to lose accuracy. In addition, depending on the supply voltage, saturation of the output limits the detection accuracy above 10 dBm. Calibration points should be chosen in the linear region, avoiding the nonlinear ranges at the high and low extremes.

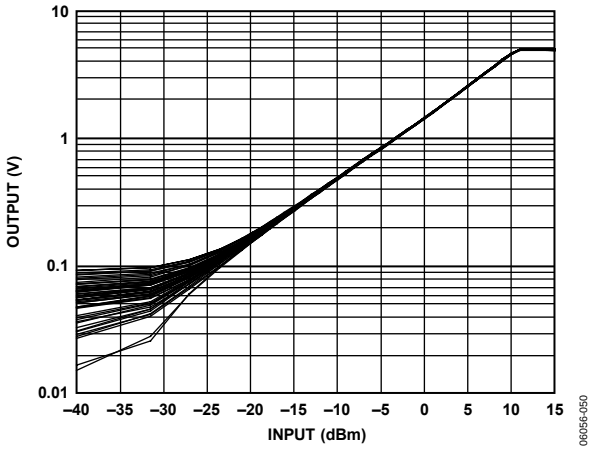


Figure 50. Output vs. Input Level Distribution of 50 Devices, Frequency 900 MHz, Supply 5.0 V

Figure 50 shows the distribution of the output response vs. the input power for multiple devices. The ADL5501 loses accuracy at low input powers as the output response begins to fan out. As the input power is reduced, the spread of the output response increases along with the error. Although some devices follow the ideal linear response at very low input powers, not all devices continue the ideal linear regression to a near 0 V y-intercept. Some devices exhibit output responses that rapidly decrease, and some flatten out. With no RF signal applied, the ADL5501 has a typical output offset of 50 mV (with a maximum of 150 mV).

DEVICE CALIBRATION AND ERROR CALCULATION

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. In general, calibration is performed by applying two input power levels to the ADL5501 and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear operating range of the device. The best-fit line is characterized by calculating the conversion gain (or slope) and intercept using the following equations:

$$Gain = (V_{RMS2} - V_{RMS1})/(V_{IN2} - V_{IN1}) \quad (3)$$

$$Intercept = V_{RMS1} - (Gain \times V_{IN1}) \quad (4)$$

where:

V_{IN} is the rms input voltage to RFIN.

V_{RMS} is the voltage output at VRMS.

Once gain and intercept are calculated, an equation can be written that allows calculation of an (unknown) input power based on the measured output voltage.

$$V_{IN} = (V_{RMS} - Intercept)/Gain \quad (5)$$

For an ideal (known) input power, the law conformance error of the measured data can be calculated as

$$ERROR\ (\text{dB}) = 20 \times \log\left[(V_{RMS,\,MEASURED} - Intercept)/(Gain \times V_{IN,\,IDEAL})\right] \quad (6)$$

Figure 51 includes a plot of the error at 25°C, the temperature at which the ADL5501 is calibrated. Note that the error is not zero. This is because the ADL5501 does not perfectly follow the ideal linear equation, even within its operating region. The error at the calibration points is, however, equal to 0 by definition.

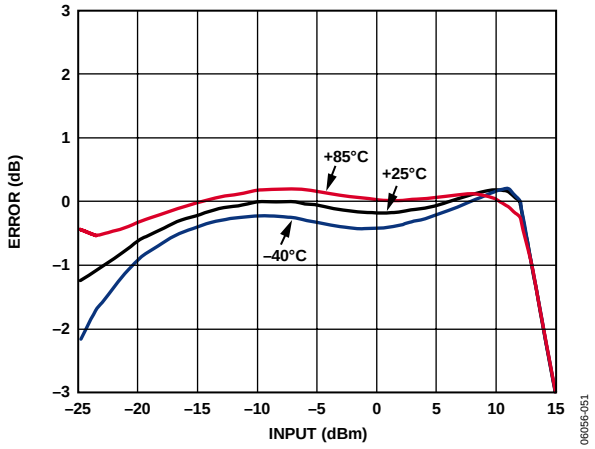


Figure 51. Error from Linear Reference vs. Input at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 1900 MHz, Supply 5.0 V

Figure 51 also includes error plots for the output voltage at −40°C and +85°C. These error plots are calculated using the gain and intercept at 25°C. This is consistent with calibration in a mass-production environment where calibration at temperature is not practical.

CALIBRATION FOR IMPROVED ACCURACY

Another way of presenting the error function of the ADL5501 is shown in Figure 52. In this case, the dB error at hot and cold temperatures is calculated with respect to the transfer function at ambient. This is a key difference in comparison to the previous plots. Up to now, the errors were calculated with respect to the ideal linear transfer function at ambient. When this alternative technique is used, the error at ambient becomes equal to 0 by definition (see Figure 52).

This plot is a useful tool for estimating temperature drift at a particular power level with respect to the (nonideal) response at ambient. The linearity and dynamic range tend to be improved artificially with this type of plot because the ADL5501 does not perfectly follow the ideal linear equation (especially outside of its linear operating range). Achieving this level of accuracy in an end application requires calibration at multiple points in the operating range of the device.

In some applications, very high accuracy is required at just one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at or close to full power. The ADL5501 offers a tight error distribution in the high input power range, as shown in Figure 52. The high accuracy range, centered around 9 dBm at 1900 MHz, offers 7 dB of ±0.1 dB detection error over temperature. Multiple point calibration at ambient temperature in the reduced range offers precise power measurement with near 0 dB error from −40°C to +85°C.

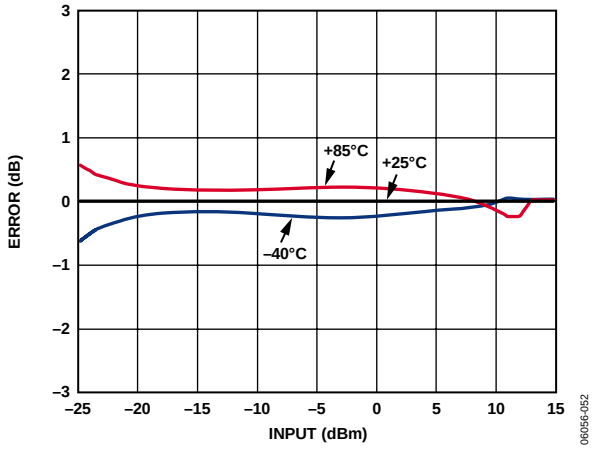


Figure 52. Error from +25°C Output Voltage at −40°C, +25°C, and +85°C After Ambient Normalization, Frequency 1900 MHz, Supply 5.0 V

The high accuracy range center varies over frequency. At 1900 MHz, the region is centered at approximately 9 dBm. At higher frequencies, the high accuracy range is centered at higher input powers (see Figure 13 through Figure 15 and Figure 19 through Figure 21).

DRIFT OVER A REDUCED TEMPERATURE RANGE

Figure 53 shows the error over temperature for a 1.9 GHz input signal. Error due to drift over temperature consistently remains within ±0.25 dB and only begins to exceed this limit when the ambient temperature goes above +25°C and below −10°C. For all frequencies using a reduced temperature range, higher measurement accuracy is achievable.

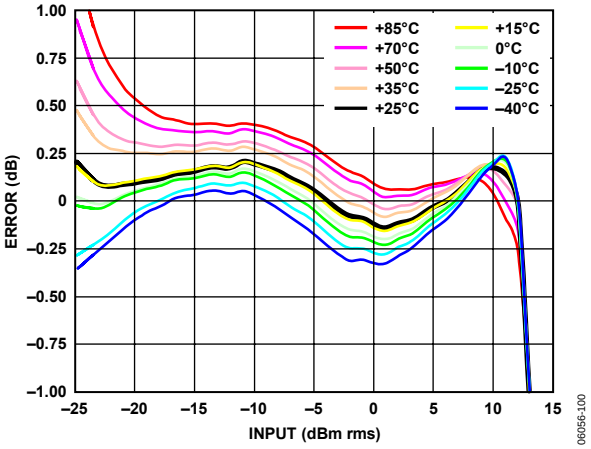


Figure 53. Typical Drift at 1.9 GHz for Various Temperatures

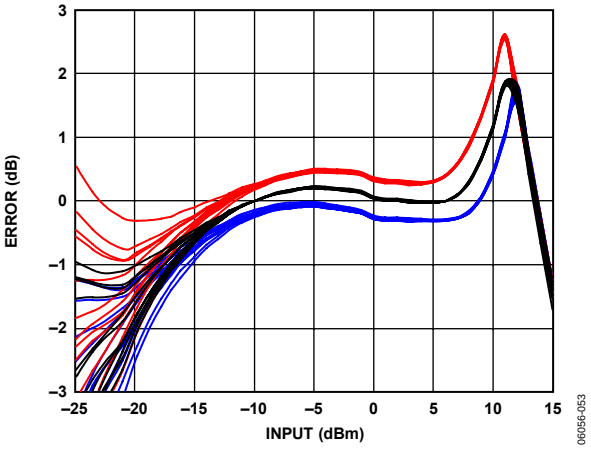


Figure 54. Temperature Drift Distributions for 12 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference; Frequency 50 MHz; Supply 5.0 V

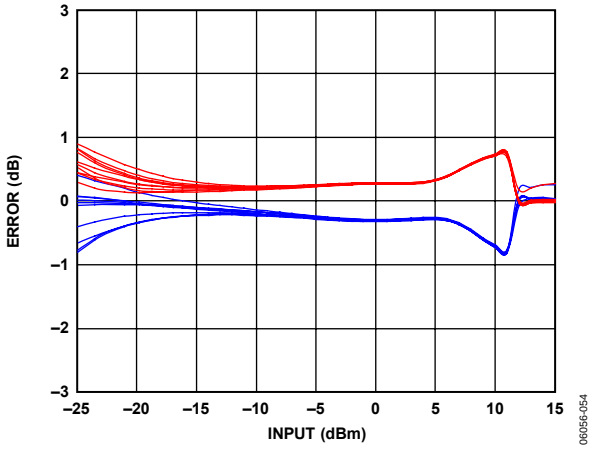


Figure 55. Output Delta from +25°C Output Voltage for 12 Devices at −40°C and +85°C, Frequency 50 MHz, Supply 5.0 V

OPERATION BELOW 100 MHZ

The ADL5501 works at frequencies below 100 MHz, but exhibits slightly higher linearity error. Figure 54 shows the error distribution of 12 devices at 50 MHz over temperature. When compared to an ideal linear transfer function at ambient, the error of the ADL5501 over temperature remains within ±0.5 dB for the central 20 dB of the dynamic range. At the higher input power levels, the error grows as the response becomes nonlinear.

Due to the repeatability of the performance from part to part, compensation can be applied to reduce the effects of temperature drift and linearity error. To detect larger dynamic ranges at lower frequencies, the transfer function at ambient can be calibrated, thus eliminating the linearity error. This technique is discussed in detail in the Calibration for Improved Accuracy section. Figure 55 shows that the dynamic range within ±0.5 dB error improves to 30 dB by using this method.

EVALUATION BOARD

Figure 56 shows the schematic of the ADL5501 evaluation board. The layout and silkscreen of the evaluation board layers are shown in Figure 57 to Figure 60. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by 100 pF and 0.1 µF capacitors. Table 5 details the various configuration options of the evaluation board.

Problems caused by impedance mismatch can arise using the evaluation board to examine the ADL5501 performance. One way to reduce these problems is to put a coaxial 3 dB attenuator on the RFIN SMA connector. Mismatches at the source, cable, and cable interconnection, as well as those occurring on the evaluation board, can cause these problems.

A simple (and common) example of such a problem is triple travel due to mismatch at both the source and the evaluation board. Here the signal from the source reaches the evaluation board and mismatch causes a reflection. When that reflection reaches the source mismatch, it causes a new reflection, which travels back to the evaluation board, adding to the original signal incident at the board. The resultant voltage varies with both cable length and frequency dependence on the relative phase of the initial and reflected signals. Placing the 3 dB pad at the input of the board improves the match at the board and, thus, reduces the sensitivity to mismatches at the source. When such precautions are taken, measurements are less sensitive to cable length and other fixture issues. In an actual application when the distance between ADL5501 and source is short and well defined, this 3 dB attenuator is not needed.

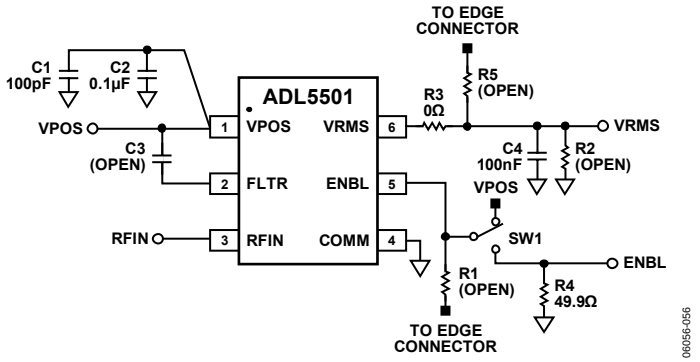


Figure 56. Evaluation Board Schematic

Table 5. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and Supply Vector Pins.	Not Applicable
C1, C2	Power Supply Decoupling. The nominal supply decoupling of 100 pF and 0.1 µF.	C1 = 100 pF (Size 0402) C2 = 0.1 µF (Size 0402)
C3	Filter Capacitor. The internal averaging capacitor can be augmented by placing additional capacitance in C3.	C3 = Open (Size 0402)
R2, R3, C4	Output Filtering. The combination of the internal 100 Ω output resistance and C4 produce a low-pass filter to reduce output ripple. The output can also be scaled down using the resistor divider pads, R3 and R2. In addition, resistors and capacitors can be placed in C4 and R2 to load test VRMS.	R2 = Open (Size 0402) R3 = 0 Ω (Size 0402) C4 = 100 nF (Size 0402)
R4, SW1	Device Enable. When the switch is set toward the SW1 label, the ENBL pin is connected to VPOS and the ADL5501 is in operating mode. In the opposite switch position, the ENBL pin is grounded (through the 49.9 Ω resistor), putting the device in power-down mode. While in this switch position, the ENBL pin can be driven by a signal generator via the SMA labeled ENBL. In this case, R4 serves as a termination resistor for generators requiring a 50 Ω match.	R4 = 49.9 Ω (Size 0402) SW1 = toward SW1 label
R1, R5	Alternate Interface. R1and R5 allow for VRMS and ENBL to be accessible from the edge connector, which is used only for characterization.	R1 = Open (Size 0402) R5 = Open (Size 0402)

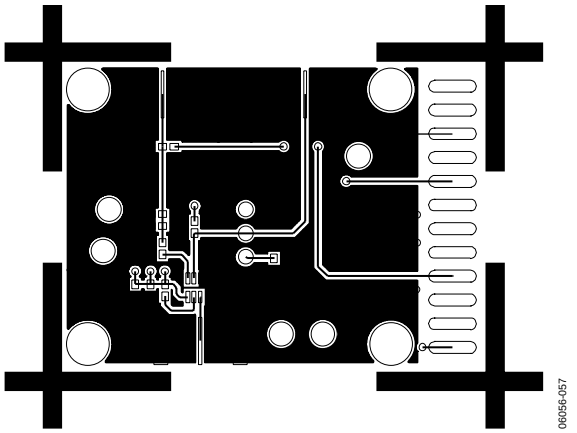


Figure 57. Layout of Component Side

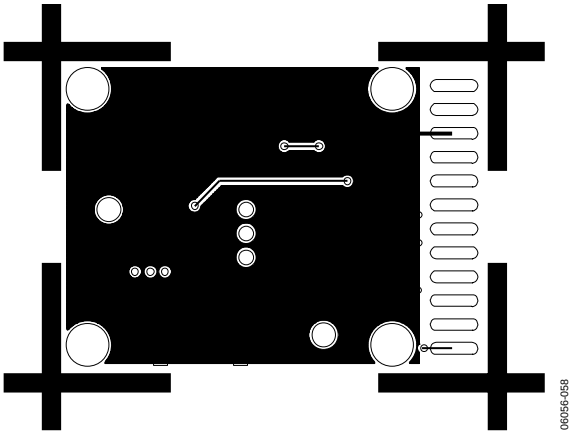


Figure 58. Layout of Circuit Side

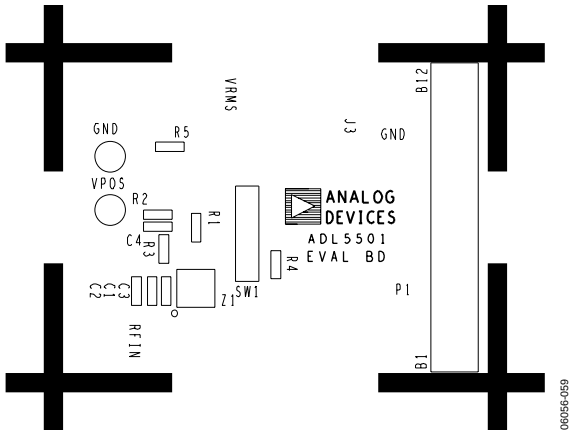


Figure 59. Silkscreen of Component Side

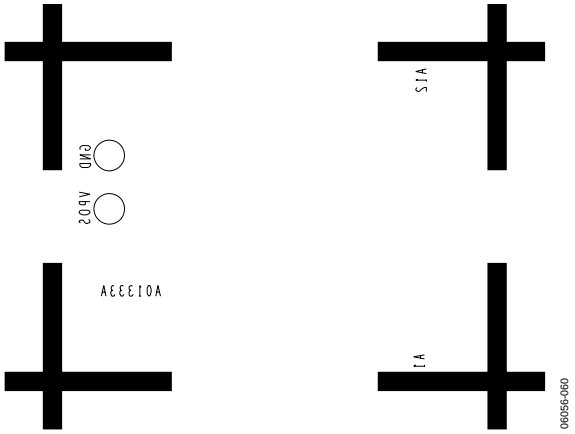
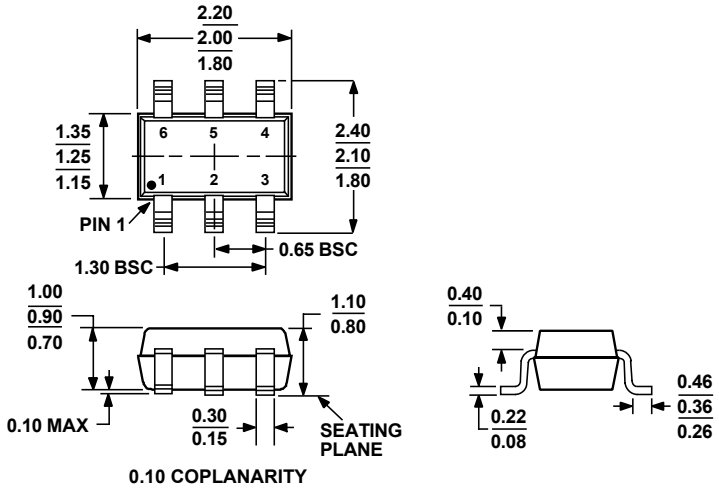


Figure 60. Silkscreen of Circuit Side

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AB

Figure 61. 6-Lead Thin Shrink Small Outline Transistor Package [SC-70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5501AKSZ-R7[1]	–40°C to +85°C	6-Lead SC-70, 7″ Tape and Reel	KS-6	Q0Z	3,000
ADL5501AKSZ-R2[1]	–40°C to +85°C	6-Lead SC-70, 7″ Tape and Reel	KS-6	Q0Z	250
ADL5501-EVALZ[1]		Evaluation Board			

[1] Z = Pb-free part.

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