LC²MOS 8-/16-Channel High Performance Analog Multiplexers

ADG406/ADG407/ADG426

FEATURES

44 V supply maximum ratings
V_{SS} to V_{DD} analog signal range
Low on resistance (80 Ω maximum)
Low power
Fast switching
t_{ON} < 160 ns
t_{OFF} < 150 ns
Break-before-make switching action

APPLICATIONS

Audio and video routing
Automatic test equipment
Data acquisition systems
Battery powered systems
Sample hold systems
Communication systems
Avionics

PRODUCT HIGHLIGHTS

1. Extended Signal Range.
2. The ADG406/ADG407/ADG426 are fabricated on an enhanced LC²MOS process giving an increased signal range which extends to the supply rails.
3. Low Power Dissipation.
4. Low R_{ON}.
5. Single/Dual Supply Operation.
6. Single Supply Operation.
7. For applications where the analog signal is unipolar, the ADG406/ADG407/ADG426 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and remain functional with single supplies as low as +5 V.

FUNCTIONAL BLOCK DIAGRAMS

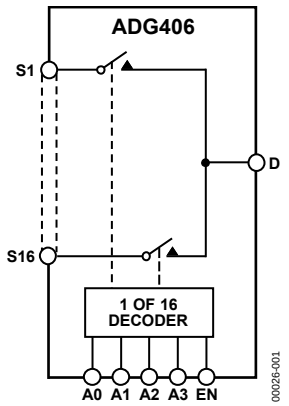

Figure 1.

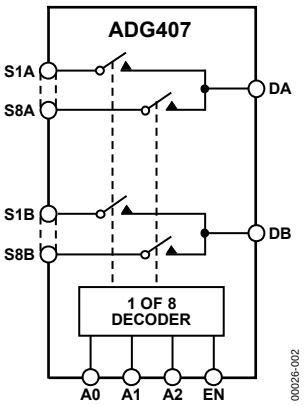

Figure 2.

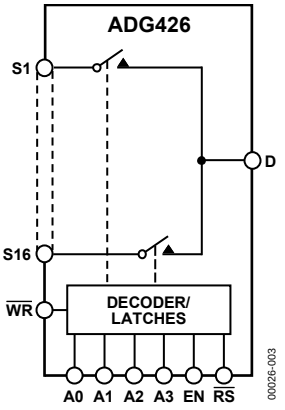

Figure 3.

Rev. B

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Added Table 8 11
Updated Outline Dimensions 18
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4/94—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADG406, ADG407, and ADG426 are monolithic CMOS analog multiplexers. The ADG406 and ADG426 switch one of sixteen inputs to a common output as determined by the 4-bit binary address lines: A0, A1, A2, and A3. The ADG426 has on-chip address and control latches that facilitate microprocessor interfacing. The ADG407 switches one of eight differential inputs to a common differential output as determined by the 3-bit binary address lines A0, A1 and A2. An EN input on all devices is used to enable or disable the device. When disabled, all channels are switched off.

The ADG406/ADG407/ADG426 are designed on an enhanced LC^2MOS process that provides low power dissipation yet gives high switching speed and low on resistance. These features make the parts suitable for high speed data acquisition systems and audio signal switching. Low power dissipation makes the parts suitable for battery powered systems. Each channel conducts equally well in both directions when on and has an input signal range which extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter[1]	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
R_{ON}	50		Ω typ	V_D = ±10 V, I_S = −1 mA
	80	125	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
R_{ON} Match	4		Ω typ	V_D = 0 V, I_S = −1 mA
LEAKAGE CURRENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage I_S (Off)	±0.5	±20	nA max	V_D = ±10 V, V_S = ∓10 V, see Figure 26
Drain Off Leakage I_D (Off)				V_D = ±10 V, V_S = ∓10 V; see Figure 27
ADG406, ADG426	±1	±20	nA max	
ADG407	±1	±20	nA max	
Channel On Leakage I_D, I_S (On)				V_S = V_D = ±10 V; see Figure 28
ADG406, ADG426	±1	±20	nA max	
ADG407	±1	±20	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}		±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	120		ns typ	R_L = 300 Ω, C_L = 35 pF; V_1 = ±10 V, V_2 = ∓10 V; see Figure 29
	150	250	ns max	
Break Before Make Delay, t_{OPEN}	10	10	ns min	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V, see Figure 30
t_{ON} (EN, $\overline{WR}$)	120	175	ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 5 V, see Figure 31
	160	225	ns max	
t_{OFF} (EN, $\overline{RS}$)	110	130	ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 5 V, see Figure 31
	150	180	ns max	
ADG426 Only				
t_W, Write Pulse Width		100	ns min	
t_S, Address, Enable Setup Time		100	ns min	
t_H, Address, Enable Hold Time		10	ns min	
t_{RS}, Reset Pulse Width		100	ns min	V_S = +5 V
Charge Injection	8		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; See Figure 34
Off Isolation	−75		dB typ	R_L = 1 kΩ, f = 100 kHz; V_{EN} = 0 V, see Figure 35
Channel-to-Channel Crosstalk	85		dB typ	R_L = 1 kΩ, f = 100 kHz, see Figure 36
C_S (Off)	5		pF typ	f = 1 MHz
C_D (Off)				f = 1 MHz
ADG406, ADG426	50		pF typ	
ADG407	25		pF typ	
C_D, C_S (On)				f = 1 MHz
ADG406, ADG426	60		pF typ	
ADG407	40		pF typ	

Parameter[1]	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}		1	µA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5	µA max	
I_{SS}		1	µA typ	
		5	µA max	
I_{DD}	100		µA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	µA max	
I_{SS}		1	µA typ	
		5	µA max	

[1] Temperature ranges is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter[1]	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
R_{ON}	90		Ω typ	V_D = +3 V, +8.5 V, I_S = −1 mA;
	125	200	Ω max	V_{DD} = +10.8 V
LEAKAGE CURRENTS				V_{DD} = +13.2 V
Source Off Leakage I_S (Off)	±0.5	±20	nA max	V_D = 8 V/0.1 V, V_S = 0.1 V/8 V; see Figure 26
Drain Off Leakage I_D (Off)				V_D = 8 V/0.1 V, V_S = 0.1 V/8 V; see Figure 27
ADG406, ADG426	±1	±20	nA max	
ADG407	±1	±20	nA max	
Channel On Leakage I_D, I_S (On)				V_S = V_D = 8 V/0.1 V, see Figure 28
ADG406, ADG426	±1	±20	nA max	
ADG407	±1	±20	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}		±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	180		ns typ	R_L = 300 Ω, C_L = 35 pF; V_1 = 8 V/0 V, V_2 = 0 V/8 V; see Figure 29
	220	350	ns max	
Break Before Make Delay, t_{OPEN}	10		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 5 V, see Figure 30
t_{ON} (EN, $\overline{WR}$)	180		ns typ	R_L = 300 Ω, C_L = 35 pF;
	240	350	ns max	V_S = +5 V, see Figure 31
t_{OFF} (EN, $\overline{RS}$)	135		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 5 V, see Figure 31
	180	220	ns max	
ADG426 Only				
t_W, Write Pulse Width		100	ns min	
t_S, Address, Enable Setup Time		100	ns min	
t_H, Address, Enable Hold Time		10	ns min	
t_{RS}, Reset Pulse Width		100	ns min	V_S = +5 V
Charge Injection	5		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 34
Off Isolation	−75		dB typ	R_L = 1 kΩ, f = 100 kHz; see Figure 35
Channel-to-Channel Crosstalk	85		dB typ	R_L = 1 kΩ, f = 100 kHz; see Figure 36
C_S (Off)	8		pF typ	f = 1 MHz
C_D (Off)				f = 1 MHz
ADG406, ADG426	80		pF typ	
ADG407	40		pF typ	f = 1 MHz
C_D, C_S (On)				
ADG406, ADG426	100		pF typ	
ADG407	50		pF typ	
POWER REQUIREMENTS				V_{DD} = +13.2 V
I_{DD}		1	μA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5	μA max	
I_{DD}	100		μA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	μA max	

[1] Temperature range is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

ADG426 TIMING DIAGRAMS

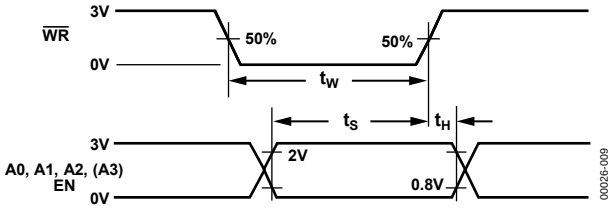


Figure 4. Timing Sequence for Latching the Switch Address and Enable Inputs

Figure 4 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

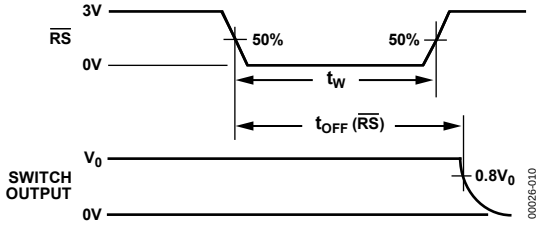


Figure 5. Reset Pulse Width and Reset Turn Off Time

Figure 5 shows the reset pulse width, t_{rs}, and the reset turn off time, t_{OFF} ($\overline{RS}$).

Note that all digital input signals rise and fall times are measured from 10% to 90% of 3 V; $t_R = t_F = 20$ ns.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs[1]	V_{SS} − 2 V to V_{DD} + 2 V or 20 mA, whichever occurs first
Continuous Current, S or D	20 mA
Peak Current, S or D	40 mA (Pulsed at 1 ms, 10% duty cycle max)
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Plastic Package	
θ_{JA}, Thermal Impedance	75°C/W
Lead Temperature, Soldering (10 sec)	260°C
PLCC Package	
θ_{JA}, Thermal Impedance	80°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
SSOP Package	
θ_{JA}, Thermal Impedance	122°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] Overvoltages at A, S, D, $\overline{WR}$, or $\overline{RS}$ will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

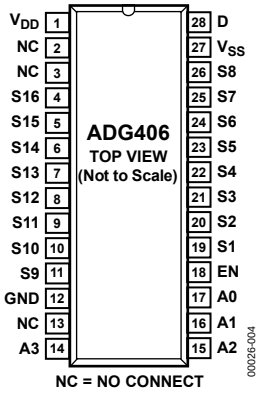


Figure 6. 28-Lead PDIP

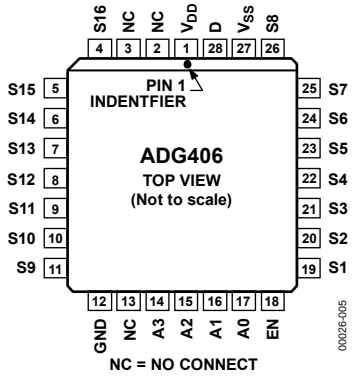


Figure 7. 28-Lead PLCC

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Most Positive Power Supply Potential.
2, 3, 13	NC	No Connect.
4 to 11	S16 to S9	Source Terminal 16 to Source Terminal 9. These pins can be inputs or outputs.
12	GND	Ground (0 V) Reference.
14 to 17	A3 to A0	Logic Control Input.
18	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19 to 26	S1 to 8	Source Terminal 1 to Source Terminal 8. These pins can be inputs or outputs.
27	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	D	Drain Terminal. This pin can be an input or an output.

Table 5. Truth Table (ADG406)

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

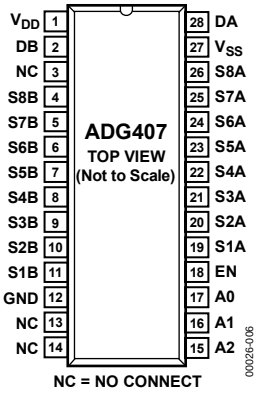


Figure 8. 28-Lead PDIP

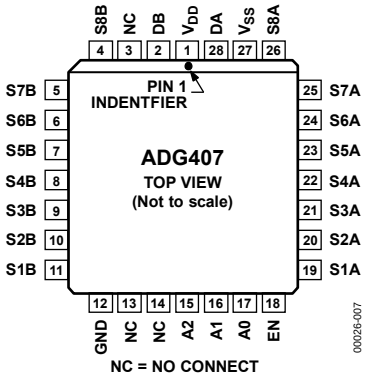


Figure 9. 28-Lead PLCC

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Most Positive Power Supply Potential.
2	DB	Drain Terminal B. This pin can be an input or an output.
3, 13, 14	NC	No Connect.
4 to 11	S8B to S1B	Source Terminal 8B to Source Terminal 1B. These pins can be inputs or outputs.
12	GND	Ground (0 V) Reference.
15 to 17	A2 to A0	Logic Control Input.
18	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19 to 26	S1A to S8A	Source Terminal 1A to Source Terminal 8A. These pins can be inputs or outputs.
27	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	DA	Drain Terminal A. This pin can be an input or an output.

Table 7. Truth Table (ADG407)

A2	A1	A0	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

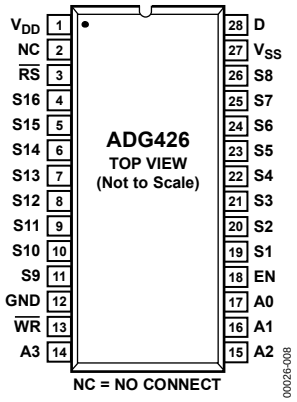


Figure 10. 28-Lead PDIP/SSOP

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Most Positive Power Supply Potential.
2	NC	No Connect.
3	$\overline{RS}$	Active Low Logic Input. When this pin is low, all switches are open, and address and enable latches registers are cleared to 0.
4 to 11	S16 to S9	Source Terminal 16 to Source Terminal 9. These pins can be inputs or outputs.
12	GND	Ground (0 V) Reference.
13	$\overline{WR}$	The rising edge of the $\overline{WR}$ signal latches the state of the address control lines and the enable line.
14 to 17	A3 to A0	Logic Control Input.
18	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19 to 26	S1 to S8	Source Terminal 1 to Source Terminal 8. These pins can be inputs or outputs.
27	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	D	Drain Terminal. This pin can be an input or an output.

Table 9. Truth Table (ADG426)

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	On switch
X	X	X	X	X	↓	1	Retains previous switch condition
X	X	X	X	X	X	0	None (address and enable latches cleared)
X	X	X	X	0	0	1	None
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

TYPICAL PERFORMANCE CHARACTERISTICS

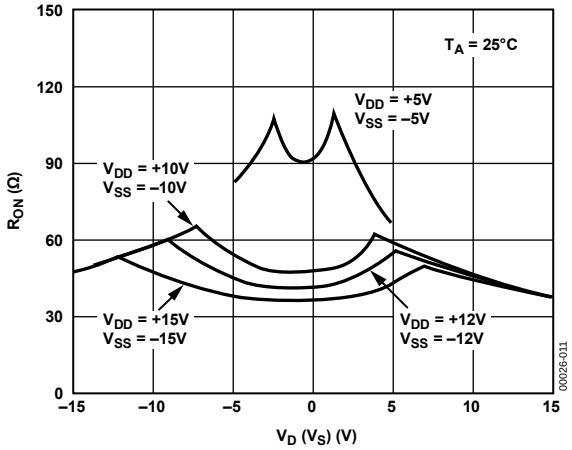


Figure 11. R_{ON} as a Function of V_D (V_S): Dual Supplies

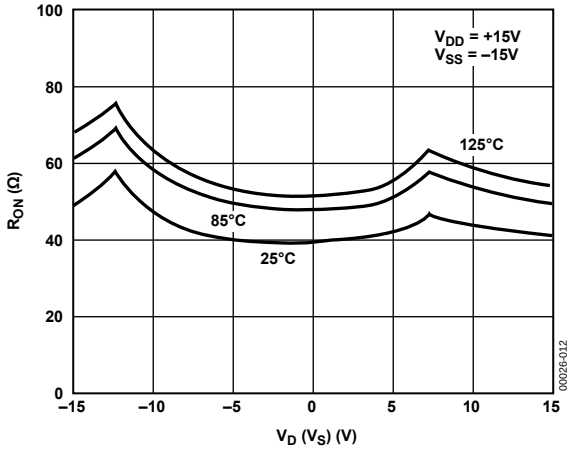


Figure 12. R_{ON} as a Function of V_D (V_S) for Different Temperatures

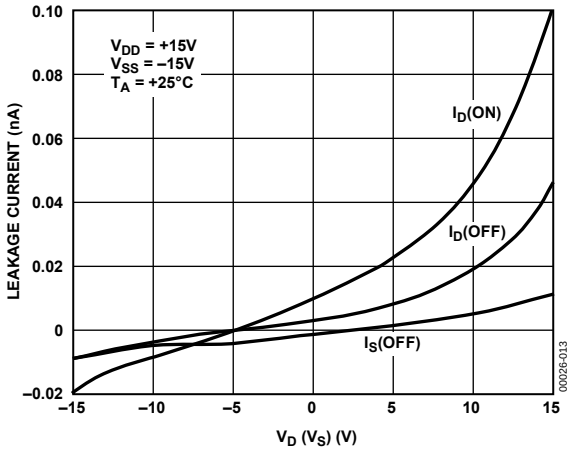


Figure 13. Leakage Currents as a Function of V_D (V_S)

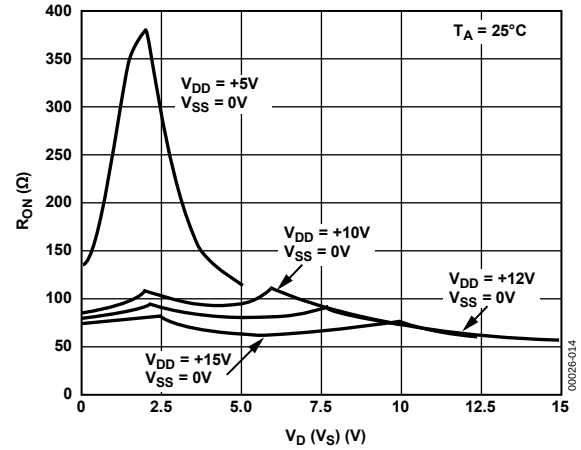


Figure 14. R_{ON} as a Function of V_D (V_S): Single Supplies

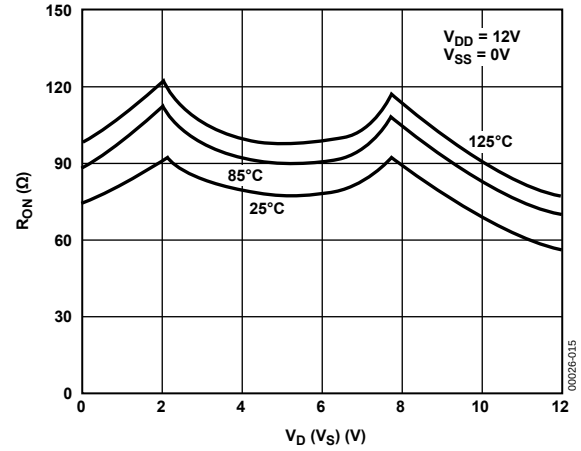


Figure 15. R_{ON} as a Function of V_D (V_S) for Different Temperatures

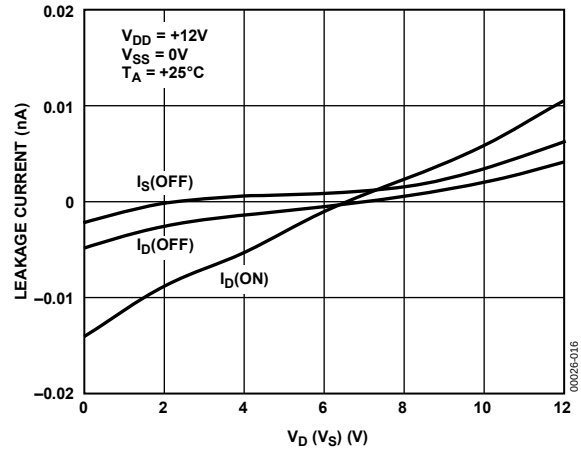


Figure 16. Leakage Currents as a Function of V_D (V_S)

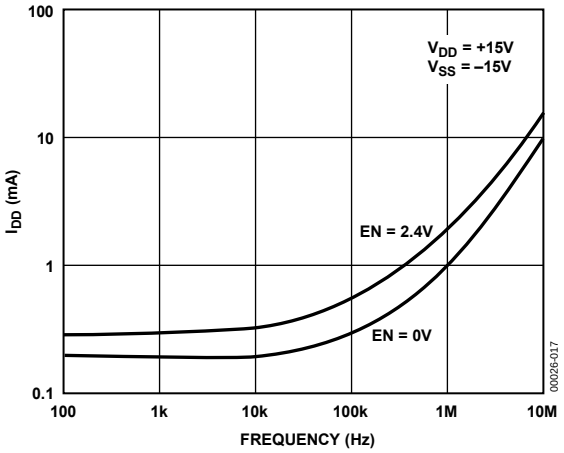


Figure 17. Positive Supply Current vs. Switching Frequency

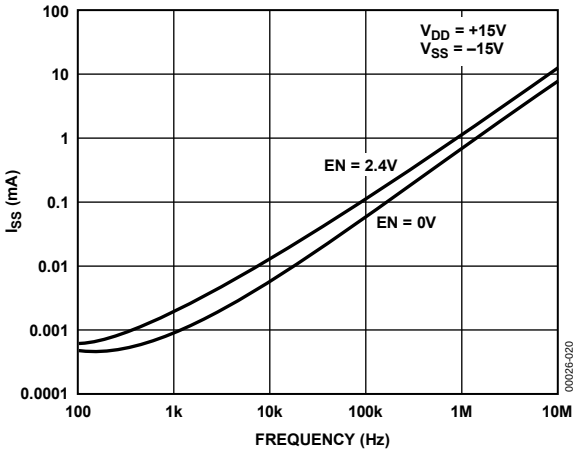


Figure 20. Negative Supply Current vs. Switching Frequency

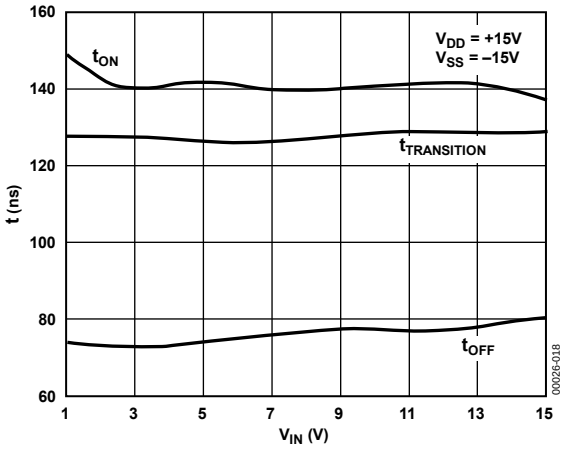


Figure 18. Switching Time vs. V_{IN} (Bipolar Supply)

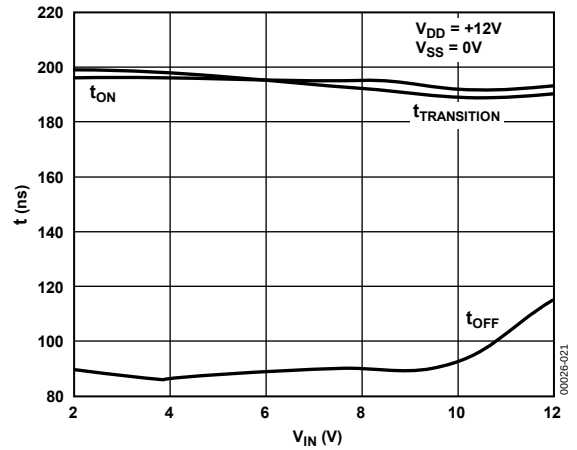


Figure 21. Switching Time vs. V_{IN} (Single Supply)

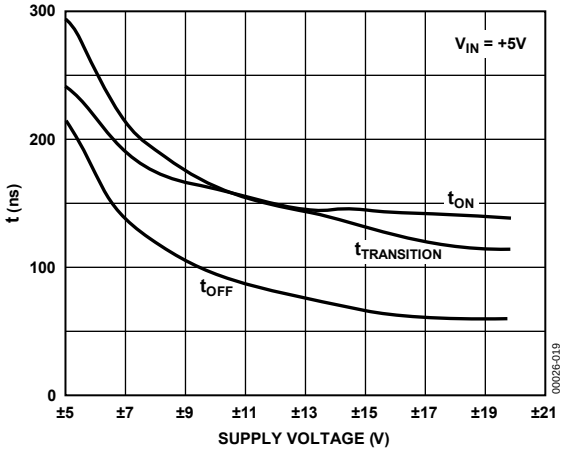


Figure 19. Switching Time vs. Bipolar Supply

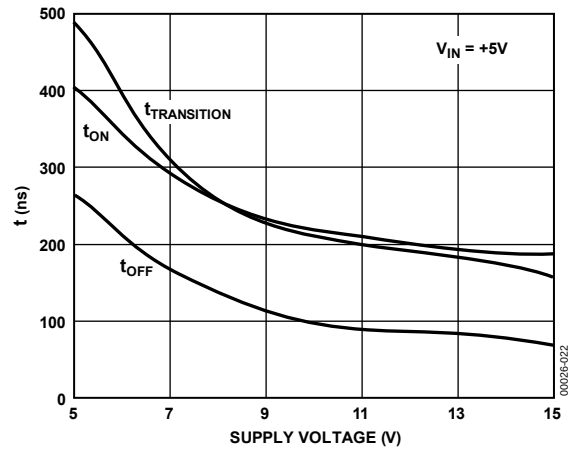


Figure 22. Switching Time vs. Single Supply

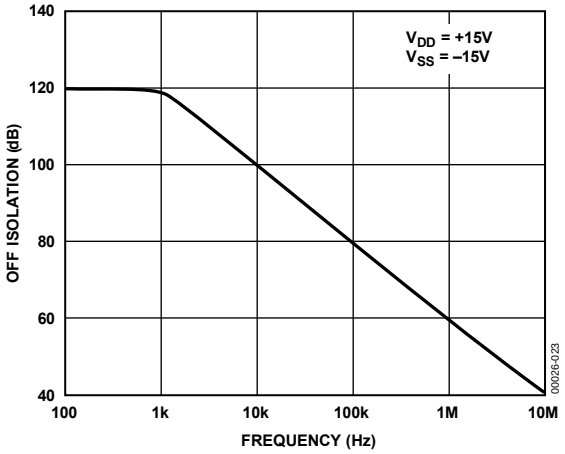


Figure 23. Off Isolation vs. Frequency

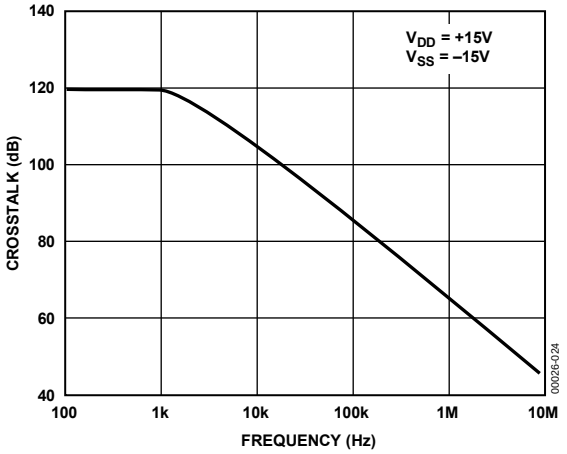


Figure 24. Crosstalk vs. Frequency

TEST CIRCUITS

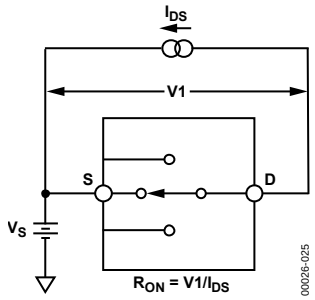


Figure 25. On Resistance

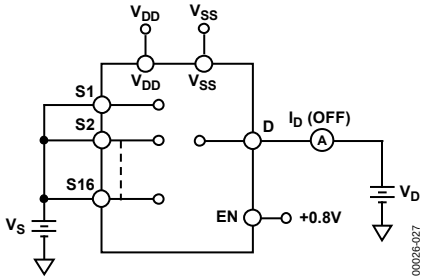


Figure 27. I_D (Off)

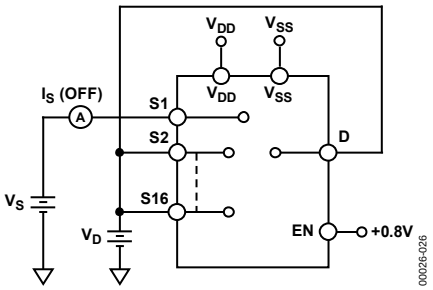


Figure 26. I_S (Off)

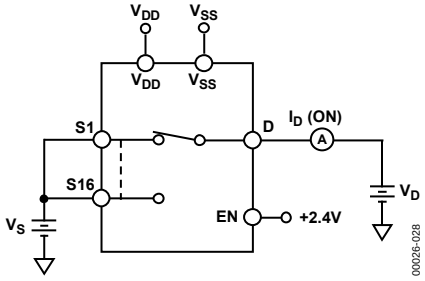
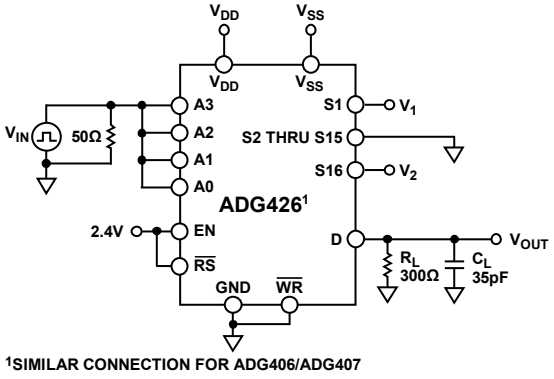


Figure 28. I_D (On)



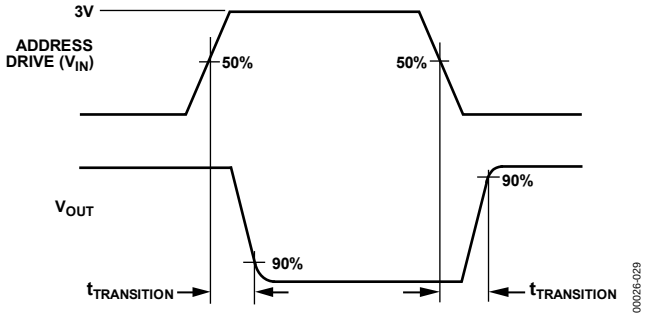
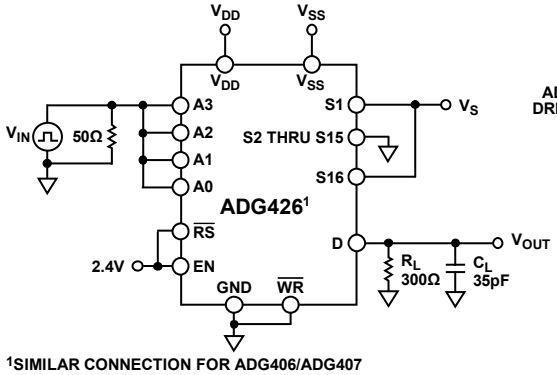


Figure 29. Switching Time of Multiplexer, $t_{TRANSITION}$



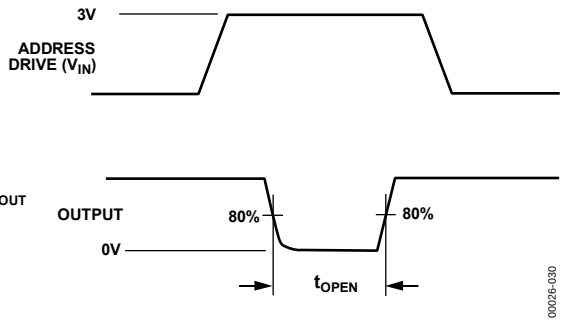


Figure 30. Break-Before-Make Delay, t_{OPEN}

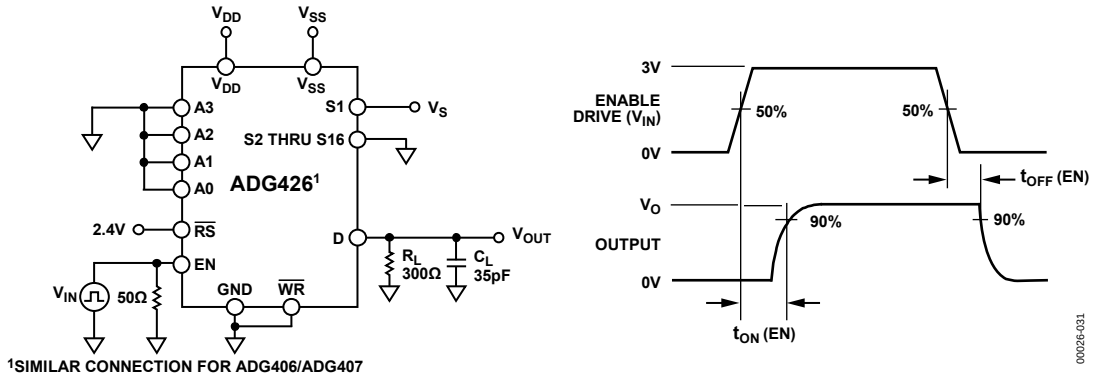


Figure 31. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

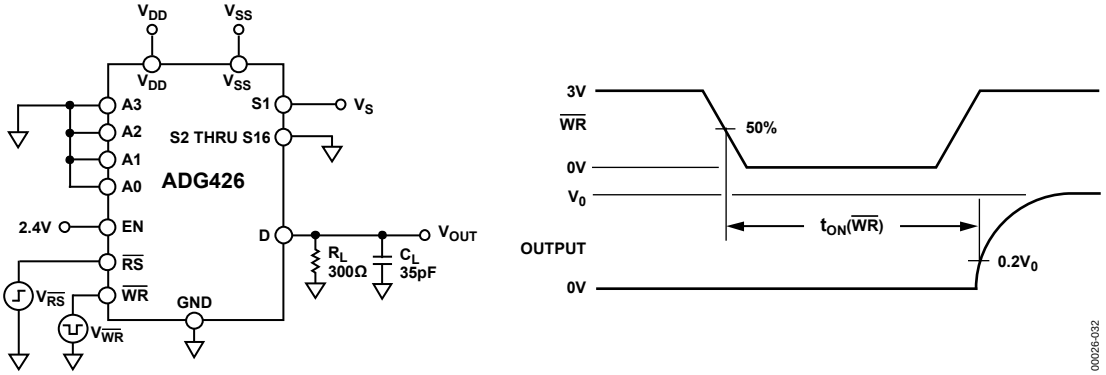


Figure 32. Write Turn-On Time, t_{ON} ($\overline{WR}$)

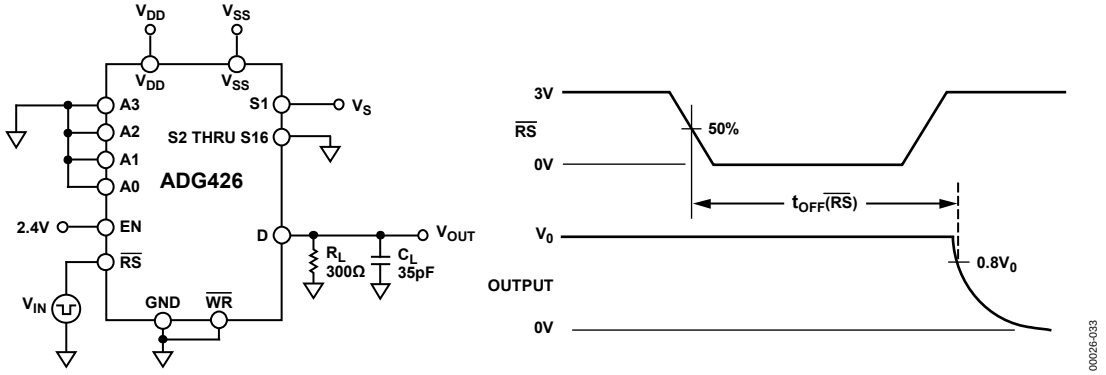
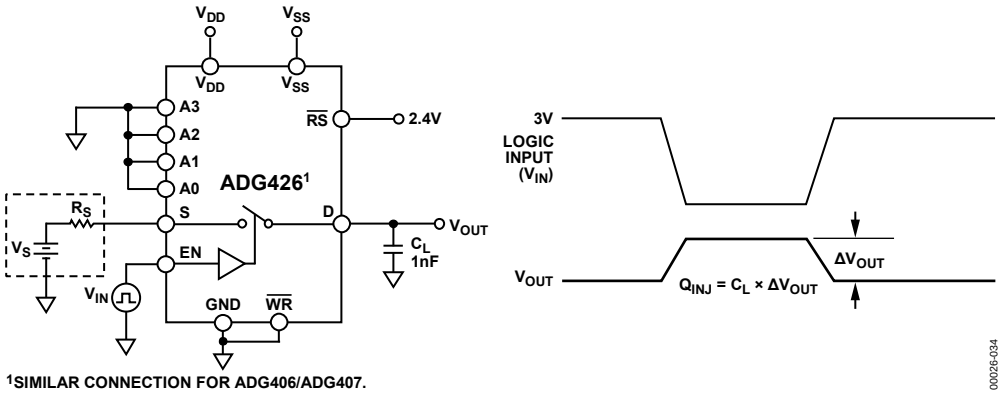
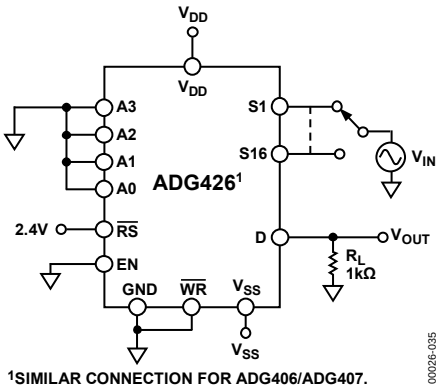


Figure 33. Reset Turn-Off Time, t_{OFF} ($\overline{RS}$)



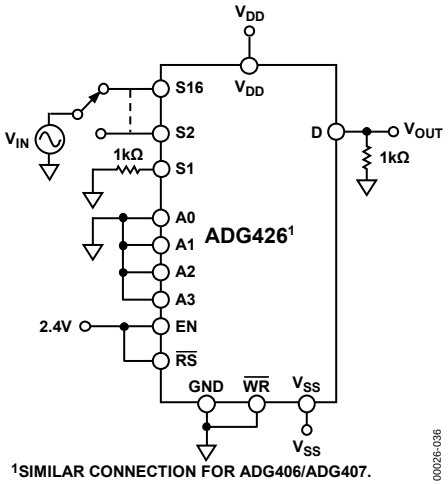
[1]SIMILAR CONNECTION FOR ADG406/ADG407.

Figure 34. Charge Injection



[1]SIMILAR CONNECTION FOR ADG406/ADG407.

Figure 35. Off Isolation



[1]SIMILAR CONNECTION FOR ADG406/ADG407.

Figure 36. Crosstalk

TERMINOLOGY

V_{DD}
Most positive power supply potential.

V_{SS}
Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.

GND
Ground (0 V) reference.

R_{ON}
Ohmic resistance between the D and S terminals.

R_{ON} Match

Difference between the R_{ON} of any two channels.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D, Terminal S.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (ON)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{OPEN}
Off time measured between 80% points of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

Crosstalk
A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

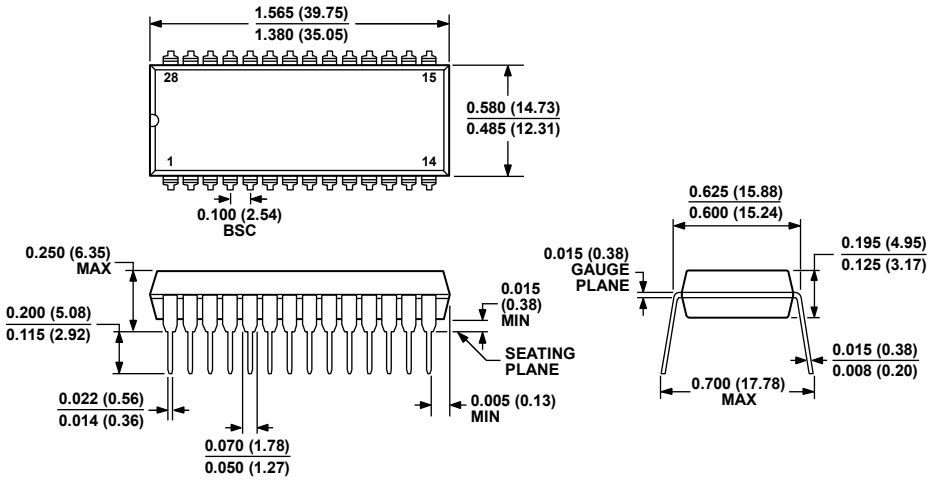
Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

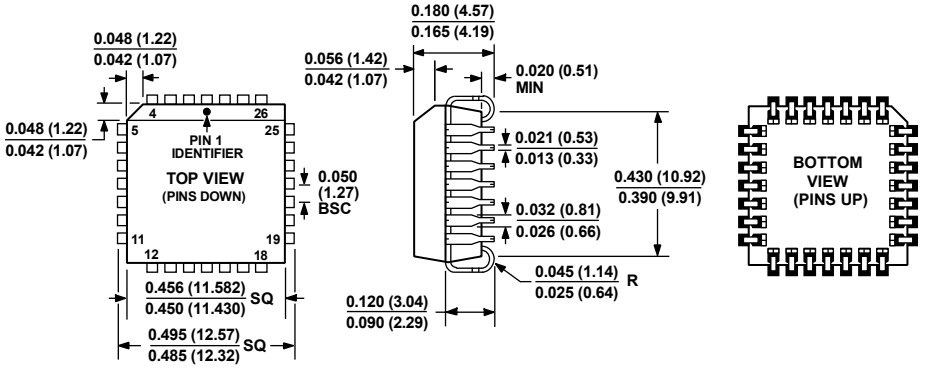
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-011
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE LEADS.

071006-A

Figure 37. 28-Lead Plastic Dual In-Line Package {PDIP}
Wide Body
(N-28-2)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

042508-A

Figure 38. 28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28)
Dimensions shown in inches and (millimeters)

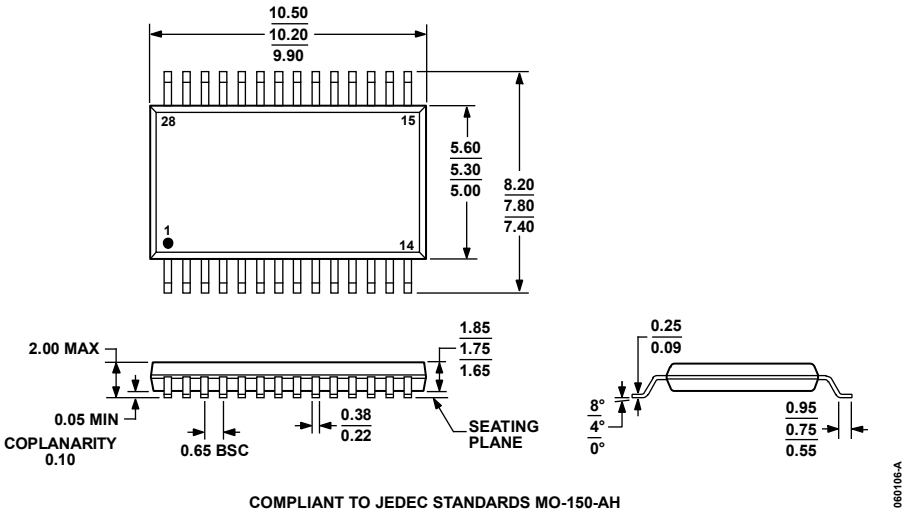


Figure 39. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
ADG406BN	−40°C to +85°C	28-Lead PDIP	N-28-2
ADG406BNZ	−40°C to +85°C	28-Lead PDIP	N-28-2
ADG406BP	−40°C to +85°C	28-Lead PLCC	P-28
ADG406BP-REEL	−40°C to +85°C	28-Lead PLCC	P-28
ADG406BPZ	−40°C to +85°C	28-Lead PLCC	P-28
ADG406BPZ-REEL	−40°C to +85°C	28-Lead PLCC	P-28
ADG407BN	−40°C to +85°C	28-Lead PDIP	N-28-2
ADG407BNZ	−40°C to +85°C	28-Lead PDIP	N-28-2
ADG407BP	−40°C to +85°C	28-Lead PLCC	P-28
ADG407BP-REEL	−40°C to +85°C	28-Lead PLCC	P-28
ADG407BPZ	−40°C to +85°C	28-Lead PLCC	P-28
ADG407BPZ-RL	−40°C to +85°C	28-Lead PLCC	P-28
ADG407BCHIPS	−40°C to +85°C		DIE
ADG426BN	−40°C to +85°C	28-Lead PDIP	N-28-2
ADG426BNZ	−40°C to +85°C	28-Lead PDIP	N-28-2
ADG426BRS	−40°C to +85°C	28-Lead SSOP	RS-28
ADG426BRS-REEL	−40°C to +85°C	28-Lead SSOP	RS-28
ADG426BRS-REEL7	−40°C to +85°C	28-Lead SSOP	RS-28
ADG426BRSZ	−40°C to +85°C	28-Lead SSOP	RS-28
ADG426BRSZ-REEL	−40°C to +85°C	28-Lead SSOP	RS-28

[1] Z = RoHS Compliant Part.
[2] N = Plastic DIP, P = Plastic Leaded Chip Carrier (PLCC), RS = Shrink Small Outline Package (SSOP).