Tiny, Low Power JFET-Input Op Amp

ADA4062-2

FEATURES

- **Low input bias current: 50 pA maximum**
- **Offset voltage**
  - **1.5 mV maximum for ADA4062-2 B grade**
  - **2.5 mV maximum for ADA4062-2 A grade**
- **Offset voltage drift: 4 µV/°C typical**
- **Slew rate: 3.3 V/µs typical**
- **CMRR: 90 dB typical**
- **Low supply current: 165 µA typical**
- **High input impedance**
- **Unity-gain stable**
- **Packaging: SOIC, MSOP**

APPLICATIONS

- **Power control and monitoring**
- **Active filters**
- **Industrial/process control**
- **Body probe electronics**
- **Data acquisition**
- **Integrators**
- **Input buffering**

GENERAL DESCRIPTION

The ADA4062-2 is a dual JFET-input amplifier with industry-leading performance. It offers lower power, offset voltage, drift and ultralow bias current. The ADA4062-2 B grade features typical low offset voltage of 0.5 mV, offset drift of 4 µV/°C, and bias current of 2 pA. The ADA4062-2 is ideal for various applications, including process control, industrial and instrumentation equipment, active filtering, data conversion, buffering, and power control and monitoring. With a low supply current of 165 µA per amplifier, it is also very well suited for lower power applications. The ADA4062-2 is specified for the extended industrial temperature range of −40°C to +125°C and is available in lead-free SOIC and MSOP packages.

PIN CONFIGURATIONS

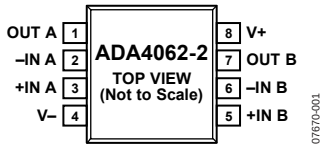

Figure 1. 8-Lead Narrow-Body SOIC

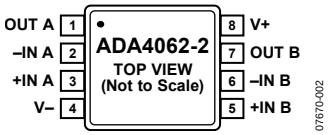

Figure 2. 8-Lead MSOP

Table 1. Low Power Op Amps

Supply	40 V	36 V	12 V to 16 V	5 V
Single	OP97	AD820	AD8641 AD8663	AD8541
Dual	OP297	OP282 AD8682 AD822	AD8642 AD8667	AD8542
Quad	OP497	OP482 AD8684 AD824	AD8643 AD8669	AD8544

Rev. 0

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REVISION HISTORY

10/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
B Grade				0.5	1.5	mV
		−40°C ≤ T_A ≤ +125°C			3	mV
A Grade				0.75	2.5	mV
		−40°C ≤ T_A ≤ +125°C			5	mV
Input Bias Current	I_B			2	50	pA
		−40°C ≤ T_A ≤ +125°C			5	nA
Input Offset Current	I_{OS}			0.5	25	pA
		−40°C ≤ T_A ≤ +125°C			2.5	nA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	−11.5		+15	V
Common-Mode Rejection Ratio	CMRR					
B Grade		V_{CM} = −11.5 V to +11.5 V	80	90		dB
		−40°C ≤ T_A ≤ +125°C	80			dB
A Grade		V_{CM} = −11.5 V to +11.5 V	74	90		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −10 V to +10 V	76	83		dB
		−40°C ≤ T_A ≤ +125°C	72			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		4		µV/°C
Input Resistance	R_{IN}			10		TΩ
Input Capacitance, Differential Mode	C_{INDM}			1.5		pF
Input Capacitance, Common Mode	C_{INCM}			4.8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	13	13.5		V
		−40°C ≤ T_A ≤ +125°C	12.5			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−13.8	−13	V
		−40°C ≤ T_A ≤ +125°C			−12.5	V
Short-Circuit Current	I_{SC}			20		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR					
B Grade		V_{SY} = ±4 V to ±18 V	80	90		dB
		−40°C ≤ T_A ≤ +125°C	80			dB
A Grade		V_{SY} = ±4 V to ±18 V	74	90		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		165	200	µA
		−40°C ≤ T_A ≤ +125°C			220	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = 1		3.3		V/µs
Settling Time	t_S	To 0.01%, V_{IN} = 2 V step, C_L = 100 pF, R_L = 5 kΩ, A_V = 1		3.5		µs
Gain Bandwidth Product	GBP	R_L = 10 kΩ, A_V = 1		1.4		MHz
Phase Margin	Φ_M	R_L = 10 kΩ, A_V = 1		80		Degrees
Channel Separation	CS	f = 10 kHz		130		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		5		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$\pm V_{SY}$
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. It was measured using a standard 2-layer board.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	158	43	°C/W
8-Lead MSOP	210	45	°C/W

POWER SEQUENCING

The op amp supply voltages must be established simultaneously with, or before, any input signals are applied. If this is not possible, the input current must be limited to 10 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

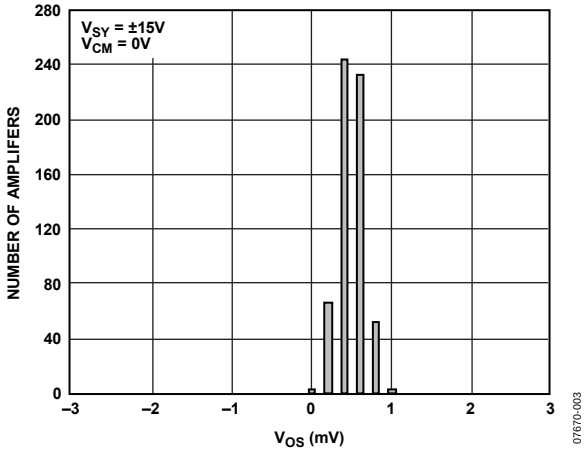


Figure 3. Input Offset Voltage Distribution

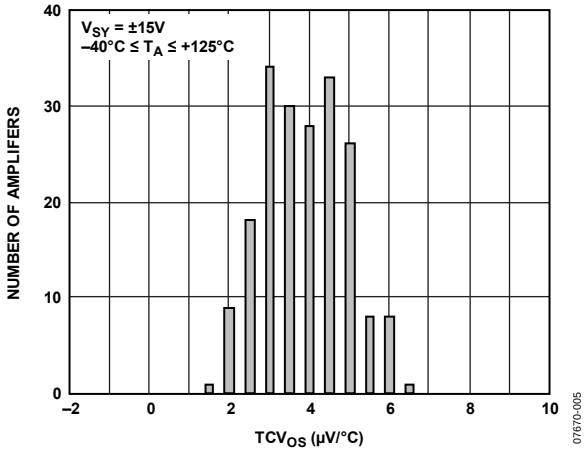


Figure 4. Input Offset Voltage Drift Distribution

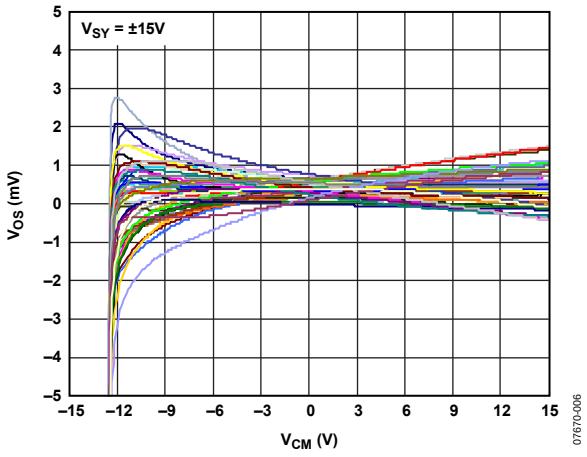


Figure 5. Input Offset Voltage vs. Common-Mode Voltage

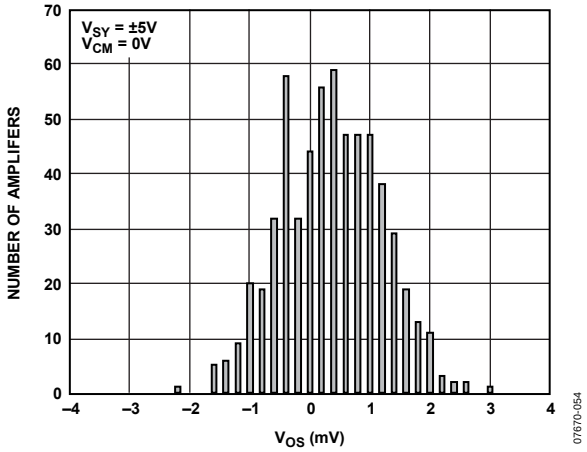


Figure 6. Input Offset Voltage Distribution

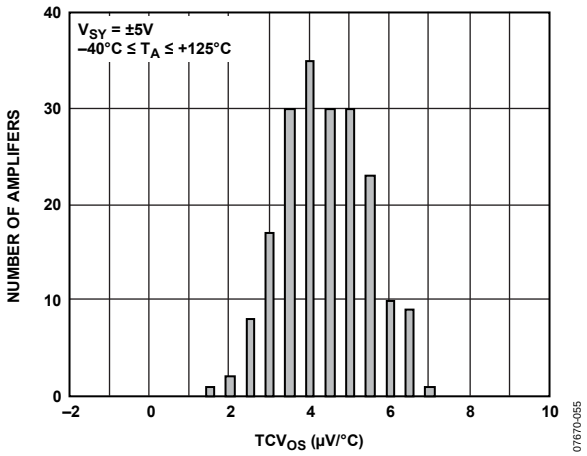
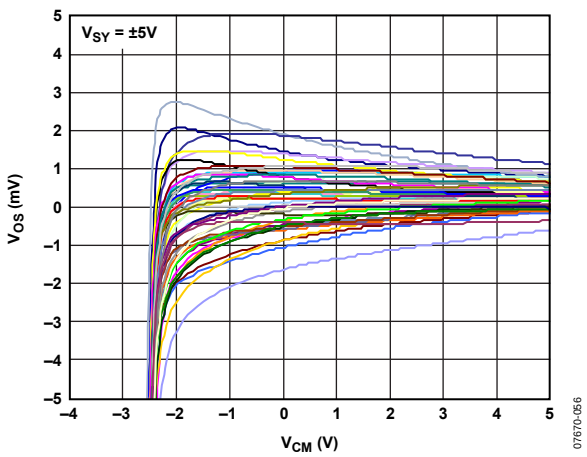


Figure 7. Input Offset Voltage Drift Distribution



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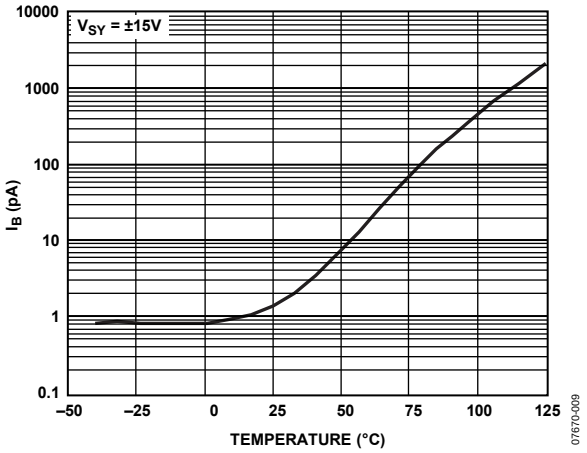


Figure 9. Input Bias Current vs. Temperature

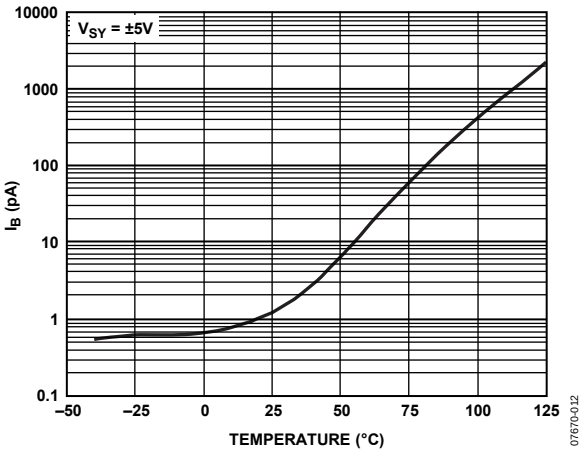


Figure 12. Input Bias Current vs. Temperature

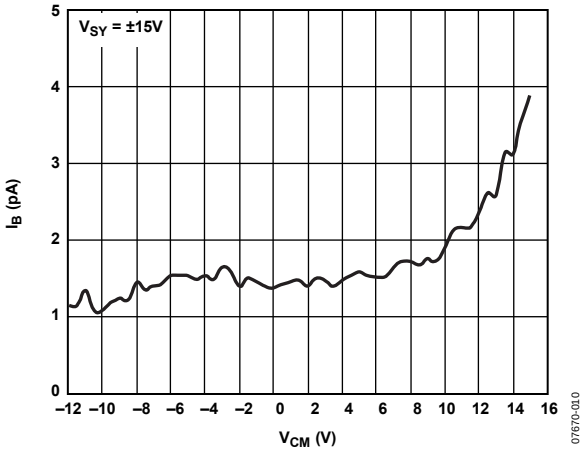


Figure 10. Input Bias Current vs. Input Common-Mode Voltage

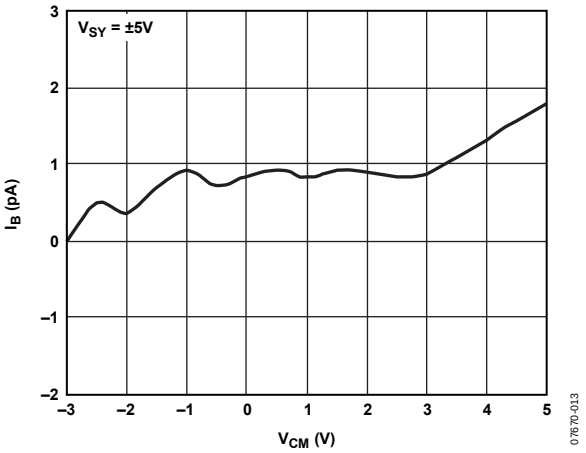


Figure 13. Input Bias Current vs. Input Common-Mode Voltage

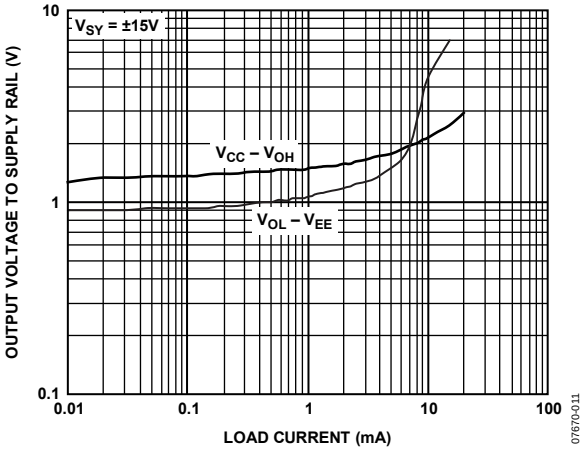
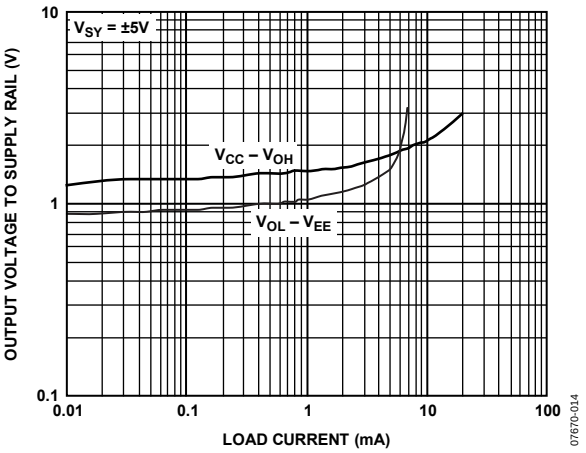


Figure 11. Output Voltage to Supply Rail vs. Load Current



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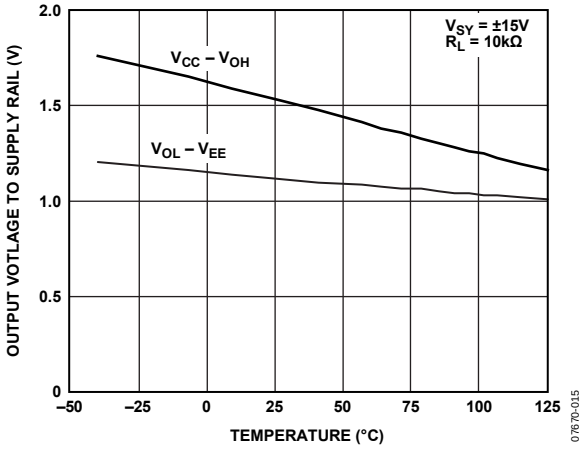

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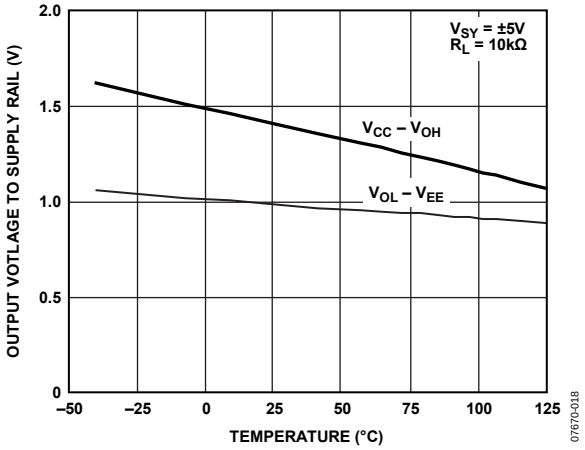

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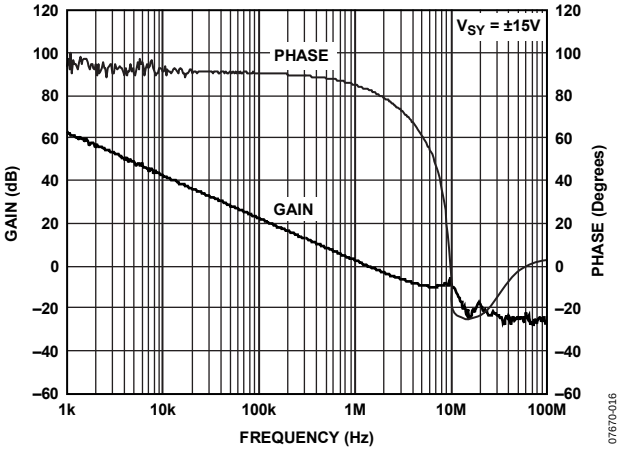
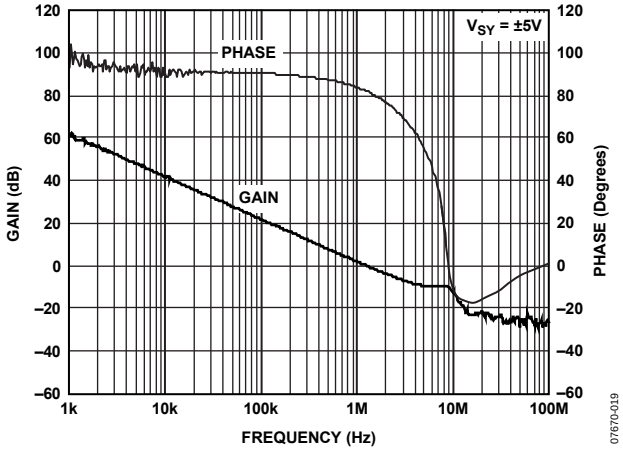


Figure 16. Open-Loop Gain and Phase vs. Frequency



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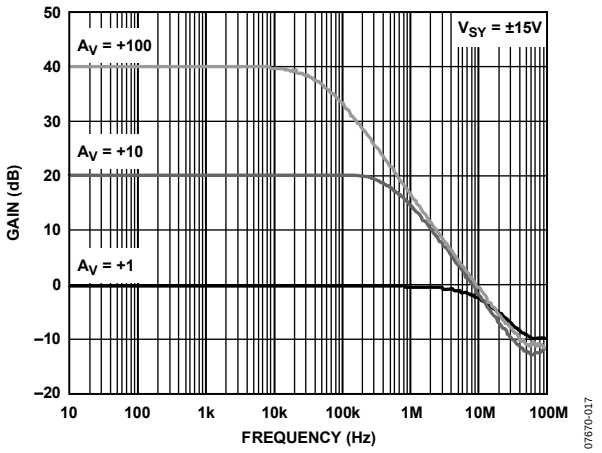

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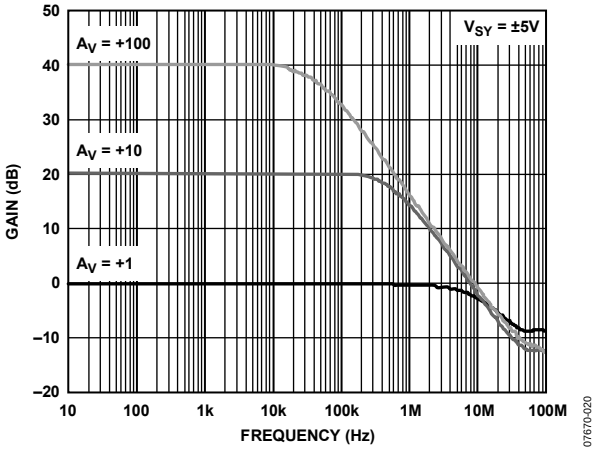


Figure 20. Closed-Loop Gain vs. Frequency

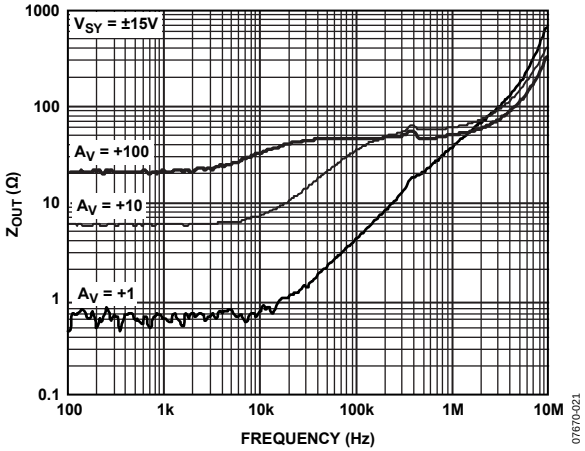
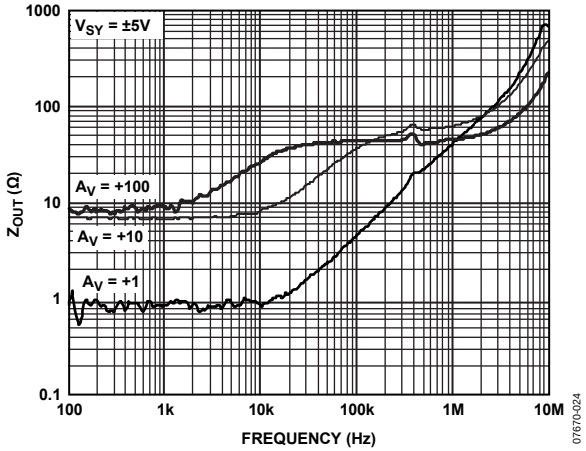


Figure 21. Output Impedance vs. Frequency



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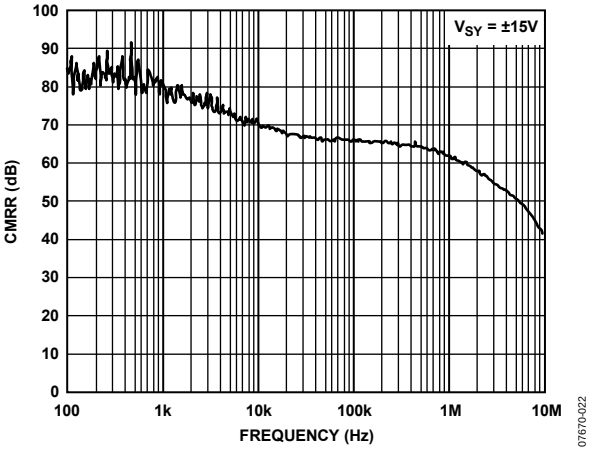


Figure 22. CMRR vs. Frequency

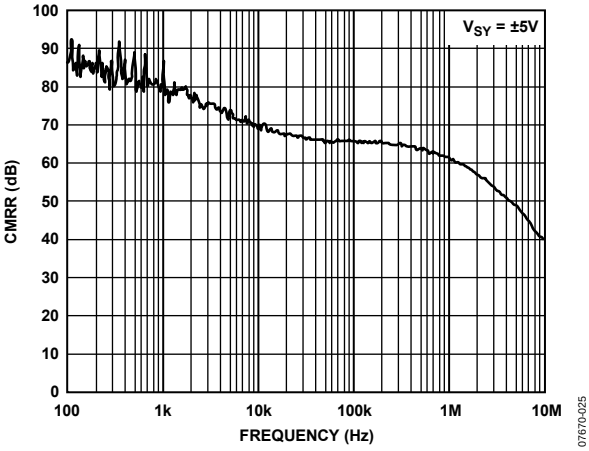


Figure 25. CMRR vs. Frequency

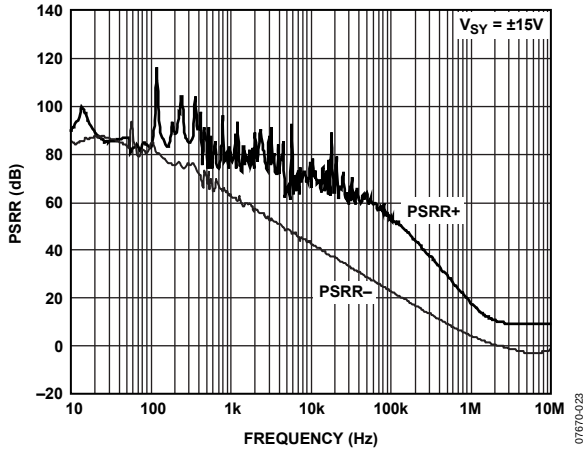


Figure 23. PSRR vs. Frequency

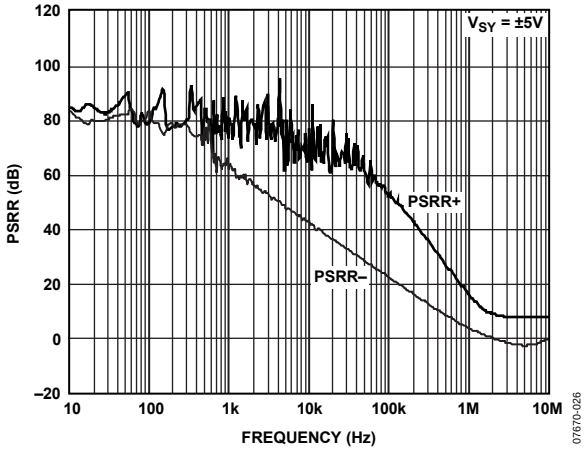


Figure 26. PSRR vs. Frequency

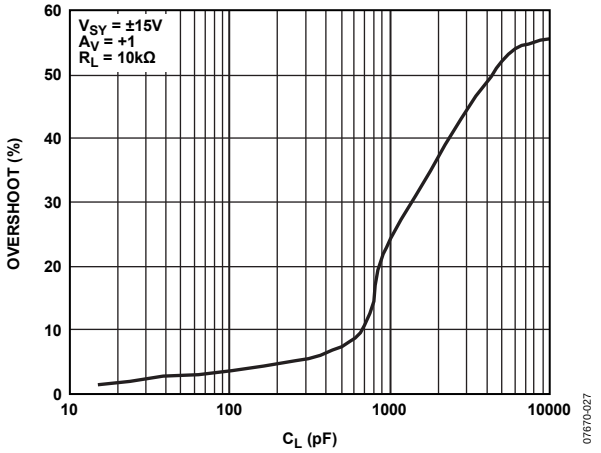


Figure 27. Small-Signal Overshoot vs. Load Capacitance

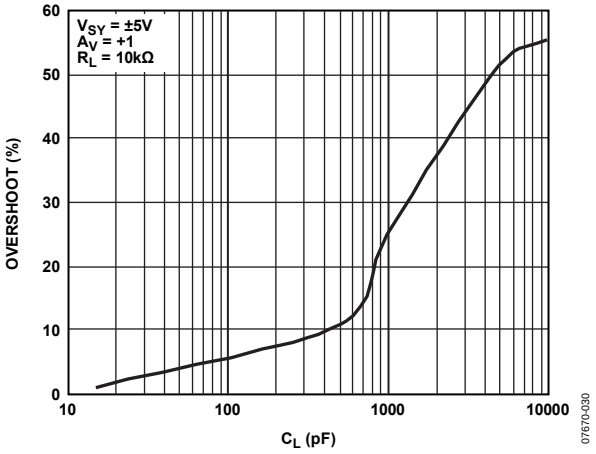


Figure 30. Small-Signal Overshoot vs. Load Capacitance

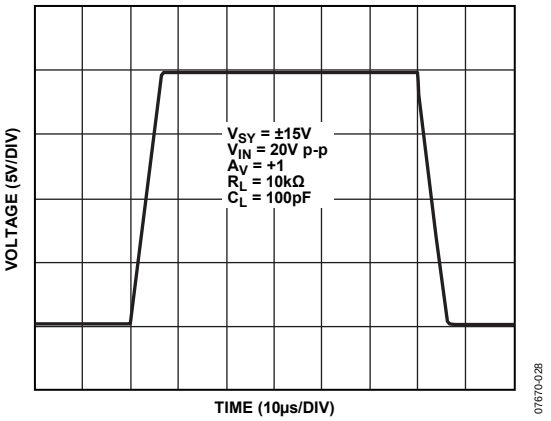


Figure 28. Large-Signal Transient Response

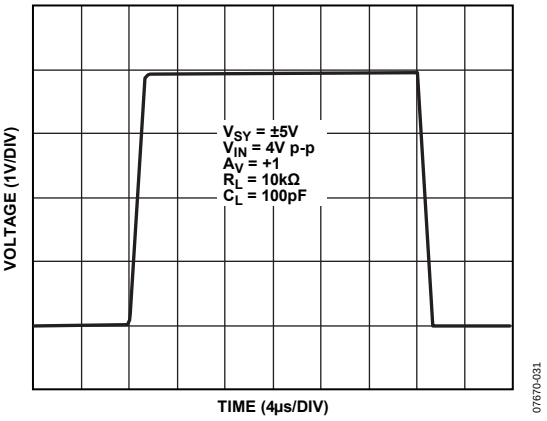


Figure 31. Large-Signal Transient Response

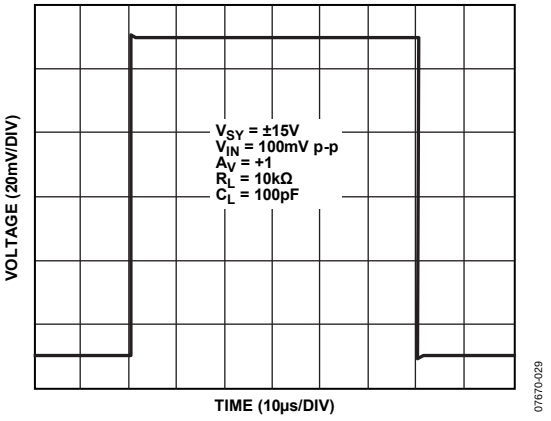


Figure 29. Small-Signal Transient Response

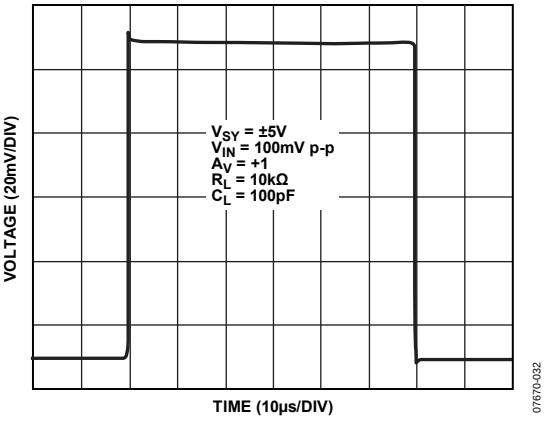


Figure 32. Small-Signal Transient Response

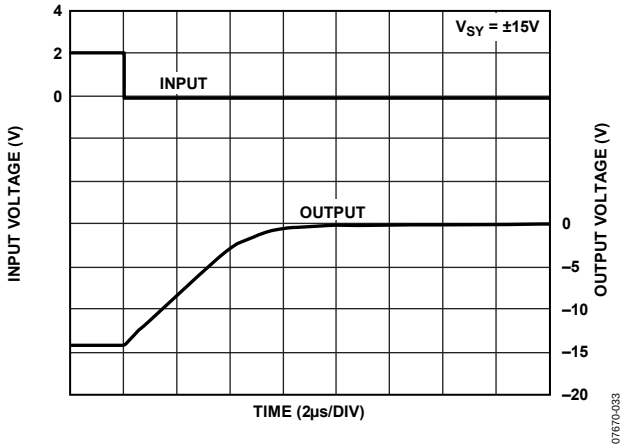


Figure 33. Negative Overload Recovery

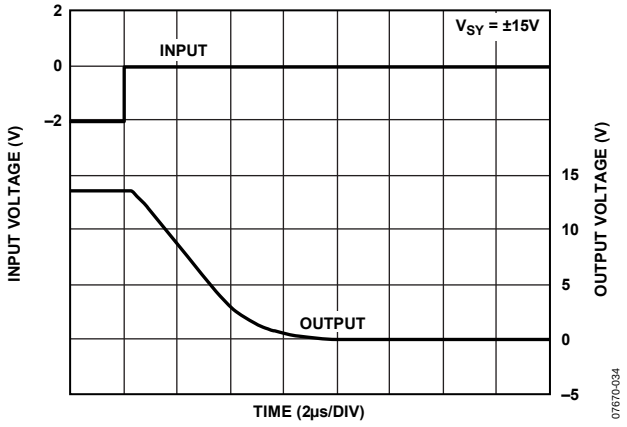


Figure 34. Positive Overload Recovery

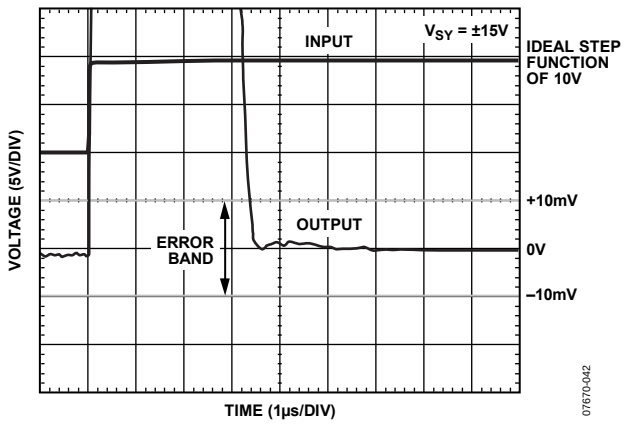


Figure 35. Positive Settling Time to 0.01%

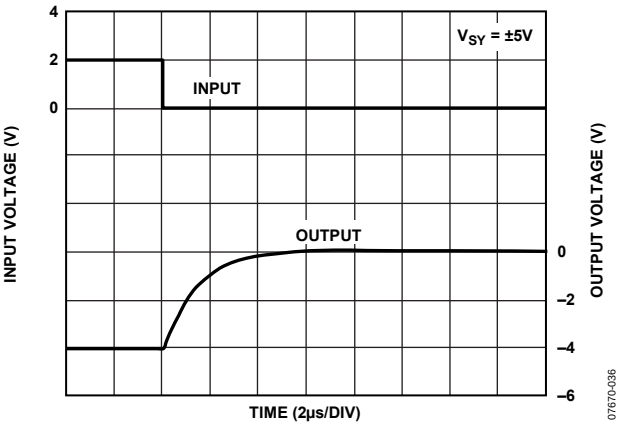


Figure 36. Negative Overload Recovery

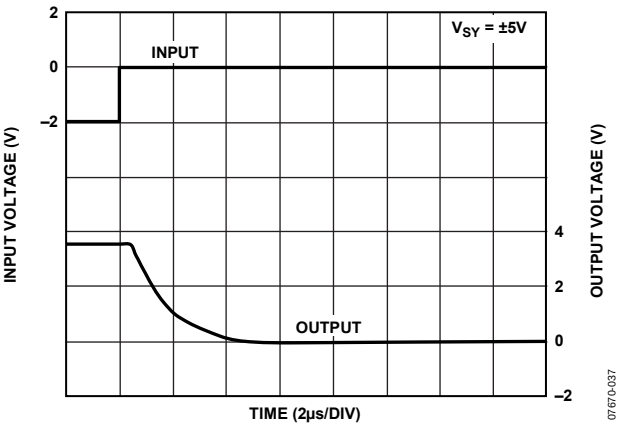
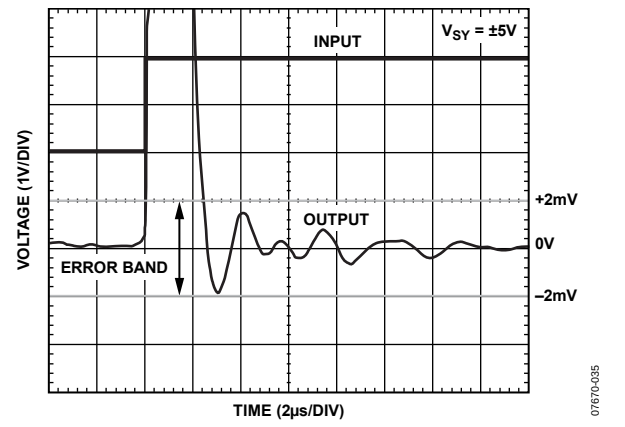


Figure 37. Positive Overload Recovery



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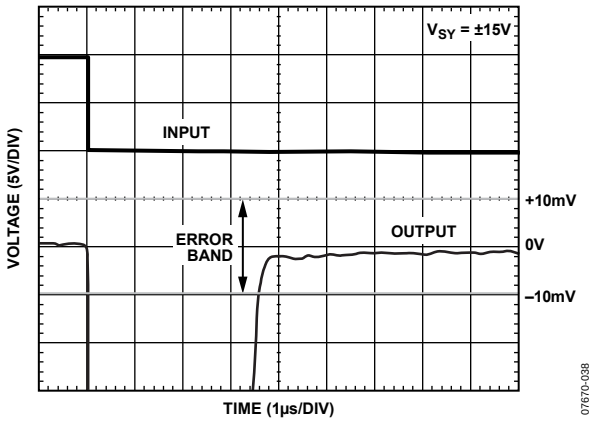


Figure 39. Negative Settling Time to 0.01%

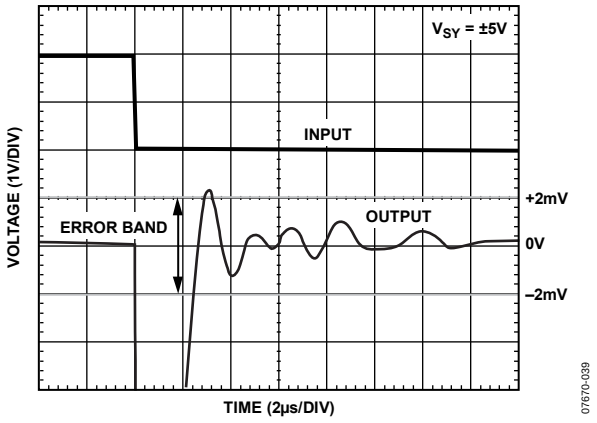


Figure 42. Negative Settling Time to 0.01%

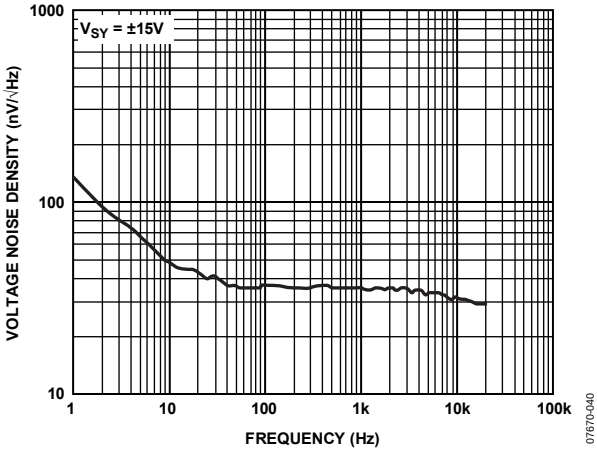


Figure 40. Voltage Noise Density

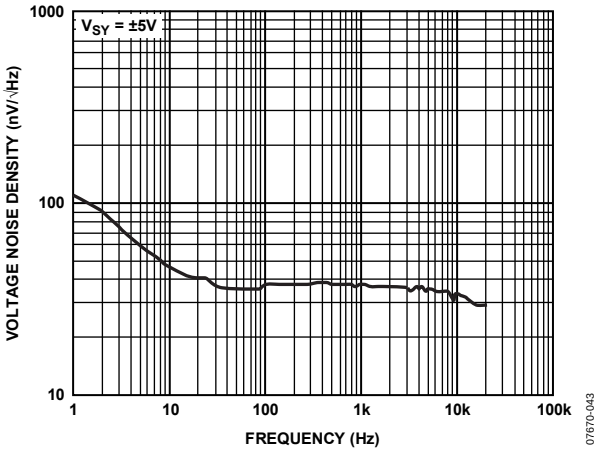


Figure 43. Voltage Noise Density

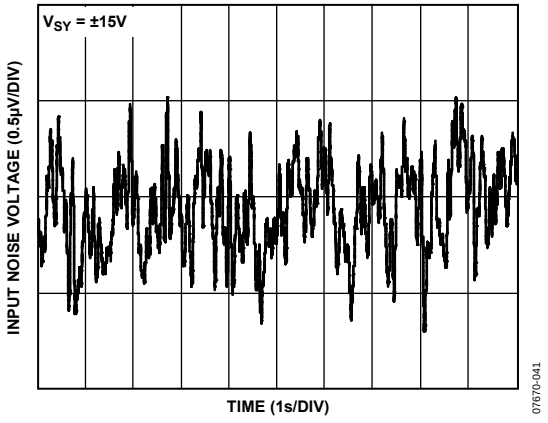


Figure 41. 0.1 Hz to 10 Hz Noise

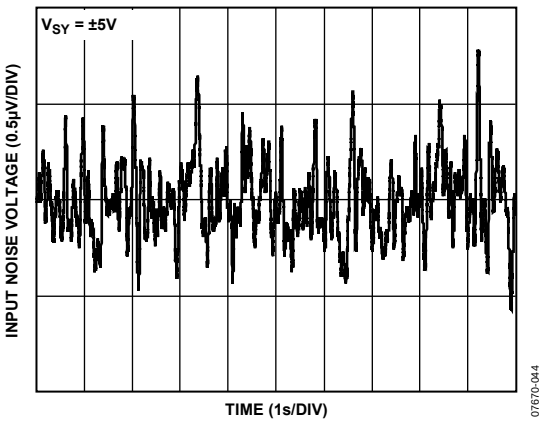


Figure 44. 0.1 Hz to 10 Hz Noise

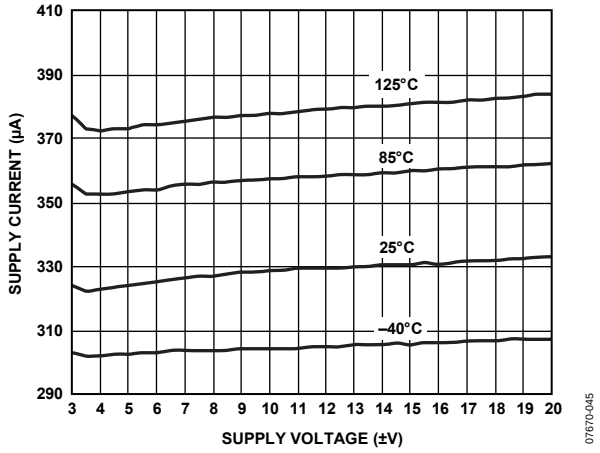


Figure 45. Supply Current vs. Supply Voltage

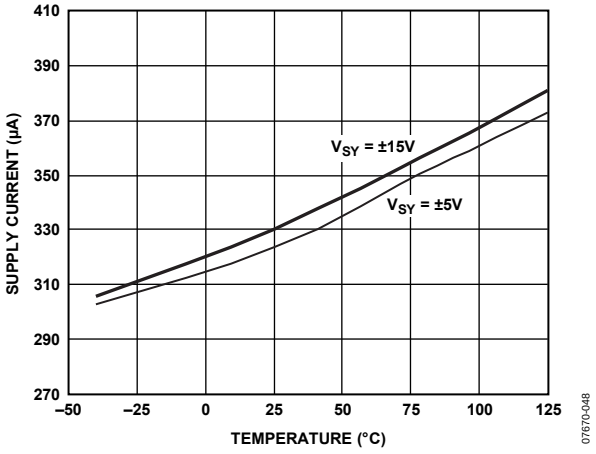


Figure 48. Supply Current vs. Temperature

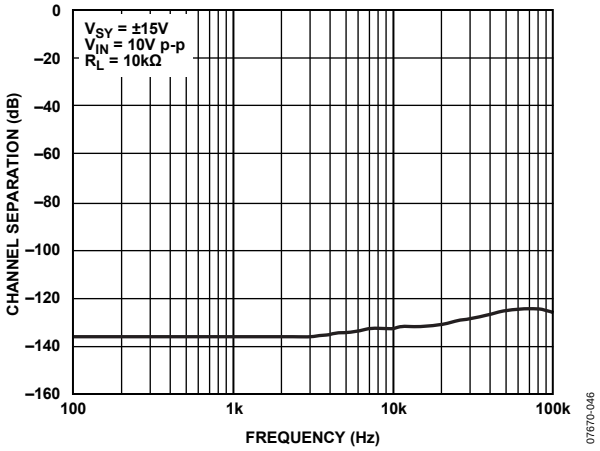


Figure 46. Channel Separation vs. Frequency

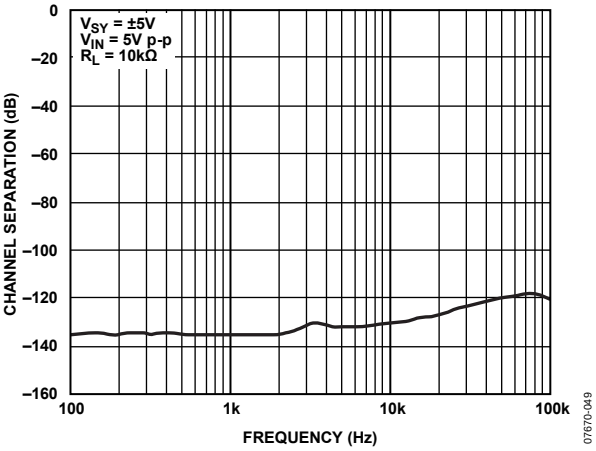


Figure 49. Channel Separation vs. Frequency

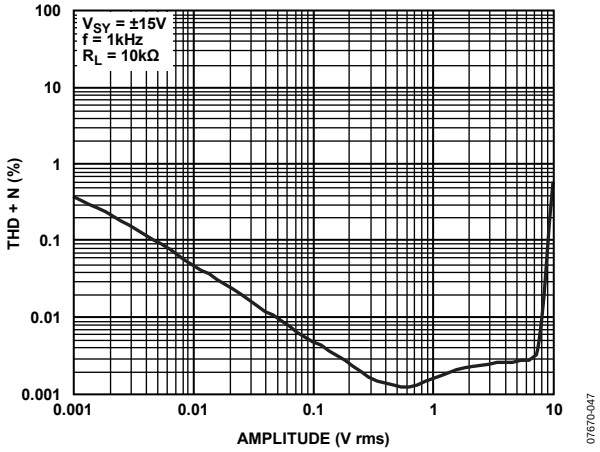


Figure 47. THD + N vs. Amplitude

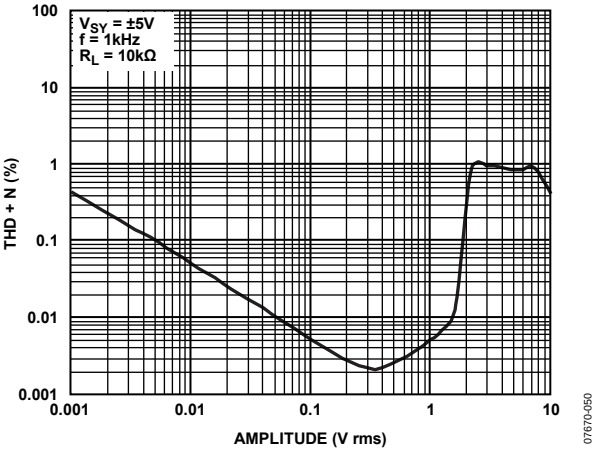


Figure 50. THD + N vs. Amplitude

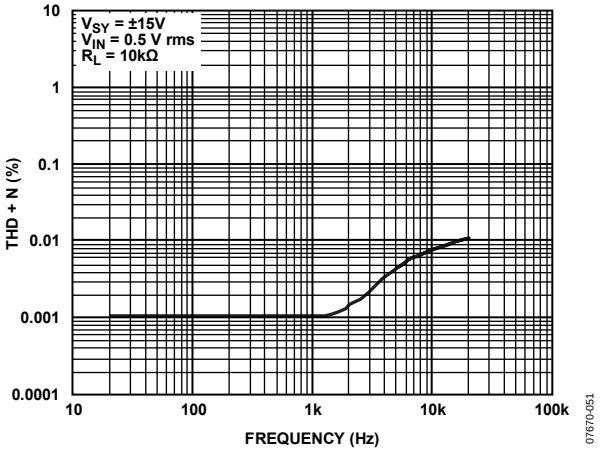


Figure 51. THD + N vs. Frequency

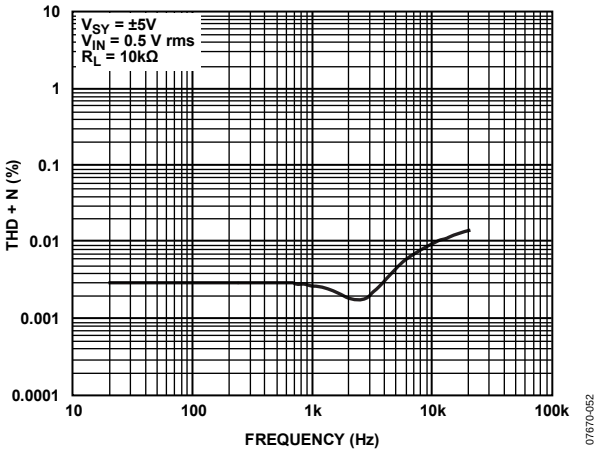


Figure 52. THD + N vs. Frequency

APPLICATIONS INFORMATION

NOTCH FILTER

A notch filter rejects a specific interfering frequency and can be implemented using a single op amp. Figure 53 shows a 60 Hz notch filter that uses the twin T network with the ADA4062-2 configured as a voltage follower. The ADA4062-2 works as a buffer that provides high input resistance and low output impedance. The low bias current (2 pA typical) and high input resistance (10 TΩ typical) of the ADA4062-2 enable large resistors and small capacitors to be used.

Alternatively, different combinations of resistors and capacitors values can be used to achieve the desired notch frequency. However, the major drawback to this circuit topology is the need to ensure that all the resistors and capacitors be closely matched. If they are not closely matched, the notch frequency offset and drift cause the circuit to attenuate at a frequency other than the ideal notch frequency.

Therefore, to achieve the desired performance, 1% or better component tolerances are usually required. In addition, a notch filter requires an op amp with a bandwidth of at least 100 to 200 times the center frequency. Hence, using the ADA4062-2 with a bandwidth of 1.4 MHz is excellent for a 60 Hz notch filter. Figure 54 shows the gain of the notch filter with respect to frequency. At 60 Hz, the notch filter has about 50 dB attenuation of signal.

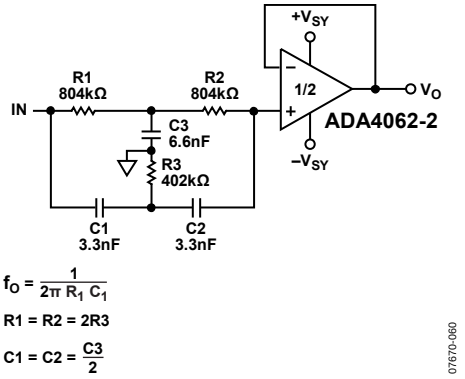


Figure 53. Notch Filter Circuit

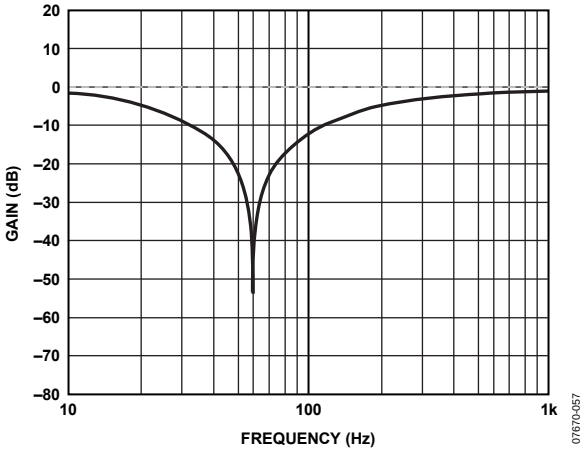


Figure 54. Notch Filter: Gain vs. Frequency

HIGH-SIDE SIGNAL CONDITIONING

There are many applications that require the sensing of signals near the positive rail. The ADA4062-2 can be used in high-side current sensing applications. Figure 55 shows a high-side signal conditioning circuit using the ADA4062-2. The ADA4062-2 has an input common-mode range that includes the positive supply ($-11.5\ V \le V_{CM} \le +15\ V$). In the circuit, the voltage drop across a low value resistor, such as the 0.1 Ω shown in Figure 55, is amplified by a factor of 5 using the ADA4062-2.

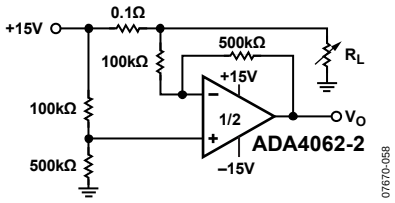


Figure 55. High-Side Signal Conditioning

MICROPOWER INSTRUMENTATION AMPLIFIER

The ADA4062-2 is a dual amplifier and is perfectly suited for applications that require lower supply currents. For supply voltages of ±15 V, the supply current per amplifier is 165 μA typical. The ADA4062-2 also offers a typical low offset voltage drift of 4 μV/°C and a very low bias current of 2 pA, which makes it well suited for instrumentation amplifiers.

Figure 56 shows the classic 2-op-amp instrumentation amplifier with four resistors using the ADA4062-2. The key to high CMRR for this instrumentation amplifier are resistors that are well matched to both the resistive ratio and relative drift. For true difference amplification, matching of the resistor ratio is very important, where R3/R4 = R1/R2. Assuming perfectly matched resistors, the gain of the circuit is 1 + R2/R1, which is approximately 100. Tighter matching of two op amps in one package, as is the case with the ADA4062-2, offers a significant boost in performance over the 3-op-amp configuration. Overall, the circuit only requires about 330 μA of supply current.

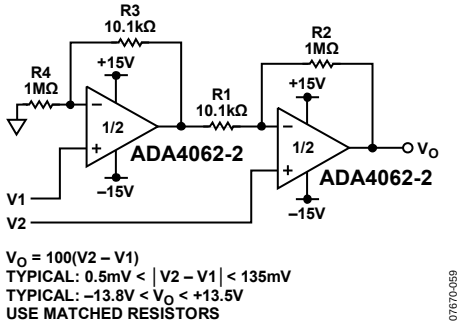


Figure 56. Micropower Instrumentation Amplifier

PHASE REVERSAL

Phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. When the voltage driving the input to these amplifiers exceeds the maximum input common-mode voltage range, the output of the amplifiers changes polarity.

Most JFET input amplifiers have phase reversal if either input exceeds the input common-mode range.

For the ADA4062-2, the output does not phase reverse if one or both of the inputs exceeds the input voltage range but stays below the positive supply rail and 0.5 V above the negative supply rail. With a supply voltage of ±15 V, phase reversal occurs when the input voltage is a negative signal greater than −14.5 V. This is due to saturation of the input stage leading to forward biasing of the gate-drain diode. Phase reversal in ADA4062-2 can be prevented by using a Schottky diode to clamp the input terminals to each other. In the simple buffer circuit in Figure 57, D1 protects the op amp against phase reversal and R limits the input current that flows into the op amp.

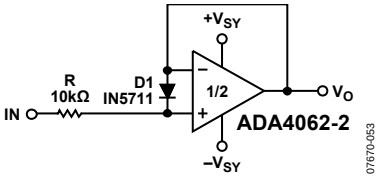


Figure 57. Phase Reversal Solution Circuit

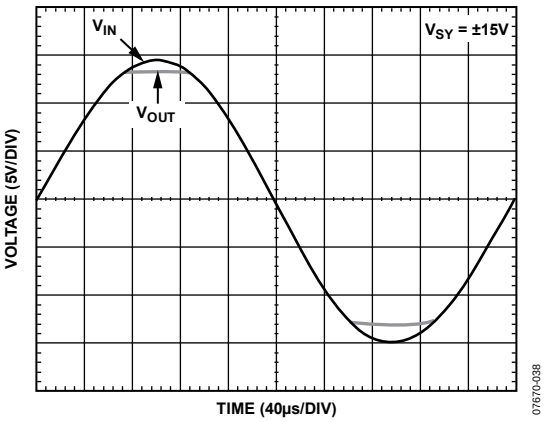


Figure 58. No Phase Reversal

SCHEMATIC

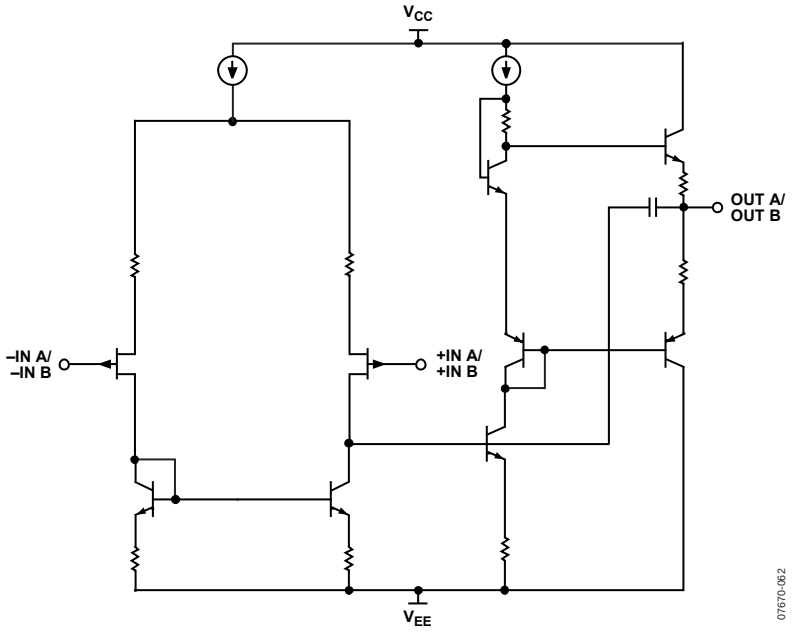
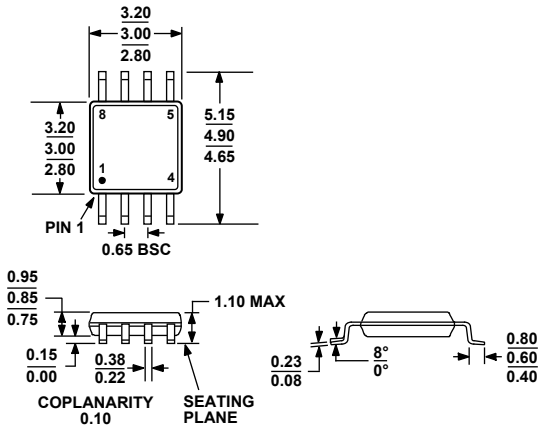


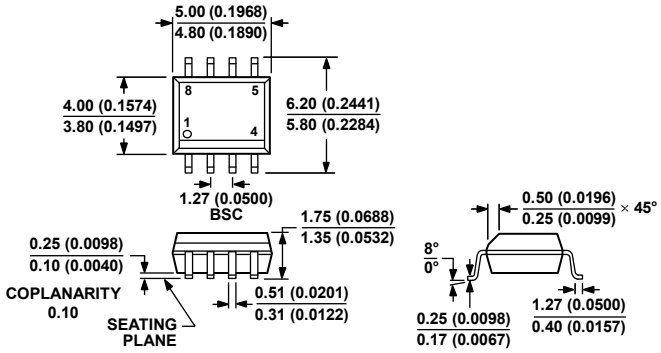
Figure 59. Simplified Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 60. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 61. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADA4062-2ARMZ[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A25
ADA4062-2ARMZ-RL[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A25
ADA4062-2ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2ARZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2ARZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2BRZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2BRZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4062-2BRZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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