ANALOG DEVICES

Xstream™ 6.25 Gbps, 4 × 4, Digital Crosspoint Switch with EQ

AD8156

FEATURES

4 × 4, fully differential, nonblocking array
Configurable for dual 2 × 2 operation
DC to 6.25 Gbps per channel, NRZ data rate
Programmable input equalization compensates for over 40"
   of FR-4 at 6.25 Gbps
Multicast and broadcast modes of operation
Programmable output swing
   100 mV p-p to 1.6 V p-p differential
Power supply: 3.3 V (±10%)
Low power
   No EQ: 400 mW typical
   Maximum EQ: 700 mW typical
Inputs: ac-coupled or dc-coupled
Wide set of dc-coupled input standards
   3.3 V/2.5 V/1.8 V CML or 3.3 V LVPECL
Control: LVTTL- or LVCMOS-compatible
Low additive jitter: 25 ps p-p typical
Low random jitter: 0.8 ps rms
Integrated 50 Ω termination impedance at inputs/outputs
Individual output disable for power savings
49-ball, 8 mm × 8 mm BGA, 1 mm pitch

APPLICATIONS

Backplane equalization
SONET/SDH
Gigabit Ethernet
XAUI
Fibre Channel

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The AD8156, a member of the Xstream line of products, is a high speed, fully differential, digital crosspoint switch. The part can function as a 4 × 4 crosspoint switch with double-latched memory, allowing simultaneous updates, or as a dual 2 × 2 with direct output control. The AD8156 has low power dissipation, typically 700 mW on 3.3 V with all outputs and input equalizers active. It operates at any data rate from dc to 6.25 Gbps per port.

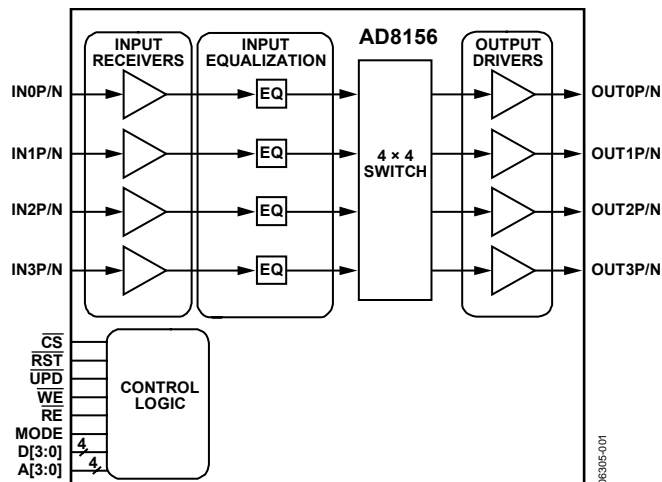Each input channel on the AD8156 has a programmable input equalizer to compensate for signal loss over a backplane.

The AD8156 high speed inputs are compatible with both ac-coupled and dc-coupled 3.3 V, 2.5 V, or 1.8 V CML, as well as 3.3 V LVPECL data levels. The control interface is LVTTL- and LVCMOS-compatible at 3.3 V. All input and output termination resistors are integrated for ease of layout and to minimize impedance mismatch. Input equalization and unused outputs can be individually disabled to minimize power dissipation.

The AD8156 is packaged in a 49-ball, 8 mm × 8 mm, BGA package with a 1 mm ball pitch. It operates over the industrial temperature range of −40°C to 85°C.

AD8156

TABLE OF CONTENTS

REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

$V_{TTI} = V_{TTO} = V_{CC} = 3.3$ V, $V_{EE} = 0$ V, $R_L = 50$ Ω, differential output swing = 800 mV, ac-coupled, data rate = 6.25 Gbps, PRBS $2^{23}-1$, $V_{IN} = 1$ V p-p differential, $T_A = 25°C$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Maximum Data Rate		NRZ data	6.25			Gbps
Deterministic Jitter		Data date < 6.25 Gbps		25		ps p-p
Random Jitter				0.8		ps rms
Propagation Delay	t_{PD}	Input to output		1000		ps
Propagation Delay Match				50		ps
Output Fall Time	t_F	Differential, 20% to 80%		75		ps
Output Rise Time	t_R	Differential, 20% to 80%		75		ps
INPUT CHARACTERISTICS						
Input Voltage Swing	V_{IN}	Differential	200		2000	mV p-p
Input Voltage Range		Single-ended	$V_{EE} + 1.5$		V_{CC}	V
Input Voltage Range	V_{CM}	Common-mode	$V_{EE} + 1.6$		V_{CC}	V
Input Termination	R_{IN}	Single-ended		50		Ω
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_{OUT}	Differential, programmable	50	800	1850	mV p-p
Output Voltage Range		Common-mode	$V_{EE} + 1.6$		V_{CC}	V
Output Termination	R_{OUT}	Single-ended		50		Ω
POWER SUPPLY						
V_{CC} Operating Range	V_{CC}	$V_{EE} = 0$ V	3.0	3.3	3.6	V
Supply Current	I_{CC}[1]	All disabled		19		mA
	I_{CC}[1]	All outputs on, no equalization		67		mA
	I_{CC}[1]	All outputs and equalizers on		141		mA
	I_{TTI}	800 mV differential swing		32		mA
	I_{TTO}	800 mV differential swing		32		mA
Power Dissipation[2]		All disabled		60		mW
		All outputs on, no equalization		400		mW
		All outputs and equalizers on		700		mW
THERMAL CHARACTERISTICS						
Operating Temperature Range			−40		85	°C
LOGIC INPUT CHARACTERISTICS		$V_{CC} = 3.3$ V dc				
Input V_{IN} High			2.0	V_{CC}		V
Input V_{IN} Low			0		0.8	V

[1] I_{CC} supply current excludes input and output termination currents. Currents at V_{TTI} and V_{TTO} count in power dissipation, but are not included in I_{CC}. Note that in a CML output structure with separate termination supplies, all of the output and input current is drawn from V_{TTI} and the termination resistors, not from Vcc.

[2] Power dissipation includes power due to 800 mV p-p differential input and output voltages; this is the true representation of power dissipated on and used by the chip at an 800 mV p-p differential signal level.

AD8156

TIMING SPECIFICATIONS

$V_{TTI} = V_{TTO} = V_{CC} = 3.3$ V, $V_{EE} = 0$ V, $R_L = 50$ Ω, differential output swing = 800 mV, ac-coupled, data rate = 6.25 Gbps, PRBS $2^{23} - 1$, $V_{IN} = 1$ V p-p differential, $T_A = 25°C$, unless otherwise noted.

Table 2.

| Parameter	Symbol	Min	Typ	Max	Unit
FIRST RANK WRITE CYCLE					
$\overline{CS}$ to $\overline{WE}$ Setup Time	t_{CSW}	0			ns
Address Setup Time	t_{ASW}	0			ns
Data Setup Time	t_{DSW}	1			ns
$\overline{WE}$ to $\overline{CS}$ Hold Time	t_{CHW}	0			ns
Address Hold Time	t_{AHW}	0			ns
Data Hold Time	t_{DHW}	0			ns
$\overline{WE}$ Pulse Width	t_{WP}	10			ns
SECOND RANK UPDATE CYCLE					
$\overline{CS}$ to $\overline{UPD}$ Setup Time	t_{CSU}	0			ns
$\overline{UPD}$ to $\overline{CS}$ Hold Time	t_{CHU}	0			ns
Output Enable	t_{UOE}		20		ns
Output Switch	t_{UOT}		10		ns
Output Disable	t_{UOD}		20		ns
$\overline{UPD}$ Pulse Width	t_{UW}	10			ns
TRANSPARENT WRITE AND UPDATE CYCLE					
Output Enable	t_{WOE}		35	50	ns
Output Toggle	t_{WOT}		25	45	ns
Output Disable	t_{WOD}		25	45	ns
SECOND RANK READBACK CYCLE					
$\overline{CS}$ to $\overline{RE}$ Setup Time	t_{CSR}	0			ns
$\overline{RE}$ to $\overline{CS}$ Hold Time	t_{CHR}	0			ns
ADDR from $\overline{RE}$	t_{RHA}	5			ns
DATA from $\overline{RE}$	t_{RDE}		15		ns
Access Time	t_{AA}		15	30	ns
$\overline{RE}$ to Read Disable	t_{RDD}		50		ns
ASYNCHRONOUS RESET					
Output Disable	t_{TOD}		10	25	ns
$\overline{RST}$ Pulse Width	t_{TW}	10			ns

TIMING DIAGRAMS
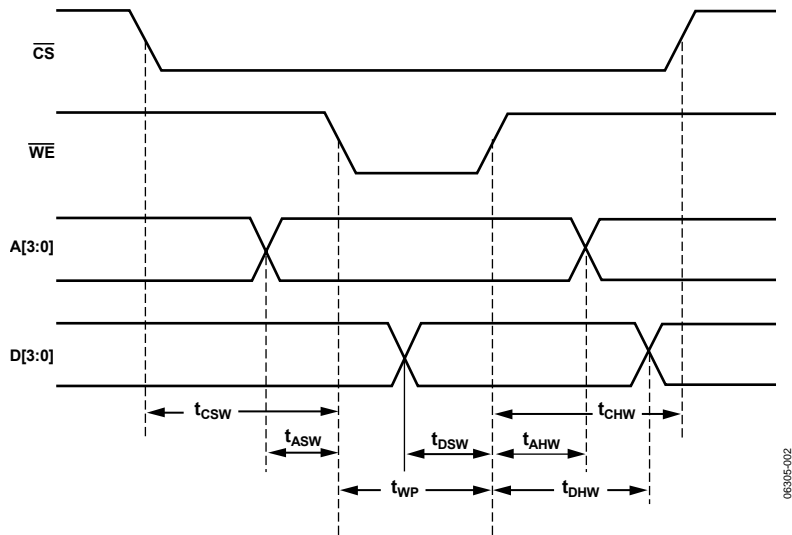
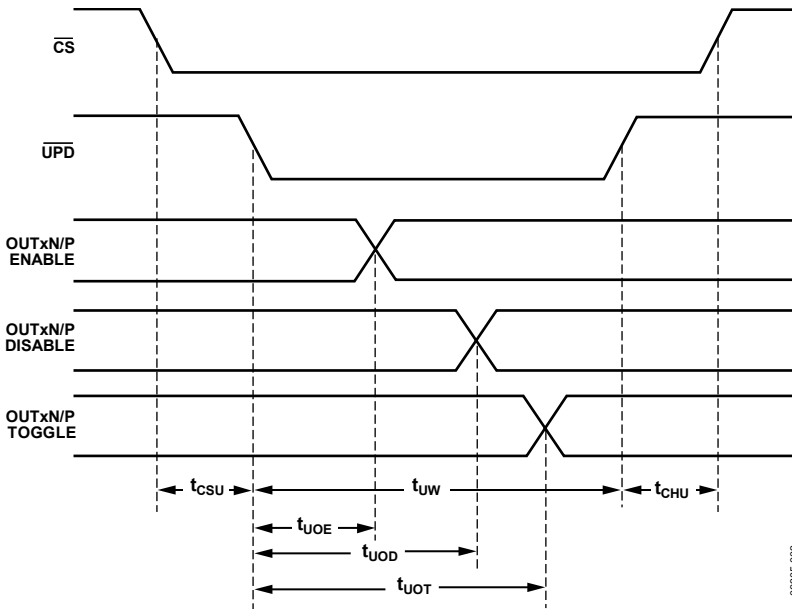*Figure 2. First Rank Write Cycle*
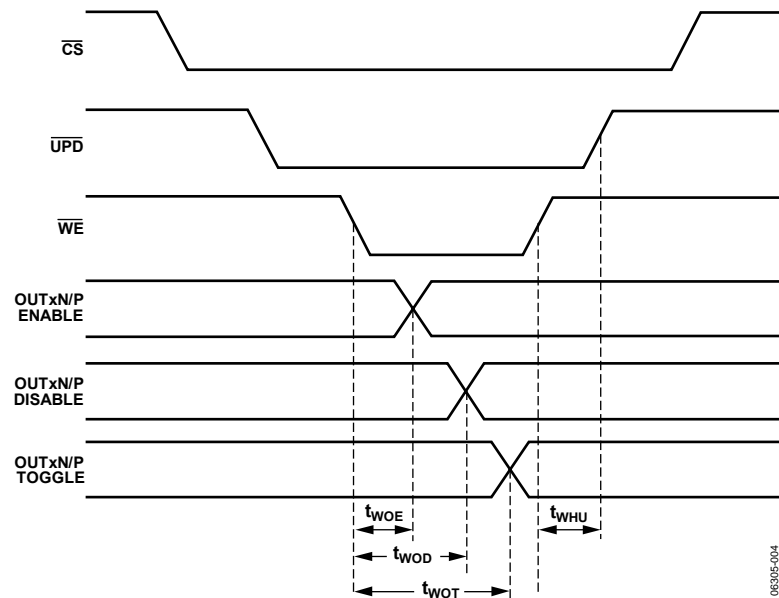

Figure 3. Second Rank Update Cycle

Figure 4. Transparent Write and Update Cycle
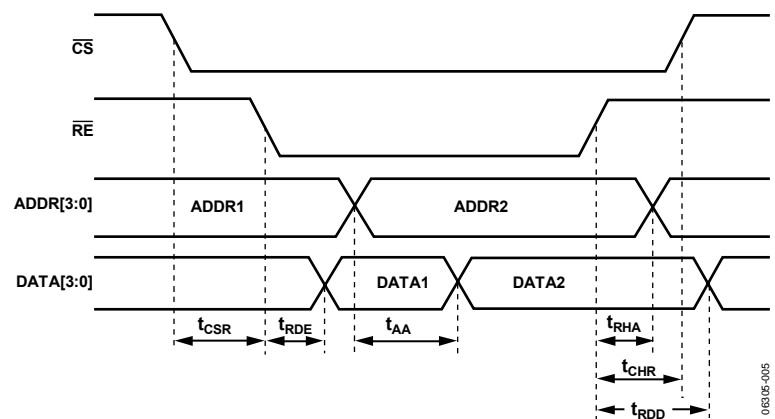
Figure 5. Second Rank Readback Cycle

Figure 6. Asynchronous Reset
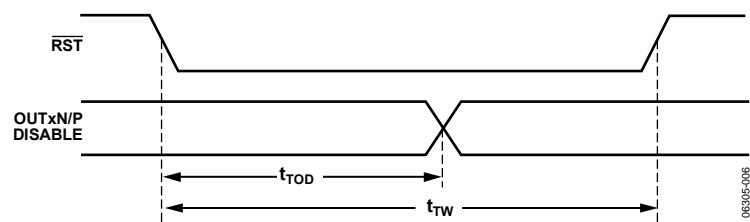
ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{CC} to V_{EE}	3.6 V
V_{TTI}	V_{CC} + 0.6 V
V_{TTO}	V_{CC} + 0.6 V
Internal Power Dissipation[1]	1.92 W
Input Voltage	V_{CC} + 0.6 V
Logic Input Voltage	V_{EE} − 0.3 V < V_{IN} < V_{CC} + 0.6 V
Storage Temperature Range	−65°C to +125°C
Junction Temperature	150°C
Lead Temperature Range	300°C

[1] Specification for T_A = 25°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
49-Ball CSP_BGA	65	28	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
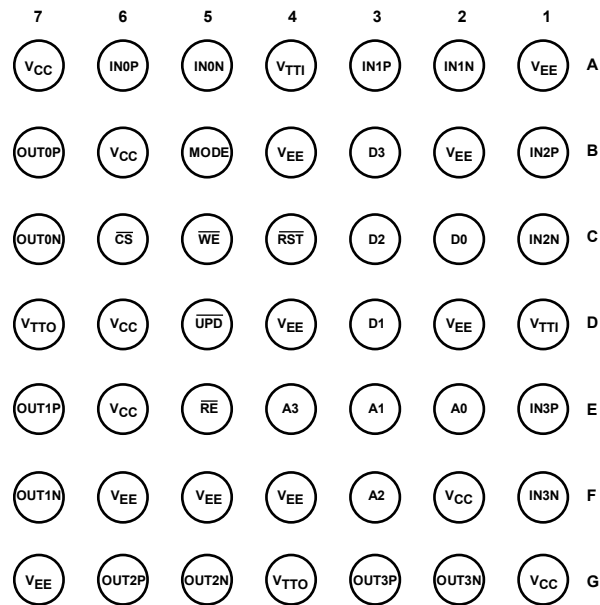
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

	7	6	5	4	3	2	1	
A	V_{CC}	IN0P	IN0N	V_{TTI}	IN1P	IN1N	V_{EE}	A
B	OUT0P	V_{CC}	MODE	V_{EE}	D3	V_{EE}	IN2P	B
C	OUT0N	$\overline{CS}$	$\overline{WE}$	$\overline{RST}$	D2	D0	IN2N	C
D	V_{TTO}	V_{CC}	$\overline{UPD}$	V_{EE}	D1	V_{EE}	V_{TTI}	D
E	OUT1P	V_{CC}	$\overline{RE}$	A3	A1	A0	IN3P	E
F	OUT1N	V_{EE}	V_{EE}	V_{EE}	A2	V_{CC}	IN3N	F
G	V_{EE}	OUT2P	OUT2N	V_{TTO}	OUT3P	OUT3N	V_{CC}	G

Figure 7. Pin Configuration (Bottom View)

06305-007

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description	Pin No.	Mnemonic	Description
A1	V_{EE}	Negative Supply.	D5	$\overline{UPD}$	Second Bank Write Enable.
A2	IN1N	High Speed Input Complement.	D6	V_{CC}	Positive Supply.
A3	IN1P	High Speed Input.	D7	V_{TTO}	Output Termination Supply.
A4	V_{TTI}	Input Termination Supply.	E1	IN3P	High Speed Input.
A5	IN0N	High Speed Input Complement.	E2	A0	Address Pin (LSB).
A6	IN0P	High Speed Input.	E3	A1	Address Pin.
A7	V_{CC}	Positive Supply.	E4	A3	Address Pin (MSB).
B1	IN2P	High Speed Input.	E5	$\overline{RE}$	Second Bank Read Enable.
B2	V_{EE}	Negative Supply.	E6	V_{CC}	Positive Supply.
B3	D3	Input Address Pin (MSB).	E7	OUT1P	High Speed Output.
B4	V_{EE}	Negative Supply.	F1	IN3N	High Speed Input Complement.
B5	MODE	Mode Select Pin.	F2	V_{CC}	Positive Supply.
B6	V_{CC}	Positive Supply.	F3	A2	Address Pin.
B7	OUT0P	High Speed Output.	F4	V_{EE}	Negative Supply.
C1	IN2N	High Speed Input Complement.	F5	V_{EE}	Negative Supply.
C2	D0	Input Address Pin (LSB).	F6	V_{EE}	Negative Supply.
C3	D2	Input Address Pin.	F7	OUT1N	High Speed Output Complement.
C4	$\overline{RST}$	Reset/Disable Outputs.	G1	V_{CC}	Positive Supply.
C5	$\overline{WE}$	First Bank Write Enable.	G2	OUT3N	High Speed Output Complement.
C6	$\overline{CS}$	Chip Select Enable.	G3	OUT3P	High Speed Output.
C7	OUT0N	High Speed Output Complement.	G4	V_{TTO}	Output Termination Supply.
D1	V_{TTI}	Input Termination Supply.	G5	OUT2N	High Speed Output Complement.
D2	V_{EE}	Negative Supply.	G6	OUT2P	High Speed Output.
D3	D1	Input Address Pin.	G7	V_{EE}	Negative Supply.
D4	V_{EE}	Negative Supply.			

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{TTI} = V_{TTO} = V_{CC} = 3.3$ V, $V_{EE} = 0$ V, $R_L = 50$ Ω, differential output swing = 800 mV, ac-coupled, data rate = 6.25 Gbps, PRBS $2^{23} - 1$, $V_{IN} = 1$ V p-p differential, $T_A = 25°C$, unless otherwise noted.
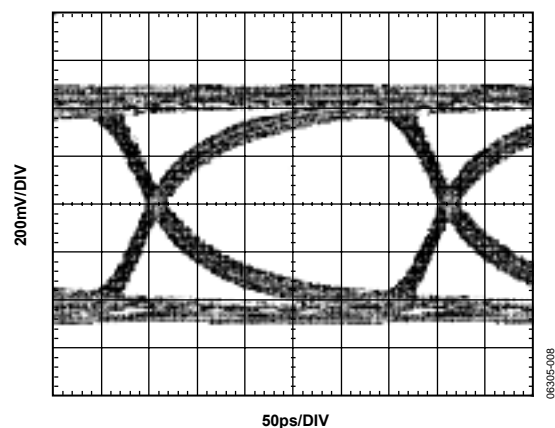

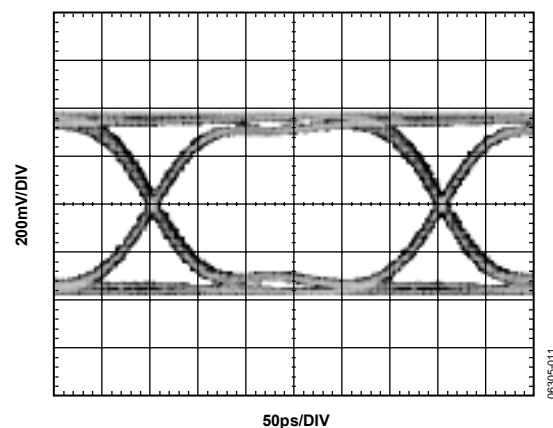Figure 8. Input Eye Diagram at 3.2 Gbps, 10" FR4

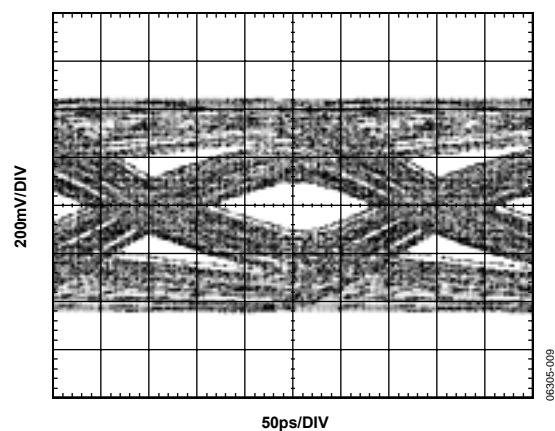Figure 11. Output Eye Diagram at 3.2 Gbps, 10" FR4, Optimal EQ

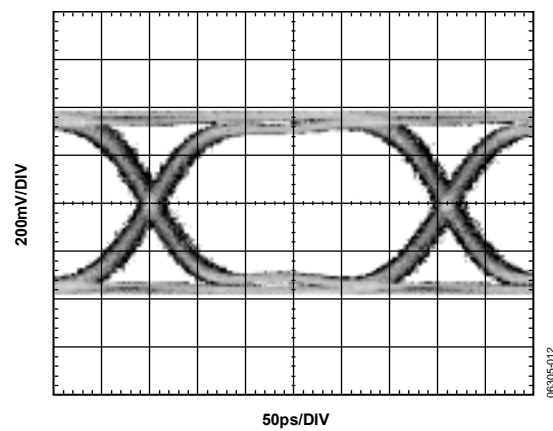Figure 9. Input Eye Diagram at 3.2 Gbps, 40" FR4

Figure 12. Output Eye Diagram at 3.2 Gbps, 40" FR4, Optimal EQ

Figure 10. Input Eye Diagram at 6.25 Gbps, 10" FR4
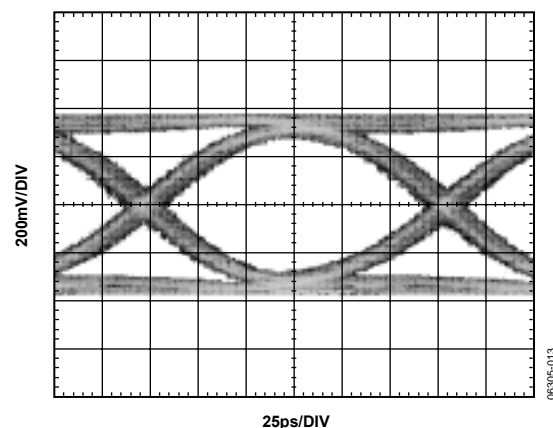
Figure 13. Output Eye Diagram at 6.25 Gbps, 10" FR4, Optimal EQ
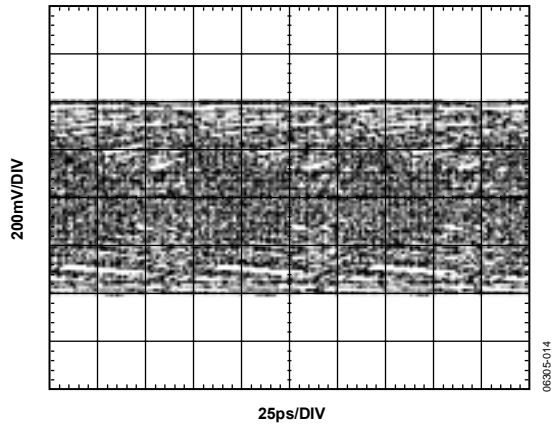
Figure 14. Input Eye Diagram at 6.25 Gbps, 40" FR4
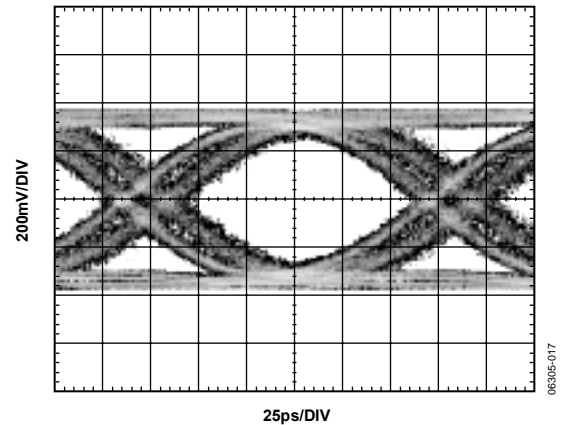
Figure 17. Output Eye Diagram at 6.25Gbps, 40" FR4, Optimal EQ
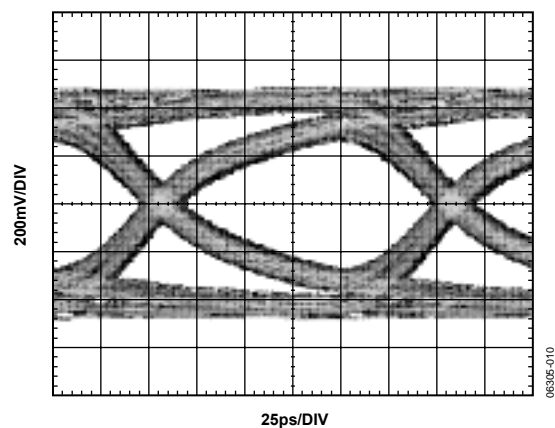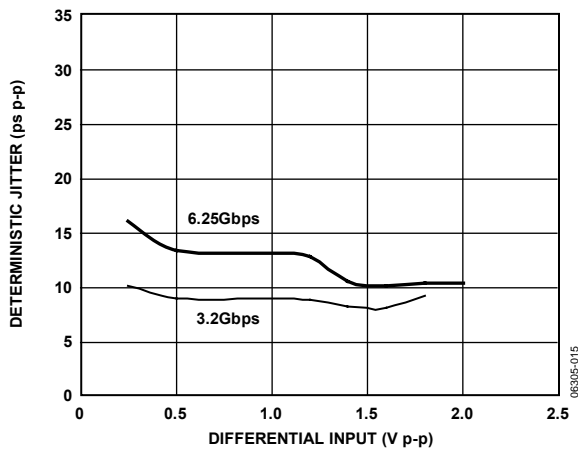

Figure 15. Deterministic Jitter vs. Input Signal Level (No EQ)
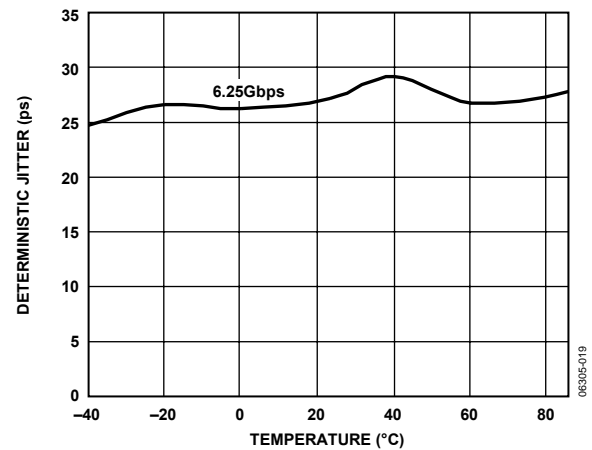
Figure 18. Deterministic Jitter vs. Temperature (Optimal EQ, 20" FR4)
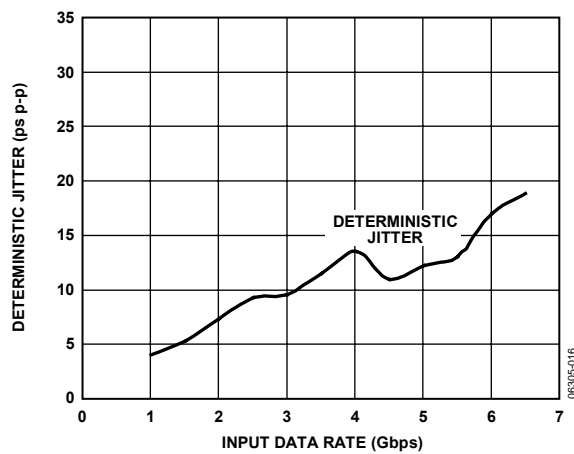
Figure 16. Deterministic Jitter vs. Data Rate (No EQ)
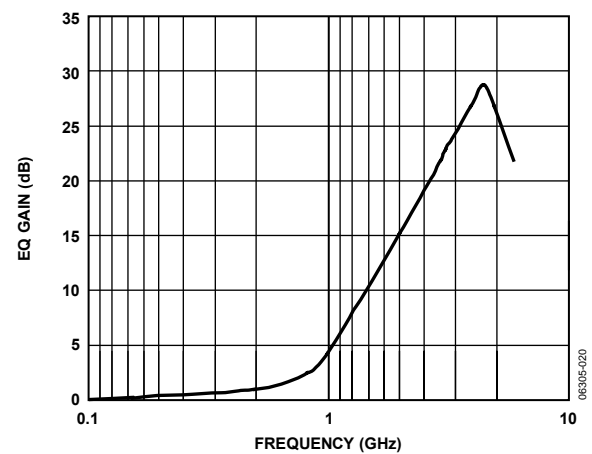
Figure 19. Input EQ Gain vs. Frequency
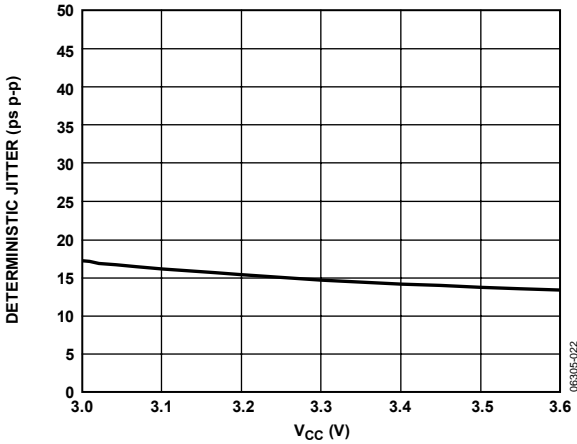
Figure 20. Deterministic Jitter vs. V_{CC}
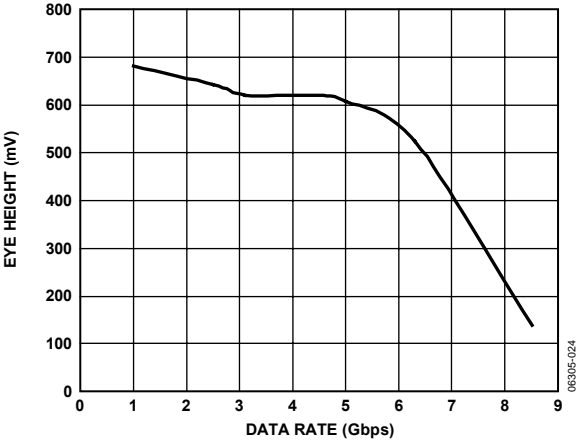
Figure 22. Eye Height vs. Data Rate
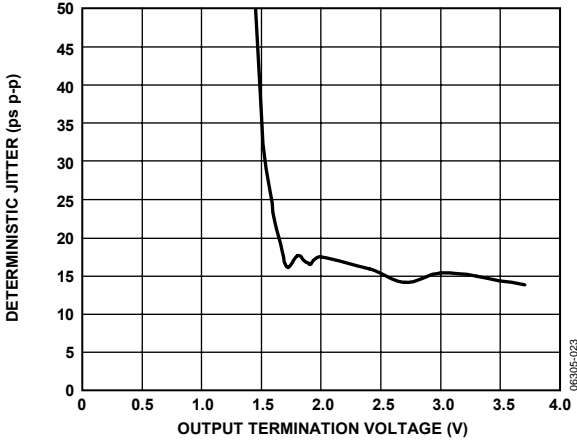
Figure 21. Deterministic Jitter vs. Output Termination Voltage

TEST CIRCUIT
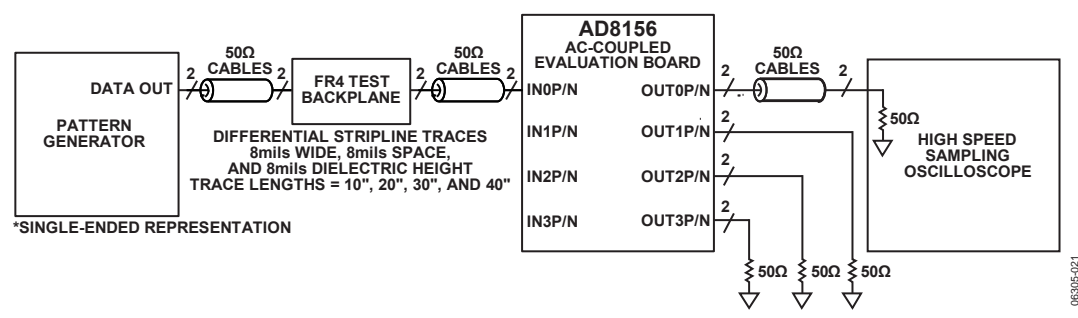
Figure 23. AD8156 Test Circuit

THEORY OF OPERATION

The AD8156 is a 4 × 4 crosspoint switch with programmable input equalization and programmable output current levels. It can be used as a nonblocking and fully programmable 4 × 4 crosspoint switch, or as a dual 2 × 2 protection switch with fast channel switching. Each lane can run at any rate from dc to 6.25 Gbps independent of the other lanes.

In 4 × 4 mode, the user writes the control data to double-latched memory cells through a simple CPU interface. Connectivity, individual output disables, output current level, and input equalization are all individually programmable. Broadcast addresses can be used to simultaneously program the functionality of all channels. A global reset disables the part and resets all equalizers and output current levels to their default states. A chip select pin can be used in applications where a single bus is controlling multiple switches.

When in dual 2 × 2 mode, the part functions as two individual 2 × 2 switches whose connectivity is asynchronously controlled by the D3 to D0 pins, and output enable is controlled by the A3 to A0 pins. The dual 2 × 2 mode allows for sub-10 ns output channel switching or output enable. Output swing control and input equalization cannot be controlled in dual 2 × 2 mode because all the data and address pins are used as asynchronous control pins. However, settings are retained when switching modes, so the user can set the desired swing and input equalization settings in 4 × 4 mode on startup and then switch to dual 2 × 2 mode.

The user can switch at will between 4 × 4 mode and dual 2 × 2 mode by toggling the MODE pin. When switching from 4 × 4 mode to dual 2 × 2 mode, EQ and output current settings are retained, but the output connectivity control is instantly switched to the asynchronous interface of A[3:0] and D[3:0]. To have uninterrupted data flow when switching from 4 × 4 mode to dual 2 × 2 mode, the address and data pins should be set into the desired states for dual 2 × 2 mode before changing the MODE pin. When switching from dual 2 × 2 mode to 4 × 4 mode, EQ and the output current settings are also retained, but the connectivity specified by the values of A[3:0] and D[3:0] when MODE went low are retained in memory. Until some other connectivity is set using the 4 × 4 control interface, the last dual 2 × 2 mode settings are stored in memory.

4 × 4 MODE

Pulling the MODE pin low puts the AD8156 in 4 × 4 mode. In this mode, the chip is controlled by the values stored in the on-chip memory. This memory is organized as two banks of latches; the second bank controls the chip, and the first bank allows the next set of configuration data to be written while the chip is operating based on the second bank data. To write to the first bank of memory, the user sets data and address to the desired states and pulls $\overline{WE}$ low. This writing process is repeated until all desired configuration data is stored in the first bank of latches, and then the chip configuration is simultaneously updated by pulling $\overline{UPD}$ low.

If desired for verification, the value of the second bank of latches can be read back by pulling $\overline{RE}$ low. When $\overline{RE}$ is low, Data Pin D3 to Data Pin D0 are driven by the chip. The timing of this operation is shown in Figure 5. Because the interface is entirely asynchronous, the only limitation on the timing of the read cycle is that each period must be a minimum of 15 ns.

Connectivity Control

Connection between an output and an input is set by addressing a specific output and connecting it to an input. Each output has a disable bit. Table 10 shows how to set the crosspoint connectivity.

Output Current Control

Output current is controlled by addressing a specific output and choosing the output current. The output current is equal to

$$2 \text{ mA} + (2 \text{ mA} \times D[3:0])$$

For example, the default code for D[3:0] is b0111. Therefore, the output current level is 2 mA + (2 mA × 7) = 16 mA. Table 11 and Table 13 show how to set the output current levels.

Input Equalization Control

Input equalization is set per input lane. The equalization is set in ~1.53 dB steps, from 0 dB to 23 dB of equalization at 3.125 GHz (roughly corresponding to a 6.25 Gbps bit rate). The amount of equalization is

$$gain(f) = \frac{D[3:0]}{15} \times 40 \log_{10} \frac{f}{0.83 \text{ GHz}}$$

A value of 0000 disables the equalizer, saving power.

Global Setting

By writing to one of three broadcast addresses, the user can set all connectivity, output current, or input equalization settings to the same value. Broadcast addresses are controlled similarly to other control addresses. See Table 12, Table 13, and Table 14 for broadcast mode programming.

DUAL 2 × 2 MODE

Pulling the MODE pin high puts the AD8156 in dual 2 × 2 mode. In this mode, the part is asynchronously controlled by the address and data pins, A[3:0] and D[3:0], respectively. In dual 2 × 2 mode, the switch is configured as two individual 2 × 2 switches, and each output can be individually disabled. OUT0 and OUT1 can be connected to either IN0 or IN1, and OUT2 and OUT3 can connect to either IN2 or IN3. There are no connectivity options in dual 2 × 2 mode to connect OUT0/OUT1 to IN2/IN3, or OUT2/OUT3 to IN0/IN1.

In dual 2 × 2 mode, input equalization and output level settings are not accessible. If these functions are needed, the user should program these functions in 4 × 4 mode and then return to dual 2 × 2 mode. Output swing and equalization settings are retained from 4 × 4 mode to dual 2 × 2 mode. Readback is not available in dual 2 × 2 mode.

AD8156

When in dual 2 × 2 mode, the A[3:0] and D[3:0] pins set the AD8156 configuration state when $\overline{CS}$ is low. This configuration method allows the user to have multiple AD8156s share the control bus while each device has its own dedicated $\overline{CS}$ control signal.
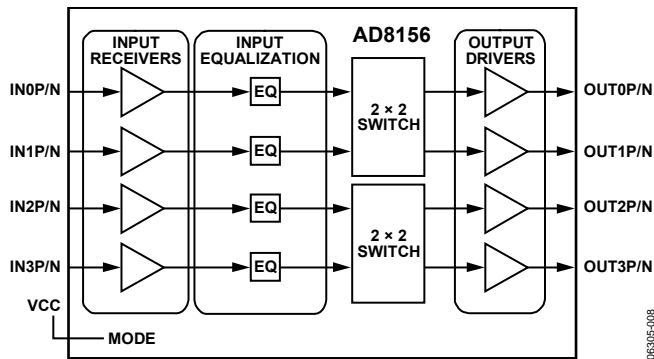
Figure 24. AD8156 in Dual 2 × 2 Mode

INPUT EQUALIZATION

The AD8156 input equalization is an active scheme that is fully linear over all operating ranges. The useful range of equalization covers dc to 3.125 GHz frequencies or dc to 6.25 Gbps data rates. Other key features include:

- 15 steps of gain, linear in dB, programmable through the 4 × 4 control interface
- Gain has a 40 dB per decade slope

- Peak gain of 23 dB at 3.125 GHz (~6.25 Gbps)
- Equalizes more than 40" of typical FR4 backplane with associated connectors and vias at all speeds
- 0.10 UI p-p residual deterministic jitter typ @ 3.125 Gbps
- 0.15 UI p-p residual deterministic jitter typ @ 6.25 Gbps

As with all equalizers, the gain setting is the key. The ideal method of choosing the proper gain setting is to run the equalizer with the channel, and choose the setting with minimum jitter. If this process is not possible or is too time consuming for the number of channels required, the loss of the channel at 3.125 GHz should be measured. The best equalizer setting is usually 2 dB to 4 dB more than the loss at 3.125 GHz. Using the 40 dB slope of the equalizer gain, the gain at other frequencies can be calculated based on the peak gain at 3.125 GHz. The formula to use is

$$gain(f) = \frac{D[3:0]}{15} \times 40 \log_{10} \frac{f}{0.83 \text{ GHz}}$$

where f is the fundamental frequency of the data, or the data rate divided by 2 (that is, 6.25 Gbps → f = 3.125 GHz).

Performance of the equalizer is heavily dependent on the channel used. Operation at high speeds depends on features such as dielectric used (for example, FR4, Nelco3000, or Rogers), connector quality, via stub length, and routing geometry and topology.

CONTROL INTERFACE DESCRIPTION

The control interface for the AD8156 consists of a set of address, data, and several control pins. All control pins are active low. The control interface is level sensitive.

CONTROL PINS

All control pins on the chip are level-sensitive, not edge-triggered. The preferred programming method is to assert the data and address pins to their desired configuration, wait one control bit period, then pull $\overline{WE}$ low to write to the first bank of registers. After one control bit period, $\overline{WE}$ is pulled high. After an additional control bit period, the address and data pins can be set to their next values, and the cycle repeats. Using this method, each write takes three control bit periods.

After the first bank of registers is programmed, $\overline{UPD}$ is pulled low, which transfers the data from the first bank of latches to the second bank of latches. When $\overline{UPD}$ is pulled low, the full chip updates, regardless of the status of the address, data, $\overline{WE}$, or $\overline{RE}$ pins.

Writing to the part while $\overline{UPD}$ is pulled low writes through the first bank of registers and into the second bank, immediately affecting the connectivity and output current of the part. It is recommended that the user write to the first bank with one data bit cycle, and subsequently activate the $\overline{UPD}$ pin low, because data and address pin skews presented to the part can lead to errors when writing through both banks simultaneously. If skews are properly controlled, a transparent write can allow a very quick change of states in 4×4 mode.

$\overline{RST}$ Pin

At any time, a reset pulse to $\overline{RST}$ can be applied to the control interface to globally reset all first and second bank latches to their default values. The device has an internal power-on reset circuit, but it is recommended that $\overline{RST}$ be held low during power-up. The default values for the chip include disabling all outputs, turning off equalization, and setting output current code to the default, b0111 (16 mA). The default connection is the buffer state, or IN0 → OUT0, IN1 → OUT1, IN2 → OUT2, IN3 → OUT3;

all outputs are connected but disabled. $\overline{RST}$ overrides all of the other control pins.

$\overline{CS}$ Pin

The chip select pin, an active low signal, facilitates multiple chip address decoding. All control signals, except the reset signal, are ignored when $\overline{CS}$ is pulled high. The pin disables the control signals and does not affect operation of the chip. $\overline{CS}$ does not power down any of the latches, preserving any data programmed in the latches.

MODE Pin

The MODE pin sets the part in 4×4 mode or dual 2×2 mode. Pulling MODE low sets the part in 4×4 mode, and pulling MODE high sets the part in dual 2×2 mode. In dual 2×2 mode, the $\overline{WE}$, $\overline{RE}$, and $\overline{UPD}$ pins are unused.

$\overline{WE}$ Pin

This pin is the write enable to the first bank of registers. Forcing $\overline{WE}$ to logic low allows the data on the D[3:0] pins to be stored in the first bank of latches for the function specified by A[3:0]. The $\overline{WE}$ pin must be returned to logic high state before changing the other pins after a write cycle to avoid overwriting the first bank data.

$\overline{UPD}$ Pin

This pin is the write enable to the second bank of registers. Forcing $\overline{UPD}$ to logic low transfers the data stored in all first bank latches to the second bank latches, which is the active set of registers. The chip functions update during this operation.

$\overline{RE}$ Pin

This pin is the read enable for the second bank of registers. Forcing $\overline{RE}$ to logic low enables the on-chip drivers to drive the bidirectional D[3:0] pins. The on-chip drivers are only intended to drive high impedance loads, so any external drivers of D[3:0] must be disabled when $\overline{RE}$ is low.

Table 6. Basic Control Pin Functions

$\overline{RST}$	$\overline{CS}$	MODE	$\overline{WE}$	$\overline{RE}$	$\overline{UPD}$	Function
1	1	x	x	x	x	Control Interface Disabled. Prior settings are stored, and the chip is run based on the configuration data stored (in 4×4 mode) or set (in dual 2×2 mode) previously.
0	x	x	x	x	x	Global Reset. Disables all outputs and equalizers. Output current code set to 0111 (16 mA).
1	0	0	1	1	1	4×4 Mode. Address and data pins are ignored (values in the AD8156 memory control connectivity, output current, and EQ setting).
1	0	0	0	1	1	Write Enable. Writes to the first bank of registers.
1	0	0	1	0	1	Readback Enable. Reads back data on D[3:0] from the addressed latch (second bank of registers).
1	0	0	1	x	0	Global Update. Transfers data from first bank of registers to second bank of registers (active set). Chip functions update.
1	0	0	0	x	0	Transparent Write. Writes and updates simultaneously through first bank to the second bank of registers. Chip functions update.
1	0	1	x	x	x	Dual 2×2 Mode. Address and data pins asynchronously control the device.

AD8156

ADDRESS PINS, A[3:0] INPUTS

The AD8156 feature sets can be set port by port or globally. A[3:2] specify what is being programmed or read back when the part is being configured port by port. Connectivity, output current, equalization, or global programming features are chosen based on the values of A[3:2]. Similarly, A[1:0] address the port that is being programmed or read back. In global programming, A[1:0] serve a different function. Refer to Table 9 to Table 15 for programming examples.

DATA PINS, D[3:0] INPUTS/OUTPUTS

In readback mode, the D[3:0] pins are low impedance outputs indicating the stored values in the memory to be read. The readback drivers are designed to drive high impedances only, so external drivers connected to D[3:0] must be disabled during readback mode.

CONTROL INTERFACE LEVELS

The AD8156 control interface shares the data path supply pins, V_{CC} and V_{EE}. The potential between the positive logic supply V_{CC} and the negative supply V_{EE} must be at least 3.0 V and no more than 3.7 V. Regardless of supply, the logic threshold is approximately one-half the supply range, allowing the interface to be used with most LVCMOS- and LVTTL-logic drivers.

Table 7. Dual 2 × 2 Mode Programming Table

Address A[3:0]	Data D[3:0]
Input A3 to Input A0 enable Output 3 to Output 0, respectively.	Input D3 to Input D0 control the connectivity of Output 3 to Output 0, respectively.
1 = Enables the output (for all A[3:0] inputs)	0 = Input 2, 1 = Input 3 (for D2 and D3)
0 = Disables the output (for all A[3:0] inputs)	0 = Input 0, 1 = Input 1 (for D0 and D1)

Table 8. 4 × 4 Mode Programming Table

| Mode	Address A[3:0]	Data D[3:0]
Write/Read Connectivity and Disable	0 0 A1 A0 A1 and A0 determine which output is being programmed.	0 D2 D1 D0 D1 and D0 determine which input is connected to which output; D2 determines the enabled/disabled state of that output, with D2 = 1 (enable). When writing or reading, D3 is always 0.
Write/Read Output Current Level	0 1 A1 A0 A1 and A0 determine which output is being programmed.	D3 D2 D1 D0 D0 to D3 binarily program the output current level/voltage swing with the output current = 2 mA + (2 mA × decimal (D[3:0])).
Broadcast Connectivity/Disable	1 0 0 0	0 D2 D1 D0 D1 and D0 determine which input is connected to all of the outputs. D2 determines the enabled/disabled state of all outputs with D2 = 1 (enable). When writing or reading, D3 is always 0.
Broadcast Output Current Level	1 0 0 1	D3 D2 D1 D0 D0 to D3 binarily program the output current level/voltage swing with the output current = 2 mA + (2 mA × decimal (D[3:0])). The value is written to all outputs.
Broadcast EQ Setting	1 0 1 1	D3 D2 D1 D0 Data inputs D0 to D3 set the input equalization level where: Gain(f) = D[3:0]/15 × 40 $\log_{10}$(f/0.83 GHz).
Program EQ Setting	1 1 A1 A0 A1 and A0 determine which input is being programmed.	D3 D2 D1 D0 D0 to D3 set the input equalization level, where: Gain(f) = D[3:0]/15 × 40 $\log_{10}$(f/0.83 GHz).

PROGRAMMING EXAMPLES
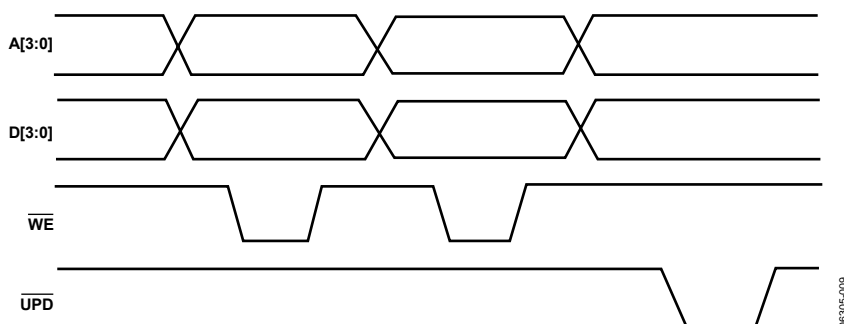
Figure 25. Sample Timing Diagram for 4x4 Mode Programming Examples

DUAL 2 × 2 MODE (MODE PIN = 1) PROGRAMMING EXAMPLES

Table 9. Dual 2 × 2 Mode Programming

Address Pins				Data Pins				
A3	A2	A1	A0	D3	D2	D1	D0	Description
1	0	0	0	0	x	x	x	A[3] = 1 enables OUT3. D[3] = 0 connects IN2 to OUT3.
1	0	0	0	1	x	x	x	A[3] = 1 enables OUT3. D[3] = 1 connects IN3 to OUT3.
1	1	0	0	0	0	x	x	A[3:2] = b11 enables OUT2 and OUT3. D[3:2] = b00 connects IN2 to both OUT2 and OUT3.
1	1	0	0	1	0	x	x	A[3:2] = b11 enables OUT2 and OUT3. D[3:2] = b10 connects IN2 to OUT2 and connects IN3 to OUT3.
0	0	1	0	x	x	0	x	A[1] = 1 enables OUT1. D[1] = 0 connects IN0 to OUT1.
0	0	1	1	x	x	1	1	D[1:0] = b11 enables OUT0 and OUT1. D[1:0] = b11 connects IN1 to both OUT0 and OUT1.
1	1	1	1	0	1	0	1	A[3:0] = b1111 enables all outputs. D[3:0] = b0101 connects IN2 to OUT3, IN3 to OUT2, IN0 to OUT1, IN1 to OUT0.

4 × 4 MODE (MODE PIN = 0) PROGRAMMING EXAMPLES

Table 10. Connectivity Programming, A[3:2] = b00

Address Pins				Data Pins				
A3	A2	A1	A0	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	0	A[1:0] = 0 selects OUT0. D2 = 1 enables OUT0. D[1:0] = 0 connects IN0 to OUT0.
0	0	0	0	0	0	0	0	A[1:0] = 0 selects OUT0. D2 = 0 disables OUT0. D[1:0] = 0 connects IN0 to OUT0.
0	0	1	0	0	1	0	1	A[1:0] = b10 selects OUT2. D2 = 1 enables OUT2. D[1:0] = b01 connects IN1 to OUT2.
0	0	1	1	0	1	0	0	A[1:0] = b11 selects OUT3. D2 = 1 enables OUT3. D[1:0] = b00 connects IN0 to OUT3.

Table 11. Output Level Programming, A[3:2] = b01

Address Pins				Data Pins				
A3	A2	A1	A0	D3	D2	D1	D0	Description (Output Current = 2 mA + (2 mA × D[3:0])
0	1	0	0	0	1	0	0	A[1:0] = 0 selects OUT0. D[3:0] = b0100 sets OUT0 current to 2 mA + (2 mA × 4) = 10 mA.
0	1	0	0	1	0	0	0	A[1:0] = 0 selects OUT0. D[3:0] = b1000 sets OUT0 current to 2 mA + (2 mA × 8) = 18 mA.
0	1	1	0	1	1	0	1	A[1:0] = b10 selects OUT2. D[3:0] = b1101 sets OUT2 current to 2 mA + (2 mA × 13) = 28 mA.
0	1	1	1	0	0	0	0	A[1:0] = b11 selects OUT3. D[3:0] = b0000 sets OUT3 current to 2 mA + (2 mA × 0) = 2 mA.

Table 12. Broadcast Connectivity Programming, A[3:0] = b1000

Address Pins				Data Pins				
A3	A2	A1	A0	D3	D2	D1	D0	Description
1	0	0	0	0	1	0	0	D2 = 1 enables all outputs. D[1:0] = b00 connects IN0 to all outputs.
1	0	0	0	0	1	1	1	D2 = 1 enables all outputs. D[1:0] = b11 connects IN3 to all outputs.
1	0	0	0	0	0	1	0	D2 = 0 disables all outputs. D[1:0] = b10 connects IN2 to all outputs, but all outputs are disabled.

Table 13. Broadcast Output Level Programming, A[3:0] = b1001

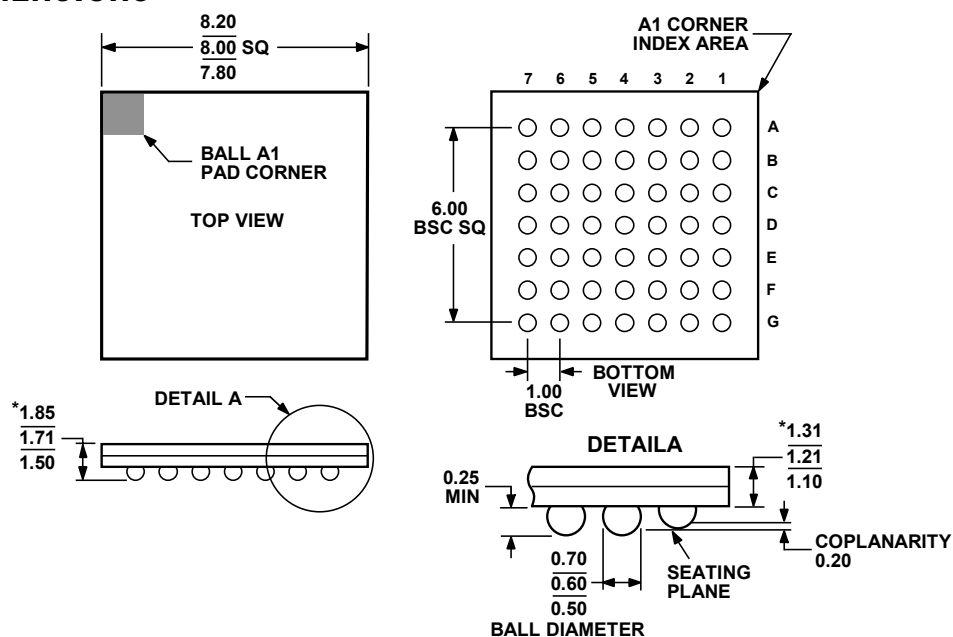| Address Pins				Data Pins				
A3	A2	A1	A0	D3	D2	D1	D0	Description (Output Current = 2 mA + (2 mA × D[3:0])
1	0	0	1	0	1	0	0	D[3:0] = b0100 sets current of all outputs to 2 mA + (2 mA × 4) = 10 mA.
1	0	0	1	1	1	0	1	D[3:0] = b1101 sets current of all outputs to 2 mA + (2 mA × 13) = 28 mA.
1	0	0	1	0	0	0	0	D[3:0] = b0000 sets current of all outputs to 2 mA + (2 mA × 0) = 2 mA.

Table 14. Broadcast Equalization (EQ) Programming, A[3:0] = b1011

Address Pins				Data Pins				
A3	A2	A1	A0	D3	D2	D1	D0	Description (Gain(f) = D[3:0]/15 × 40 $\log_{10}$(f/0.83 GHz)), assume f = 2.25 GHz
1	0	1	1	0	1	0	0	D[3:0] = b0100 sets all input EQ = (4/15 × 40 $\log_{10}$(2.25 GHz/0.83 GHz)) = 4.6 dB.
1	0	1	1	1	1	0	1	D[3:0] = b1101 sets all input EQ = (13/15 × 40 $\log_{10}$(2.25 GHz/0.83 GHz)) =14.95 dB.
1	0	1	1	0	0	0	0	D[3:0] = b0000 sets all input EQ = (0/15 × 40 $\log_{10}$(2.25 GHz/0.83 GHz)) = 0 dB.

Table 15. Individual Input EQ Programming, A[3:2] = b11

Address Pins				Data Pins				
A3	A2	A1	A0	D3	D2	D1	D0	Description (Gain(f) = D[3:0]/15 × 40$\log_{10}$(f/0.83 GHz)), assume f = 2.25 GHz
1	1	0	0	0	1	0	0	A[1:0] = b00 selects IN0. D[3:0] = b0100 sets EQ = (4/15 × 40 $\log_{10}$(2.25 GHz/0.83 GHz)) = 4.6 dB.
1	1	0	1	1	1	0	1	A[1:0] = b01 selects IN1. D[3:0] = b1101 sets EQ = (13/15 × 40 $\log_{10}$(2.25 GHz/0.83 GHz)) = 14.95 dB.
1	1	1	0	1	1	1	1	A[1:0] = b10 selects IN2. D[3:0] = b1111 sets EQ = (15/15 × 40 $\log_{10}$(2.25 GHz/0.83 GHz)) = 17.25 dB.
1	1	1	1	0	0	0	0	A[1:0] = b11 selects IN3. D[3:0] = b0000 sets EQ = (0/15 × 40 $\log_{10}$(2.25 GHz/0.83 GHz)) = 0 dB.

OUTLINE DIMENSIONS

8.20
8.00 SQ
7.80

BALL A1
PAD CORNER

TOP VIEW

A1 CORNER
INDEX AREA

7 6 5 4 3 2 1

A
B
C
D
E
F
G

6.00
BSC SQ

BOTTOM
VIEW

1.00
BSC

DETAIL A

*1.85
1.71
1.50

DETAIL A

*1.31
1.21
1.10

0.25
MIN

0.70
0.60
0.50

BALL DIAMETER

SEATING
PLANE

COPLANARITY
0.20

012006-0

*COMPLIANT WITH JEDEC STANDARDS MO-192-ABB-1
WITH EXCEPTION TO PACKAGE HEIGHT AND THICKNESS.

Figure 26. 49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-49-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8156ABCZ[1]	−40°C to +85°C	49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-49-3
AD8156-EVALZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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