LC²MOS Loop-Powered Signal Conditioning ADC

AD7713

FEATURES

Charge Balancing ADC
- 24 Bits No Missing Codes
- ±0.0015% Nonlinearity

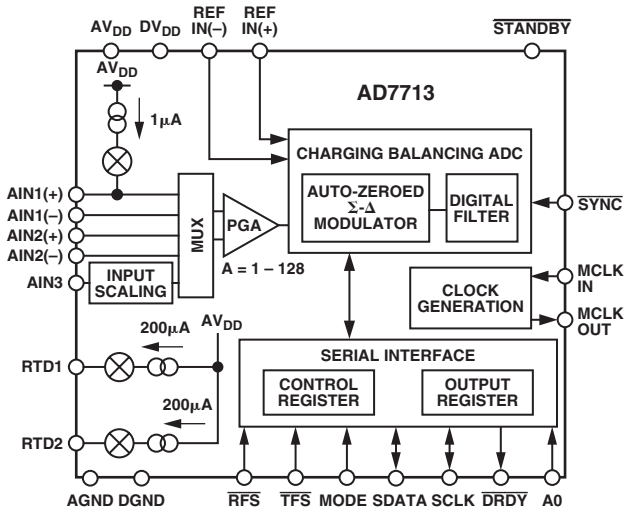
3-Channel Programmable Gain Front End
- Gains from 1 to 128
- 2 Differential Inputs
- 1 Single-Ended High Voltage Input

Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Single-Supply Operation
Low Power (3.5 mW typ) with Power-Down Mode (150 μW typ)

APPLICATIONS

Loop Powered (Smart) Transmitters
RTD Transducers
Process Control
Portable Industrial Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7713 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer or high level signals ($4 \times V_{REF}$) and outputs a serial digital word. It employs Σ-Δ conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register, allowing adjustment of the filter cutoff and settling time.

The part features two differential analog inputs and one single-ended high level analog input as well as a differential reference input. It can be operated from a single supply (AV_{DD} and DV_{DD} at 5 V). The part provides two current sources that can be used to provide excitation in 3-wire and 4-wire RTD configurations. The AD7713 thus performs all signal conditioning and conversion for a single-, dual- or three-channel system.

The AD7713 is ideal for use in smart, microcontroller-based systems. Gain settings, signal polarity, and RTD current control can be configured in software using the bidirectional serial port. The AD7713 contains self-calibration, system calibration, and background calibration options and also allows the user to read and to write the on-chip calibration registers.

CMOS construction ensures low power dissipation, and a hardware programmable power-down mode reduces the standby power consumption to only 150 μW typical. The part is available in a 24-lead, 0.3 inch wide, PDIP and CERDIP as well as a 24-lead SOIC package.

PRODUCT HIGHLIGHTS

1. The AD7713 consumes less than 1 mA in total supply current, making it ideal for use in loop-powered systems.
2. The two programmable gain channels allow the AD7713 to accept input signals directly from a transducer removing a considerable amount of signal conditioning. To maximize the flexibility of the part, the high level analog input accepts $4 \times V_{REF}$ signals. On-chip current sources provide excitation for 3-wire and 4-wire RTD configurations.
3. No missing codes ensures true, usable, 24-bit dynamic range coupled with excellent ±0.0015% accuracy. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero-scale and full-scale errors.
4. The AD7713 is ideal for microcontroller or DSP processor applications with an on-chip control register, which allows control over filter cutoff, input gain, signal polarity, and calibration modes. The AD7713 allows the user to read and write the on-chip calibration registers.

REV. D

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AD7713* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-202: An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change
- AN-283: Sigma-Delta ADCs and DACs
- AN-311: How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging
- AN-348: Avoiding Passive-Component Pitfalls
- AN-388: Using Sigma-Delta Converters-Part 1
- AN-389: Using Sigma-Delta Converters-Part 2
- AN-397: Electrically Induced Damage to Standard Linear Integrated Circuits:
- AN-406: Using the AD771X Family of 24-Bit Sigma-Delta A/D Converters
- AN-553: Adjusting the Calibration Coefficients on the AD771X Family of ADCs
- AN-607: Selecting a Low Bandwidth (<15 kSPS) Sigma-Delta ADC
- AN-615: Peak-to-Peak Resolution Versus Effective Resolution

Data Sheet

- AD7713: LC^{2}MOS, Loop-Powered Signal Conditioning ADC Data Sheet

TOOLS AND SIMULATIONS

- Sigma-Delta ADC Tutorial

REFERENCE MATERIALS

Technical Articles

- Delta-Sigma Rocks RF, As ADC Designers Jump On Jitter
- MS-2210: Designing Power Supplies for High Speed ADC
- Part 1: Circuit Suggestions Using Features and Functionality of New Sigma-Delta ADCs
- Part 2: Circuit Suggestions Using Features and Functionality of New Sigma-Delta ADCs

DESIGN RESOURCES

- AD7713 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7713 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

AD7713—SPECIFICATIONS (AV_{DD} = 5 V ± 5%; DV_{DD} = 5 V ± 5%; REF IN(+) = 2.5 V; REF IN(–) = AGND; MCLK IN = 2 MHz, unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, S Versions[1]	Unit	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	24	Bits min	Guaranteed by Design. For Filter Notches ≤ 12 Hz.
	22	Bits min	For Filter Notch = 20 Hz.
	18	Bits min	For Filter Notch = 50 Hz.
	15	Bits min	For Filter Notch = 100 Hz.
	12	Bits min	For Filter Notch = 200 Hz.
Output Noise	See Tables I and II		Depends on Filter Cutoffs and Selected Gain.
Integral Nonlinearity	±0.0015	% of FSR max	Filter Notches ≤ 12 Hz; Typically ±0.0003%.
Positive Full-Scale Error[2, 3, 4]			
Full-Scale Drift[5]	1	µV/°C typ	For Gains of 1, 2.
	0.3	µV/°C typ	For Gains of 4, 8, 16, 32, 64, 128.
Unipolar Offset Error[2, 4]			
Unipolar Offset Drift[5]	0.5	µV/°C typ	For Gains of 1, 2.
	0.25	µV/°C typ	For Gains of 4, 8, 16, 32, 64, 128.
Bipolar Zero Error[2, 4]			
Bipolar Zero Drift[5]	0.5	µV/°C typ	For Gains of 1, 2.
	0.25	µV/°C typ	For Gains of 4, 8, 16, 32, 64, 128.
Gain Drift	2	ppm/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.0004	% of FSR max	Typically ±0.0006%.
Bipolar Negative Full-Scale Drift[5]	1	µV/°C typ	For Gains of 1, 2.
	0.3	µV/°C typ	For Gains of 4, 8, 16, 32, 64, 128.
ANALOG INPUTS			
Input Sampling Rate, f_S	See Table III		
Normal-Mode 50 Hz Rejection[6]	100	dB min	For Filter Notches of 2 Hz, 5 Hz, 10 Hz, 25 Hz, 50 Hz, ±0.02 × f_{NOTCH}.
Normal-Mode 60 Hz Rejection[6]	100	dB min	For Filter Notches of 2 Hz, 6 Hz, 10 Hz, 30 Hz, 60 Hz, ±0.02 × f_{NOTCH}.
AIN1, AIN2[7]			
Input Voltage Range[8]			For Normal Operation. Depends on Gain Selected.
	0 to $+V_{REF}$[9]	V max	Unipolar Input Range (B/U Bit of Control Register = 1).
	$\pm V_{REF}$	V max	Bipolar Input Range (B/U Bit of Control Register = 0).
Common-Mode Rejection (CMR)	100	dB min	At dc and AV_{DD} = 5 V.
	90	dB min	At dc and AV_{DD} = 10 V.
Common-Mode 50 Hz Rejection[6]	150	dB min	For Filter Notches of 2 Hz, 5 Hz, 10 Hz, 25 Hz, 50 Hz, ±0.02 × $f_{NOTCH.}$
Common-Mode 60 Hz Rejection[6]	150	dB min	For Filter Notches of 2 Hz, 6 Hz, 10 Hz, 30 Hz, 60 Hz, ±0.02 × $f_{NOTCH.}$
Common-Mode Voltage Range[10]	AGND to AV_{DD}	V min to V max	
DC Input Leakage Current @ 25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
Sampling Capacitance[6]	20	pF max	
AIN3			
Input Voltage Range	0 to + 4 × V_{REF}	V max	For Normal Operation. Depends on Gain Selected.
Gain Error[11]	±0.05	% typ	Additional Error Contributed by Resistor Attenuator.
Gain Drift	1	ppm/°C typ	Additional Drift Contributed by Resistor Attenuator.
Offset Error[11]	4	mV max	Additional Error Contributed by Resistor Attenuator.
Input Impedance	30	kΩ min	

Parameter	A, S Versions[1]	Unit	Conditions/Comments
REFERENCE INPUT			
REF IN(+) – REF IN(–) Voltage	2.5 to AV_{DD}/1.8	V min to V max	For Specified Performance. Part Is Functional with Lower V_{REF} Voltages.
Input Sampling Rate, f_S	$f_{CLK\ IN}$/512		
Normal-Mode 50 Hz Rejection[6]	100	dB min	For Filter Notches of 2 Hz, 5 Hz, 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$.
Normal-Mode 60 Hz Rejection[6]	100	dB min	For Filter Notches of 2 Hz, 6 Hz, 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$.
Common-Mode Rejection (CMR)	100	dB min	At DC.
Common-Mode 50 Hz Rejection[6]	150	dB min	For Filter Notches of 2 Hz, 5 Hz, 10 Hz, 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$.
Common-Mode 60 Hz Rejection[6]	150	dB min	For Filter Notches of 2 Hz, 6 Hz, 10 Hz, 30 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$.
Common-Mode Voltage Range[10]	AGND to AV_{DD}	V min to V max	
DC Input Leakage Current @ 25°C	10	pA max	
T_{MIN} to T_{MAX}	1	nA max	
LOGIC INPUTS			
Input Current	±10	μA max	
All Inputs Except MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	2.0	V min	
MCLK IN Only			
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
LOGIC OUTPUTS			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA.
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 100 μA.
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[12]	9	pF typ	
TRANSDUCER BURN-OUT			
Current	1.2	μA nom	
Initial Tolerance @ 25°C	±10	% typ	
Drift	0.1	%/°C typ	
RTD EXCITATION CURRENTS (RTD1, RTD2)			
Output Current	200	μA nom	
Initial Tolerance @ 25°C	±20	% max	
Drift	20	ppm/°C typ	
Initial Matching @ 25°C	±1	% max	Matching Between RTD1 and RTD2 Currents.
Drift Matching	3	ppm/°C typ	Matching Between RTD1 and RTD2 Current Drift.
Line Regulation (AV_{DD})	200	nA/V max	AV_{DD} = 5 V.
Load Regulation	200	nA/V max	
SYSTEM CALIBRATION			
AIN1, AIN2			
Positive Full-Scale Calibration Limit[13]	$+(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Negative Full-Scale Calibration Limit[13]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Offset Calibration Limit[14, 15]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Input Span[14]	$+(0.8 \times V_{REF})/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128).
	$+(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).

Parameter	A, S Versions[1]	Unit	Conditions/Comments
AIN3			
Positive Full-Scale Calibration Limit[13]	$+(4.2 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Offset Calibration Limit[15]	0 to $V_{REF}/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
Input Span	$+(3.2 \times V_{REF})/GAIN$	V min	GAIN Is the Selected PGA Gain (Between 1 and 128).
	$+(4.2 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (Between 1 and 128).
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage[16]	5 to 10	V nom	±5% for Specified Performance.
DV_{DD} Voltage[17]	5	V nom	±5% for Specified Performance.
Power Supply Currents			
AV_{DD} Current	0.6	mA max	AV_{DD} = 5 V.
	0.7	mA max	AV_{DD} = 10 V.
DV_{DD} Current	0.5	mA max	$f_{CLK\ IN}$ = 1 MHz. Digital Inputs 0 V to DV_{DD}.
	1	mA max	$f_{CLK\ IN}$ = 2 MHz. Digital Inputs 0 V to DV_{DD}.
Power Supply Rejection[18]			Rejection w.r.t. AGND.
(AV_{DD} and DV_{DD})[19]		dB typ	
Power Dissipation			
Normal Mode	5.5	mW max	AV_{DD} = DV_{DD} = 5 V, $f_{CLK\ IN}$ = 1 MHz; Typically 3.5 mW.
Standby (Power-Down) Mode	300	μW max	AV_{DD} = DV_{DD} = 5 V, Typically 150 μW.

NOTES

[1] Temperature range is: A Version, –40°C to +85°C; S Version, –55°C to +125°C.

[2] Applies after calibration at the temperature of interest.

[3] Positive full-scale error applies to both unipolar and bipolar input ranges.

[4] These errors will be of the order of the output noise of the part as shown in Table I after system calibration. These errors will be 20 μV typical after self-calibration or background calibration.

[5] Recalibration at any temperature or use of the background calibration mode will remove these drift errors.

[6] These numbers are guaranteed by design and/or characterization.

[7] The AIN1 and AIN2 analog inputs present a very high impedance dynamic load that varies with clock frequency and input sample rate. The maximum recommended source resistance depends on the selected gain.

[8] The analog input voltage range on the AIN1(+) and AIN2(+) inputs is given here with respect to the voltage on the AIN1(–) and AIN2(–) inputs. The input voltage range on the AIN3 input is with respect to AGND. The absolute voltage on the AIN1 and AIN2 inputs should not go more positive than AV_{DD} + 30 mV or more negative than AGND – 30 mV.

[9] V_{REF} = REF IN(+) – REF IN(–).

[10] This common-mode voltage range is allowed, provided that the input voltage on AIN(+) and AIN(–) does not exceed AV_{DD} + 30 mV and AGND – 30 mV.

[11] This error can be removed using the system calibration capabilities of the AD7713. This error is not removed by the AD7713's self-calibration feature. The offset drift on the AIN3 input is four times the value given in the Static Performance section of the specifications.

[12] Guaranteed by design, not production tested.

[13] After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, the device will output all 0s.

[14] These calibration and span limits apply provided the absolute voltage on the AIN1 and AIN2 analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND – 30 mV.

[15] The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[16] Operating with AV_{DD} voltages in the range 5.25 V to 10.5 V is guaranteed only over the 0°C to 70°C temperature range.

[17] The ±5% tolerance on the DV_{DD} input is allowed provided that DV_{DD} does not exceed AV_{DD} by more than 0.3 V.

[18] Measured at dc and applies in the selected pass band. PSRR at 50 Hz will exceed 120 dB with filter notches of 2 Hz, 5 Hz, 10 Hz, 25 Hz, or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 2 Hz, 6 Hz, 10 Hz, 30 Hz, or 60 Hz.

[19] PSRR depends on gain: gain of 1 = 70 dB typ; gain of 2 = 75 dB typ; gain of 4 = 80 dB typ; gains of 8 to 128 = 85 dB typ.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (DV_{DD} = 5 V ± 5%; AV_{DD} = 5 V or 10 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 2 MHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (A, S Versions)	Unit	Conditions/Comments
$f_{CLK\ IN}$[3, 4]	400	kHz min	Master Clock Frequency: Crystal Oscillator or
	2	MHz max	Externally Supplied for Specified Performance
$t_{CLK\ IN\ LO}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input Low Time; $t_{CLK\ IN}$ = 1/$f_{CLK\ IN}$
$t_{CLK\ IN\ HI}$	0.4 × $t_{CLK\ IN}$	ns min	Master Clock Input High Time
t_r[5]	50	ns max	Digital Output Rise Time; Typically 20 ns
t_f[5]	50	ns max	Digital Output Fall Time; Typically 20 ns
t_1	1000	ns min	$\overline{SYNC}$ Pulse Width
Self-Clocking Mode			
t_2	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_3	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_4	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_5	0	ns min	A0 to $\overline{RFS}$ Hold Time
t_6	4 × $t_{CLK\ IN}$ + 20	ns max	$\overline{RFS}$ Low to SCLK Falling Edge
t_7[6]	4 × $t_{CLK\ IN}$ +20	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_8[6]	$t_{CLK\ IN}$/2	ns min	SCLK Falling Edge to Data Valid Delay
	$t_{CLK\ IN}$/2 + 30	ns max	
t_9	$t_{CLK\ IN}$/2	ns nom	SCLK High Pulse Width
t_{10}	3 × $t_{CLK\ IN}$/2	ns nom	SCLK Low Pulse Width
t_{14}	50	ns min	A0 to $\overline{TFS}$ Setup Time
t_{15}	0	ns min	A0 to $\overline{TFS}$ Hold Time
t_{16}	4 × $t_{CLK\ IN}$ + 20	ns max	$\overline{TFS}$ to SCLK Falling Edge Delay Time
t_{17}	4 × $t_{CLK\ IN}$	ns min	$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{18}	0	ns min	Data Valid to SCLK Setup Time
t_{19}	10	ns min	Data Valid to SCLK Hold Time
External-Clocking Mode			
f_{SCLK}	$f_{CLK\ IN}$/5	MHz max	Serial Clock Input Frequency
t_{20}	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Setup Time
t_{21}	0	ns min	$\overline{DRDY}$ to $\overline{RFS}$ Hold Time
t_{22}	2 × $t_{CLK\ IN}$	ns min	A0 to $\overline{RFS}$ Setup Time
t_{23}	0	ns min	A0 to $\overline{RFS}$ Hold Time
t_{24}[6]	4 × $t_{CLK\ IN}$	ns max	Data Access Time ($\overline{RFS}$ Low to Data Valid)
t_{25}[6]	10	ns min	SCLK Falling Edge to Data Valid Delay
	2 × $t_{CLK\ IN}$ + 20	ns max	
t_{26}	2 × $t_{CLK\ IN}$	ns min	SCLK High Pulse Width
t_{27}	2 × $t_{CLK\ IN}$	ns min	SCLK Low Pulse Width
t_{28}	$t_{CLK\ IN}$ + 10	ns max	SCLK Falling Edge to $\overline{DRDY}$ High
t_{29}[7]	10	ns min	SCLK to Data Valid Hold Time
	$t_{CLK\ IN}$ + 10	ns max	
t_{30}	10	ns min	$\overline{RFS}$/$\overline{TFS}$ to SCLK Falling Edge Hold Time
t_{31}[7]	5 × $t_{CLK\ IN}$/2 + 50	ns max	$\overline{RFS}$ to Data Valid Hold Time
t_{32}	0	ns min	A0 to $\overline{TFS}$ Setup Time
t_{33}	0	ns min	A0 to $\overline{TFS}$ Hold Time
t_{34}	4 × $t_{CLK\ IN}$	ns min	SCLK Falling Edge to $\overline{TFS}$ Hold Time
t_{35}	2 × $t_{CLK\ IN}$ – SCLK High	ns min	Data Valid to SCLK Setup Time
t_{36}	30	ns min	Data Valid to SCLK Hold Time

NOTES

[1]Guaranteed by design, not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]See Figures 10 to 13.

[3]CLK IN duty cycle range is 45% to 55%. CLK IN must be supplied whenever the AD7713 is not in standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7713 is production tested with $f_{CLK\ IN}$ at 2 MHz. It is guaranteed by characterization to operate at 400 kHz.

[5]Specified using 10% and 90% points on waveform of interest.

[6]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[7]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 100 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

AV_{DD} to AGND . . . . . –0.3 V to +12 V
AV_{DD} to DGND . . . . . –0.3 V to +12 V
DV_{DD} to AGND . . . . . –0.3 V to +6 V
DV_{DD} to DGND . . . . . –0.3 V to +6 V
AGND to DGND . . . . . –0.3 V to +6 V
AIN1, AIN2 Input Voltage
to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
AIN3 Input Voltage to AGND . . . . . –0.3 V to +22 V
Reference Input Voltage to AGND . . . –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND . . . –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (A Version) . . . . . –40°C to +85°C
Extended (S Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
PDIP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 105°C/W
Lead Temperature, Soldering (10 sec) . . . . . 260°C
CERDIP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 70°C/W
Lead Temperature, Soldering . . . . . 300°C
SOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 secs) . . . . . 220°C
Power Dissipation (Any Package) to 75°C . . . . . 450 mW

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7713AN	–40°C to +85°C	N-24
AD7713AR	–40°C to +85°C	RW-24
AD7713AR-REEL	–40°C to +85°C	RW-24
AD7713AR-REEL7	–40°C to +85°C	RW-24
AD7713AQ	–40°C to +85°C	Q-24
AD7713SQ	–55°C to +125°C	Q-24

*N = PDIP; Q = CERDIP; RW = SOIC.

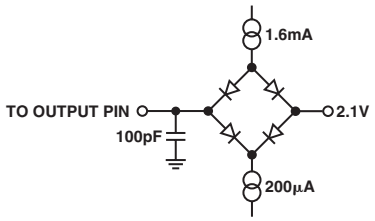
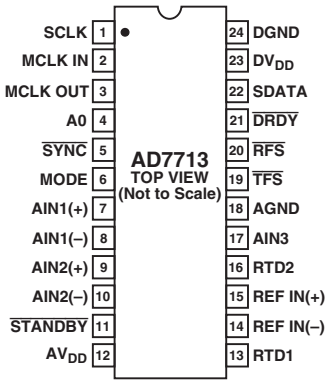


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7713 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
PDIP, CERDIP, AND SOIC



PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Logic input/output, depending on the status of the MODE pin. When MODE is high, the device is in its self-clocking mode, and the SCLK pin provides a serial clock output. This SCLK becomes active when $\overline{RFS}$ or $\overline{TFS}$ goes low, and it goes high impedance when either $\overline{RFS}$ or $\overline{TFS}$ returns high or when the device has completed transmission of an output word. When MODE is low, the device is in its external clocking mode and the SCLK pin acts as an input. This input serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7713 in smaller batches of data.
2	MCLK IN	Master Clock Signal for the Device. This can be provided in the form of a crystal or external clock. A crystal can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The clock input frequency is nominally 2 MHz.
3	MCLK OUT	When the master clock for the device is a crystal, the crystal is connected between MCLK IN and MCLK OUT.
4	A0	Address Input. With this input low, reading and writing to the device is to the control register. With this input high, access is to either the data register or the calibration registers.
5	$\overline{SYNC}$	Logic Input. Allows for synchronization of the digital filters when using a number of AD7713s. It resets the nodes of the digital filter.
6	MODE	Logic Input. When this pin is high, the device is in its self-clocking mode. With this pin low, the device is in its external clocking mode.
7	AIN1(+)	Analog Input Channel 1. Positive input of the programmable gain differential analog input. The AIN1(+) input is connected to an output current source that can be used to check that an external transducer has burnt out or gone open circuit. This output current source can be turned on/off via the control register.
8	AIN1(–)	Analog Input Channel 1. Negative input of the programmable gain differential analog input.
9	AIN2(+)	Analog Input Channel 2. Positive input of the programmable gain differential analog input.
10	AIN2(–)	Analog Input Channel 2. Negative input of the programmable gain differential analog input.
11	$\overline{STANDBY}$	Logic Input. Taking this pin low shuts down the internal analog and digital circuitry, reducing power consumption to less than 100 μW.
12	AV_{DD}	Analog Positive Supply Voltage, 5 V to 10 V.
13	RTD1	Constant Current Output. A nominal 200 μA constant current is provided at this pin, which can be used as the excitation current for RTDs. This current can be turned on or off via the control register.
14	REF IN(–)	Reference Input. The REF IN(–) can lie anywhere between AV_{DD} and AGND, provided REF IN(+) is greater than REF IN(–).
15	REF IN(+)	Reference Input. The reference input is differential providing that REF IN(+) is greater than REF IN(–). REF IN(+) can lie anywhere between AV_{DD} and AGND.

Pin No.	Mnemonic	Function
16	RTD2	Constant Current Output. A nominal 200 μA constant current is provided at this pin, which can be used as the excitation current for RTDs. This current can be turned on or off via the control register. This second current can be used to eliminate lead resistanced errors in 3-wire RTD configurations.
17	AIN3	Analog Input Channel 3. High level analog input that accepts an analog input voltage range of $4 \times V_{REF}$/GAIN. At the nominal V_{REF} of 2.5 V and a gain of 1, the AIN3 input voltage range is 0 V to ±10 V.
18	AGND	Ground Reference Point for Analog Circuitry.
19	$\overline{TFS}$	Transmit Frame Synchronization. Active low logic input used to write serial data to the device with serial data expected after the falling edge of this pulse. In the self-clocking mode, the serial clock becomes active after $\overline{TFS}$ goes low. In the external clocking mode, $\overline{TFS}$ must go low before the first bit of the data-word is written to the part.
20	$\overline{RFS}$	Receive Frame Synchronization. Active low logic input used to access serial data from the device. In the self-clocking mode, both the SCLK and SDATA lines become active after $\overline{RFS}$ goes low. In the external clocking mode, the SDATA line becomes active after $\overline{RFS}$ goes low.
21	$\overline{DRDY}$	Logic Output. A falling edge indicates that a new output word is available for transmission. The $\overline{DRDY}$ pin will return high upon completion of transmission of a full output word. $\overline{DRDY}$ is also used to indicate when the AD7713 has completed its on-chip calibration sequence.
22	SDATA	Serial Data. Input/output with serial data being written to either the control register or the calibration registers and serial data being accessed from the control register, calibration registers, or the data register. During an output data read operation, serial data becomes active after $\overline{RFS}$ goes low (provided $\overline{DRDY}$ is low). During a write operation, valid serial data is expected on the rising edges of SCLK when $\overline{TFS}$ is low. The output data coding is natural binary for unipolar inputs and offset binary for bipolar inputs.
23	DV_{DD}	Digital Supply Voltage, 5 V. DV_{DD} should not exceed AV_{DD} by more than 0.3 V in normal operation.
24	DGND	Ground Reference Point for Digital Circuitry.

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000...000 to 000...001) and full scale, a point 0.5 LSB above the last code transition (111...110 to 111...111). The error is expressed as a percentage of full scale.

Positive Full-Scale Error

Positive full-scale error is the deviation of the last code transition (111...110 to 111...111) from the ideal input full-scale voltage. For AIN1(+) and AIN2(+), the ideal full-scale input voltage is (AIN1(–) + V_{REF}/GAIN – 3/2 LSBs), where AIN(–) is either AIN1(–) or AIN2(–) as appropriate; for AIN3, the ideal full-scale voltage is $4 \times V_{REF}$/GAIN – 3/2 LSBs. Positive full-scale error applies to both unipolar and bipolar analog input ranges.

Unipolar Offset Error

Unipolar offset error is the deviation of the first code transition from the ideal voltage. For AIN1(+) and AIN2(+), the ideal input voltage is (AIN1(–) + 0.5 LSB); for AIN3, the ideal input is 0.5 LSB when operating in the unipolar mode.

Bipolar Zero Error

This is the deviation of the midscale transition (0111 ... 111 to 1000 ... 000) from the ideal input voltage. For AIN1(+) and AIN2(+), the ideal input voltage is (AIN1(–) – 0.5 LSB); AIN3 can accommodate only unipolar input ranges.

Bipolar Negative Full-Scale Error

This is the deviation of the first code transition from the ideal input voltage. For AIN1(+) and AIN2(+), the ideal input voltage is (AIN1(–) – V_{REF}/GAIN + 0.5 LSB); AIN3 can only accommodate unipolar input ranges.

Positive Full-Scale Overrange

Positive full-scale overrange is the amount of overhead available to handle input voltages on AIN1(+) and AIN2(+) inputs greater than (AIN1(–) + V_{REF}/GAIN) or on AIN3 of greater than $4 \times V_{REF}$/GAIN (for example, noise peaks or excess voltages due to system gain errors in system calibration routines) without introducing errors due to overloading the analog modulator or to overflowing the digital filter.

Negative Full-Scale Overrange

This is the amount of overhead available to handle voltages on AIN1(+) and AIN2(+) below (AIN1(–) – V_{REF}/GAIN) without overloading the analog modulator or overflowing the digital filter.

Offset Calibration Range

In the system calibration modes, the AD7713 calibrates its offset with respect to the analog input. The offset calibration range specification defines the range of voltages that the AD7713 can accept and still calibrate offset accurately.

Full-Scale Calibration Range

This is the range of voltages that the AD7713 can accept in the system calibration mode and still calibrate full scale correctly.

Input Span

In system calibration schemes, two voltages applied in sequence to the AD7713's analog input define the analog input range. The input span specification defines the minimum and maximum input voltages from zero to full scale that the AD7713 can accept and still calibrate gain accurately.

CONTROL REGISTER (24 BITS)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register. The control register is 24 bits wide. When writing to the register, 24 bits of data must be written; otherwise, the data will not be loaded to the control register. In other words, it is not possible to write just the first 12 bits of data into the control register. If more than 24 clock pulses are provided before $\overline{TFS}$ returns high, then all clock pulses after the 24th clock pulse are ignored. Similarly, a read operation from the control register should access 24 bits of data.

MSB

MD2	**MD1**	**MD0**	**G2**	**G1**	**G0**	**CH1**	**CH0**	**WL**	**RO**	**BO**	**B/U**
FS11	**FS10**	**FS9**	**FS8**	**FS7**	**FS6**	**FS5**	**FS4**	**FS3**	**FS2**	**FS1**	**FS0**

LSB

Operating Mode			
MD2	**MD1**	**MD0**	**Operating Mode**
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device with A0 high accesses data from the data register. This is the default condition of these bits after the internal power-on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH0 and CH1. This is a 1-step calibration sequence, and when complete, the part returns to normal mode (with MD2, MD1, MD0 of the control registers returning to 0, 0, 0). The $\overline{DRDY}$ output indicates when this self-calibration is complete. For this calibration type, the zero-scale calibration is done internally on shorted (zeroed) inputs, and the full-scale calibration is done on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH0 and CH1. This is a 2-step calibration sequence, with the zero-scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero-scale calibration is complete. The part returns to normal mode at the end of this first step in the 2-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when the full-scale calibration is complete. When this calibration is complete, the part returns to normal mode.
1	0	0	Activate System Offset Calibration. This activates system offset calibration on the channel selected by CH0 and CH1. This is a 1-step calibration sequence and, when complete, the part returns to normal mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero-scale calibration is done on the selected input channel, and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH0 and CH1. If the background calibration mode is on, the AD7713 provides continuous self-calibration of the reference and shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of 6. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, the shorted (zeroed) inputs and V_{REF}, as well as the analog input voltage, are continuously monitored, and the calibration registers of the device are updated.
1	1	0	Read/Write Zero-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero-scale calibration coefficients of the channel selected by CH0 and CH1. A write to the device with A0 high writes data to the zero-scale calibration coefficients of the channel selected by CH0 and CH1. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written; otherwise, the new data will not be transferred to the calibration register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH0 and CH1. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH0 and CH1. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written; otherwise, the new data will not be transferred to the calibration register.

PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition after the Internal Power-On Reset)
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH1	CH0	Channel	
0	0	AIN1	(Default Condition after the Internal Power-On Reset)
0	1	AIN2	
1	0	AIN3	

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition after the Internal Power-On Reset)
1	24-Bit	

RTD Excitation Currents

RO		
0	Off	(Default Condition after the Internal Power-On Reset)
1	On	

Burn-Out Current

BO		
0	Off	(Default Condition after the Internal Power-On Reset)
1	On	

Bipolar/Unipolar Selection (Both Inputs)

B/U		
0	Bipolar	(Default Condition after the Internal Power-On Reset)
1	Unipolar	

Filter Selection (FS11 to FS0)

The on-chip digital filter provides a $sinc^3$ (or $(sinx/x)^3$) filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter, and the data rate for the part. In association with the gain selection, it also determines the output noise (and therefore the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/code$ where *code* is the decimal equivalent of the code in Bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 2 MHz, this results in a first notch frequency range from 1.952 Hz to 205.59 kHz. To ensure correct operation of the AD7713, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figures 2a and 2b show the effect of the filter notch frequency and gain on the effective resolution of the AD7713. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 10 Hz, then a new word is available at a 10 Hz rate or every 100 ms. If the first notch is at 200 Hz, a new word is available every 5 ms.

The settling time of the filter to a full-scale step input change is worst case $4 \times 1/(Output\ Data\ Rate)$. This settling time is to 100% of the final value. For example, with the first filter notch at 100 Hz, the settling time of the filter to a full-scale step input change is 400 ms max. If the first notch is at 200 Hz, the settling time of the filter to a full-scale input step is 20 ms max. This settling time can be reduced to $3 \times 1/(Output\ Data\ Rate)$ by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with $\overline{SYNC}$ low, the settling time will be $3 \times 1/(Output\ Data\ Rate)$. If a change of channels takes place, the settling time is $3 \times 1/(Output\ Data\ Rate)$ regardless of the $\overline{SYNC}$ input.

The –3 dB frequency is determined by the programmed first notch frequency according to the relationship:

$$Filter - 3\ dB\ Frequency = 0.262 \times First\ Notch\ Frequency$$

Tables I and II show the output rms noise for some typical notch and –3 dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of 2.5 V. These numbers are typical and are generated with an analog input voltage of 0 V. The output noise from the part comes from two sources. First, there is the electrical noise in the semiconductor devices used in the implementation of the modulator (device noise). Second, when the analog input signal is converted into the digital domain, quantization noise is added. The device noise is at a low level and is largely independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 12 Hz approximately) tend to be device noise dominated while higher notch settings are dominated by quantization noise. Changing the filter notch and cutoff frequency in the quantization noise dominated region results in a more dramatic improvement in noise performance than it does in the device noise dominated region as shown in Table I. Furthermore, quantization noise is added after the PGA, so effective resolution is independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA and, therefore, effective resolution suffers a little at high gains for lower notch frequencies.

At the lower filter notch settings (below 12 Hz), the no missing codes performance of the device is at the 24-bit level. At the higher settings, more codes will be missed until at 200 Hz notch setting, no missing codes performance is guaranteed only to the 12-bit level. However, since the effective resolution of the part is 10.5 bits for this filter notch setting; this no missing codes performance should be more than adequate for all applications.

The effective resolution of the device is defined as the ratio of the output rms noise to the input full scale. This does not remain constant with increasing gain or with increasing bandwidth. Table II is the same as Table I except that the output is expressed in terms of effective resolution (the magnitude of the rms noise with respect to $2 \times V_{REF}$/GAIN, i.e., the input full scale). It is possible to do post filtering on the device to improve the output data rate for a given –3 dB frequency and also to further reduce the output noise (see the Digital Filtering section).

Table I. Output Noise vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate[1]	–3 dB Frequency	Typical Output RMS Noise (μV)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
2 Hz[2]	0.52 Hz	1.0	0.78	0.48	0.33	0.25	0.25	0.25	0.25
5 Hz[2]	1.31 Hz	1.8	1.1	0.63	0.5	0.44	0.41	0.38	0.38
6 Hz[2]	1.57 Hz	2.5	1.31	0.84	0.57	0.46	0.43	0.4	0.4
10 Hz[2]	2.62 Hz	4.33	2.06	1.2	0.64	0.54	0.46	0.46	0.46
12 Hz[2]	3.14 Hz	5.28	2.36	1.33	0.87	0.63	0.62	0.6	0.56
20 Hz[3]	5.24 Hz	13	6.4	3.7	1.8	1.1	0.9	0.65	0.65
50 Hz[3]	13.1 Hz	130	75	25	12	7.5	4	2.7	1.7
100 Hz[3]	26.2 Hz	0.6×10^3	0.26×10^3	140	70	35	25	15	8
200 Hz[3]	52.4 Hz	3.1×10^3	1.6×10^3	0.7×10^3	0.29×10^3	180	120	70	40

NOTES
[1]The default condition (after the internal power-on reset) for the first notch of filter is 60 Hz.
[2]For these filter notch frequencies, the output rms noise is primarily dominated by device noise, and, as a result, is independent of the value of the reference voltage. Therefore, increasing the reference voltage will give an increase in the effective resolution of the device (i.e., the ratio of the rms noise to the input full scale is increased since the output rms noise remains constant as the input full scale increases).
[3]For these filter notch frequencies, the output rms noise is dominated by quantization noise, and, as a result, is proportional to the value of the reference voltage.

Table II. Effective Resolution vs. Gain and First Notch Frequency

First Notch of Filter and O/P Data Rate	–3 dB Frequency	Effective Resolution* (Bits)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
2 Hz	0.52 Hz	22.5	21.5	21.5	21	20.5	19.5	18.5	17.5
5 Hz	1.31 Hz	21.5	21	21	20	19.5	18.5	17.5	16.5
6 Hz	1.57 Hz	21	21	20.5	20	19.5	18.5	17.5	16.5
10 Hz	2.62 Hz	20	20	20	19.5	19	18.5	17.5	16.5
12 Hz	3.14 Hz	20	20	20	19.5	19	18	17	16
20 Hz	5.24 Hz	18.5	18.5	18.5	18.5	18	17.5	17	16
50 Hz	13.1 Hz	15	15	15.5	15.5	15.5	15.5	15	14.5
100 Hz	26.2 Hz	13	13	13	13	13	12.5	12.5	12.5
200 Hz	52.4 Hz	10.5	10.5	11	11	11	10.5	10	10

*Effective resolution is defined as the magnitude of the output rms noise with respect to the input full scale (i.e., $2 \times V_{REF}$/GAIN). Table II applies for a V_{REF} of 2.5 V and resolution numbers are rounded to the nearest 0.5 LSB.

Figures 2a and 2b gives similar information to that outlined in Table I. In this plot, the output rms noise is shown for the full range of available cutoff frequencies rather than for some typical cutoff frequencies as in Tables I and II. The numbers given in these plots are typical values at 25°C.

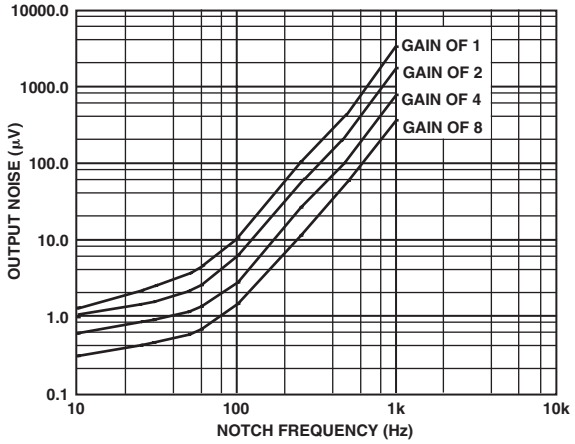


Figure 2a. Plot of Output Noise vs. Gain and Notch Frequency (Gains of 1 to 8)

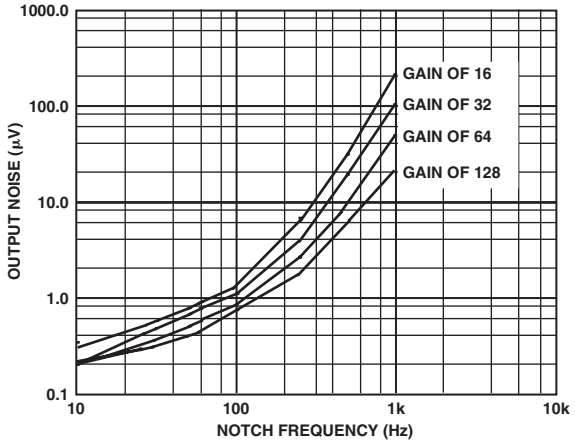


Figure 2b. Plot of Output Noise vs. Gain and Notch Frequency (Gains of 16 to 128)

CIRCUIT DESCRIPTION

The AD7713 is a Σ-Δ ADC with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals, such as those in industrial control or process control applications. It contains a Σ-Δ (or charge balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter, and a bidirectional serial communications port.

The part contains three analog input channels, two programmable gain differential input channels, and one programmable gain high-level single-ended input channel. The gain range on both inputs is from 1 to 128. For the AIN1 and AIN2 inputs, this means that the input can accept unipolar signals of between 0 mV to 20 mV and 0 V to 2.5 V or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals 2.5 V. The input voltage range for the AIN3 input is $4 \times V_{REF}$/GAIN and is 0 V to 10 V with the nominal reference of 2.5 V and a ANALOG gain of 1. The input signal to the selected analog input channel is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain (see Table III). A charge balancing ADC (Σ-Δ modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this Σ-Δ modulator with the input sampling frequency being modified to give the higher gains. A $sinc^3$ digital low-pass filter processes the output of the Σ-Δ modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and therefore its –3 dB frequency) can be programmed via an on-chip control register. The programmable range for this first notch frequency is from 1.952 Hz to 205.59 Hz, giving a programmable range for the –3 dB frequency of 0.52 Hz to 53.9 Hz.

The basic connection diagram for the part is shown in Figure 3. This shows the AD7713 in the external clocking mode with both the AV_{DD} and DV_{DD} pins of the AD7713 being driven from the analog 5 V supply. Some applications will have separate supplies for both AV_{DD} and DV_{DD}, and in some of these cases, the analog supply will exceed the 5 V digital supply (see the Power Supplies and Grounding section).

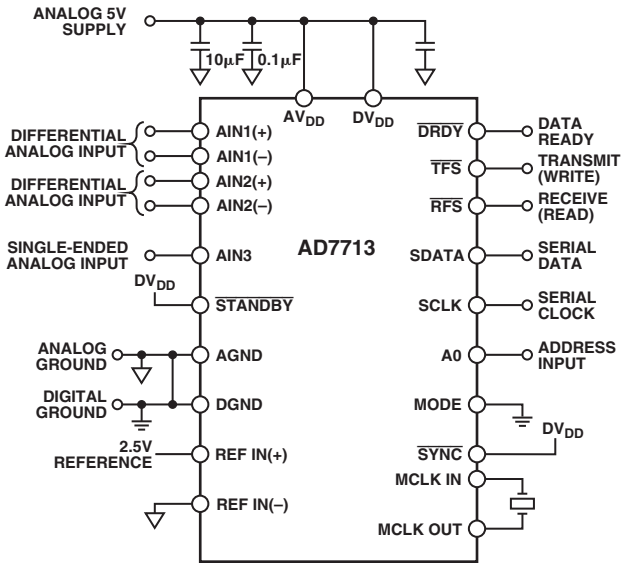


Figure 3. Basic Connection Diagram

The AD7713 provides a number of calibration options that can be programmed via the on-chip control register. A calibration cycle can be initiated at any time by writing to this control register. The part can perform self-calibration using the on-chip calibration microcontroller and SRAM to store calibration parameters. Other system components may also be included in the calibration loop to remove offset and gain errors in the input channel using the system calibration mode. Another option is a background calibration mode where the part continuously performs self-calibration and updates the calibration coefficients. Once the part is in this mode, the user does not have to worry about issuing periodic calibration commands to the device or asking the device to recalibrate when there is a change in the ambient temperature or power supply voltage.

The AD7713 gives the user access to the on-chip calibration registers, allowing the microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in E^2PROM. This gives the microprocessor much greater control over the AD7713's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM.

For battery-operated or low power systems, the AD7713 offers a standby mode (controlled by the $\overline{\text{STANDBY}}$ pin) that reduces idle power consumption to typically 150 μW.

THEORY OF OPERATION

The general block diagram of a Σ-Δ ADC is shown in Figure 4. It contains the following elements:

- A sample-hold amplifier
- A differential amplifier or subtracter
- An analog low-pass filter
- A 1-bit ADC (comparator)
- A 1-bit DAC

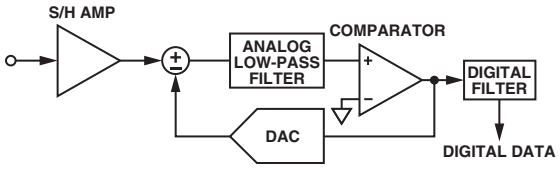


Figure 4. General Σ-Δ ADC

In operation, the analog signal sample is fed to the subtracter, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal sampling frequency (oversampling).

Oversampling is fundamental to the operation of Σ-Δ ADCs. Using the quantization noise formula for an ADC

$$SNR = \left(6.02 \times Number\ of\ Bits + 1.76\right) dB$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

The AD7713 samples the input signal at a frequency of 7.8 kHz or greater (see Table III). As a result, the quantization noise is spread over a much wider frequency than that of the band of interest. The noise in the band of interest is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies outside the bandwidth of interest. The noise performance is thus improved from this 1-bit level to the performance outlined in Tables I and II and in Figures 2a and 2b.

The output of the comparator provides the digital input for the 1-bit DAC, so that the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data-word using a digital filter.

Σ-Δ ADCs are generally described by the order of the analog low-pass filter. A simple example of a first-order Σ-Δ ADC is shown in Figure 5. This contains only a first-order low-pass filter or integrator. It also illustrates the derivation of the alternative name for these devices: charge balancing ADCs.

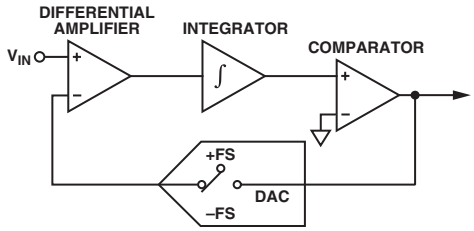


Figure 5. Basic Charge-Balancing ADC

It consists of a differential amplifier (whose output is the difference between the analog input and the output of a 1-bit DAC), an integrator, and a comparator. The term *charge balancing* comes from the fact that this system is a negative feedback loop that tries to keep the net charge on the integrator capacitor at 0 by balancing charge injected by the input voltage with charge injected by the 1-bit DAC. When the analog input is 0, the only contribution to the integrator output comes from the 1-bit DAC. For the net charge on the integrator capacitor to be 0, the DAC output must spend half its time at +FS and half its time at –FS. Assuming ideal components, the duty cycle of the comparator will be 50%.

When a positive analog input is applied, the output of the 1-bit DAC must spend a larger proportion of the time at +FS, so the duty cycle of the comparator increases. When a negative input voltage is applied, the duty cycle decreases.

The AD7713 uses a second-order Σ-Δ modulator and a digital filter that provides a rolling average of the sampled output. After power-up or if there is a step change in the input voltage, there is a settling time that must elapse before valid data is obtained.

Input Sample Rate

The modulator sample frequency for the device remains at $f_{CLK\ IN}/512$ (3.9 kHz @ $f_{CLK\ IN}$ = 2 MHz) regardless of the selected gain. However, gains greater than ×1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of the reference capacitor to input capacitor. As a result of the multiple sampling, the input the sample rate of the device varies with the selected gain (see Table III). The effective input impedance is $1/C \times f_S$, where C is the input sampling capacitance and f_S is the input sample rate.

Table III. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLK\ IN}/256$ (7.8 kHz @ $f_{CLK\ IN}$ = 2 MHz)
2	$2 \times f_{CLK\ IN}/256$ (15.6 kHz @ $f_{CLK\ IN}$ = 2 MHz)
4	$4 \times f_{CLK\ IN}/256$ (31.2 kHz @ $f_{CLK\ IN}$ = 2 MHz)
8	$8 \times f_{CLK\ IN}/256$ (62.4 kHz @ $f_{CLK\ IN}$ = 2 MHz)
16	$8 \times f_{CLK\ IN}/256$ (62.4 kHz @ $f_{CLK\ IN}$ = 2 MHz)
32	$8 \times f_{CLK\ IN}/256$ (62.4 kHz @ $f_{CLK\ IN}$ = 2 MHz)
64	$8 \times f_{CLK\ IN}/256$ (62.4 kHz @ $f_{CLK\ IN}$ = 2 MHz)
128	$8 \times f_{CLK\ IN}/256$ (62.4 kHz @ $f_{CLK\ IN}$ = 2 MHz)

DIGITAL FILTERING

The AD7713's digital filter behaves like a similar analog filter, with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this, and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7713 has overrange headroom built into the Σ-Δ modulator and digital filter, which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

Filter Characteristics

The cutoff frequency of the digital filter is determined by the value loaded to Bits FS0 to FS11 in the control register. At the maximum clock frequency of 2 MHz, the minimum cutoff frequency of the filter is 0.52 Hz, while the maximum programmable cutoff frequency is 53.9 Hz.

Figure 6 shows the filter frequency response for a cutoff frequency of 0.52 Hz, which corresponds to a first filter notch frequency of 2 Hz. This is a $(\sin x/x)^3$ response (also called sinc^3) that provides >100 dB of 50 Hz and 60 Hz rejection. Programming a different cutoff frequency via FS0 to FS11 does not alter the profile of the filter response; it changes the frequency of the notches as outlined in the Control Register section.

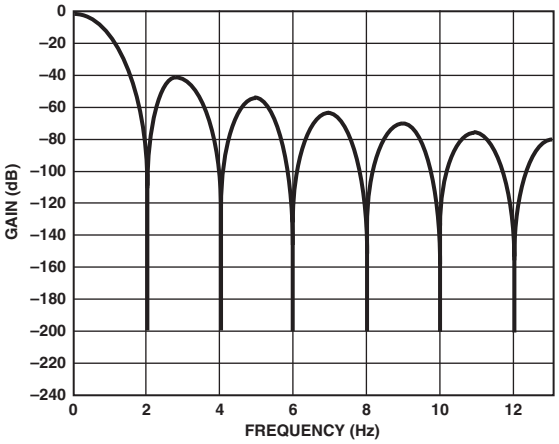


Figure 6. Frequency Response of AD7713 Filter

Since the AD7713 contains this on-chip, low-pass filtering, there is a settling time associated with step function inputs, and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the notch frequency chosen for the filter. The output data rate equates to this filter notch frequency, and the settling time of the filter to a full-scale step input is four times the output data period. In applications using both input channels, the settling time of the filter must be allowed to elapse before data from the second channel is accessed.

Post Filtering

The on-chip modulator provides samples at a 3.9 kHz output rate. The on-chip digital filter decimates these samples to provide data at an output rate that corresponds to the programmed first notch frequency of the filter. Since the output data rate exceeds the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. However, there may be some applications that require a higher data rate for a given bandwidth and noise performance. Applications that need this higher data rate will require some post filtering following the digital filter of the AD7713.

For example, if the required bandwidth is 1.57 Hz but the required update rate is 20 Hz, the data can be taken from the AD7713 at the 20 Hz rate giving a –3 dB bandwidth of 5.24 Hz. Post filtering can be applied to this to reduce the bandwidth and output noise, to the 1.57 Hz bandwidth level, while maintaining an output rate of 20 Hz.

Post filtering can also be used to reduce the output noise from the device for bandwidths below 0.52 Hz. At a gain of 128, the output rms noise is 250 nV. This is essentially device noise or white noise, and since the input is chopped, the noise has a flat frequency response. By reducing the bandwidth below 0.52 Hz, the noise in the resultant pass band can be reduced. A reduction in bandwidth by a factor of 2 results in a $\sqrt{2}$ reduction in the output rms noise. This additional filtering will result in a longer settling time.

Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency (n × 3.9 kHz, where n = 1, 2, 3...). This means that there are frequency bands, $\pm f_3$ dB wide (f_3 dB is cutoff frequency selected by FS0 to FS11), where noise passes unattenuated to the output. However, due to the AD7713's high oversampling ratio, these bands occupy only a small fraction of the spectrum, and most broadband noise is filtered. In any case, because of the high oversampling ratio, a simple, RC, single-pole filter is generally sufficient to attenuate the signals in these bands on the analog input and thus provide adequate antialiasing filtering.

If passive components are placed in front of the AIN1 and AIN2 inputs of the AD7713, care must be taken to ensure that the source impedance is low enough so as not to introduce gain errors in the system. The dc input impedance for the AIN1 and AIN2 inputs is over 1 GΩ. The input appears as a dynamic load that varies with the clock frequency and with the selected gain (see Figure 7). The input sample rate, as shown in Table III, determines the time allowed for the analog input capacitor, C_{IN}, to be charged. External impedances result in a longer charge time for this capacitor, which result in gain errors being introduced on the analog inputs. Both inputs of the differential input channels look into similar input circuitry.

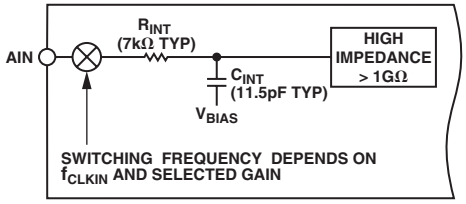


Figure 7. AIN1, AIN2 Input Impedance

In any case, the error introduced due to longer charging times is a gain error that can be removed using the system calibration capabilities of the AD7713 provided that the resultant span is within the span limits of the system calibration techniques for the AD7713.

The AIN3 input contains a resistive attenuation network as outlined in Figure 8. The typical input impedance on this input is 44 kΩ. As a result, the AIN3 input should be driven from a low impedance source.

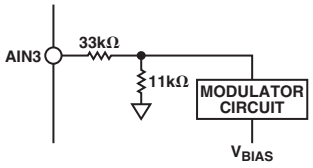


Figure 8. AIN3 Input Impedance

ANALOG INPUT FUNCTIONS

Analog Input Ranges

The analog inputs on the AD7713 provide the user with considerable flexibility in terms of analog input voltage ranges. Two of the inputs are differential, programmable-gain, input channels that can handle either unipolar or bipolar input signals. The common-mode range of these inputs is from AGND to AV_{DD}, provided that the absolute value of the analog input voltage lies between AGND – 30 mV and AV_{DD} + 30 mV. The third analog input is a single-ended, programmable gain high-level input that accepts analog input ranges of 0 to 4 × V_{REF}/GAIN.

The dc input leakage current on the AIN1 and AIN2 inputs is 10 pA maximum at 25°C (±1 nA over temperature). This results in a dc offset voltage developed across the source impedance. However, this dc offset effect can be compensated for by a combination of the differential input capability of the part and its system calibration mode. The dc input current on the AIN3 input depends on the input voltage. For the nominal input voltage range of 10 V, the input current is 225 μA typ.

Burn Out Current

The AIN1(+) input of the AD7713 contains a 1 μA current source that can be turned on/off via the control register. This current source can be used in checking that a transducer has not burnt out or gone open circuit before attempting to take measurements on that channel. If the current is turned on and is allowed flow into the transducer and a measurement of the input voltage on the AIN1 input is taken, it can indicate that the transducer is not functioning correctly. For normal operation, this burn out current is turned off by writing a 0 to the BO bit in the control register.

RTD Excitation Currents

The AD7713 also contains two matched 200 μA constant current sources which are provided at the RTD1 and RTD2 pins of the device. These currents can be turned on/off via the control register. Writing a 1 to the RO bit of the control register enables these excitation currents.

For 4-wire RTD applications, one of these excitation currents is used to provide the excitation current for the RTD; the second current source can be left unconnected. For 3-wire RTD configurations, the second on-chip current source can be used to eliminate errors due to voltage drops across lead resistances. Figures 19 and 20 in the Application section show some RTD configurations with the AD7713.

The temperature coefficient of the RTD current sources is typically 20 ppm/°C with a typical matching between the temperature coefficients of both current sources of 3 ppm/°C. For applications where the absolute value of the temperature coefficient is too large, the following schemes can be used to remove the drift error.

The conversion result from the AD7713 is ratiometric to the V_{REF} voltage. Therefore, if the V_{REF} voltage varies with the RTD temperature coefficient, the temperature drift from the current source will be removed. For 4-wire RTD applications, the reference voltage can be made ratiometric to the RTD current source by using the second current with a low TC resistor to generate the reference voltage for the part. In this case, if a 12.5 kΩ resistor is used, the 200 μA current source generates 2.5 V across the resistor. This 2.5 V can be applied to the REF IN(+) input of the AD7713 and the REF IN(–) input at ground will supply a V_{REF} of 2.5 V for the part. For 3-wire RTD configurations, the reference voltage for the part is generated by placing a low TC resistor (12.5 kΩ for 2.5 V reference) in series with one of the constant current sources. The RTD current sources can be driven to within 2 V of AV_{DD}. The reference input of the AD7713 is differential so the REF IN(+) and REF IN(–) of the AD7713 are driven from either side of the resistor. Both schemes ensure that the reference voltage for the part tracks the RTD current sources over temperature and, thereby, removes the temperature drift error.

Bipolar/Unipolar Inputs

Two analog inputs on the AD7713 can accept either unipolar or bipolar input voltage ranges while the third channel accepts only unipolar signals. Bipolar or unipolar options for AIN1 and AIN2 are chosen by programming the B/U bit of the control register. This programs both channels for either unipolar or bipolar operation. Programming the part for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding. The data coding is binary for unipolar inputs and offset binary for bipolar inputs.

The AIN1 and AIN2 input channels are differential, and as a result, the voltage to which the unipolar and bipolar signals are referenced is the voltage on the AIN1(–) and AIN2(–) inputs. For example, if AIN1(–) is 1.25 V and the AD7713 is configured for unipolar operation with a gain of 1 and a V_{REF} of 2.5 V, the input voltage range on the AIN1(+) input is 1.25 V to 3.75 V. For the AIN3 input, the input signals are referenced to AGND.

REFERENCE INPUT

The reference inputs of the AD7713, REF IN(+) and REF IN(–), provide a differential reference input capability. The common-mode range for these differential inputs is from V_{SS} to AV_{DD}. The nominal differential voltage, V_{REF} (REF IN(+) – REF IN(–)), is 2.5 V for specified operation, but the reference voltage can go to 5 V with no degradation in performance, provided that the absolute value of REF IN(+) and REF IN(–) does not exceed its AV_{DD} and AGND limits. The part is also functional with V_{REF} voltages down to 1 V, but with degraded performance as the output noise will, in terms of LSB size, be larger. REF IN(+) must always be greater than REF IN(–) for correct operation of the AD7713.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs. The maximum dc input leakage current is 10 pA (±1 nA over temperature), and source resistance may result in gain errors on the part. The reference inputs

look like the AIN1 analog input (see Figure 7). In this case, R_{INT} is 5 kΩ typ and C_{INT} varies with gain. The input sample rate is $f_{CLK\ IN}/256$ and does not vary with gain. For gains of 1 to 8, C_{INT} is 20 pF; for a gain of 16, it is 10 pF; for a gain of 32, it is 5 pF; for a gain of 64, it is 2.5 pF; and for a gain of 128, it is 1.25 pF.

The digital filter of the AD7713 removes noise from the reference input just as it does with the analog input, and the same limitations apply regarding lack of noise rejection at integer multiples of the sampling frequency. The output noise performance outlined in Tables I and II assumes a clean reference. If the reference noise in the bandwidth of interest is excessive, it can degrade the performance of the AD7713. A recommended reference source for the AD7713 is the AD680, a 2.5 V reference.

USING THE AD7713 SYSTEM DESIGN CONSIDERATIONS

The AD7713 operates differently from successive approximation ADCs or integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate determined by the first notch of the filter, and the output can be read at any time, either synchronously or asynchronously.

Clocking

The AD7713 requires a master clock input, which may be an external TTL/CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal of the correct frequency can be connected between MCLK IN and MCLK OUT, in which case the clock circuit will function as a crystal controlled oscillator. For lower clock frequencies, a ceramic resonator may be used instead of the crystal. For these lower frequency oscillators, external capacitors may be required on either the ceramic resonator or on the crystal.

The input sampling frequency, the modulator sampling frequency, the –3 dB frequency, output update rate, and calibration time are all directly related to the master clock frequency, $f_{CLK\ IN}$. Reducing the master clock frequency by a factor of two will halve the above frequencies and update rate and will double the calibration time.

The current drawn from the DV_{DD} power supply is also directly related to $f_{CLK\ IN}$. Reducing $f_{CLK\ IN}$ by a factor of two will halve the DV_{DD} current but will not affect the current drawn from the AV_{DD} power supply.

System Synchronization

If multiple AD7713s are operated from a common master clock, they can be synchronized to update their output registers simultaneously. A falling edge on the $\overline{SYNC}$ input resets the filter and places the AD7713 into a consistent, known state. A common signal to the AD7713's $\overline{SYNC}$ inputs will synchronize their operation. This would normally be done after each AD7713 has performed its own calibration or has had calibration coefficients loaded to it.

The $\overline{SYNC}$ input can also be used to reset the digital filter in systems where the turn-on time of the digital power supply (DV_{DD}) is very long. In such cases, the AD7713 will start operating internally before the DV_{DD} line has reached its minimum operating level, 4.75 V. With a low DV_{DD} voltage, the AD7713's internal digital filter logic does not operate correctly. Thus, the AD7713 may have clocked itself into an incorrect operating condition by the time that DV_{DD} has reached its correct level. The digital filter will be reset upon issue of a calibration, command (whether it is self-calibration, system calibration or background calibration) to the AD7713. This ensures correct operation of the AD7713. In systems where the power-on default conditions of the AD7713 are acceptable, and no calibration is performed after power-on, issuing a $\overline{SYNC}$ pulse to the AD7713 will reset the AD7713's digital filter logic. An R, C on the $\overline{SYNC}$ line, with R, C time constant longer than the DV_{DD} power-on time, will perform the $\overline{SYNC}$ function.

Accuracy

Σ-Δ ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity, and inherently offer no missing codes performance. The AD7713 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7713 uses digital calibration techniques that minimize offset and gain error.

Autocalibration

Autocalibration on the AD7713 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected gain, filter notch, or bipolar/unipolar input range. However, if the AD7713 is in its background calibration mode, the above changes are all automatically taken care of (after the settling time of the filter has been allowed for).

The AD7713 offers self-calibration, system calibration, and background calibration facilities. For calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are zero-scale and full-scale points. With these readings, the microcontroller can calculate the gain slope for the input to output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of either 16 bits or 24 bits.

The AD7713 also provides the facility to write to the on-chip calibration registers, and, in this manner, the span and offset for the part can be adjusted by the user. The offset calibration register contains a value that is subtracted from all conversion results, while the full-scale calibration register contains a value that is multiplied by all conversion results. The offset calibration coefficient is subtracted from the result prior to the multiplication by the full-scale coefficient. In the first three modes outlined here, the $\overline{DRDY}$ line indicates that calibration is complete by going low. If $\overline{DRDY}$ is low before (or goes low during) the calibration command, it may take up to one modulator cycle before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, the $\overline{DRDY}$ line should be ignored for up to one modulator cycle after the last bit of the calibration command is written to the control register.

Self-Calibration

In the self-calibration mode with a unipolar input range, the zero-scale point used in determining the calibration coefficients is with both inputs shorted and the full-scale point is V_{REF}. The zero-scale coefficient is determined by converting an internal shorted inputs node. The full-scale coefficient is determined from the span between this shorted inputs conversion and a conversion on an internal V_{REF} node. The self-calibration mode

is invoked by writing the appropriate values (0, 0, 1) to the MD2, MD1, and MD0 bits of the control register. In this calibration mode, the shorted inputs node is switched in to the modulator first and a conversion is performed; the V_{REF} node is then switched in, and another conversion is performed. When the calibration sequence is complete, the calibration coefficients updated, and the filter resettled to the analog input voltage, the $\overline{DRDY}$ output goes low. The self-calibration procedure takes into account the selected gain on the PGA.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points that the AD7713 calibrates are midscale (bipolar zero) and positive full scale.

System Calibration

System calibration allows the AD7713 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented by the system to the AIN inputs for the zero-scale and full-scale points. System calibration is a 2-step process. The zero-scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. System calibration is initiated by writing the appropriate values (0, 1, 0) to the MD2, MD1, and MD0 bits of the control register. The $\overline{DRDY}$ output from the device will signal when the step is complete by going low. After the zero-scale point is calibrated, the full-scale point is applied and the second step of the calibration process is initiated by again writing the appropriate values (0, 1, 1) to MD2, MD1, and MD0. Again, the full-scale voltage must be set up before the calibration is initiated, and it must remain stable throughout the calibration step. $\overline{DRDY}$ goes low at the end of this second step to indicate that the system calibration is complete. In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

This 2-step system calibration mode offers another feature. After the sequence has been completed, additional offset or gain calibrations can be performed by themselves to adjust the zero reference point or the system gain. This is achieved by performing the first step of the system calibration sequence (by writing 0, 1, 0 to MD2, MD1, and MD0). This will adjust the zero-scale or offset point but will not change the slope factor from what was set during a full system calibration sequence.

System calibration can also be used to remove any errors from an antialiasing filter on the analog input. A simple R, C antialiasing filter on the front end may introduce a gain error on the analog input voltage but the system calibration can be used to remove this error.

System Offset Calibration

System offset calibration is a variation of both the system calibration and self-calibration. In this case, the zero-scale point for the system is presented to the AIN input of the converter. System offset calibration is initiated by writing 1, 0, 0 to MD2, MD1, and MD0. The system zero-scale coefficient is determined by converting the voltage applied to the AIN input, while the full-scale coefficient is determined from the span between this AIN conversion and a conversion on V_{REF}. The zero-scale point should be applied to the AIN input for the duration of the calibration sequence. This is a 1-step calibration sequence with $\overline{DRDY}$ going low when the sequence is completed. In the unipolar mode, the system offset calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale and positive full scale.

Background Calibration

The AD7713 also offers a background calibration mode where the part interleaves its calibration procedure with its normal conversion sequence. In the background calibration mode, the same voltages are used as the calibration points as are used in the self-calibration mode, i.e., shorted inputs and V_{REF}. The background calibration mode is invoked by writing 1, 0, 1 to MD2, MD1, and MD0 of the control register. When invoked, the background calibration mode reduces the output data rate of the AD7713 by a factor of 6 while the –3 dB bandwidth remains unchanged. Its advantage is that the part is continually performing calibration and automatically updating its calibration coefficients. As a result, the effects of temperature drift, supply sensitivity and time drift on zero- and full-scale errors are automatically removed. When the background calibration mode is turned on, the part will remain in this mode until Bits MD2, MD1, and MD0 of the control register are changed. With background calibration mode on, the first result from the AD7713 will be incorrect as the full-scale calibration will not have been performed. For a step change on the input, the second output update will have settled to 100% of the final value.

Table IV summarizes the calibration modes and the calibration points associated with them. It also gives the duration from when the calibration is invoked to when valid data is available to the user.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span that can be accommodated. The range of input span in both the unipolar and bipolar modes for AIN1 and AIN2 has a minimum value of $0.8 \times V_{REF}/GAIN$ and a maximum value of $2.1 \times V_{REF}/GAIN$. For AIN3, the minimum value is $3.2 \times V_{REF}/GAIN$, while the maximum value is $4.2 \times V_{REF}/GAIN$.

Table IV. Calibration Truth Table

Calibration Type	MD2, MD1, MD0	Zero-Scale Calibration	Full-Scale Calibration	Sequence	Duration
Self-Calibration	0, 0, 1	Shorted Inputs	V_{REF}	1-Step	9 × 1/Output Rate
System Calibration	0, 1, 0	AIN		2-Step	4 × 1/Output Rate
System Calibration	0, 1, 1		AIN	2-Step	4 × 1/Output Rate
System Offset Calibration	1, 0, 0	AIN	V_{REF}	1-Step	9 × 1/Output Rate
Background Calibration	1, 0, 1	Shorted Inputs	V_{REF}	1-Step	6 × 1/Output Rate

The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. This offset range is limited by the requirement that the positive full-scale calibration limit is ≤ 1.05 × V_{REF}/GAIN for AIN1 and AIN2. Therefore, the offset range plus the span range cannot exceed 1.05 × V_{REF}/GAIN for AIN1 and AIN2. If the span is at its minimum (0.8 × V_{REF}/GAIN), the maximum the offset can be is (0.25 × V_{REF}/GAIN) for AIN1 and AIN2. For AIN3, both ranges are multiplied by a factor of 4.

In the bipolar mode, the system offset calibration range is again restricted by the span range. The span range of the converter in bipolar mode is equidistant around the voltage used for the zero-scale point, thus the offset range plus half the span range cannot exceed (1.05 × V_{REF}/GAIN) for AIN1 and AIN2. If the span is set to 2 × V_{REF}/GAIN, the offset span cannot move more than ±(0.05 × V_{REF}/GAIN) before the endpoints of the transfer function exceed the input overrange limits ±(1.05 × V_{REF}/GAIN) for AIN1. If the span range is set to the minimum ±(0.4 × V_{REF}/GAIN), the maximum allowable offset range is ±(0.65 × V_{REF}/GAIN) for AIN1 and AIN2. The AIN3 input can only be used in the unipolar mode.

POWER-UP AND CALIBRATION

On power-up, the AD7713 performs an internal reset, which sets the contents of the control register to a known state. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7713 are low and no warm-up time is required before the initial calibration is performed. However, the external reference must have stabilized before calibration is initiated.

Drift Considerations

The AD7713 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter or by operating the part in the background calibration mode. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES AND GROUNDING

The analog and digital supplies to the AD7713 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital supply (DV_{DD}) must not exceed the analog positive supply (AV_{DD}) by more than 0.3 V. If separate analog and digital supplies are used, the recommended decoupling scheme is shown in Figure 9. In systems where AV_{DD} = 5 V and DV_{DD} = 5 V, it is recommended that AV_{DD} and DV_{DD} are driven from the same 5 V supply, although each supply should be decoupled separately as shown in Figure 9. It is preferable that the common supply is the system's analog 5 V supply.

It is also important that power is applied to the AD7713 before signals at REF IN, AIN, or the logic input pins in order to avoid excessive current. If separate supplies are used for the AD7713 and the system digital circuitry, then the AD7713 should be powered up first. If it is not possible to guarantee this, then current limiting resistors should be placed in series with the logic inputs.

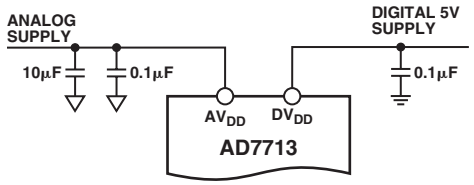


Figure 9. Recommended Decoupling Scheme

DIGITAL INTERFACE

The AD7713's serial communications port provides a flexible arrangement to allow easy interfacing to industry-standard microprocessors, microcontrollers, and digital signal processors. A serial read to the AD7713 can access data from the output register, the control register, or from the calibration registers. A serial write to the AD7713 can write data to the control register or the calibration registers.

Two different modes of operation are available, optimized for different types of interface where the AD7713 can act either as master in the system (it provides the serial clock) or as slave (an external serial clock can be provided to the AD7713). These two modes, labeled self-clocking mode and external clocking mode, are discussed in detail in the following sections.

Self-Clocking Mode

The AD7713 is configured for its self-clocking mode by tying the MODE pin high. In this mode, the AD7713 provides the serial clock signal used for the transfer of data to and from the AD7713. This self-clocking mode can be used with processors that allow an external device to clock their serial port, including most digital signal processors and microcontrollers, such as the 68HC11 and 68HC05. It also allows easy interfacing, to serial parallel conversion circuits in systems with parallel data communication, allowing interfacing to 74XX299 universal shift registers without any additional decoding. In the case of shift registers, the serial clock line should have a pull-down resistor instead of the pull-up resistor shown in Figure 10 and Figure 11.

Read Operation

Data can be read from either the output register, the control register, or the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0 signal must remain valid for the duration of the serial read operation. With A0 high, data is accessed from either the output register or from the calibration registers. With A0 low, data is accessed from the control register.

The function of the $\overline{DRDY}$ line is dependent on only the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ goes low when a new data-word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If data is not read from the output register, the $\overline{DRDY}$ line will remain low. The output register will continue to be updated at the output update rate, but $\overline{DRDY}$ will not indicate this. A read from the device in this circumstance will access the most recent

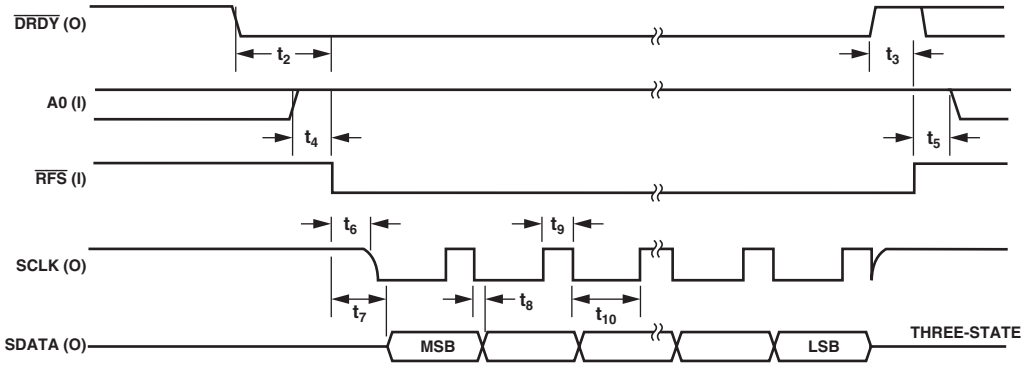


Figure 10. Self-Clocking Mode, Output Data Read Operation

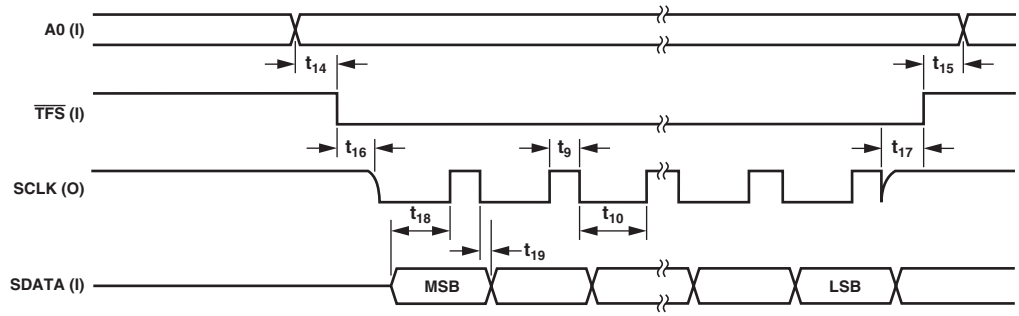


Figure 11. Self-Clocking Mode, Control/Calibration Register Write Operation

word in the output register. If a new data-word becomes available to the output register while data is being read from the output register, DRDY will not indicate this and the new data-word will be lost to the user. DRDY is not affected by reading from the control register or the calibration registers.

Data can be accessed from the output data register only when DRDY is low. If RFS goes low with DRDY high, no data transfer will take place. DRDY does not have any effect on reading data from the control register or from the calibration registers.

Figure 10 shows a timing diagram for reading from the AD7713 in the self-clocking mode. This read operation shows a read from the AD7713's output data register. A read from the control register or calibration registers is similar, but, in these cases, the DRDY line is not related to the read function. Depending on the output update rate, it can go low at any stage in the control/calibration register read cycle without affecting the read and its status should be ignored. A read operation from either the control or calibration registers must always read 24 bits of data from the respective register.

Figure 10 shows a read operation from the AD7713. For the timing diagram shown, it is assumed that there is a pull-up resistor on the SCLK output. With DRDY low, the RFS input is brought low. RFS going low enables the serial clock of the AD7713 and also places the MSB of the word on the serial data line. All subsequent data bits are clocked out on a high-to-low transition of the serial clock and are valid prior to the following rising edge of this clock. The final active falling edge of SCLK clocks out the LSB, and this LSB is valid prior to the final active rising edge of SCLK. Coincident with the next falling edge of SCLK, DRDY is reset high. DRDY going high turns off the SCLK and the SDATA outputs, this means that the data hold time for the LSB is slightly shorter than for all other bits.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the DRDY line, and the write operation does not have any effect on the status of DRDY. A write operation to the control register or the calibration register must always write 24 bits to the respective register.

Figure 11 shows a write operation to the AD7713. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. The falling edge of TFS enables the internally generated SCLK output. The serial data to be loaded to the AD7713 must be valid on the rising edge of this SCLK signal. Data is clocked into the AD7713 on the rising edge of the SCLK signal, with the MSB transferred first. On the last active high time of SCLK, the LSB is loaded to the AD7713. Subsequent to the next falling edge of SCLK, the SCLK output is turned off. (The timing diagram of Figure 11 assumes a pull-up resistor on the SCLK line.)

External Clocking Mode

The AD7713 is configured for its external clocking mode by tying the MODE pin low. In this mode, SCLK of the AD7713 is configured as an input, and an external serial clock must be provided to this SCLK pin. This external clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output, including microcontrollers, such as the 80C51, 87C51, 68HC11, and 68HC05, and most digital signal processors.

Read Operation

As with the self-clocking mode, data can be read from either the output register, the control register, or the calibration registers. A0 determines whether the data read accesses data from the control register or from the output/calibration registers. This A0

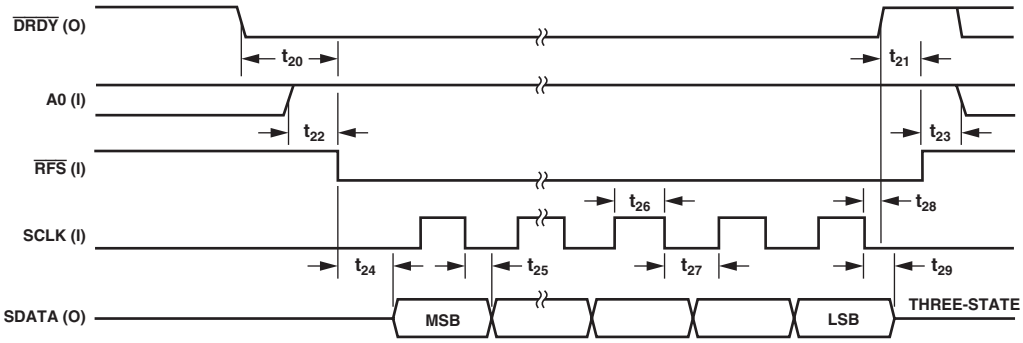


Figure 12a. External Clocking Mode, Output Data Read Operation

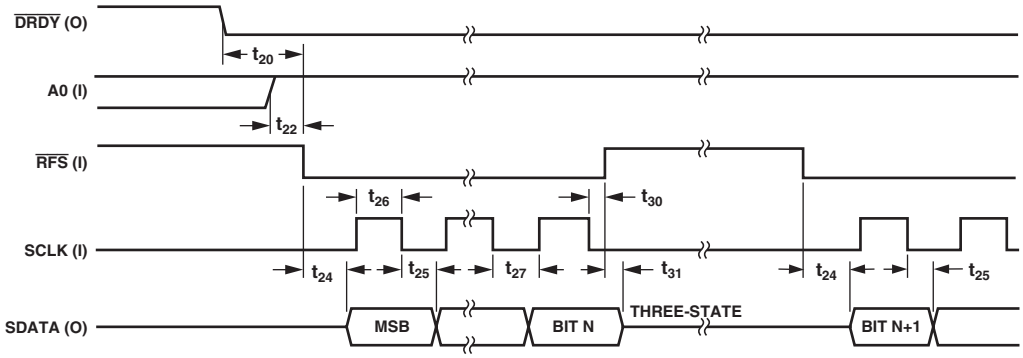


Figure 12b. External Clocking Mode, Output Data Read ($\overline{RFS}$ Returns High During Read Operation)

signal must remain valid for the duration of the serial read operation. With A0 high, data is accessed from either the output register or from the calibration registers. With A0 low, data is accessed from the control register.

The function of the $\overline{DRDY}$ line is dependent on only the output update rate of the device and the reading of the output data register. $\overline{DRDY}$ goes low when a new data-word is available in the output data register. It is reset high when the last bit of data (either 16th bit or 24th bit) is read from the output register. If data is not read from the output register, the $\overline{DRDY}$ line will remain low. The output register will continue to be updated at the output update rate, but $\overline{DRDY}$ will not indicate this. A read from the device in this circumstance will access the most recent word in the output register. If a new data-word becomes available to the output register while data is being read from the output register, $\overline{DRDY}$ will not indicate this, and the new data-word will be lost to the user. $\overline{DRDY}$ is not affected by reading from the control register or the calibration register.

Data can be accessed from the output data register only when $\overline{DRDY}$ is low. If $\overline{RFS}$ goes low while $\overline{DRDY}$ is high, no data transfer will take place. $\overline{DRDY}$ does not have any effect on reading data from the control register or from the calibration registers.

Figures 12a and 12b show timing diagrams for reading from the AD7713 in the external clocking mode. Figure 12a shows a situation where all the data is read from the AD7713 in one read operation. Figure 12b shows a situation where the data is read from the AD7713 over a number of read operations. Both read operations show a read from the AD7713's output data register. A read from the control register or calibration registers is similar, but in these cases, the $\overline{DRDY}$ line is not related to the read function. Depending on the output update rate, it can go low at any stage in the control/calibration register read cycle without affecting the read and its status should be ignored. A read operation from either the control or calibration registers must always read 24 bits of data from the respective register.

Figure 12a shows a read operation from the AD7713 where $\overline{RFS}$ remains low for the duration of the data-word transmission. With $\overline{DRDY}$ low, the $\overline{RFS}$ input is brought low. The input SCLK signal should be low between read and write operations. $\overline{RFS}$ going low places the MSB of the word to be read on the serial data line. All subsequent data bits are clocked out on a high-to-low transition of the serial clock and are valid prior to the following rising edge of this clock. The penultimate falling edge of SCLK clocks out the LSB and the final falling edge resets the $\overline{DRDY}$ line high. This rising edge of $\overline{DRDY}$ turns off the serial data output.

Figure 12b shows a timing diagram for a read operation where $\overline{RFS}$ returns high during the transmission of the word and returns low again to access the rest of the data-word. Timing parameters and functions are very similar to that outlined for Figure 12a, but Figure 12b has a number of additional times to show timing relationships when $\overline{RFS}$ returns high in the middle of transferring a word.

$\overline{RFS}$ should return high during a low time of SCLK. On the rising edge of $\overline{RFS}$, the SDATA output is turned off. $\overline{DRDY}$ remains low and will remain low until all bits of the data-word are read from the AD7713, regardless of the number of times $\overline{RFS}$ changes state during the read operation. Depending on the time between the falling edge of SCLK and the rising edge of $\overline{RFS}$, the next bit (BIT N + 1) may appear on the data bus before $\overline{RFS}$ goes high. When $\overline{RFS}$ returns low again, it activates the SDATA output. When the entire word is transmitted, the

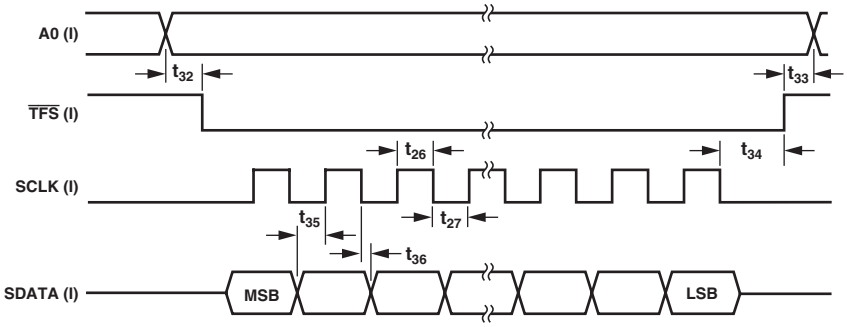


Figure 13a. External Clocking Mode, Control/Calibration Register Write Operation

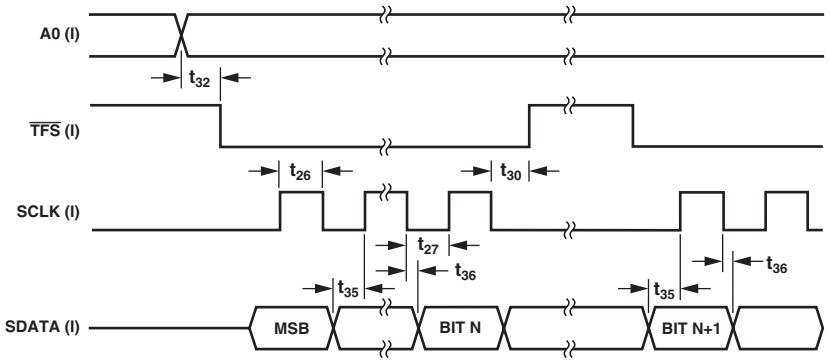


Figure 13b. External Clocking Mode, Control/Calibration Register Write Operation (TFS Returns High During Write Operation)

DRDY line will go high, turning off the SDATA output as per Figure 12a.

Write Operation

Data can be written to either the control register or calibration registers. In either case, the write operation is not affected by the DRDY line, and the write operation does not have any effect on the status of DRDY. A write operation to the control register or the calibration register must always write 24 bits to the respective register.

Figure 13a shows a write operation to the AD7713 with TFS remaining low for the duration of the write operation. A0 determines whether a write operation transfers data to the control register or to the calibration registers. This A0 signal must remain valid for the duration of the serial write operation. As before, the serial clock line should be low between read and write operations. The serial data to be loaded to the AD7713 must be valid on the high level of the externally applied SCLK signal. Data is clocked into the AD7713 on the high level of this SCLK signal with the MSB transferred first. On the last active high time of SCLK, the LSB is loaded to the AD7713.

Figure 13b shows a timing diagram for a write operation to the AD7713 with TFS returning high during the write operation and returning low again to write the rest of the data-word. Timing parameters and functions are very similar to that outlined for Figure 13a, but Figure 13b has a number of additional times to show timing relationships when TFS returns high in the middle of transferring a word.

Data to be loaded to the AD7713 must be valid prior to the rising edge of the SCLK signal. TFS should return high during the low time of SCLK. After TFS returns low again, the next bit of the data-word to be loaded to the AD7713 is clocked in on the next high level of the SCLK input. On the last active high time of the SCLK input, the LSB is loaded to the AD7713.

SIMPLIFYING THE EXTERNAL CLOCKING MODE INTERFACE

In many applications, the user may not require the facility of writing to the on-chip calibration registers. In this case, the serial interface to the AD7713 in external clocking mode can be simplified by connecting the TFS line to the A0 input of the AD7713 (see Figure 14). This means that any write to the device will load data to the control register (since A0 is low while TFS is low), and any read to the device will access data from the output data register or from the calibration registers (since A0 is high while RFS is low). It should be noted that in this arrangement, the user does not have the capability of reading from the control register. Another method of simplifying the interface is to generate the TFS signal from an inverted RFS signal. However, generating the signals the opposite way around (RFS from an inverted TFS) will cause writing errors.

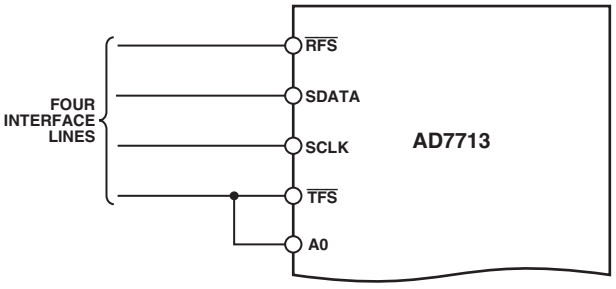


Figure 14. Simplified Interface with TFS Connected to A0

MICROCOMPUTER/MICROPROCESSOR INTERFACING

The AD7713's flexible serial interface allows easy interface to most microcomputers and microprocessors. Figure 15 shows a flowchart diagram for a typical programming sequence for reading data from the AD7713 to a microcomputer, while Figure 16 shows a flowchart diagram for writing data to the AD7713. Figures 17 and 18 show some typical interface circuits.

The flowchart in Figure 15 is for continuous read operations from the AD7713 output register. In the example shown, the $\overline{DRDY}$ line is continuously polled. Depending on the microprocessor configuration, the $\overline{DRDY}$ line may come to an interrupt input, in which case the $\overline{DRDY}$ will automatically generate an interrupt without being polled. Reading the serial buffer could be anything from one read operation up to three read operations (where 24 bits of data are read into an 8-bit serial register). A read operation to the control/calibration registers is similar, but, in this case, the status of $\overline{DRDY}$ can be ignored. The A0 line is brought low when the $\overline{RFS}$ line is brought low when reading from the control register.

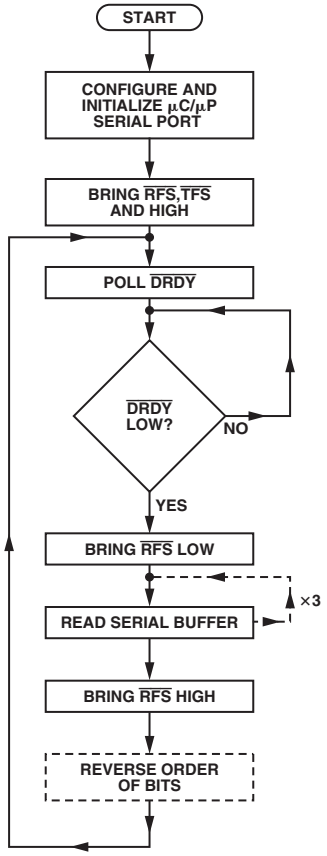


Figure 15. Flowchart for Continuous Read Operation to the AD7713

The flowchart also shows the bits being reversed after they have been read in from the serial port. This depends on whether the microprocessor expects the MSB of the word first or the LSB of the word first. The AD7713 outputs the MSB first.

The flowchart in Figure 16 is for a single 24-bit write operation to the AD7713 control or calibration registers. This shows data being transferred from data memory to the accumulator before being written to the serial buffer. Some microprocessor systems will allow data to be written directly to the serial buffer from data memory. Writing data to the serial buffer from the accumulator will generally consist of either two or three write operations, depending on the size of the serial buffer.

The flowchart also shows the option of the bits being reversed before being written to the serial buffer. This depends on whether the first bit transmitted by the microprocessor is the MSB or the LSB. The AD7713 expects the MSB as the first bit in the data stream. In cases where the data is being read or being written in bytes and the data has to be reversed, the bits will have to be reversed for every byte.

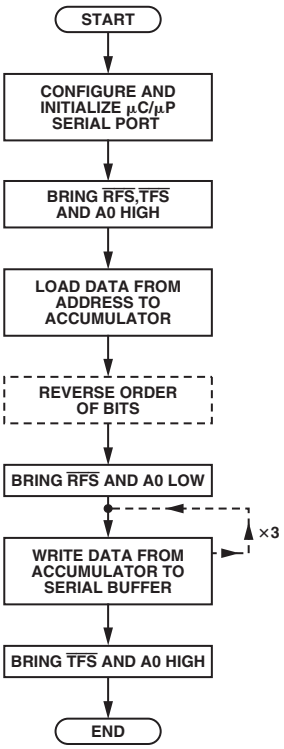


Figure 16. Flowchart for Single Write Operation to the AD7713

AD7713 to 8XC51 Interface

Figure 17 shows an interface between the AD7713 and the 8XC51 microcontroller. The AD7713 is configured for its external clocking mode, while the 8XC51 is configured in its Mode 0 serial interface mode. The $\overline{DRDY}$ line from the AD7713 is connected to the Port P1.2 input of the 8XC51, so the $\overline{DRDY}$ line is polled by the 8XC51. The $\overline{DRDY}$ line can be connected to the INT1 input of the 8XC51 if an interrupt driven system is preferred.

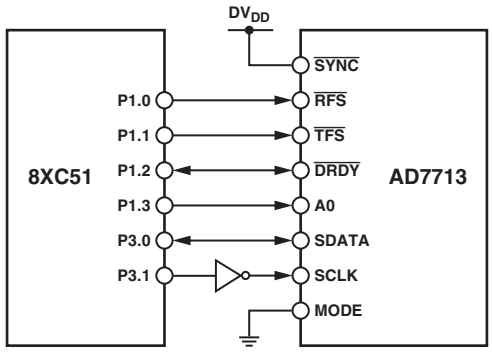


Figure 17. AD7713 to 8XC51 Interface

Table V shows some typical 8XC51 code used for a single 24-bit read from the output register of the AD7713. Table V shows some typical code for a single write operation to the control register of the AD7713. The 8XC51 outputs the LSB first in a write operation while the AD7713 expects the MSB first, so the data to be transmitted has to be rearranged before being written to the output serial register. Similarly, the AD7713 outputs the MSB first during a read operation while the 8XC51 expects the LSB first. Therefore, the data which is read into the serial buffer needs to be rearranged before the correct data-word from the AD7713 is available in the accumulator.

Table V. 8XC51 Code for Reading from the AD7713

```
MOV SCON,#00010001B;   Configure 8051 for MODE 0
   MOV IE,#00010000B;  Disable All Interrupts
   SETB 90H;           Set P1.0, Used as RFS
   SETB 91H;           Set P1.1, Used as TFS
   SETB 93H;           Set P1.3, Used as A0
   MOV R1,#003H;       Sets Number of Bytes to Be Read
                       in A Read Operation
   MOV R0,#030H;       Start Address for Where Bytes
                       Will Be Loaded
   MOV R6,#004H;       Use P1.2 as DRDY
WAIT:
   NOP;
   MOV A,P1;           Read Port 1
   ANL A,R6;           Mask Out All Bits Except DRDY
   JZ READ;            If Zero Read
   SJMP WAIT;          Otherwise Keep Polling
READ:
   CLR 90H;            Bring RFS Low
   CLR 98H;            Clear Receive Flag
POLL:
   JB 98H, READ1       Tests Receive Interrupt Flag
   SJMP POLL
READ 1:
MOV A,SBUF;            Read Buffer
RLC A;                 Rearrange Data
MOV B.0,C;             Reverse Order of Bits
  RLC A; MOV B.1,C; RLC A; MOV B.2,C;
  RLC A; MOV B.3,C; RLC A; MOV B.4,C;
  RLC A; MOV B.5,C; RLC A; MOV B.6,C;
  RLC A; MOV B.7,C;
  MOV A,B;
  MOV @R0,A;   Write Data to Memory
  INC R0;      Increment Memory Location
  DEC R1       Decrement Byte Counter
  MOV A,R1
  JZ END       Jump if Zero
  JMP WAIT     Fetch Next Byte
END:
  SETB 90H     Bring RFS High
FIN:
  SJMP FIN
```

Table VI. 8XC51 Code for Writing to the AD7713

```
MOV SCON,#00000000B;   Configure 8051 for MODE 0
                       Operation and Enable Serial
                       Reception
MOV IE,#10010000B;     Enable Transmit Interrupt
MOV IP,#00010000B;     Prioritize the Transmit Interrupt
SETB 91H;              Bring TFS High
SETB 90H;              Bring RFS High
MOV R1,#003H;          Sets Number of Bytes to Be
                       Written in a Write Operation
MOV R0,#030H;          Start Address in RAM for Bytes
MOV A,#00H;            Clear Accumulator
MOV SBUF,A;            Initialize the Serial Port
WAIT:
JMP WAIT;              Wait for Interrupt
INT ROUTINE:
NOP;                   Interrupt Subroutine
MOV A,R1;              Load R1 to Accumulator
JZ FIN;                If Zero Jump to FIN
DEC R1;                Decrement R1 Byte Counter
MOV A,@R;              Move Byte into the Accumulator
INC R0;                Increment Address
RLC A;                 Rearrange Data—From LSB
                       First to MSB First
MOV B.0,C; RLC A; MOV B.1,C; RLC A;
MOV B.2,C; RLC A; MOV B.3,C; RLC A;
MOV B.4,C; RLC A; MOV B.5,C; RLC A;
MOV B.6,C; RLC A: MOV B.7,C; MOV A,B;
CLR 93H;               Bring A0 Low
CLR 91H;               Bring TFS Low
MOV SBUF,A;            Write to Serial Port
RETI;                  Return from Subroutine
FIN:
SETB 91H;              Set TFS High
SETB 93H;              Set A0 High
RETI;                  Return from Interrupt Subroutine
```

AD7713 to 68HC11 Interface

Figure 18 shows an interface between the AD7713 and the 68HC11 microcontroller. The AD7713 is configured for its external clocking mode, while the SPI port is used on the 68HC11, which is in its single chip mode. The DRDY line from the AD7713 is connected to the Port PC2 input of the 68HC11, so the DRDY line is polled by the 68HC11. The DRDY line can be connected to the IRQ input of the 68HC11 if an interrupt driven system is preferred. The 68HC11 MOSI and MISO lines should be configured for wired-OR operation. Depending on the interface configuration, it may be necessary to provide bidirectional buffers between the 68HC11 MOSI and MISO lines.

The 68HC11 is configured in the master mode with its CPOL bit set to a Logic 0 and its CPHA bit set to a Logic 1.

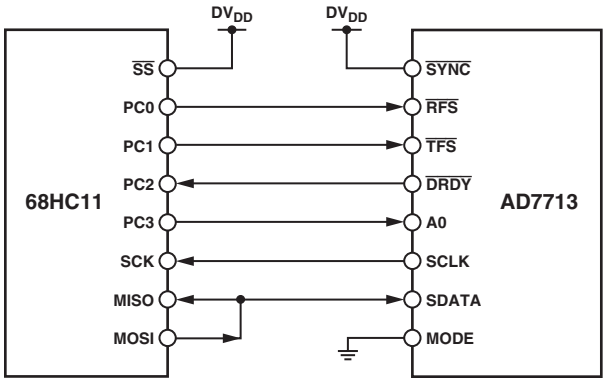


Figure 18. AD7713 to 68HC11 Interface

APPLICATIONS

4-Wire RTD Configurations

Figure 19 shows a 4-wire RTD application where the RTD transducer is interfaced directly to the AD7713. In the 4-wire configuration, there are no errors associated with lead resistances as no current flows in the measurement leads connected to AIN1(+) and AIN1(–). One of the RTD current sources is used to provide the excitation current for the RTD. A common nominal resistance value for the RTD is 100 Ω and, therefore, the RTD will generate a 20 mV signal, which can be handled directly by the analog input of the AD7713. In the circuit shown, the second RTD excitation current is used to generate the reference voltage for the AD7713. This reference voltage is developed across R_{REF} and applied to the differential reference inputs. For the nominal reference voltage of 2.5 V, R_{REF} is 12.5 kΩ. This scheme ensures that the analog input voltage span remains ratiometric to the reference voltage. Any errors in the analog input voltage due to the temperature drift of the RTD current source is compensated for by the variation in the reference voltage. The typical matching between the two RTD current sources is less than 3 ppm/°C.

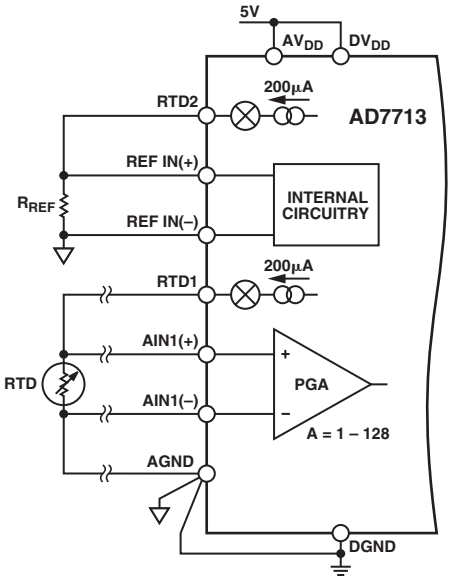


Figure 19. 4-Wire RTD Application with the AD7713

3-Wire RTD Configurations

Figure 20 shows a 3-wire RTD configuration using the AD7713. In the 3-wire configuration, the lead resistances will result in errors if only one current source is used as the 200 μA will flow through RL1 developing a voltage error between AIN1(+) and AIN1(–). In the scheme outlined below, the second RTD current source is used to compensate for the error introduced by the 200 μA flowing through RL1. The second RTD current flows through RL2. Assuming RL1 and RL2 are equal (the leads would normally be of the same material and of equal length) and RTD1 and RTD2 match, then the error voltage across RL2 equals the error voltage across RL1, and no error voltage is developed between AIN1(+) and AIN1(–). Twice the voltage is developed across RL3 but since this is a common-mode voltage, it will not introduce any errors. The reference voltage is derived from one of the current sources. This gives all the benefits of eliminating RTD temperature coefficient errors as outlined in Figure 19. The voltage on either RTD input can go to within 2 V of the AV_{DD} supply. The circuit is shown for a 2.5 V reference.

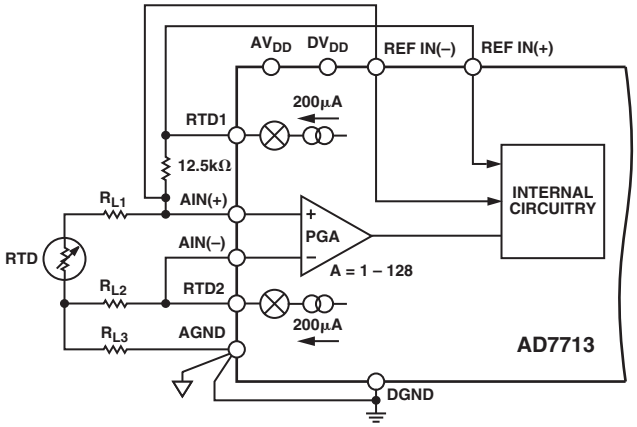


Figure 20. 3-Wire RTD Application with the AD7713

4–20 mA Loop

The AD7713's high level input can be used to measure the current in 4–20 mA loop applications as shown in Figure 21. In this case, the system calibration capabilities of the AD7713 can be used to remove the offset caused by the 4 mA flowing through the 500 Ω resistor. The AD7713 can handle an input span as low as 3.2 × V_{REF} (= 8 V with a V_{REF} of 2.5 V) even though the nominal input voltage range for the input is 10 V. Therefore, the full span of the ADC can be used for measuring the current between 4 and 20 mA.

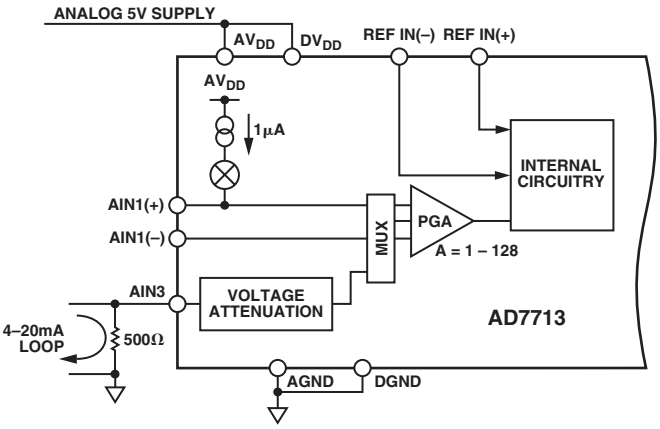


Figure 21. 4-20 mA Measurement Using the AD7713

OTHER 24-BIT SIGNAL CONDITIONING ADCS AVAILABLE FROM ANALOG DEVICES

AD7710

FEATURES

Charge Balancing
- **24 Bits No Missing Codes**
- **±0.0015% Nonlinearity**

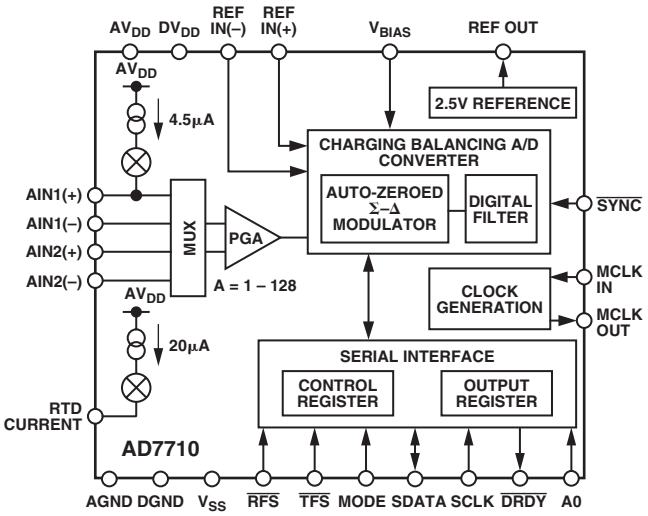
2-Channel Programmable Gain Front End
- **Gains from 1 to 128**
- **Differential Inputs**

Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single- or Dual-Supply Operation
Low Power (25 mW typ) with Power-Down Mode (7 mW typ)

APPLICATIONS

Weigh Scales
Thermocouples
Smart Transmitters
Chromatography

FUNCTIONAL BLOCK DIAGRAM



AD7711

FEATURES

Charge Balancing ADC
- **24 Bits No Missing Codes**
- **±0.0015% Nonlinearity**

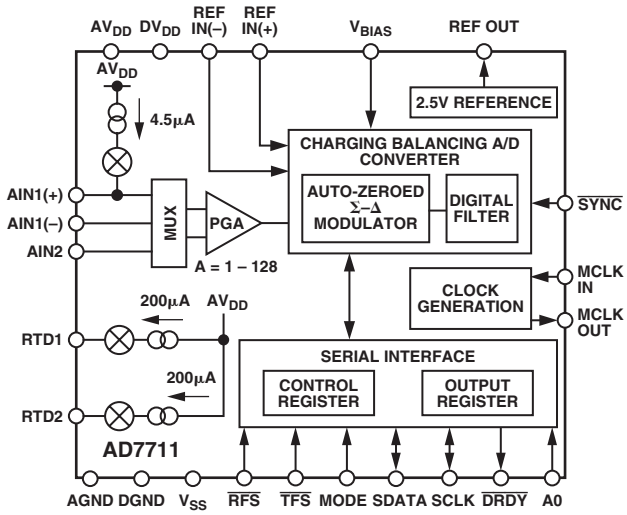
2-Channel Programmable Gain Front End
- **Gains from 1 to 128**
- **1 Differential Input**
- **1 Single-Ended Input**

Low-Pass Filter with Programmable Filter Cutoff
Ability to Read/Write Calibration Coefficients
RTD Excitation Current Sources
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single- or Dual-Supply Operation
Low Power (25 mW typ) with Power-Down Mode (7 mW typ)

APPLICATIONS

RTD Transducers
Process Control
Smart Transmitters
Portable Industrial Instruments

FUNCTIONAL BLOCK DIAGRAM



AD7712

FEATURES

Charge Balancing ADC
- 24 Bits No Missing Codes
- ±0.0015% Nonlinearity

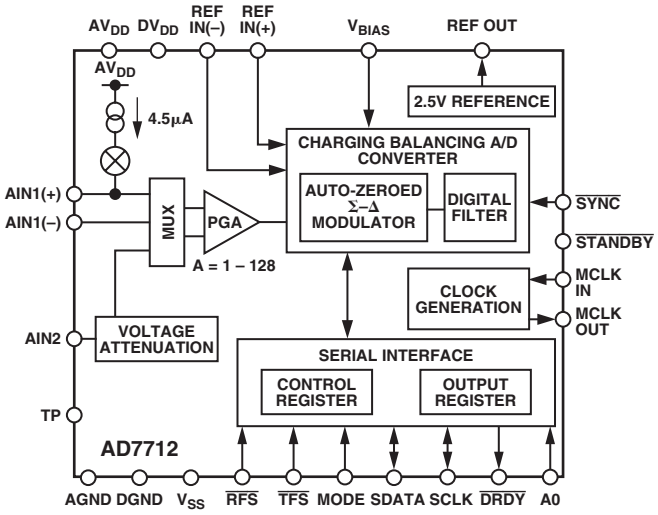
High Level and Low Level Analog Input Channels
Programmable Gain for Both Inputs
- Gains from 1 to 128
- Differential Input for Low Level Channel

Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single- or Dual-Supply Operation
Low Power (25 mW typ) with Power-Down Mode (100 μW typ)

APPLICATIONS

Process Control
Smart Transmitters
Portable Industrial Instruments

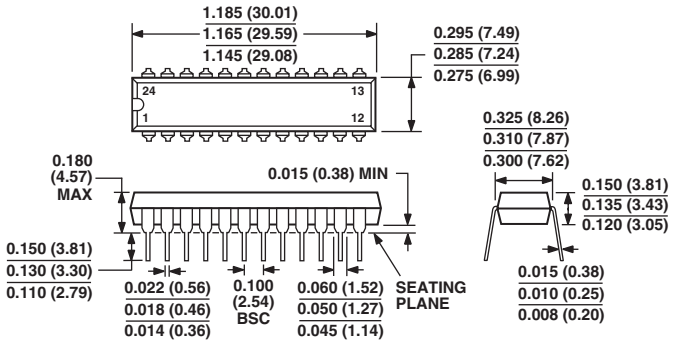
FUNCTIONAL BLOCK DIAGRAM



OUTLINE DIMENSIONS

24-Lead Plastic Dual In-Line Package [PDIP]
(N-24)

Dimensions shown in inches and (millimeters)

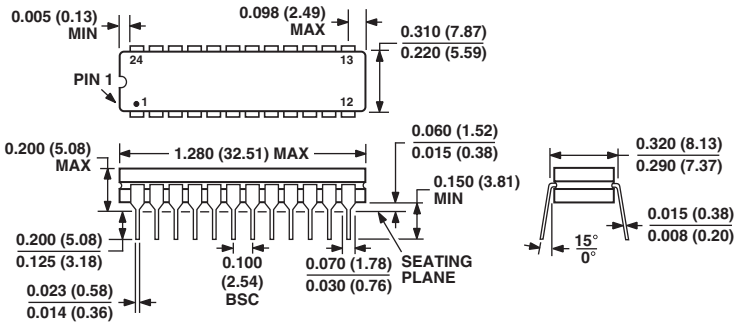


COMPLIANT TO JEDEC STANDARDS MO-095AG

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

24-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-24)

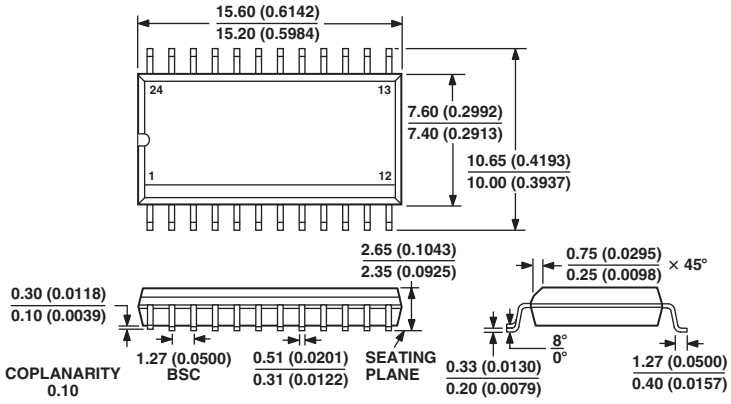
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

24-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-24)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AD

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
3/04—Data Sheet changed from REV. C to REV. D.	
Updated layout	Universal
Changes to FUNCTIONAL BLOCK DIAGRAM	1
Changes to SPECIFICATIONS	2
Changes to ORDERING GUIDE	6
Changes to Self-Calibration section	16
Changes to AD7713 to 68HC11 Interface section	23
Deleted AD7713 to ADSP-2105 Interface section	24
Deleted Figure 19 and renumbered succeeding figures	24
Updated OUTLINE DIMENSIONS	27

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