



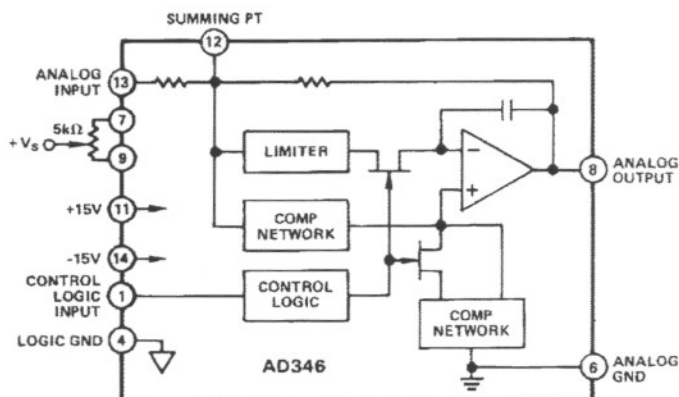
High Speed Sample-and-Hold Amplifier

AD346

FEATURES

Fast 2.0 μ s Acquisition Time to $\pm 0.01\%$
Low Droop Rate: 0.5mV/ms
Low Offset
Low Glitch: <40mV
Aperture Jitter: 400ps
Extended Temperature Range: -55°C to $+125^{\circ}\text{C}$
Internal Hold Capacitor
MIL-STD-883B Processing Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD346 is a high speed (2 μ s to 0.01%), adjustment free sample-and-hold amplifier designed for high throughput rate data acquisition applications. The fast acquisition time (2 μ s to 0.01%) and low aperture jitter (400ps) make it suitable for use with fast A/D converters to digitize signals up to 97kHz.

The AD346 is complete with an internal hold capacitor and it incorporates a compensation network which minimizes the sample to hold charge offset. The AD346 is also laser trimmed to eliminate the need for external trimming potentiometers.

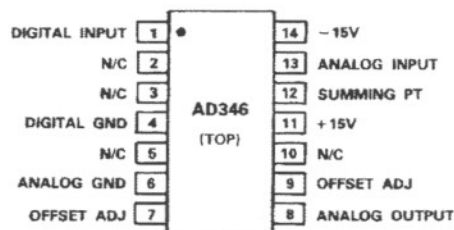
Typical applications for the AD346 include sampled data systems, D/A deglitchers, peak hold functions, strobed measurement systems and simultaneous sampling converter systems.

The device is available in two versions: the "J" specified for operation over the 0 to $+70^{\circ}\text{C}$ commercial temperature range and the "S" specified over the extended temperature range, -55°C to $+125^{\circ}\text{C}$.

PRODUCT HIGHLIGHTS

1. The AD346 is an improved second source for other sample and holds of the same pin configuration.
2. The AD346 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
3. The droop rate is only 0.5mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
4. The fast acquisition time and low aperture make it suitable for very high speed data acquisition systems.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD346JD	0 to $+70^{\circ}\text{C}$	DH-14A
AD346SD	-55° to $+125^{\circ}\text{C}$	DH-14A
AD346SD/883B	-55°C to $+125^{\circ}\text{C}$	DH-14A

*DH-14A = Ceramic DIP.

REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
 Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
 Telex: 924491 Cable: ANALOG NORWOODMASS

AD346—SPECIFICATIONS (typical @ +25°C, $V_S = \pm 15V$ unless otherwise noted)

Model	AD346JD	AD346SD	Units
ANALOG INPUT			
Voltage Range	± 10.0	*	Volts
Input Impedance	3.0	*	k Ω
DIGITAL INPUT			
"0" Input Threshold Voltage (Hold)	+ 0.8 max	*	Volts
"1" Input Current	2.0 min	*	Volts
"0" Input Current	- 360 μA (max)	*	μA
"1" Input Current	20 μA (max)	*	μA
TRANSFER CHARACTERISTICS			
Gain	- 1.0	*	V/V
Gain Error	± 0.02 max (± 0.01 typ)	*	% FSR
Gain Error, $T_{min} - T_{max}$	± 0.05 max (± 0.03 typ)	*	% FSR
Offset Voltage	± 3 max (± 1 typ)	*	mV
Offset Voltage, $T_{min} - T_{max}$	± 20 max (± 6 typ)	*	mV
Pedestal	± 4 max (± 2 typ)	*	mV
Pedestal, $T_{min} - T_{max}$	± 20 max (± 8 typ)	± 20 max (± 10 typ)	mV
Droop Rate	0.5 max (0.1 typ)	*	mV/ms
Droop Rate, $T_{min} - T_{max}$	60 max (20 typ)	650 max (200 typ)	mV/ms
DYNAMIC CHARACTERISTICS			
Full Power Bandwidth	1.4	*	MHz
$V_{OUT} = +10V, -3dB$	50	*	V/ μs
Output Slew Rate			
Acquisition Time			
To $\pm 0.01\%$ 10V Step	2.0 max (1.0 typ)	*	μs
To $\pm 0.01\%$ 20V Step	2.5 max (1.6 typ)	*	μs
Aperture Delay	60 max (30 typ)	*	ns
Aperture Jitter	0.4	*	ns
Settling Time			
Sample Mode (10V Step)	2.0 max (1.0 typ)	*	μs
Sample to Hold	500	*	ns
Feedthrough (Hold Mode)			
at 1kHz	0.02 max (0.005 typ)	*	% FSR
Transient Peak Amplitude			
Sample/Hold/Sample	40	*	mV
ANALOG OUTPUT			
Output Voltage Swing ¹	± 10.0 min	*	Volts
Output Current	3.0	*	mA
POWER REQUIREMENTS			
Operating Voltage Range	± 12 to ± 18	*	Volts
Supply Current			
+ V	18 max (9 typ)	*	mA
- V	- 10 max (- 3 typ)	*	mA
Power Supply Rejection Ratio	100	*	$\mu V/V$
Power Consumption	500 max (200 typ)	*	mW

NOTES

¹Maximum output swing is 4V less than $+V_S$.

*Specifications same as AD346JD.

Specifications subject to change without notice.

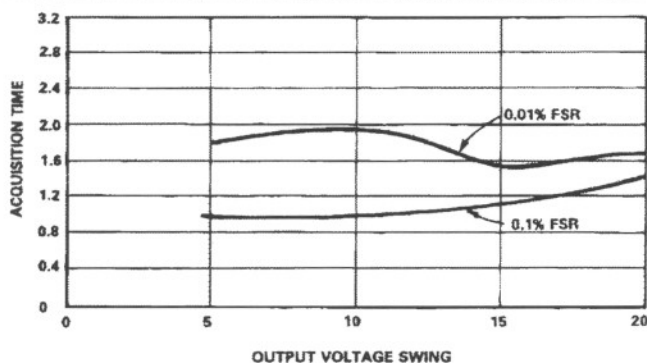
AD346


Figure 1. Acquisition Time vs. Output Voltage

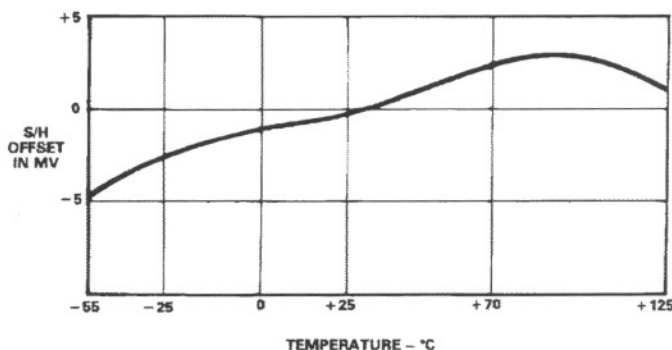


Figure 3. S/H Offset Drift (Typical)

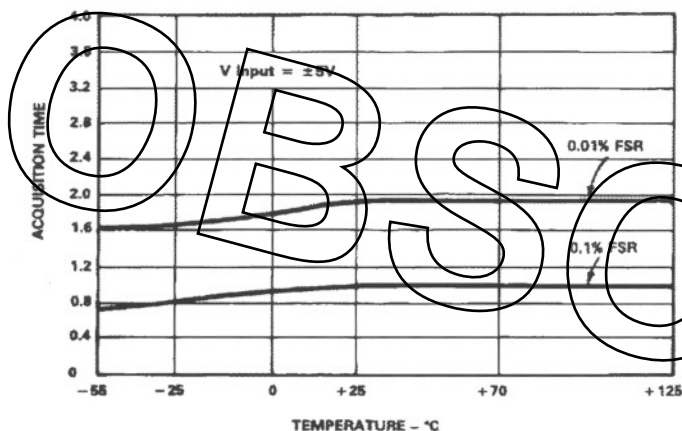
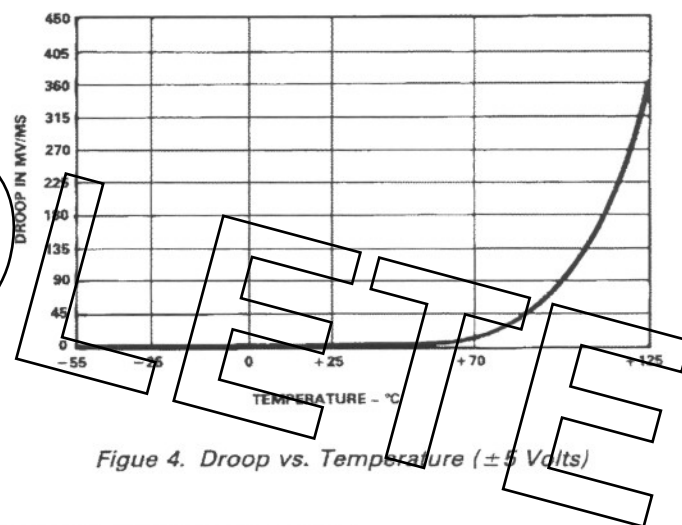


Figure 2. Acquisition Time vs. Temperature


Figure 4. Droop vs. Temperature (± 5 Volts)

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pins of the AD346. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

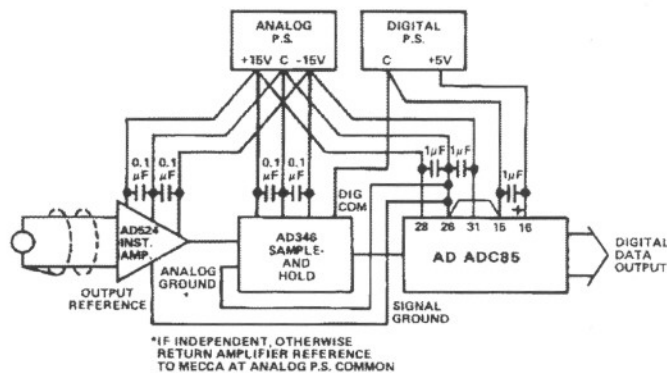


Figure 5. Basic Grounding Practice

AD346

SAMPLED DATA SYSTEMS

The fast acquisition time of the AD346 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD346 can be used with a number of different A/D converters to achieve high throughput rates. Figures 6, 7 and 8 show the use of an AD346 with the AD578, AD5240 and AD ADC85.

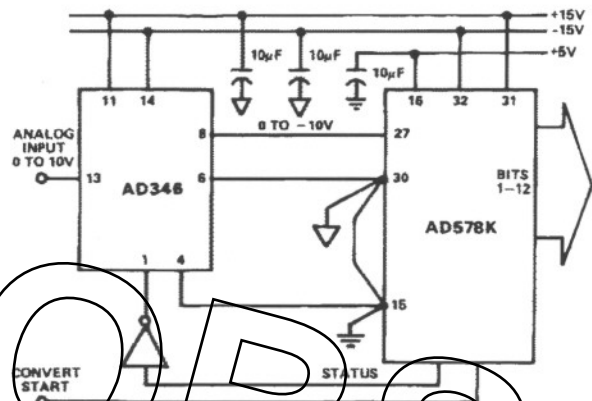


Figure 6. 153kHz-12-Bit, A/D Conversion System

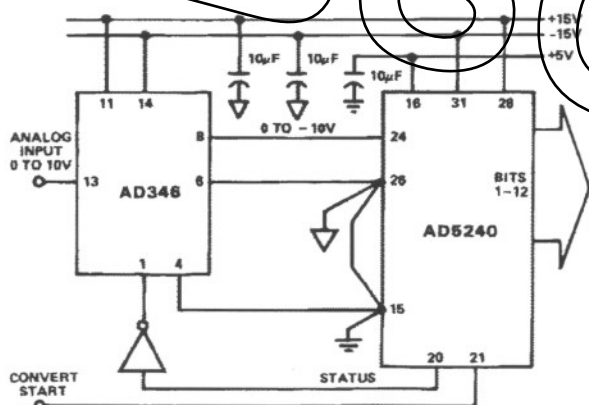


Figure 7. 142.8kHz-12-Bit, A/D Conversion System

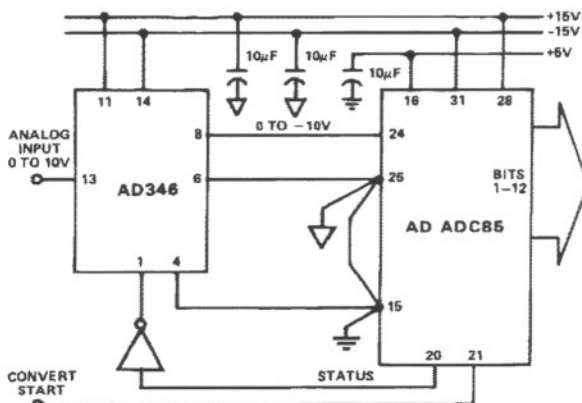


Figure 8. 83.3kHz-12-Bit, A/D Conversion System

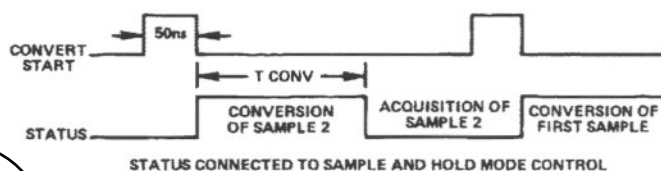


Figure 9. Start/Status Timing for Sampled Data System

CLEANLINESS, LEAKAGE AND DROOP

Sample-and-hold amplifiers usually have one or more internal nodes which operate with extremely high impedances in the hold mode. Parasitic leakage at these nodes can degrade the part's droop rate, and ac signals coupled in through parasitic capacitance can introduce noise onto the held output. One such dc leakage path can be produced by the residual oils left on the package after it has been handled with bare fingers. Most normal board cleaning and flux removal procedures will remove these contaminants. For best results finger cots should be used when handling the AD346.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

