

# High Speed CMOS Logic – 74HC139

#### Dual 1-of-4 Decoder / Demultiplexer in bare die form

### Description

The 74HC139 is fabricated using a  $2.5\mu m$  5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. This device consists of x2 independent 1–of–4 decoders, each decoding a 2 bit address to 1–of–4 active–low outputs. Active–low Selects facilitate the demultiplexing and cascading functions. The demultiplexing function is executed by using the Address inputs to select the desired device output and utilizing the Select as a data input.

#### Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL

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- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 74LS139.

# Ordering Information

The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

<u>54HC139</u>

# Die Dimensions in µm (mils)



# Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

# **Mechanical Specification**

Die Size (Unsawn)	1300 x 1400 51 x 55	µm mils	
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils	
Top Metal Composition	Al 1%Si 1.1µ	m	
Back Metal Composition	N/A – Bare Si		





# Pad Layout and Functions



# Logic Diagram

ADDRESS  $\left\{ \begin{array}{ccc} 1A & \frac{2}{3} \\ 1B & \frac{3}{3} \end{array} \right\}$   $\left\{ \begin{array}{ccc} \frac{4}{5} & 1Y1 \\ \frac{6}{5} & 1Y2 \\ \frac{6}{7} & 1Y3 \end{array} \right\}$  ACTIVE-LOW OUTPUTS



PAD	FUNCTION	COORDINATES (mm)				
FAD	1 ONO HON	X	Y			
1	1G	0.152	0.366			
2	1A	0.162	0.132			
3	1B	0.422	0.122			
4	1Y0	0.59	0.122			
5	1Y1	0.772	0.122			
6	1Y2	1.088	0.122			
7	1Y3	1.088	0.333			
8	GND	1.088	0.619			
9	2Y3	1.088	0.972			
10	2Y2	1.078	1.173			
11	2Y1	0.722	1.183			
12	2Y0	0.566	1.183			
13	2B	0.396	1.153			
14	2A	0.162	1.173			
15	2G	0.152	0.938			
16	V <sub>CC</sub>	0.122	0.591			
CON	CONNECT CHIP BACK TO V <sub>CC</sub> OR FLOAT					

# Truth Table

IN	PUTS			OUT	FPUTS	3
G	В	А	Y0	Y1	Y2	Y3
Н	Х	Х	Н	Н	Н	Н
L	L	L	L	Н	Н	Н
L	L	Н	Н	L	Н	Н
L	Н	L	Н	Н	L	Н
L	Н	Н	Н	Н	Н	L

X = don't care

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#### Absolute Maximum Ratings<sup>1</sup>

0			
PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V <sub>CC</sub>	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V <sub>IN</sub>	-1.5 to V <sub>CC</sub> +1.5	V
DC Output Voltage (Referenced to GND)	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
DC Input Current, per pin	I <sub>IN</sub>	±20	mA
DC Output Current, per pin	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> or GND Current, per pin	I <sub>cc</sub>	±50	mA
Power Dissipation in Still Air <sup>2</sup>	PD	750	mW
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

# Recommended Operating Conditions<sup>3</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage		V <sub>cc</sub>	2	6	V
DC Input or Output Voltage		V <sub>IN</sub> ,V <sub>OUT</sub>	0	V <sub>CC</sub>	V
Operating Temperature Range		TJ	0	+85	°C
	V <sub>CC</sub> = 2.0V		0	1000	
Input Rise and Fall Time	$V_{CC} = 4.5V$	t <sub>r</sub> , t <sub>f</sub>	0	500	ns
	$V_{\rm CC} = 6.0 V$		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range GND  $\leq$  ( $V_{IN}$  or  $V_{OUT}$ )  $\leq$   $V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

#### DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL V <sub>cc</sub>	Vac	c CONDITIONS	LIMITS			UNITS	
		•00		25°C	85°C	FULL RANGE <sup>4</sup>	onno	
Minimum High-Level Input Voltage	V <sub>IH</sub>	2.0V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> -0.1V   I <sub>OUT</sub>   ≤ 20µA	1.5	1.5	1.5		
		4.5V		3.15	3.15	3.15	V	
		6.0V		4.2	4.2	4.2		
Maximum Low-Level Input Voltage	el V <sub>IL</sub> 2.0V 4.5V	2.0V	2.0V	$V_{OUT} = 0.1 V \text{ or}$	0.5	0.5	0.5	
		4.5V	V <sub>cc</sub> -0.1V	1.35	1.35	1.35	V	
		6.0V	Ι <sub>Ουτ</sub>   ≤ 20μΑ	1.8	1.8	1.8		

**4.**  $0^{\circ}C \le T_{J} \le +85^{\circ}C$ 





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#### DC Electrical Characteristics (Voltages Referenced to GND) LIMITS PARAMETER SYMBOL Vcc CONDITIONS UNITS **FULL RANGE<sup>4</sup>** 25°C 85°C 2.0V 1.9 1.9 1.9 $V_{IN} = V_{IH} \text{ or } V_{IL}$ 4.5V 4.4 4.4 4.4 | I<sub>OUT</sub> | ≤ 20µA 6.0V 5.9 5.9 5.9 Minimum High-Level V VOH $V_{IN} = V_{IH} \text{ or } V_{IL}$ $|I_{OUT}| \le 4.0 \text{mA}$ **Output Voltage** 4.5V 3.98 3.84 3.84 $V_{IN} = V_{IH} \text{ or } V_{IL}$ 6.0V 5.48 5.34 5.34 | I<sub>OUT</sub> | ≤ 5.2mA 2.0V 0.1 0.1 0.1 $V_{IN} = V_{IH} \text{ or } V_{IL}$ $|I_{OUT}| \le 20 \mu A$ 4.5V 0.1 0.1 0.1 6.0V 0.1 0.1 0.1 Maximum Low-Level V Vol $V_{IN} = V_{IH} \text{ or } V_{IL}$ **Output Voltage** 4.5V 0.26 0.33 0.33 | I<sub>OUT</sub>| ≤ 4.0mÅ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $|I_{OUT}| \le 5.2 \text{mA}$ 6.0V 0.33 0.26 0.33 Maximum Input 6.0V $V_{IN} = V_{CC}$ or GND $I_{IN}$ ±0.1 ±1.0 ±1.0 μΑ Leakage Current Maximum Quiescent $V_{IN} = V_{CC}$ or GND 6.0V 4 40 40 Icc μA Supply Current I<sub>OUT</sub> = 0μA

# AC Electrical Characteristics<sup>5</sup>

PARAMETER	SYMBOL	V <sub>cc</sub>	CONDITIONS		UNITS			
				25°C	85°C	FULL RANGE <sup>4</sup>		
Maximum		2.0V		115	145	145		
Propagation Delay, Select to Output Y	$t_{PLH,} t_{PHL}$	$t_{\text{PLH}, t_{\text{PHL}}} \qquad 4.5V \\ \hline 6.0V \qquad t_r = t_f = 6r$	$C_{L} = 50 pF,$ $t_{r} = t_{f} = 6 ns$	23	29	29	ns	
(Figure 1, 3)				20	25	25		
Maximum	ppagation Delay, tt	2.0V	$C_{\rm L} = 50  \rm p E$	115	145	145		
Propagation Delay, Input A to Output Y		4.5V		23	29	29	ns	
(Figure 2,3)		6.0V		20	25	25		
Maximum Output		2.0V	• •• •	75	95	95		
Transition Time, Any Output	$t_{TLH,} t_{THL}$	4.5V	C <sub>L</sub> = 50pF, t <sub>r</sub> = t <sub>f</sub> = 6ns	15	19	19	ns	
(Figure 1,3)		6.0V	q = q = 0.03	13	16	16		
Maximum Input Capacitance	C <sub>IN</sub>	-	-	10	10	10	pF	
Power Dissipation	_	-		T <sub>J</sub> = 25°C,		TYPI	CAL	
Capacitance (Per Decoder) <sup>7</sup>	C <sub>PD</sub>		$V_{\rm CC} = 5.0 V$		5	5	pF	

6. Not production tested in die form, characterized by chip design and tested in package.

7. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

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#### Pad Description

#### ADDRESS INPUTS

#### 1A, 1B, 2A, 2B

(Pads 2, 3, 14, 13) When the respective 1–of–4 decoder is enabled these inputs determine which of its four active–low outputs is selected.

#### CONTROL INPUTS

#### 1G, 2G

(Pads 1, 15)

Active–low select inputs. For a low level on this input, the outputs for that particular decoder follow the Address inputs. A high level on this input forces all outputs to a high level.

#### OUTPUTS

1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3 (Pads 4-7, 12, 11, 10, 9)

Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

#### Switching Waveforms













\* Includes all probe and jig capacitance



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